

# GAN063-650WSA

650 V, 50 mΩ Gallium Nitride (GaN) FET

15 November 2019

Product data sheet

## 1. General description

The GAN063-650WSA is a 650 V, 50 mΩ Gallium Nitride (GaN) FET. It is a normally-off device that combines Nexperia's state-of-the-art high-voltage GaN HEMT and low-voltage silicon MOSFET technologies — offering superior reliability and performance. AEC-Q101 qualified.

## 2. Features and benefits

- Ultra-low reverse recovery charge
- Simple gate drive (0 V to +10 V or 12 V)
- Robust gate oxide ( $\pm 20$  V capability)
- High gate threshold voltage (+4 V) for very good gate bounce immunity
- Very low source-drain voltage in reverse conduction mode
- Transient over-voltage capability (800 V)
- AEC-Q101 qualified

## 3. Applications

- Hard and soft switching converters for industrial and datacom power
- Bridgeless totempole PFC
- PV and UPS inverters
- Servo motor drives

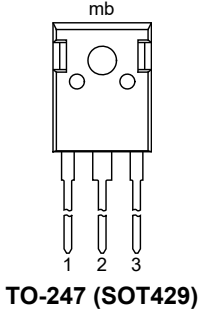
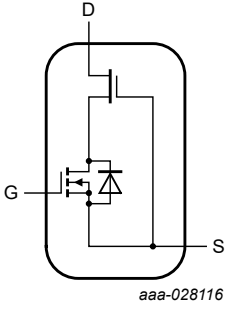
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$-55\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	650	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	34.5	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	143	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	50	60	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 400\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}$	-	4	-	nC
$Q_{G(tot)}$	total gate charge		-	15	-	nC
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25\text{ A}; di_S/dt = -1000\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; \text{Fig. 14}$	-	125	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>TO-247 (SOT429)</p>	 <p>aaa-028116</p>
2	S	source		
3	D	drain		
mb	S	mounting base; connected to source		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GAN063-650WSA	TO-247	plastic, single-ended through-hole package; 3 leads; 5.45 mm pitch; 20.45 mm x 15.6 mm x 4.95 mm body	SOT429

## 7. Marking

Table 4. Marking codes

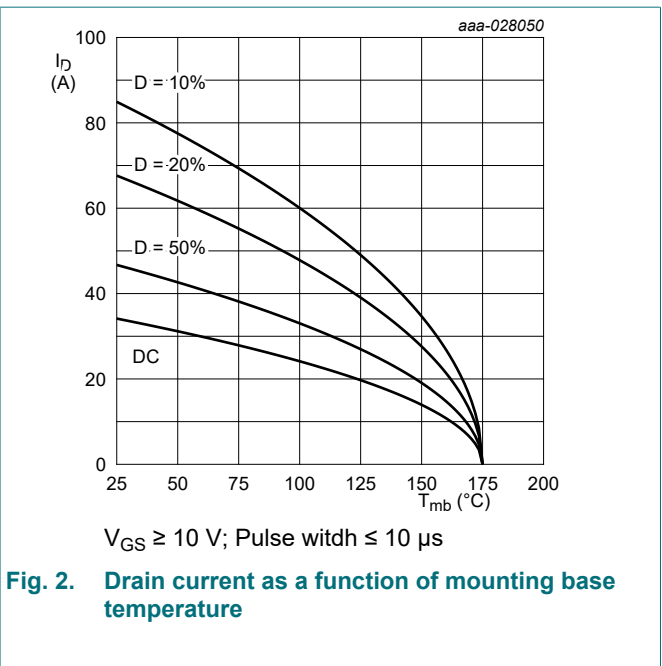
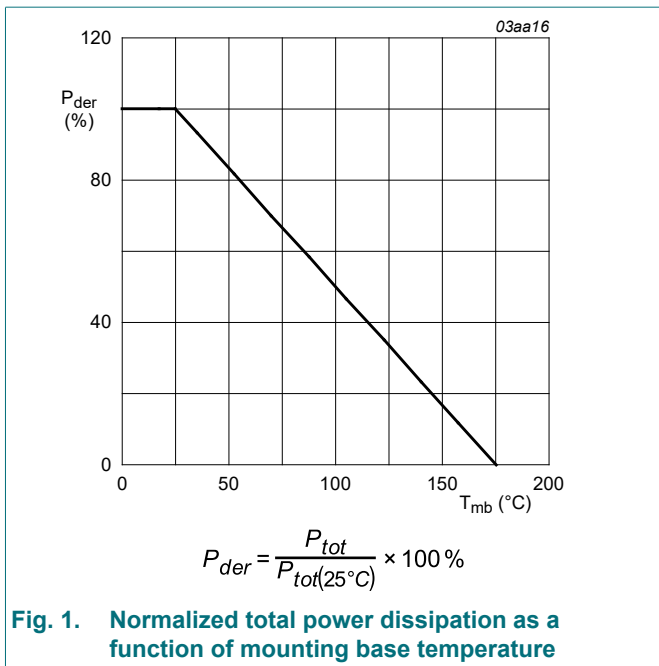
Type number	Marking code
GAN063-650WSA	GAN063-650WSA

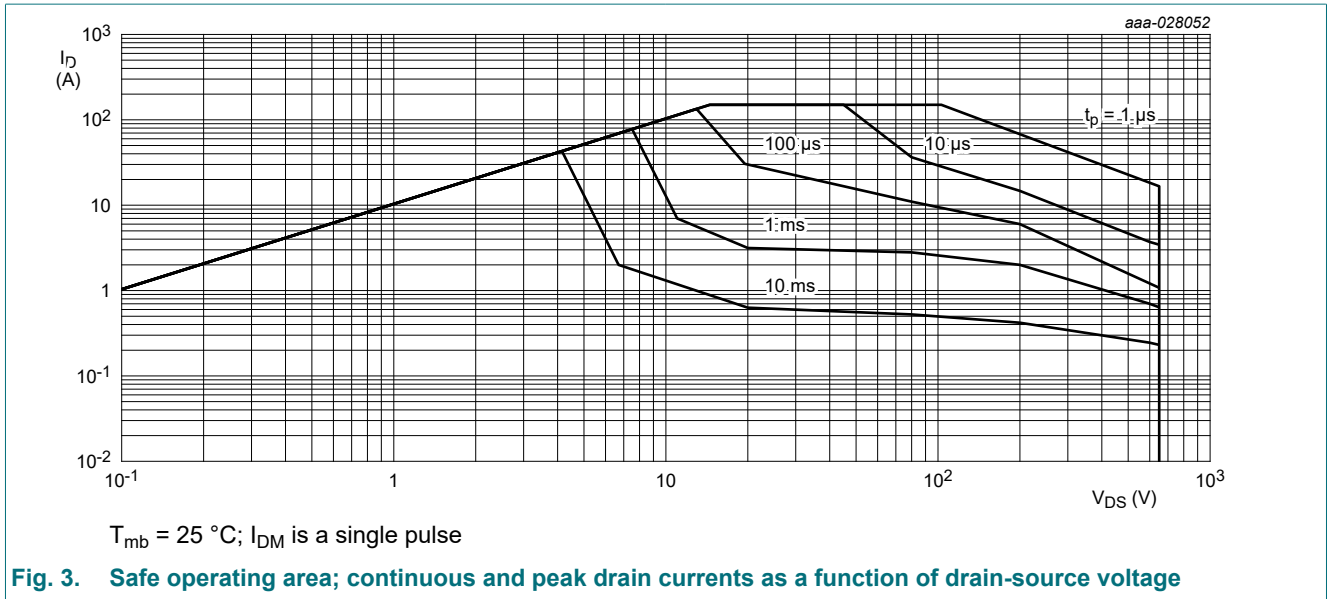
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	-55 °C ≤ T <sub>J</sub> ≤ 175 °C	-	650	V
V <sub>TDS</sub>	transient drain to source voltage	pulsed; t <sub>p</sub> = 1 μs; δ <sub>factor</sub> = 0.01	-	800	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; Fig. 1	-	143	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; Fig. 2	-	34.5	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; Fig. 2	-	24.4	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3	-	150	A
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>J</sub>	junction temperature		-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 0 V	-	34.5	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	150	A

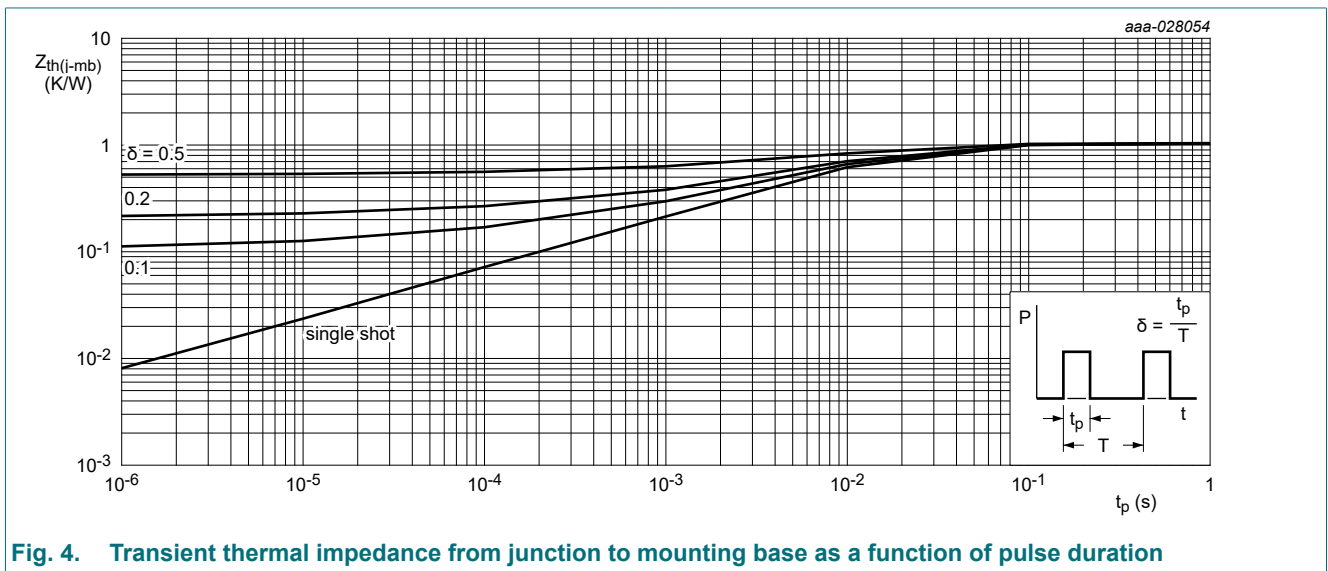




## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	-	1.05	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	-	40	K/W



## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	3.4	3.9	4.5	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	2.2	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	-	5.2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 650 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	25	$\mu\text{A}$
		$V_{DS} = 650 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	25	-	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	50	60	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	120	-	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	2.3	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 400 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	15	-	nC
$Q_{GS}$	gate-source charge		-	6	-	nC
$Q_{GD}$	gate-drain charge		-	4	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 400 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	-	1000	-	pF
$C_{oss}$	output capacitance		-	130	-	pF
$C_{rss}$	reverse transfer capacitance		-	8	-	pF
$C_{o(er)}$	effective output capacitance, energy related	$0 \text{ V} \leq V_{DS} \leq 400 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 12</a>	-	190	-	pF
$C_{o(tr)}$	effective output capacitance, time related	$0 \text{ V} \leq V_{DS} \leq 400 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	310	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 400 \text{ V}; R_L = 16 \text{ } \Omega; V_{GS} = 12 \text{ V}; R_{G(ext)} = 40 \text{ } \Omega$	-	57	-	ns
$t_r$	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	88	-	ns
$t_f$	fall time		-	11	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 400 \text{ V}$	-	125	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 13</a>	-	1.9	-	V
		$I_S = 12.5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	1.35	-	V
$t_{rr}$	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -1000 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 400 \text{ V};$ <a href="#">Fig. 14</a>	-	54	-	ns
$Q_r$	recovered charge		-	125	-	nC

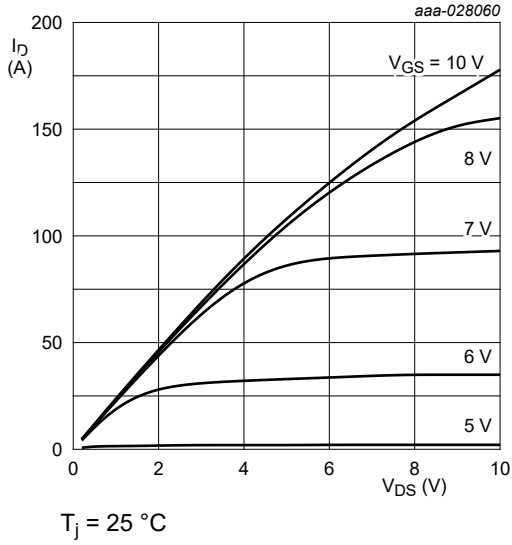


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

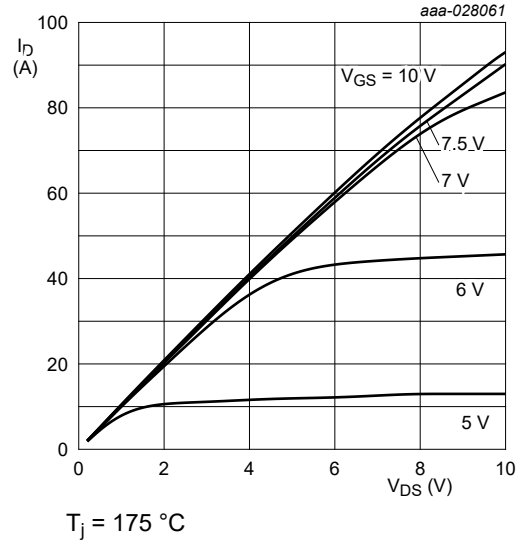


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

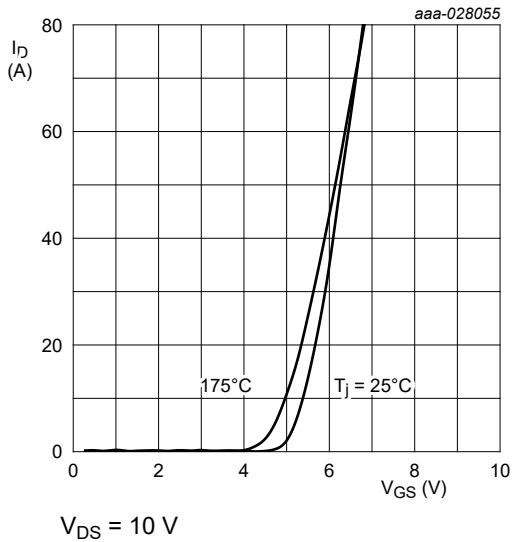


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

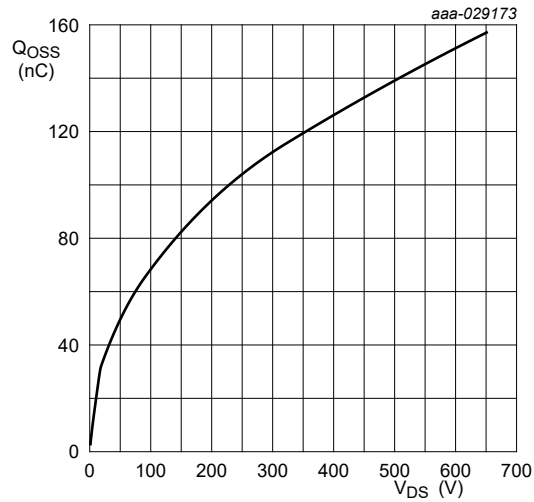
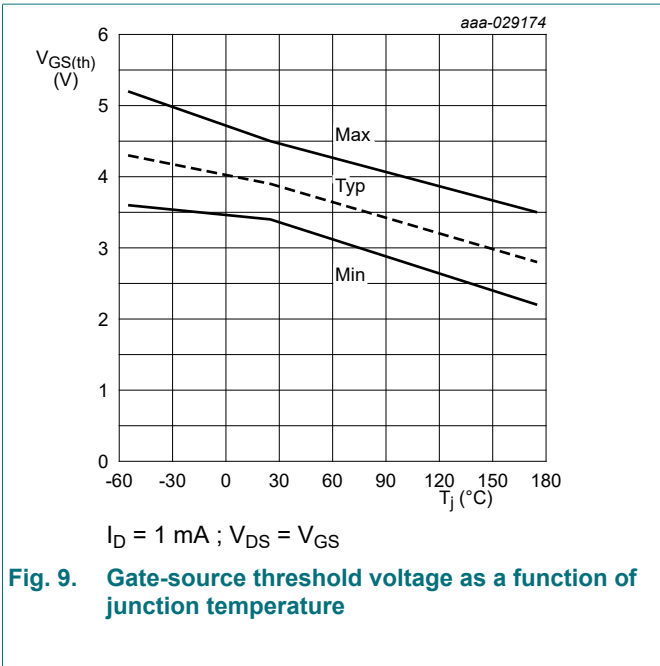
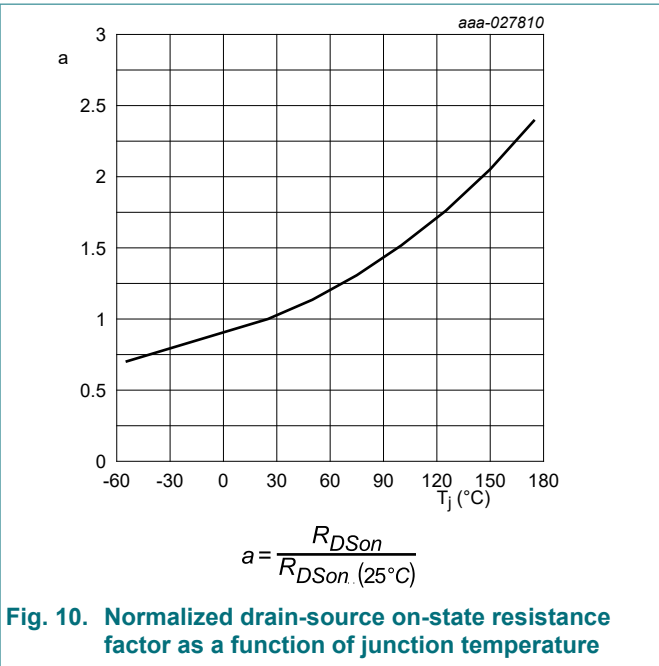


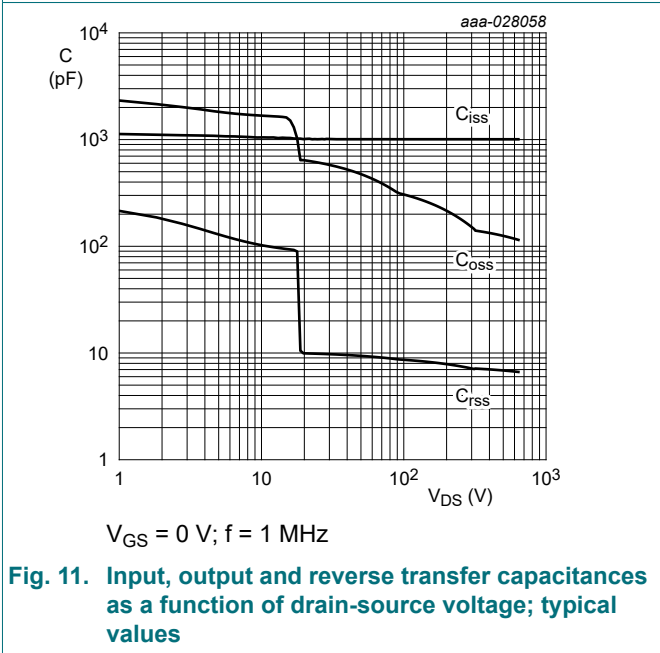
Fig. 8. Typical  $Q_{OSS}$



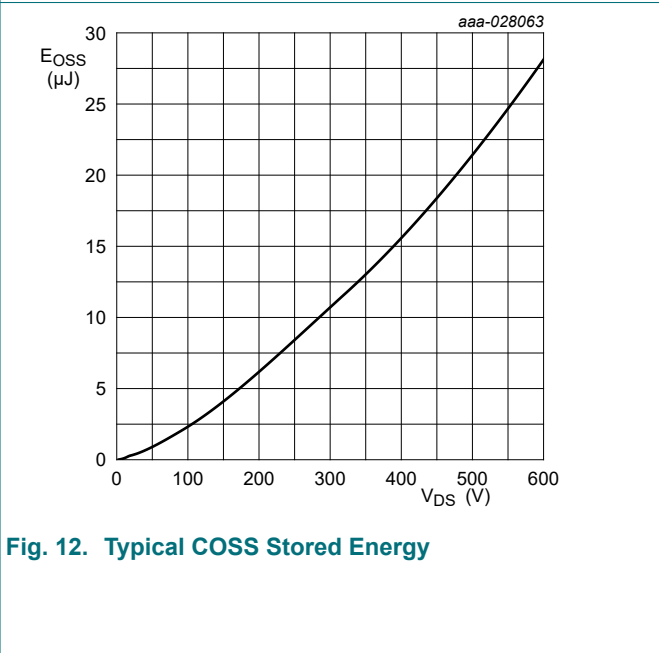
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**



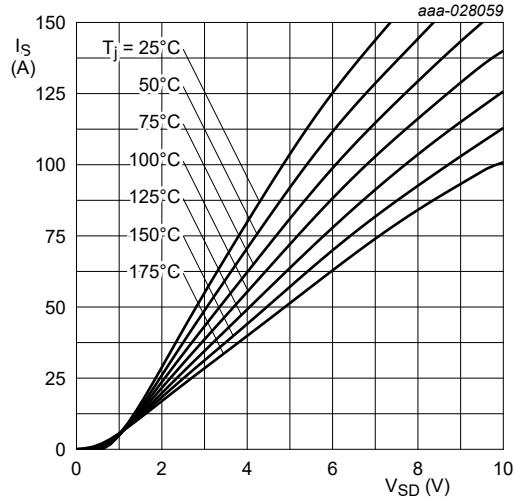
**Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature**



**Fig. 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



**Fig. 12. Typical COSS Stored Energy**



$V_{GS} = 0\text{ V}$

Fig. 13. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

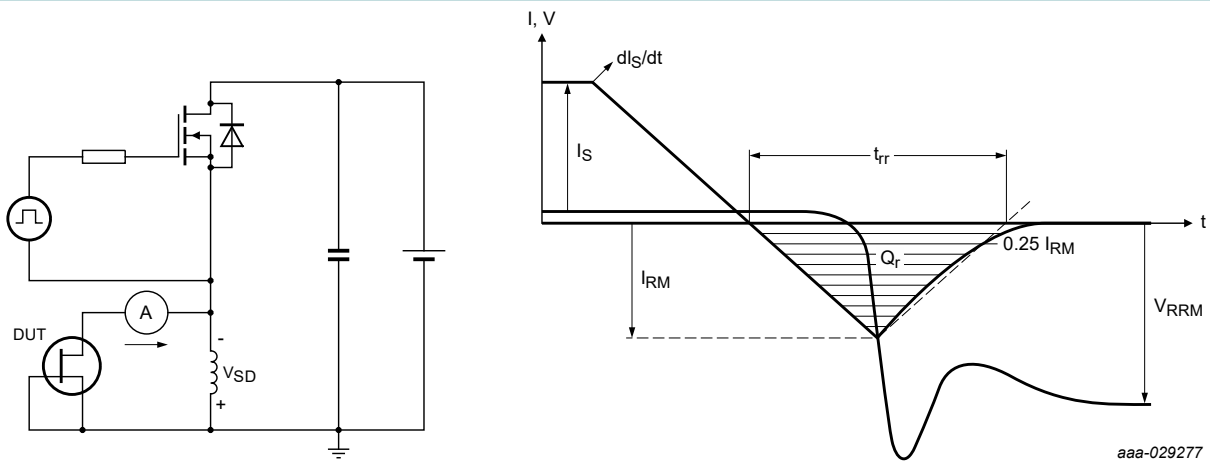


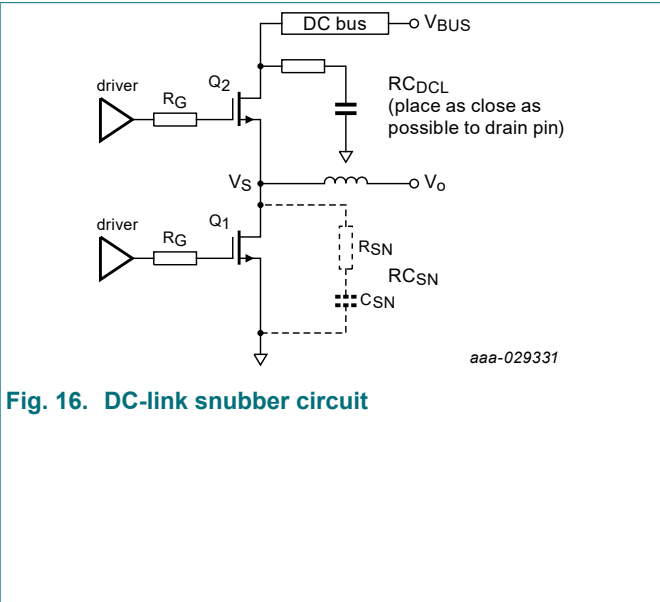
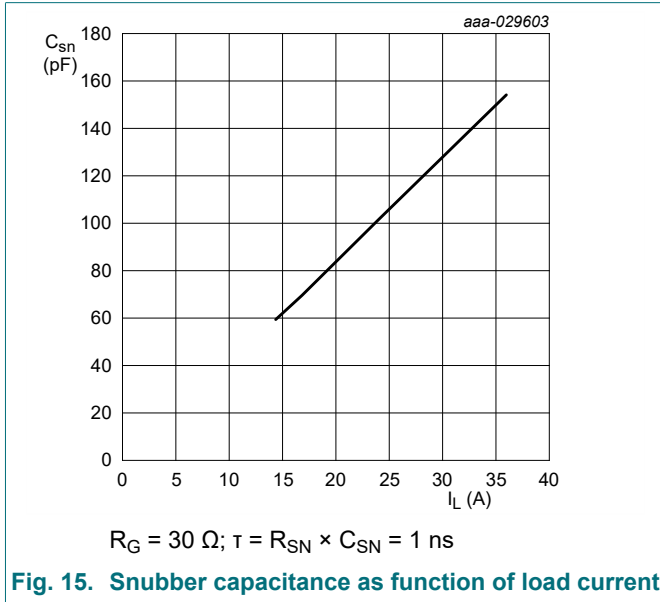
Fig. 14. Diode reverse recovery test circuit and waveform


### 11. Application information

To achieve maximum efficiency and stability when switching high currents, a switching node RC snubber ( $R_{SN}$ ,  $C_{SN}$ ) is recommended. For  $I_L < 14$  A, a switching-node snubber is not required.

$C_{SN}$  is taken from the graph.

$R_{SN}$  should be selected to achieve a time constant of 1 ns; e.g. if  $C_{SN} = 100$  pF,  $R_{SN} = 1$  ns / 100 pF = 10 Ω.



 **Note:** A DC-link snubber is recommended in all cases. Optimal is 20 nF in series with 4 Ω, most easily achieved with parallel combination 10 nF and 8 Ω. This snubber lowers the Q factor of any resonance in the bus. That resonance will act as a load on the high gain amplifier that is the GaN FET and can lead to instability. For very high current, an RC snubber is recommended for the switching node. This will increase switching loss, so this is only recommended at high power levels where the losses are a very small percentage of the total power.

12. Package outline

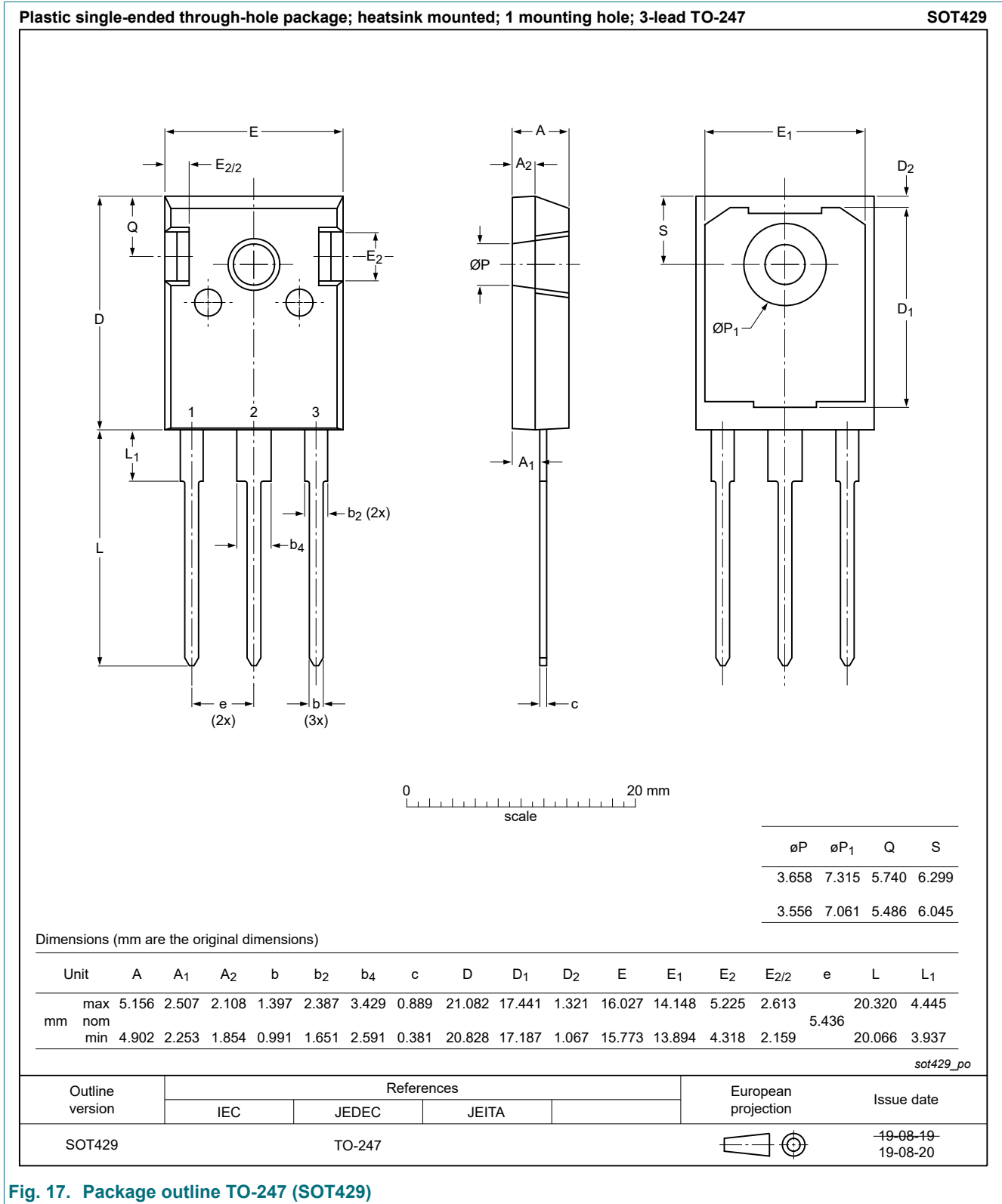


Fig. 17. Package outline TO-247 (SOT429)

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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