

MOSFET – P-Channel, QFET®

-60 V, -17 A, 70 mΩ

FQPF27P06

Description

This P-Channel enhancement mode MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

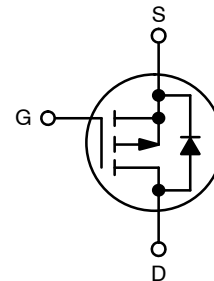
- -17 A, -60 V, $R_{DS(on)} = 70 \text{ m}\Omega$ (Max.) @ $V_{GS} = -10 \text{ V}$, $I_D = -8.5 \text{ A}$
- Low Gate Charge (Typ. 33 nC)
- Low Crss (Typ. 120 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



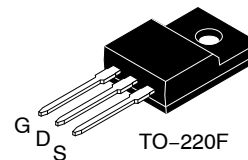
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V_{DSS}	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
-60 V	70 mΩ @ 10 V	-17 A

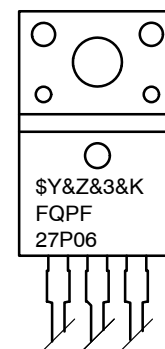


P-Channel MOSFET



TO-220 Fullpack, 3-Lead / TO-220F-3SG
CASE 221AT

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = 3-Digit Plant Code
&K = 2-Digits Lot Run Traceability Code
FQPF27P06 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FQPF27P06	TO-220-3 (Pb-Free)	1000 Units / Tube

FQPF27P06

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

Symbol	Parameter	FQPF27P06	Unit
V _{DSS}	Drain-Source Voltage	-60	V
I _D	Drain Current	- Continuous (T _C = 25°C)	-17 A
		- Continuous (T _C = 100°C)	-12 A
I _{DM}	Drain Current (Note 1)	- Pulsed	-68 A
V _{GSS}	Gate-Source Voltage	+ 25	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	560	mJ
I _{AR}	Avalanche Current (Note 1)	-17	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	4.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-7.0	V/ns
P _D	Power Dissipation (T _C = 25°C)		47 W
		- Derate above 25°C	0.31 W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +175	°C
T _L	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 2.25 mH, I_{AS} = -17 A, V_{DD} = -25 V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ -27 A, di/dt ≤ 300A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

THERMAL CHARACTERISTICS

Symbol	Characteristic	Typ	Max	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	-	3.19	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	-	62.5	°C/W

FQPF27P06

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-60	--	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C	-	-0.06	-	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	μA
		$V_{DS} = -48\text{ V}, T_C = 150^\circ\text{C}$	-	-	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.0	-	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -8.5\text{ A}$	-	0.055	0.07	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -30\text{ V}, I_D = -8.5\text{ A}$ (Note 4)	-	12	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	1100	1400	pF
C_{oss}	Output Capacitance		-	510	660	pF
C_{rss}	Reverse Transfer Capacitance		-	120	155	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -30\text{ V}, I_D = -13.5\text{ A}, R_G = 25\ \Omega$ (Note 4, 5)	-	18	45	ns
t_r	Turn-On Rise Time		-	185	380	ns
$t_{d(off)}$	Turn-Off Delay Time		-	30	70	ns
t_f	Turn-Off Fall Time		-	90	190	ns
Q_g	Total Gate Charge	$V_{DS} = -48\text{ V}, I_D = -27\text{ A}, V_{GS} = -10\text{ V}$ (Note 4, 5)	-	33	43	nC
Q_{gs}	Gate-Source Charge		-	6.8	-	nC
Q_{gd}	Gate-Drain Charge		-	18	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATING

I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	-17	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	-68	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -17\text{ A}$	-	-	-4.0	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -27\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	-	105	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.41	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$

5. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

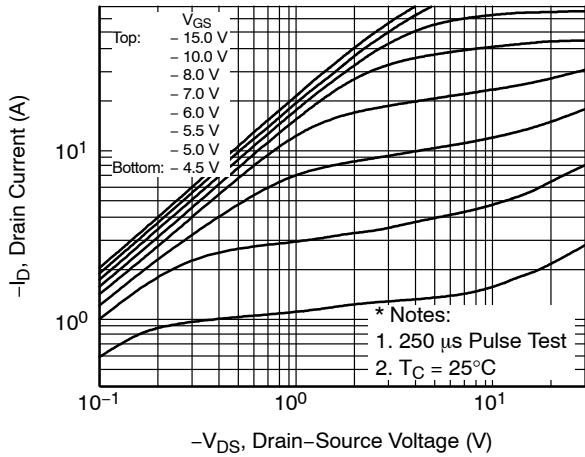


Figure 1. On-Region Characteristics

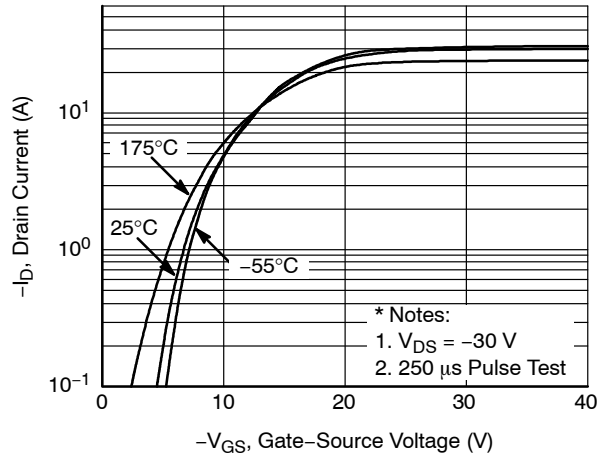


Figure 2. Transfer Characteristics

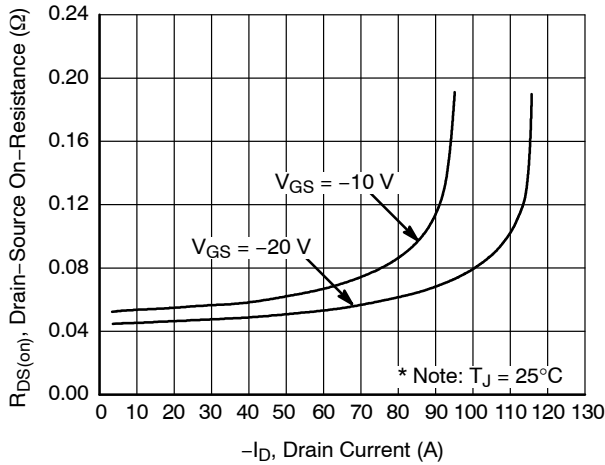


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

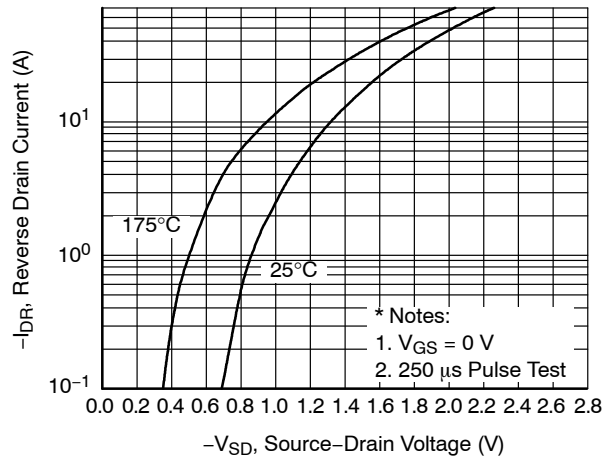


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

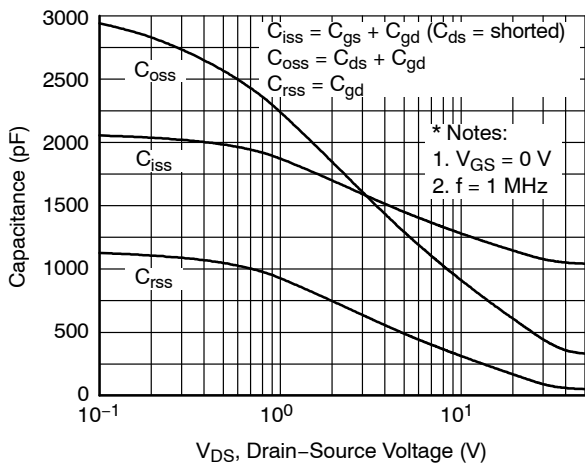


Figure 5. Capacitance Characteristics

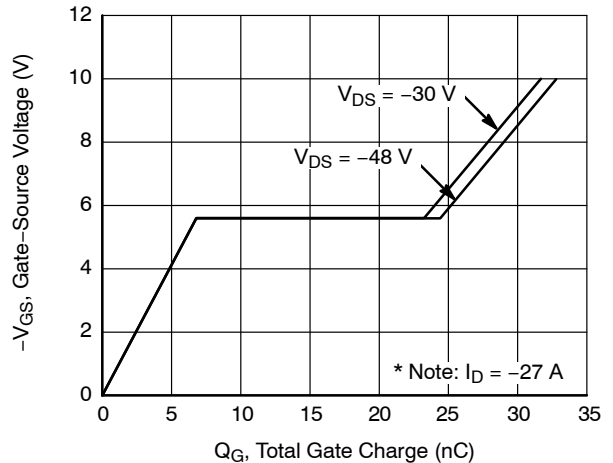


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS (Continued)

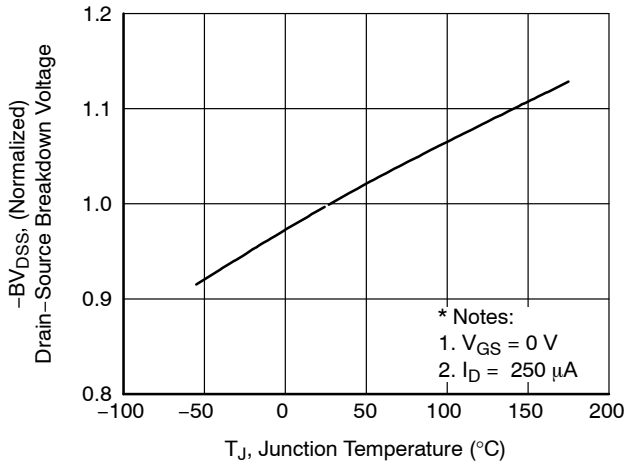


Figure 7. Breakdown Voltage Variation vs. Temperature

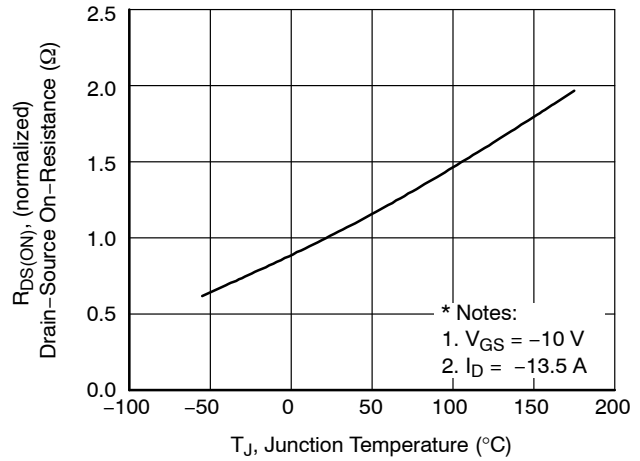


Figure 8. On-Resistance Variation vs. Temperature

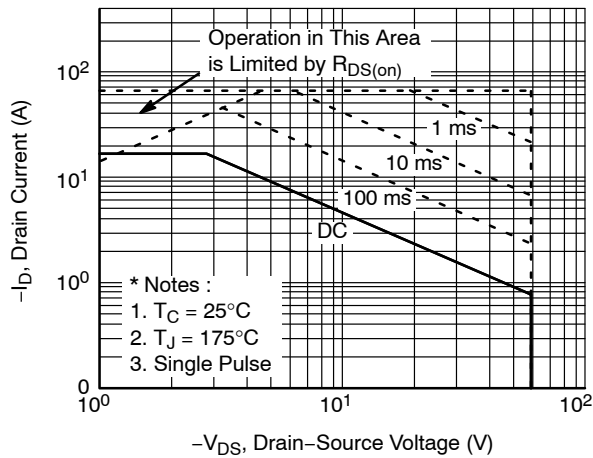


Figure 9. Maximum Safe Operating Area

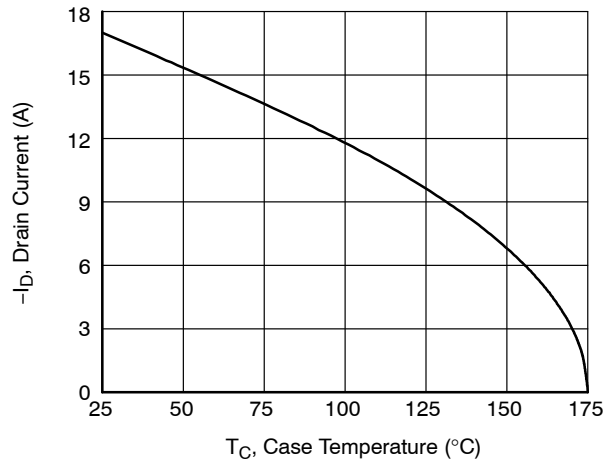


Figure 10. Maximum Drain Current vs. Case Temperature

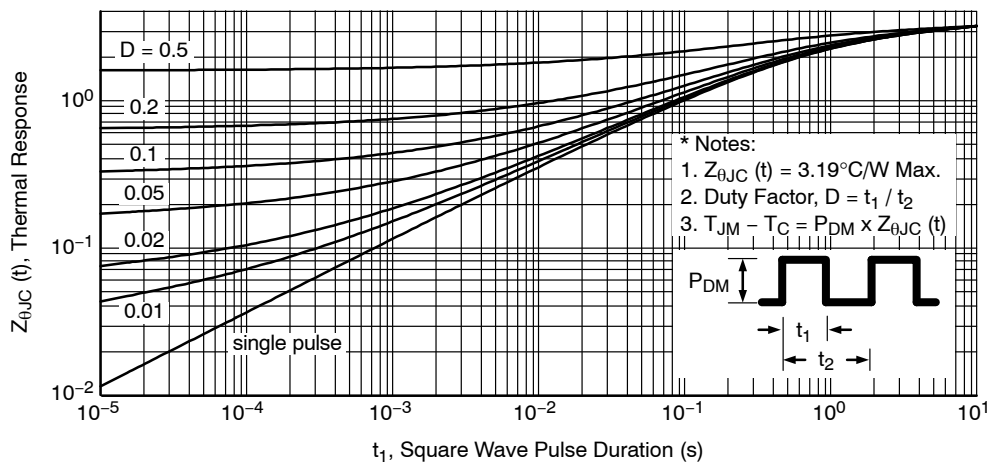


Figure 11. Transient Thermal Response Curve

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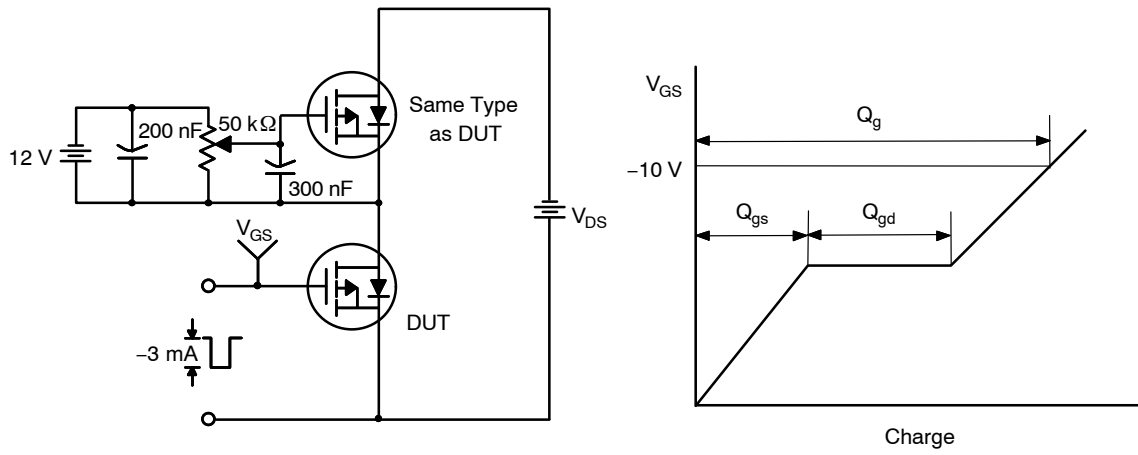


Figure 12. Gate Charge Test Circuit & Waveform

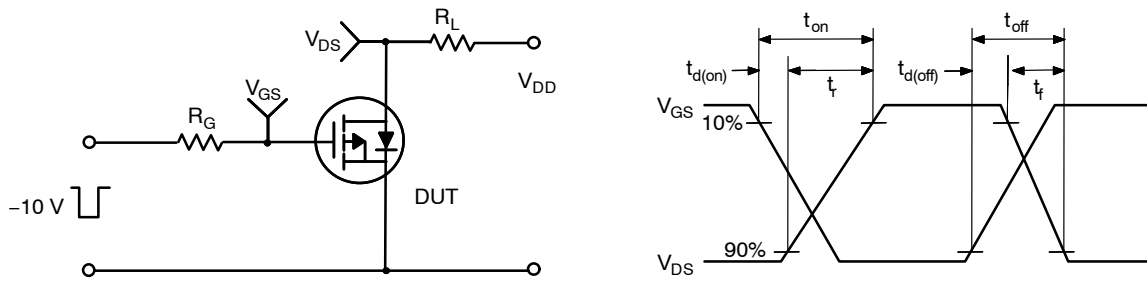


Figure 13. Resistive Switching Test Circuit & Waveforms

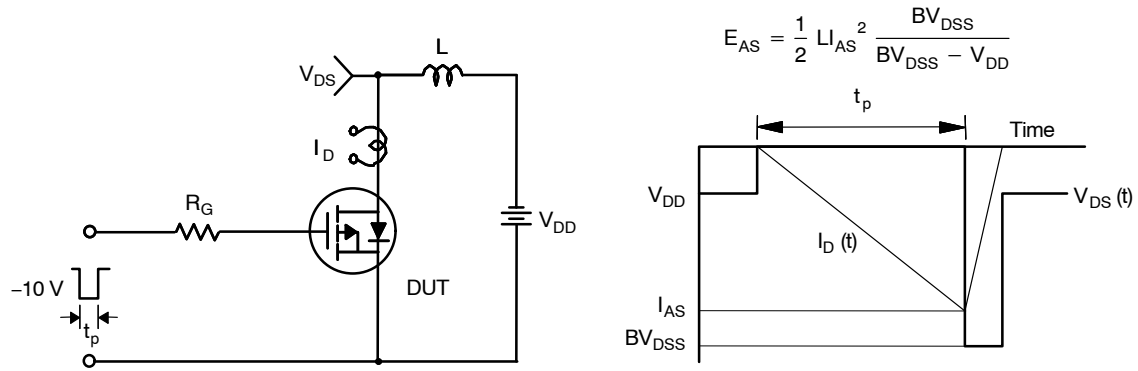


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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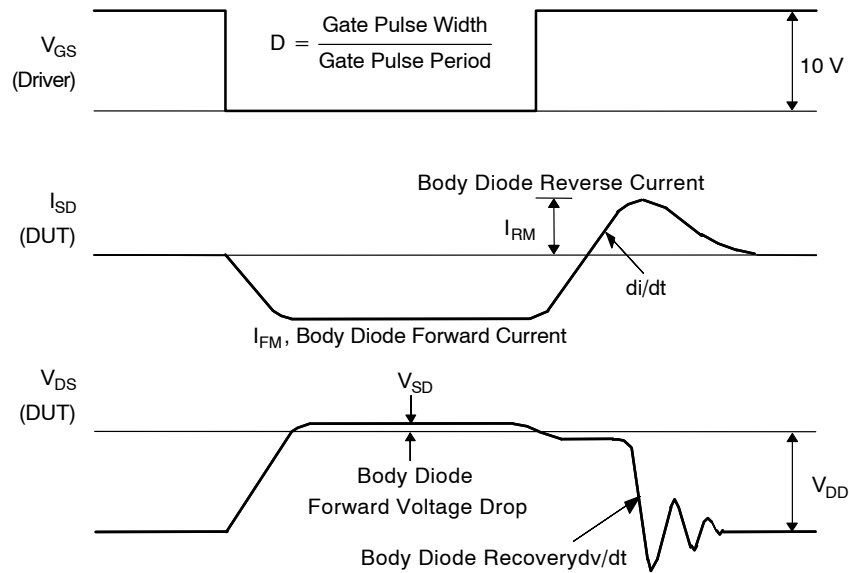
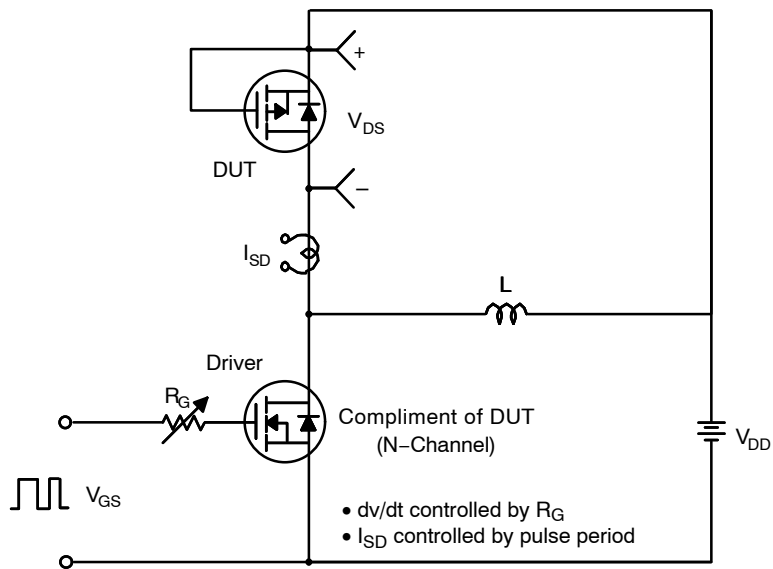


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

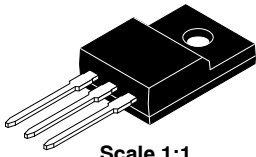
PACKAGE DIMENSIONS

ON Semiconductor®

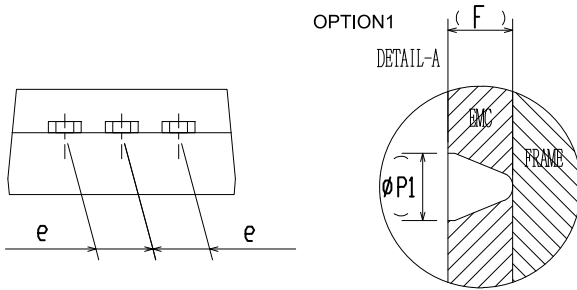
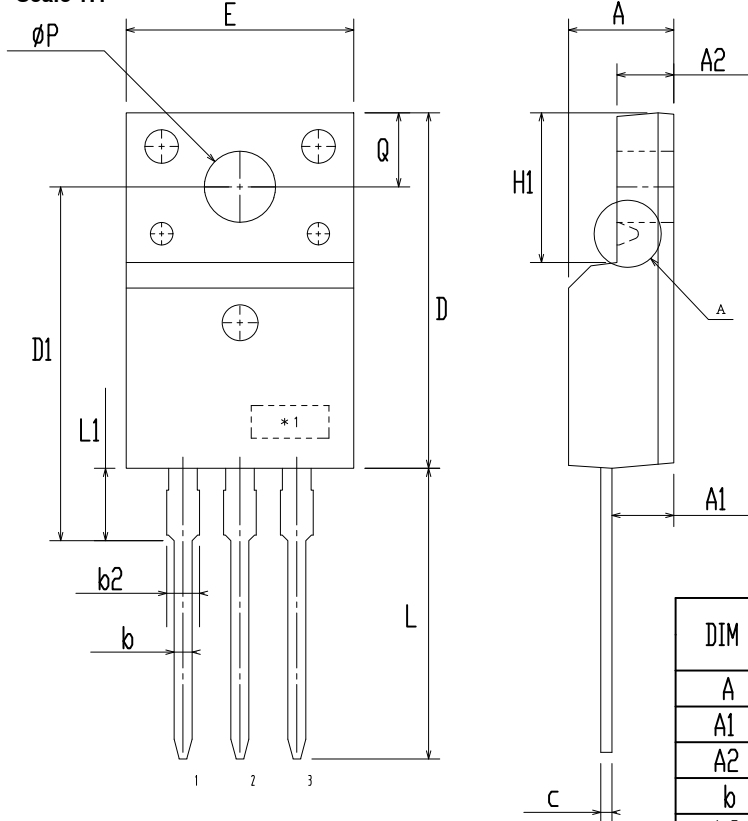


TO-220 Fullpack, 3-Lead / TO-220F-3SG CASE 221AT ISSUE B

DATE 19 JAN 2021



Scale 1:1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
phi P	2.98	3.18	3.38
phi P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:

- A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.
- C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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DESCRIPTION:	TO-220 FULLPACK, 3-LEAD / TO-220F-3SG	PAGE 1 OF 1

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