

MOSFET – Dual, N-Channel, Logic Level, POWERTRENCH®

30 V, 6 A, 28 mΩ

FDS6912A

General Description

These N-Channel Logic Level MOSFETs are produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 6.0 A, 30 V
 $R_{DS(ON)} = 28\text{ m}\Omega @ V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 35\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability
- This Device is Pb-Free and Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

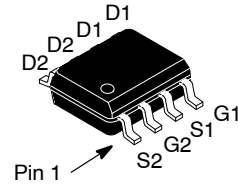
Symbol	Parameter	Ratings	Unit
V _{DSS}	Drain-Source Voltage	30	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Drain Current	- Continuous (Note 1a)	6
		- Pulsed	20
P _D	Power Dissipation for Single Operation	(Note 1a)	1.6
		(Note 1b)	1.0
		(Note 1c)	0.9
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

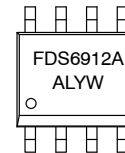
Symbol	Parameter	Ratings	Unit
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

V _{DSS}	R _{DS(ON)} MAX	I _D MAX
30 V	28 mΩ @ V _{GS} = 10 V	6.0 A
	35 mΩ @ V _{GS} = 4.5 V	5.0 A



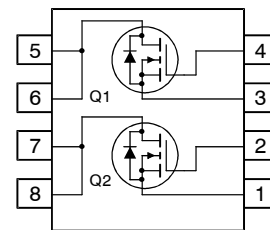
SOIC8
CASE 751EB

MARKING DIAGRAM



FDS6912A = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

PIN ASSIGNMENT



Dual N-Channel MOSFET

ORDERING INFORMATION

Device	Package	Shipping†
FDS6912A	SOIC8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDS6912A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	25	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55°C	–	–	1 10	μA
I _{GSS}	Gate–Source Leakage	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	–4.5	–	mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 6 A V _{GS} = 4.5 V, I _D = 5 A V _{GS} = 10 V, I _D = 6 A, T _J = 125°C	–	19 24 27	28 35 44	mΩ
I _{D(on)}	On–State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	20	–	–	A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 6 A	–	25	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	–	575	–	pF
C _{oss}	Output Capacitance		–	145	–	pF
C _{rss}	Reverse Transfer Capacitance		–	65	–	pF
R _G	Gate Resistance	V _{GS} = 15 mV, f = 1.0 MHz	–	2.1	–	Ω

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn–On Delay Time	V _{DD} = 15 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	8	16	ns
t _r	Turn–On Rise Time		–	5	10	ns
t _{d(off)}	Turn–Off Delay Time		–	23	37	ns
t _f	Turn–Off Fall Time		–	3	6	ns
Q _g	Total Gate Charge	V _{DS} = 15 V, I _D = 6 A, V _{GS} = 5 V	–	5.8	8.1	nC
Q _{gs}	Gate–Source Charge		–	1.7	–	nC
Q _{gd}	Gate–Drain Charge		–	2.1	–	nC

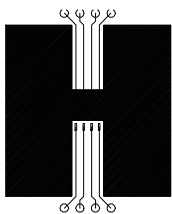
DRAIN–SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain–Source Diode Forward Current	–	–	1.3	A	
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.3 A (Note 2)	–	0.75	1.2	V
t _{rr}	Diode Reverse Recovery Time	I _F = 6 A, d _I /dt = 100 A/μs	–	20	–	ns
Q _{rr}	Diode Reverse Recovery Charge		–	10	–	nC

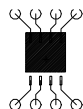
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

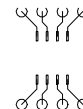
- R_{θJA} is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 78°C/W when mounted on a 0.5 in² pad of 2 oz copper



b. 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c. 135°C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

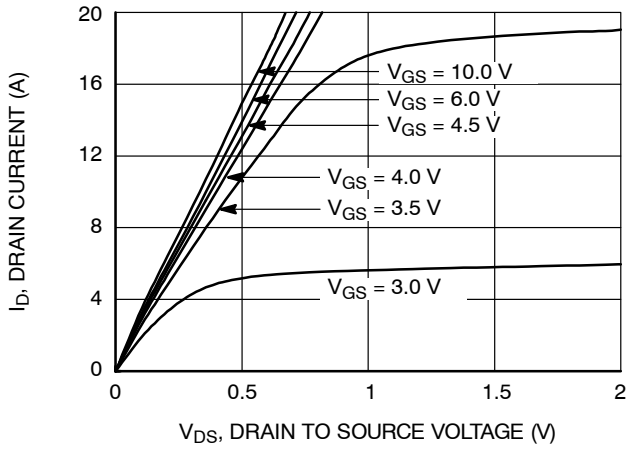


Figure 1. On-Region Characteristics

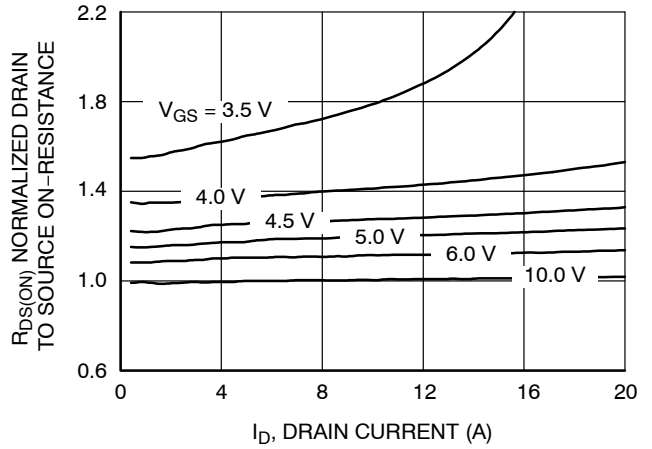


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

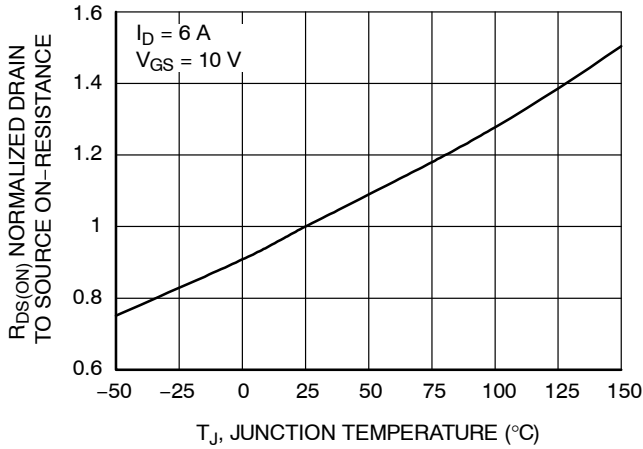


Figure 3. On-Resistance Variation with Temperature

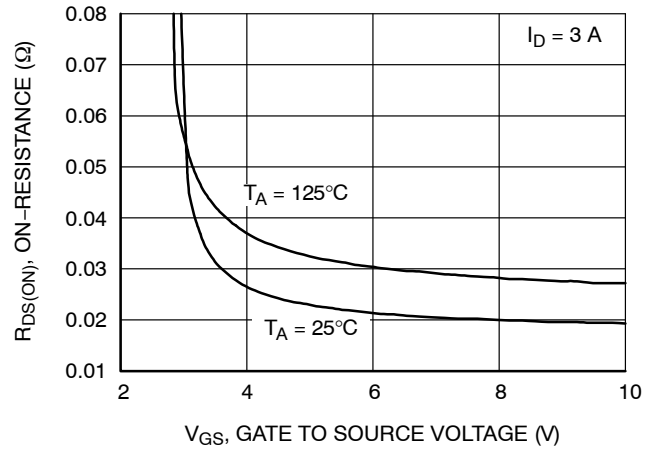


Figure 4. On-Resistance Variation with Gate to Source Voltage

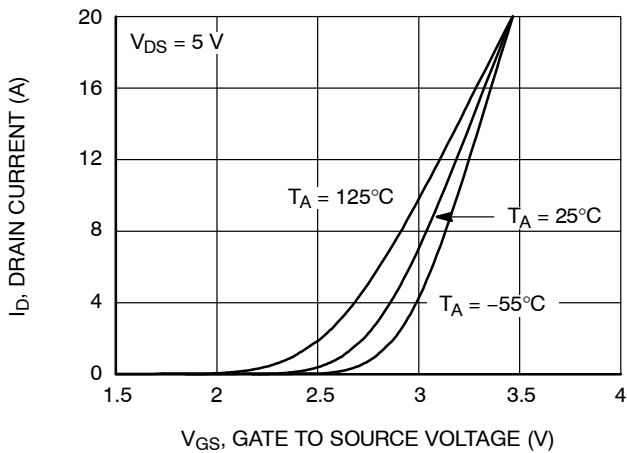


Figure 5. Transfer Characteristics

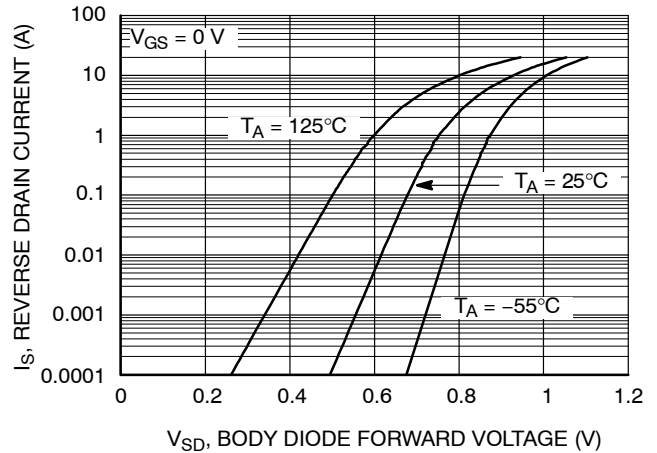


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

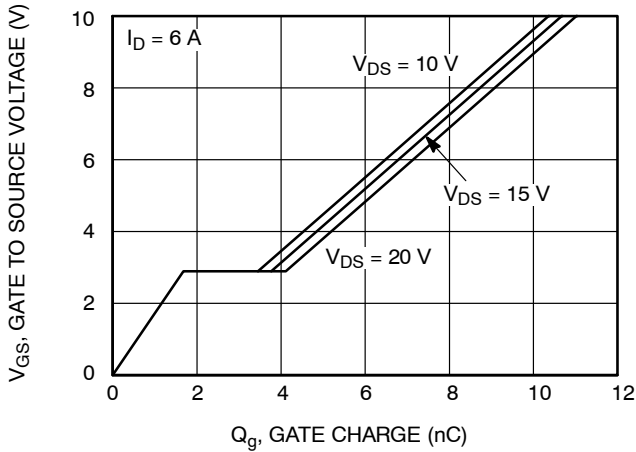


Figure 7. Gate Charge Characteristics

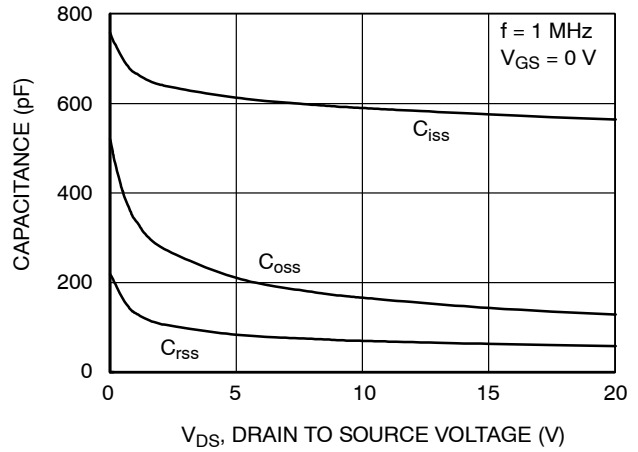


Figure 8. Capacitance Characteristics

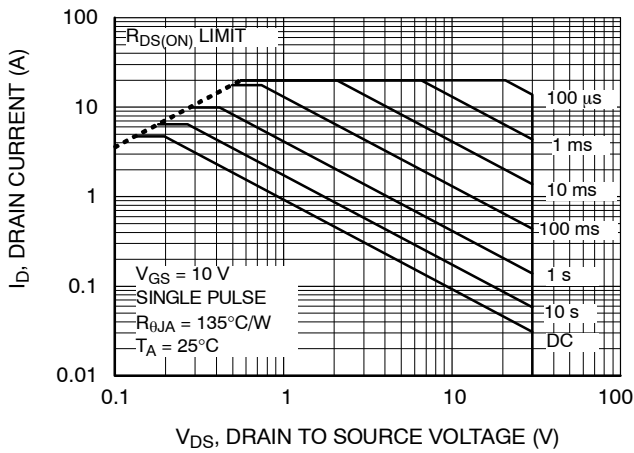


Figure 9. Maximum Safe Operating Area

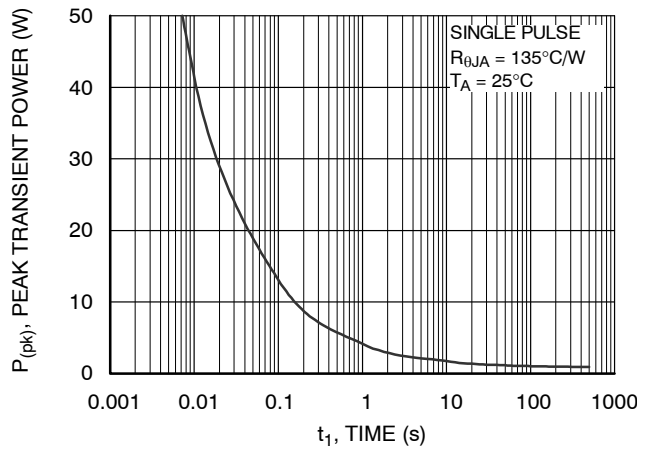


Figure 10. Single Pulse Maximum Power Dissipation

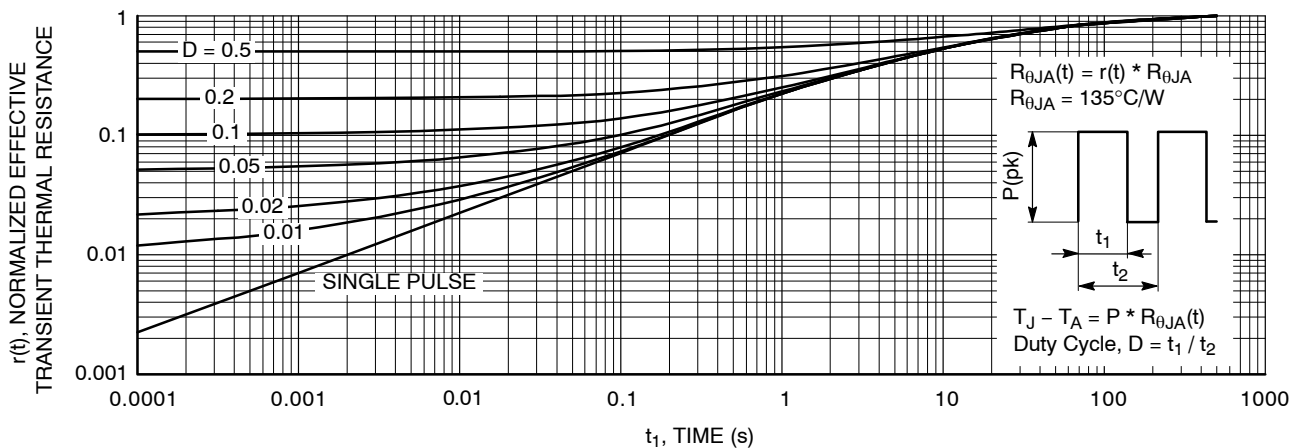


Figure 11. Transient Thermal Response Curve

(Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.)

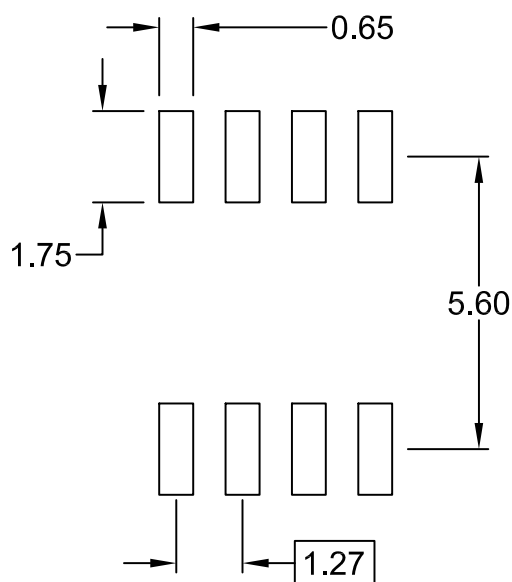
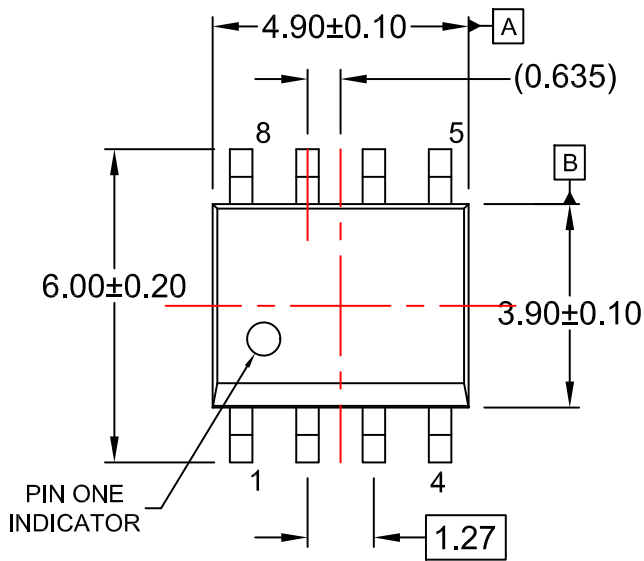
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

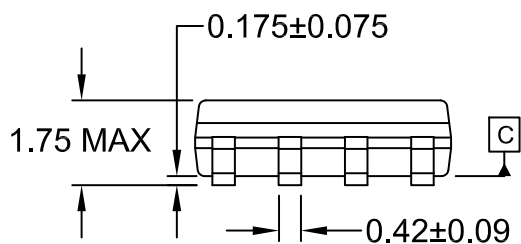


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CASE 751EB
ISSUE A

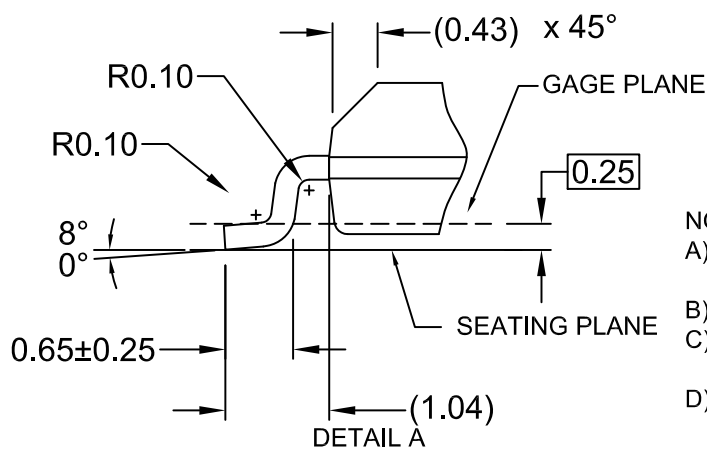
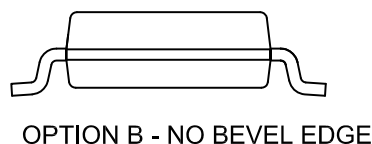
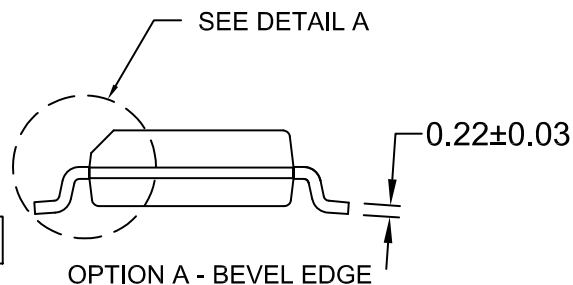
DATE 24 AUG 2017



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DETAIL A
 SCALE: 2:1

NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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