

MOSFET – N-Channel, POWERTRENCH®

150 V, 25 A, 34 mΩ

FDMC86260ET150

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Features

- Extended T_J Rating to 175°C
- Max R_{DS(on)} = 34 mΩ at V_{GS} = 10 V, I_D = 5.4 A
- Max R_{DS(on)} = 44 mΩ at V_{GS} = 6 V, I_D = 4.8 A
- High Performance Technology for Extremely Low R_{DS(on)}
- 100% UIL Tested
- Pb-Free, Halide Free and RoHS Compliant

Applications

- DC-DC Conversion

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

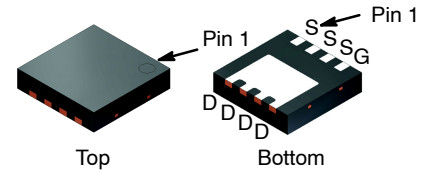
| Symbol | Parameter | Value | Unit |
|-----------------------------------|---|------------------------|------|
| V _{DS} | Drain to Source Voltage | 150 | V |
| V _{GS} | Gate to Source Voltage | ±20 | V |
| I _D | Drain Current: Continuous, T _C = 25°C (Note 5) Continuous, T _C = 100°C (Note 5) Continuous, T _A = 25°C (Note 1a) Pulsed (Note 4) | 25 18 5.4 116 | A |
| E _{AS} | Single Pulse Avalanche Energy (Note 3) | 121 | mJ |
| P _D | Power Dissipation: T _C = 25°C T _A = 25°C (Note 1a) | 65 2.8 | W |
| T _J , T _{STG} | Operating and Storage Junction Temperature Range | -55 to +175 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

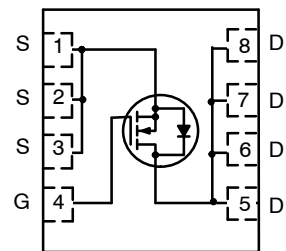
THERMAL CHARACTERISTICS

| Symbol | Parameter | Value | Unit |
|------------------|---|-------|------|
| R _{θJC} | Thermal Resistance, Junction to Case (Note 1) | 2.3 | °C/W |
| R _{θJA} | Thermal Resistance, Junction to Ambient (Note 1a) | 53 | °C/W |

| V _{DS} | R _{DS(on)} MAX | I _D MAX |
|-----------------|-------------------------|--------------------|
| 150 V | 34 mΩ @ 10 V | 25 A |
| | 44 mΩ @ 6 V | |

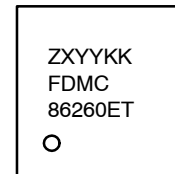


WDFN8 3.3 × 3.3, 0.65P
(Power 33)
CASE 483AW



N-CHANNEL MOSFET

MARKING DIAGRAM



Z = Assembly Plant Code
 XYY = 3-Digit Date Code Format
 KK = 2-Alphanumeric Lot Run Traceability Code
 FDMC86260ET = Specific Device Code

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|------------------------------|--------------------|
| FDMC86260ET150 | PQFN8 (Pb-Free, Halide Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|--------|-----------|----------------|-----|-----|-----|------|
|--------|-----------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|--------------------------------------|---|--|-----|-----|------|-------|
| BV _{DSS} | Drain to Source Breakdown Voltage | I _D = 250 μA, V _{GS} = 0 V | 150 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | I _D = 250 μA, referenced to 25°C | – | 110 | – | mV/°C |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 120 V, V _{GS} = 0 V | – | – | 1 | μA |
| I _{GSS} | Gate to Source Leakage Current | V _{GS} = ±20 V, V _{DS} = 0 V | – | – | ±100 | nA |

ON CHARACTERISTICS

| | | | | | | |
|--|--|--|---|-----|----|-------|
| V _{GS(th)} | Gate to Source Threshold Voltage | V _{GS} = V _{DS} , I _D = 250 μA | 2 | 2.7 | 4 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | I _D = 250 μA, referenced to 25°C | – | –9 | – | mV/°C |
| R _{DS(on)} | Static Drain to Source On Resistance | V _{GS} = 10 V, I _D = 5.4 A | – | 27 | 34 | mΩ |
| | | V _{GS} = 6 V, I _D = 4.8 A | – | 31 | 44 | |
| | | V _{GS} = 10 V, I _D = 5.4 A, T _J = 125°C | – | 55 | 69 | |
| g _{FS} | Forward Transconductance | V _{DD} = 10 V, I _D = 5.4 A | – | 19 | – | S |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|------------------|------------------------------|--|-----|------|------|----|
| C _{iss} | Input Capacitance | V _{DS} = 75 V, V _{GS} = 0 V, f = 1 MHz | – | 1000 | 1330 | pF |
| C _{oss} | Output Capacitance | | – | 105 | 140 | pF |
| C _{rss} | Reverse Transfer Capacitance | | – | 4.8 | 10 | pF |
| R _g | Gate Resistance | | 0.1 | 0.6 | 1.8 | Ω |

SWITCHING CHARACTERISTICS

| | | | | | | |
|---------------------|-------------------------------|--|---|-----|----|----|
| t _{d(on)} | Turn-On Delay Time | V _{DD} = 75 V, I _D = 5.4 A, V _{GS} = 10 V, R _{GEN} = 6 Ω | – | 9.5 | 19 | ns |
| t _r | Rise Time | | – | 2 | 10 | ns |
| t _{d(off)} | Turn-Off Delay Time | | – | 17 | 30 | ns |
| t _f | Fall Time | | – | 3.3 | 10 | ns |
| Q _{g(TOT)} | Total Gate Charge | V _{GS} = 0 V to 10 V, V _{DD} = 75 V, I _D = 5.4 A | – | 15 | 21 | nC |
| | | V _{GS} = 0 V to 6 V, V _{DD} = 75 V, I _D = 5.4 A | – | 9.7 | 14 | nC |
| Q _{gs} | Total Gate Charge | V _{DD} = 75 V, I _D = 5.4 A | – | 4.0 | – | nC |
| Q _{gd} | Gate to Drain "Miller" Charge | V _{DD} = 75 V, I _D = 5.4 A | – | 3.1 | – | nC |

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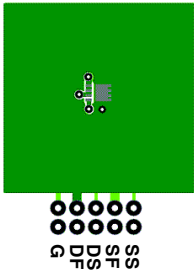
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------------------|--|-----|------|-----|------|
| DRAIN-SOURCE DIODE CHARACTERISTICS | | | | | | |
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 5.4\text{ A}$ (Note 2) | – | 0.77 | 1.3 | V |
| | | $V_{GS} = 0\text{ V}, I_S = 1.9\text{ A}$ (Note 2) | – | 0.72 | 1.2 | |
| t_{rr} | Reverse Recovery Time | $I_F = 5.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | – | 64 | 102 | ns |
| Q_{rr} | Reverse Recovery Charge | | – | 85 | 137 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) $53^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- E_{AS} of 121 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 9\text{ A}$, $V_{DD} = 150\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 22\text{ A}$.
- Pulsed I_d please refer to Figure 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

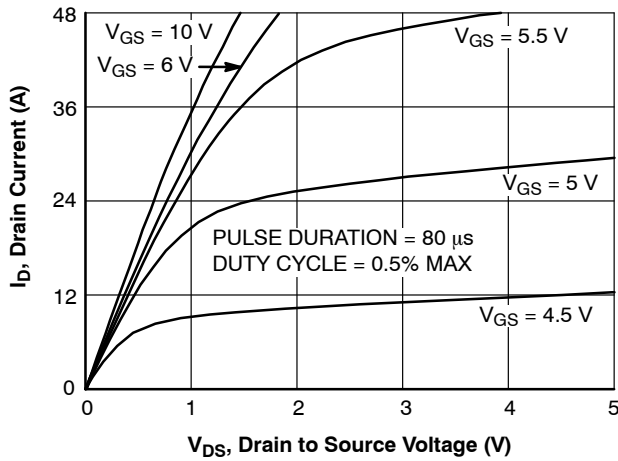


Figure 1. On-Region Characteristics

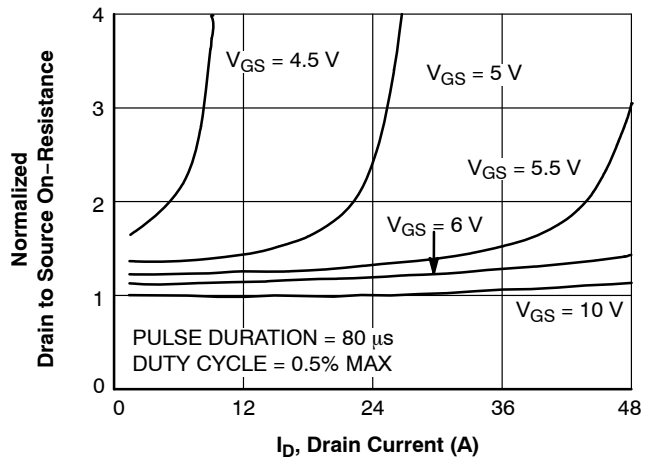


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

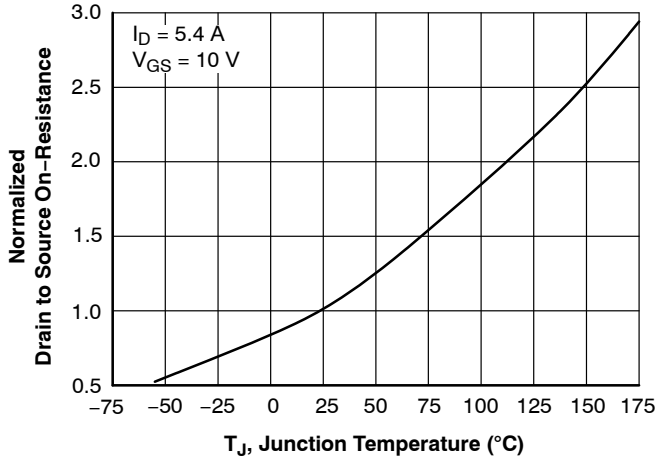


Figure 3. Normalized On-Resistance vs. Junction Temperature

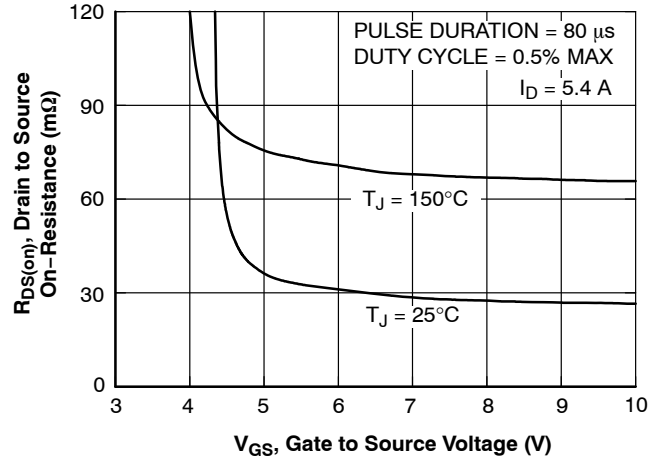


Figure 4. On-Resistance vs. Gate to Source Voltage

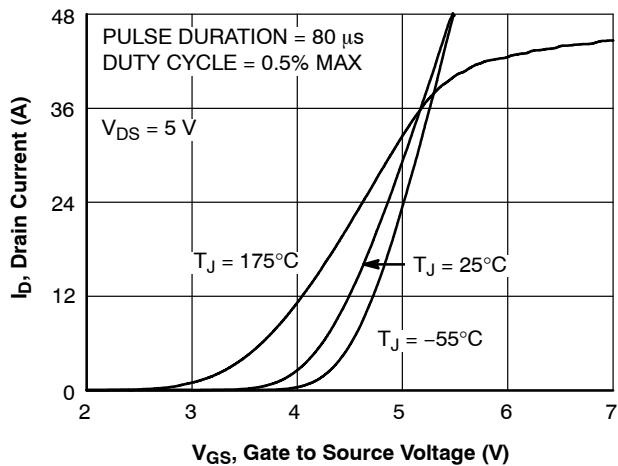


Figure 5. Transfer Characteristics

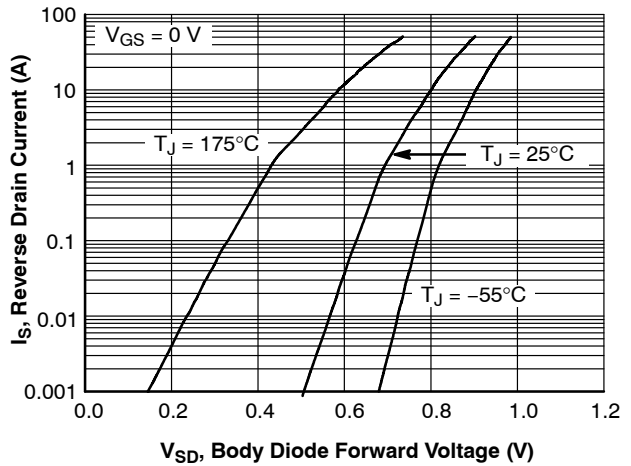


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

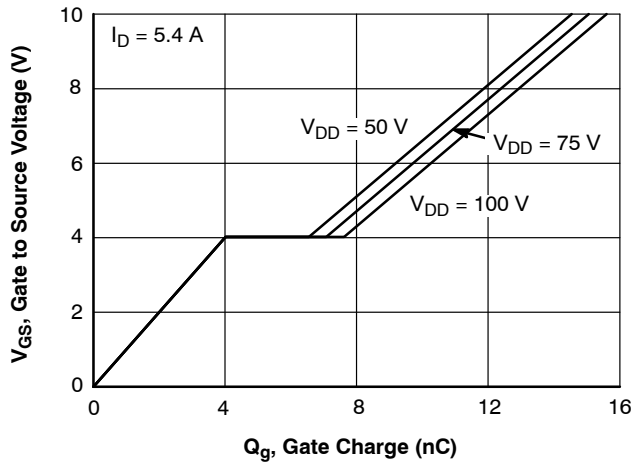


Figure 7. Gate Charge Characteristics

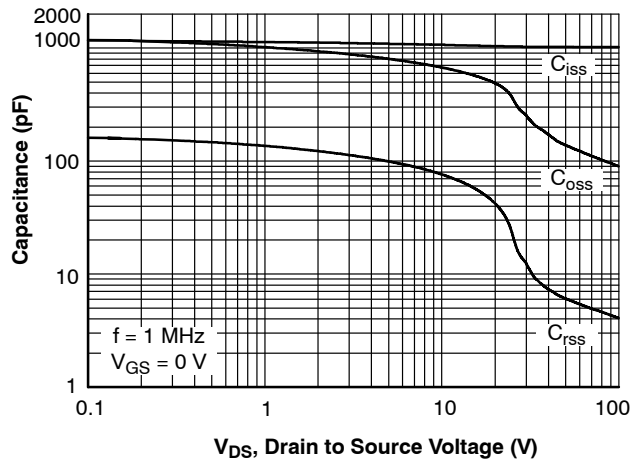


Figure 8. Capacitance vs. Drain to Source Voltage

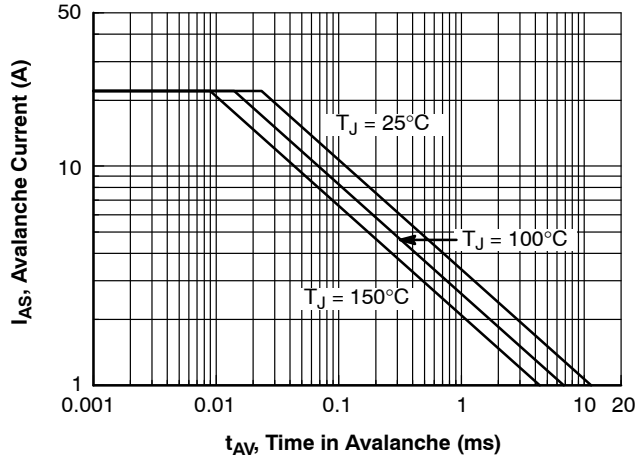


Figure 9. Unclamped Inductive Switching Capability

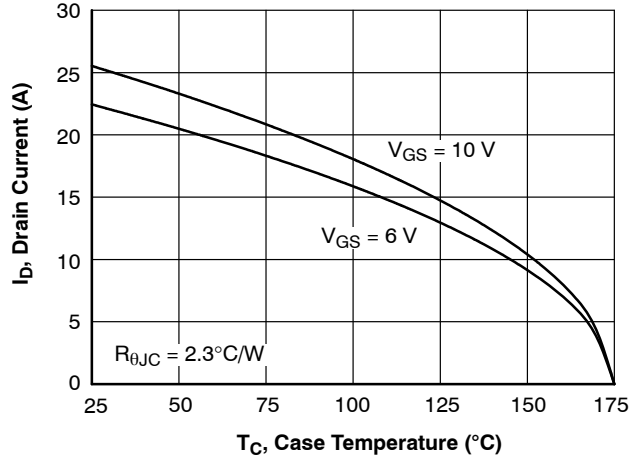


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

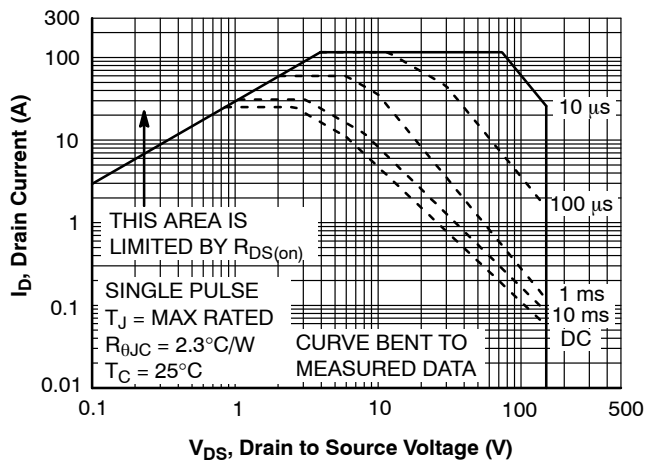


Figure 11. Forward Bias Safe Operating Area

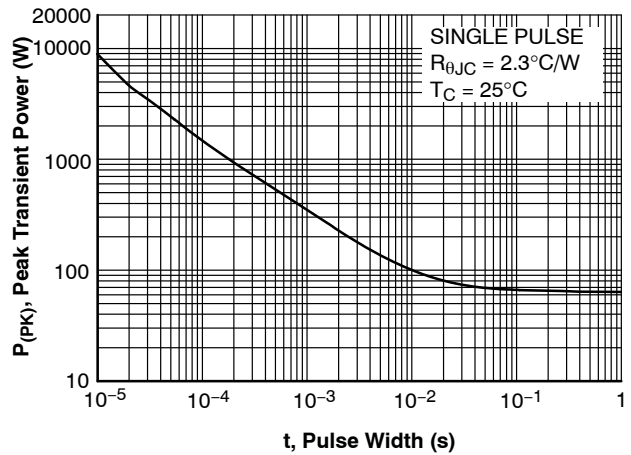


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

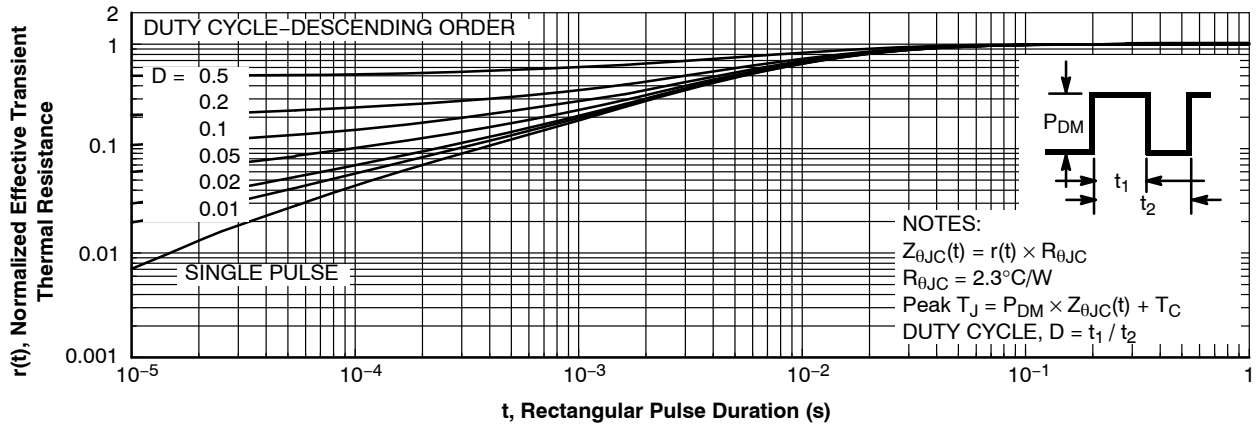
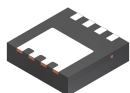


Figure 13. Junction-to-Case Transient Thermal Response Curve

MECHANICAL CASE OUTLINE

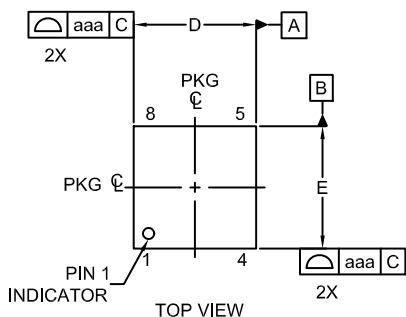
PACKAGE DIMENSIONS

ON Semiconductor®

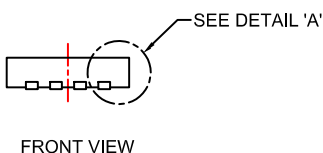


WDFN8 3.3X3.3, 0.65P
CASE 483AW
ISSUE A

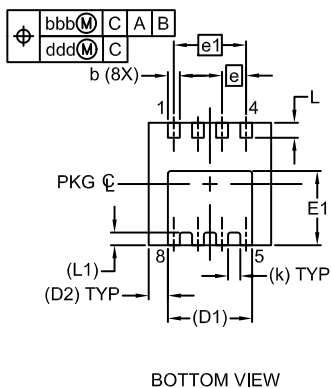
DATE 10 SEP 2019



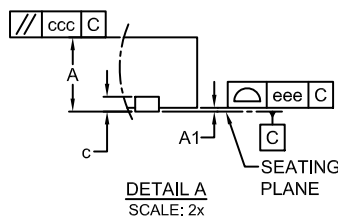
TOP VIEW



FRONT VIEW

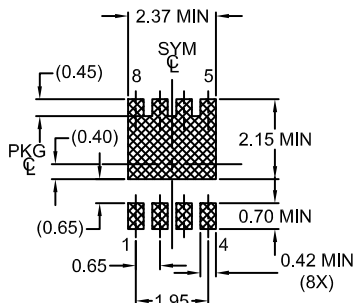


BOTTOM VIEW



DETAIL A
SCALE: 2x

LAND PATTERN RECOMMENDATION*



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | - | - | 0.05 |
| b | 0.27 | 0.32 | 0.37 |
| c | 0.15 | 0.20 | 0.25 |
| D | 3.20 | 3.30 | 3.40 |
| D1 | 2.27 REF | | |
| D2 | 0.52 REF | | |
| E | 3.20 | 3.30 | 3.40 |
| E1 | 1.85 | 1.95 | 2.05 |
| e | 0.65 BSC | | |
| e1 | 1.95 BSC | | |
| k | 0.33 REF | | |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.34 REF | | |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.05 | | |

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|-----------------------------|--|
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| DESCRIPTION: | WDFN8 3.3X3.3, 0.65P | PAGE 1 OF 1 |

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