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# FDMC013P030Z

## P-Channel PowerTrench<sup>®</sup> MOSFET

-30 V, -54 A, 7.0 mΩ

### Features

- Max  $r_{DS(on)}$  = 7.0 mΩ at  $V_{GS} = -10$  V,  $I_D = -14$  A
- Max  $r_{DS(on)}$  = 12.0 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -10$  A
- High Performance Trench Technology for Extremely Low  $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Termination is Lead-free and RoHS Compliant
- HBM ESD Capability Level > 4 kV Typical (Note 4)

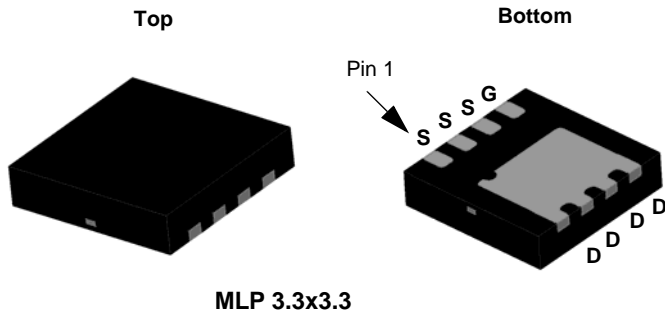


### General Description

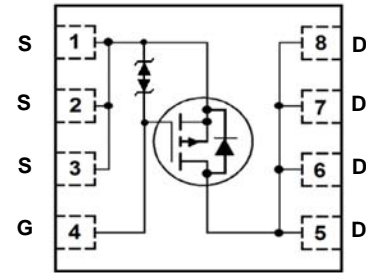
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Applications

- Battery Management
- Load Switch



MLP 3.3x3.3



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-30	V
$V_{GS}$	Gate to Source Voltage	±25	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C (Note 5)	-54	A
	Drain Current -Continuous $T_C = 100$ °C (Note 5)	-35	
	-Continuous $T_A = 25$ °C (Note 1a)	-14	
	-Pulsed (Note 4)	-309	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	54	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	30	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.4	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC013P030Z	FDMC013P030Z	MLP 3.3x3.3	13 "	12 mm	3000 units

FDMC013P030Z P-Channel PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-13		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\ \text{V}, V_{GS} = 0\ \text{V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 25\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-1	-1.6	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\ \text{V}, I_D = -14\ \text{A}$		5.0	7.0	m $\Omega$
		$V_{GS} = -4.5\ \text{V}, I_D = -10\ \text{A}$		8.0	12.0	
		$V_{GS} = -10\ \text{V}, I_D = -14\ \text{A}, T_J = 125^\circ\text{C}$		6.2	10.4	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\ \text{V}, I_D = -14\ \text{A}$		60		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -15\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1\ \text{MHz}$		4130	5785	pF
$C_{oss}$	Output Capacitance			1355	1895	pF
$C_{rss}$	Reverse Transfer Capacitance			1335	1870	pF

### Switching Characteristics

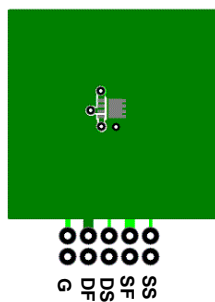
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\ \text{V}, I_D = -14\ \text{A},$ $V_{GS} = -4.5\ \text{V}, R_{GEN} = 6\ \Omega$		34	55	ns	
$t_r$	Rise Time			157	251	ns	
$t_{d(off)}$	Turn-Off Delay Time			55	88	ns	
$t_f$	Fall Time			94	150	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\ \text{V to } -10\ \text{V}$		96	135	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V to } -4.5\ \text{V}$	$V_{DD} = -15\ \text{V},$ $I_D = -14\ \text{A}$		58	81	nC
$Q_{gs}$	Gate to Source Charge				11		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				36		nC

### Drain-Source Diode Characteristics

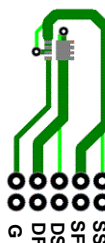
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = -14\ \text{A}$ (Note 2)		-0.8	-1.3	V
		$V_{GS} = 0\ \text{V}, I_S = -2\ \text{A}$ (Note 2)		-0.7	-1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = -14\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		44	77	ns
$Q_{rr}$	Reverse Recovery Charge			23	37	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a)  $53^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

3.  $E_{AS}$  of 54 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\ \text{mH}$ ,  $I_{AS} = 6\ \text{A}$ ,  $V_{DD} = 30\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ .

4. Pulsed Id please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

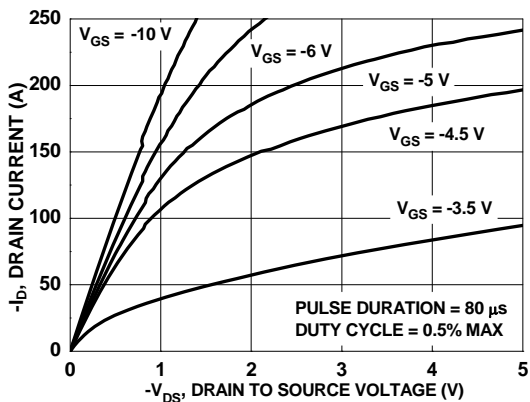


Figure 1. On Region Characteristics

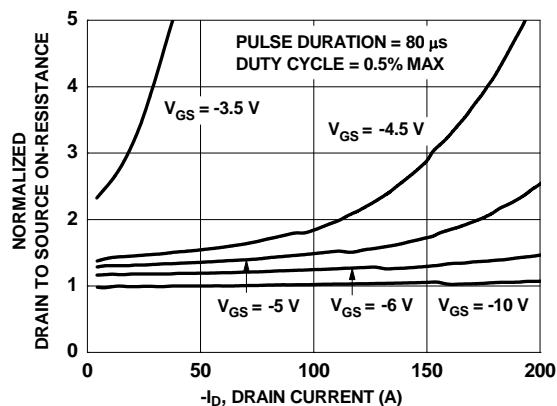


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

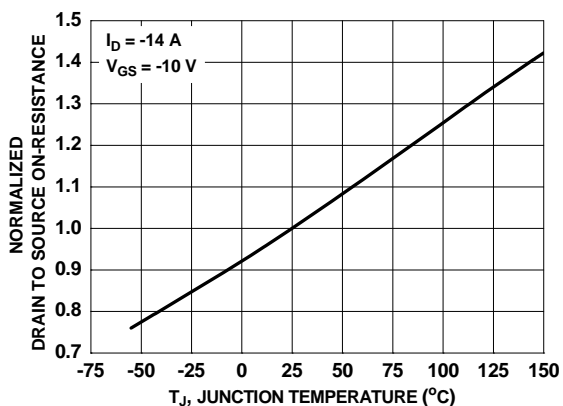


Figure 3. Normalized On Resistance vs. Junction Temperature

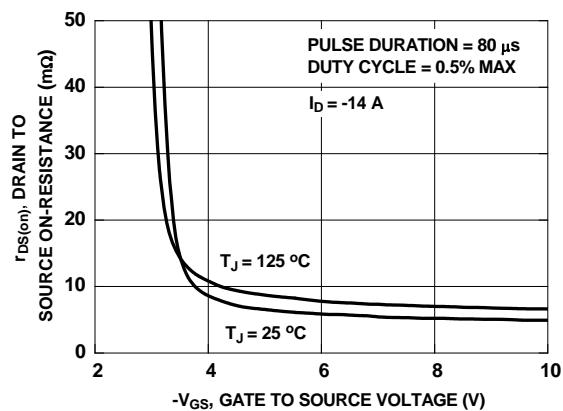


Figure 4. On-Resistance vs. Gate to Source Voltage

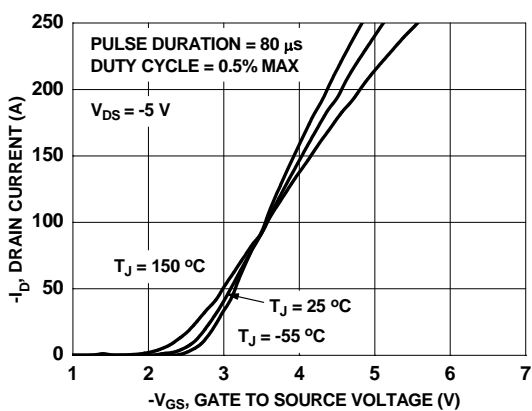


Figure 5. Transfer Characteristics

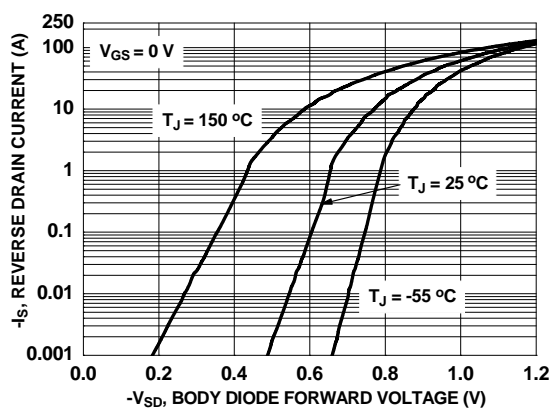
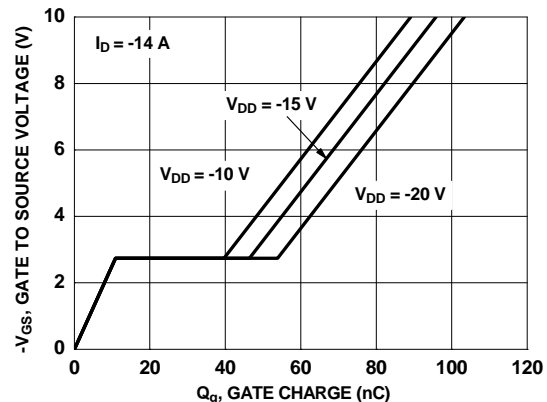
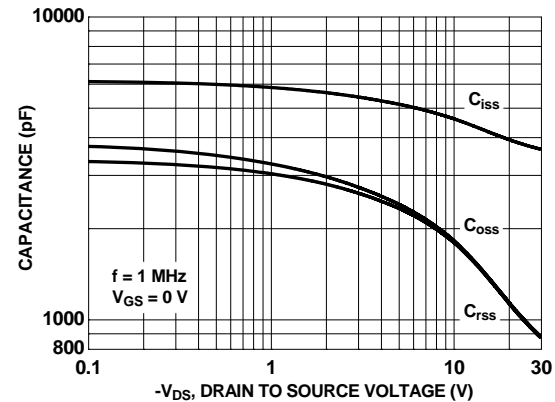


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

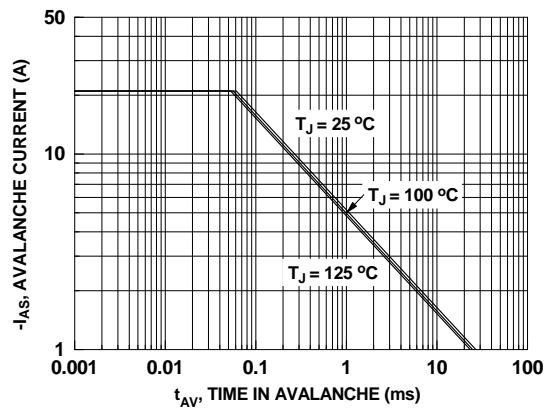
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



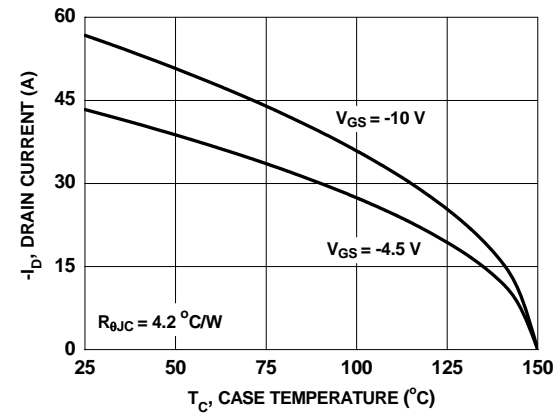
**Figure 7. Gate Charge Characteristics**



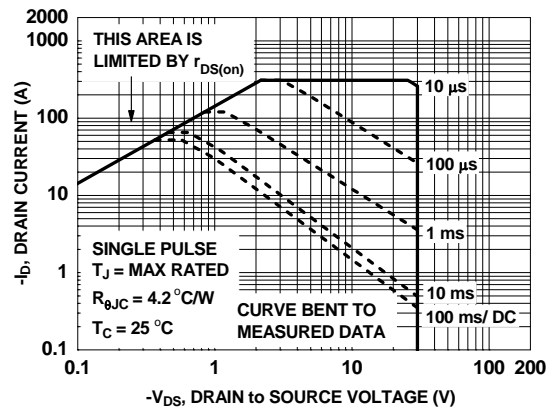
**Figure 8. Capacitance vs. Drain to Source Voltage**



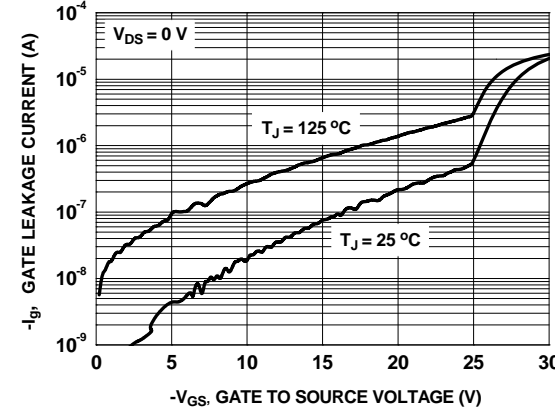
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

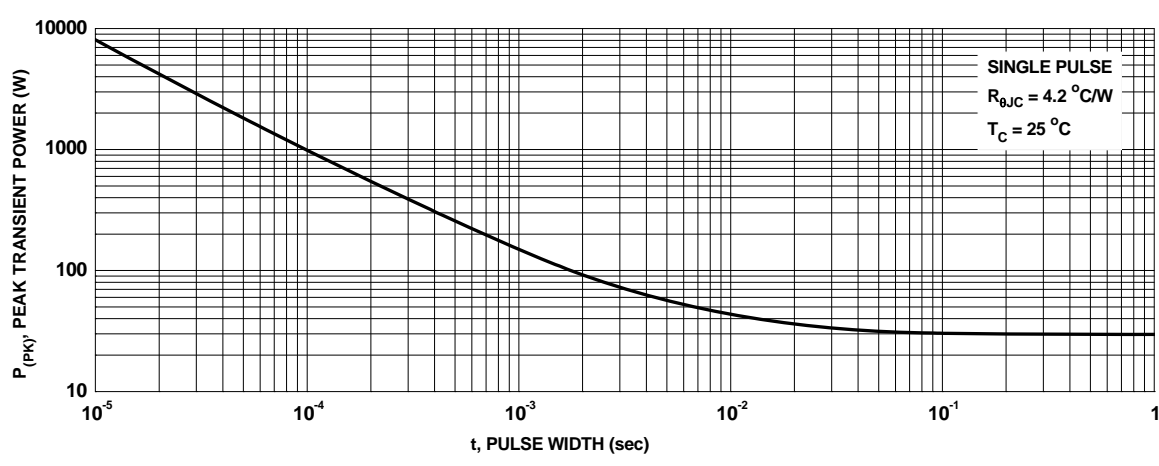


**Figure 11. Forward Bias Safe Operating Area**

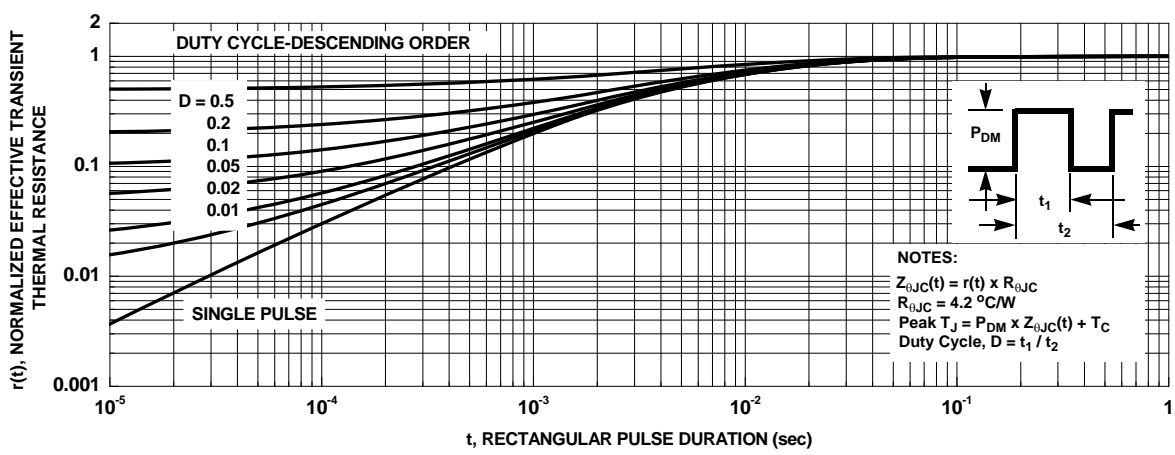


**Figure 12. I<sub>gss</sub> vs. V<sub>gs</sub>**

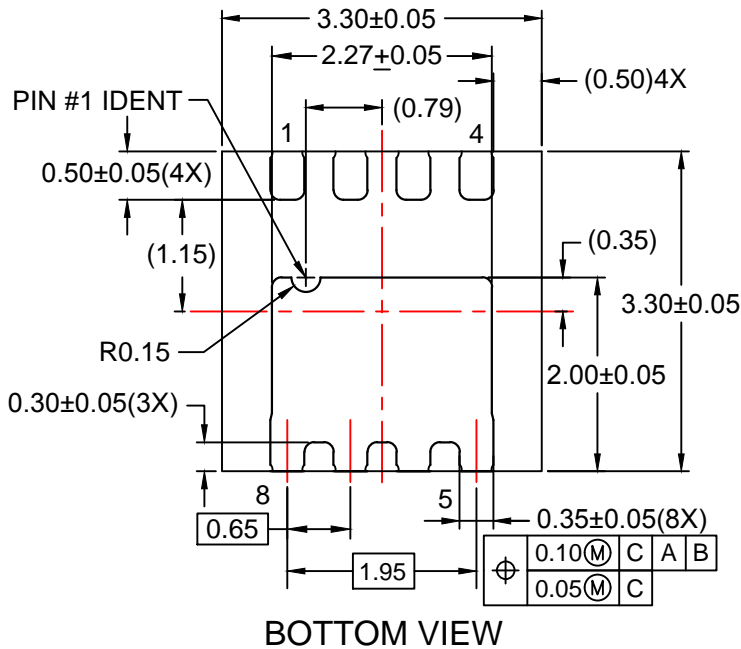
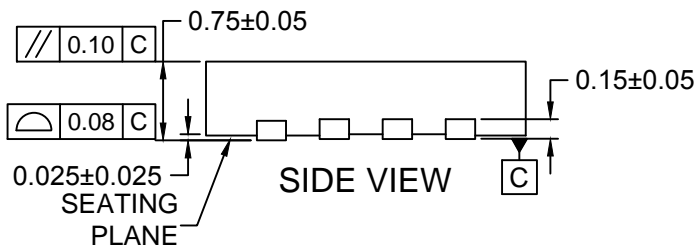
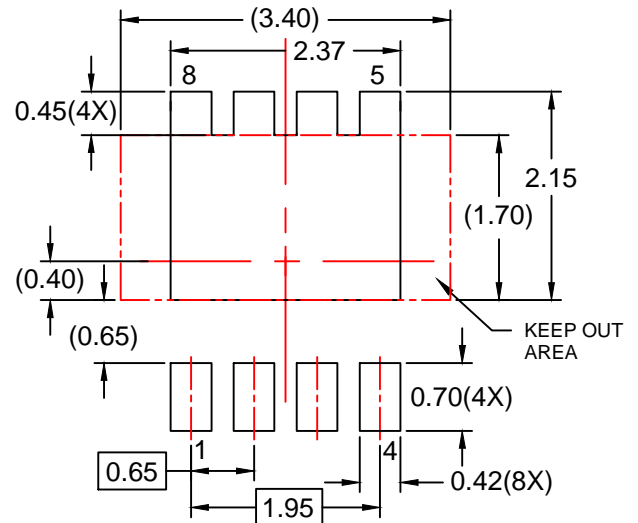
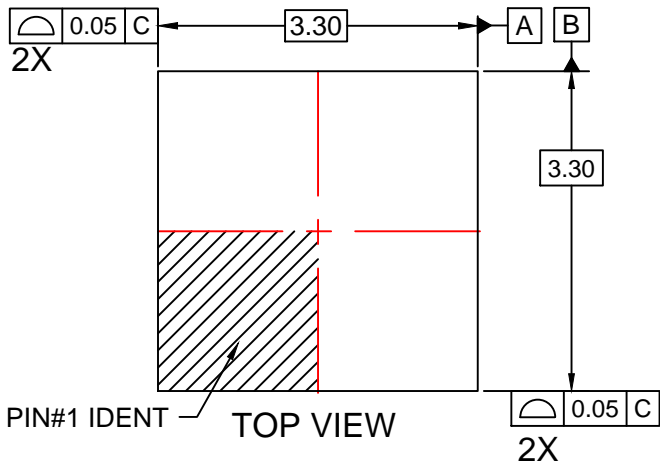
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



**Figure 13. Single Pulse Maximum Power Dissipation**



**Figure 14. Junction to Case Transient Thermal Response Curve**



**NOTES:**

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
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