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# FDMA908PZ

## Single P-Channel PowerTrench<sup>®</sup> MOSFET

-12 V, -12 A, 12.5 mΩ

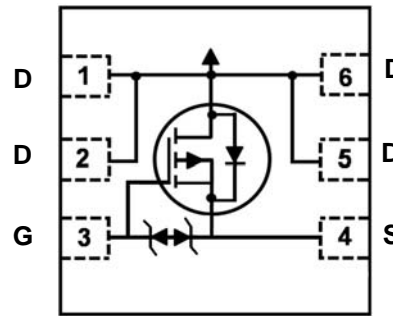
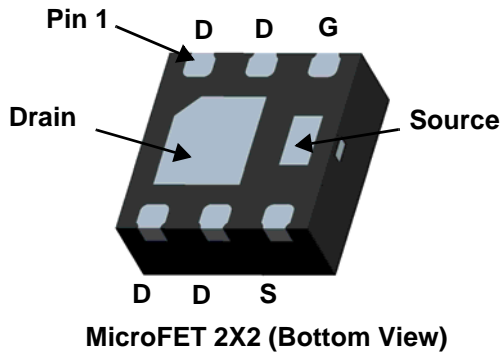
### Features

- Max  $r_{DS(on)}$  = 12.5 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -12$  A
- Max  $r_{DS(on)}$  = 18 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -10$  A
- Max  $r_{DS(on)}$  = 28 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -8$  A
- Low Profile - 0.8 mm maximum in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2.8 kV typical (Note 3)
- Free from halogenated compounds and antimony oxides
- RoHS Compliant



### General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance and zener diode protection against ESD. The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-12	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	Drain Curre -Continuous $T_A = 25$ °C (Note 1a)	-12	A
	-Pulsed	-40	
$P_D$	Power Dissipation $T_A = 25$ °C (Note 1a)	2.4	W
	Power Dissipation $T_A = 25$ °C (Note 1b)	0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
908	FDMA908PZ	MicroFET 2X2	7"	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	-12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-10		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -9.6\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	-0.4	-0.6	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		2.8		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{ V}$ , $I_D = -12\text{ A}$		10	12.5	m $\Omega$
		$V_{GS} = -2.5\text{ V}$ , $I_D = -10\text{ A}$		13	18	
		$V_{GS} = -1.8\text{ V}$ , $I_D = -8\text{ A}$		18	28	
		$V_{GS} = -4.5\text{ V}$ , $I_D = -12\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		13	16	
$g_{FS}$	Forward Transconductance	$V_{DD} = -5\text{ V}$ , $I_D = -12\text{ A}$		63		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -6\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		2638	3957	pF
$C_{oss}$	Output Capacitance			649	974	pF
$C_{rss}$	Reverse Transfer Capacitance			602	903	pF

### Switching Characteristics

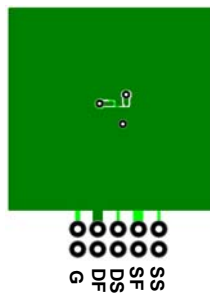
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -6\text{ V}$ , $I_D = -12\text{ A}$ , $V_{GS} = -4.5\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		11	21	ns
$t_r$	Rise Time			12	23	ns
$t_{d(off)}$	Turn-Off Delay Time			131	223	ns
$t_f$	Fall Time			71	121	ns
$Q_g$	Total Gate Charge		$V_{GS} = -4.5\text{ V}$ , $V_{DD} = -6\text{ V}$ , $I_D = -12\text{ A}$		24	34
$Q_{gs}$	Gate to Source Charge			3.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5.3		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -2\text{ A}$ (Note 2)		-0.6	-1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = -12\text{ A}$ (Note 2)		-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		26	42	ns
$Q_{rr}$	Reverse Recovery Charge			8.5	17	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $52\text{ }^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



b.  $145\text{ }^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

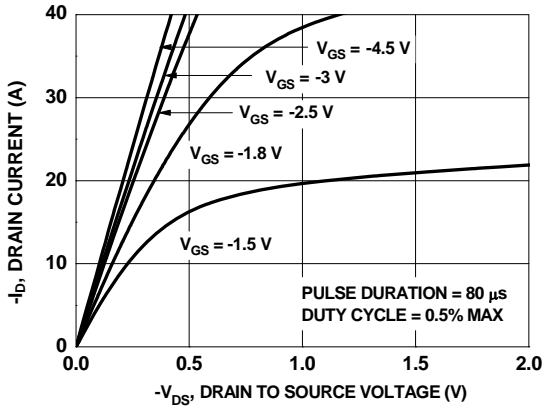


Figure 1. On-Region Characteristics

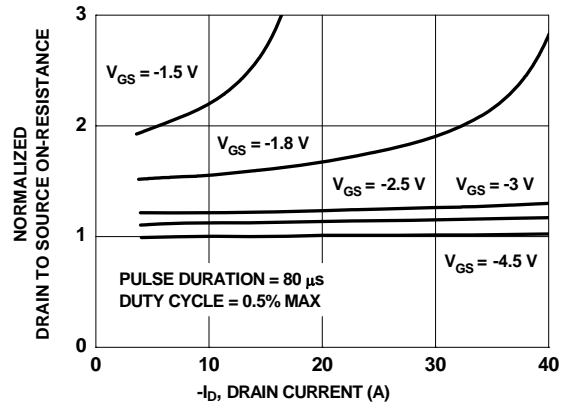


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

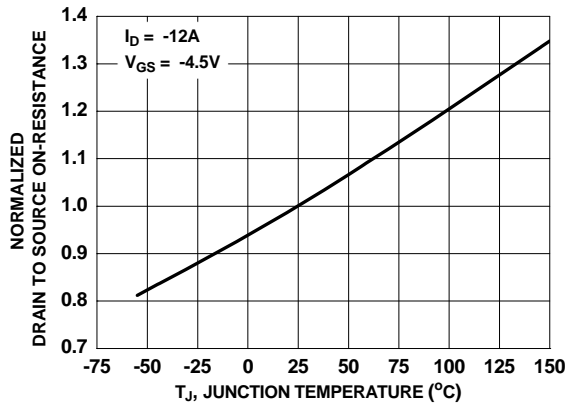


Figure 3. Normalized On-Resistance vs Junction Temperature

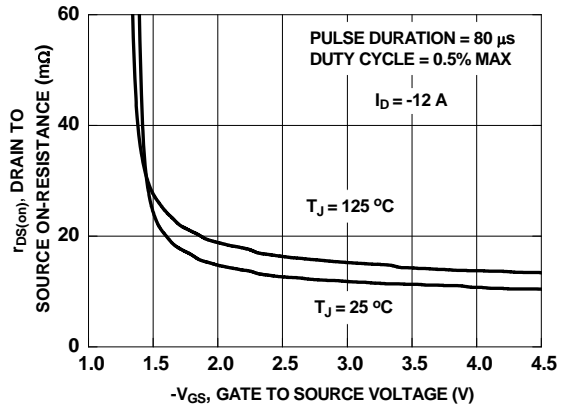


Figure 4. On-Resistance vs Gate to Source Voltage

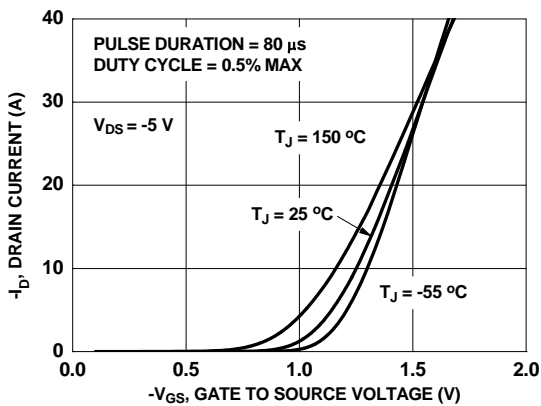


Figure 5. Transfer Characteristics

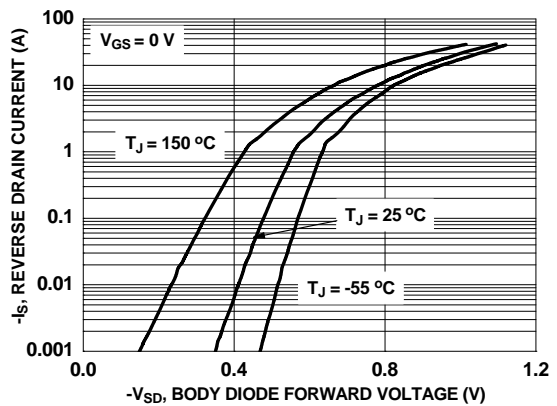
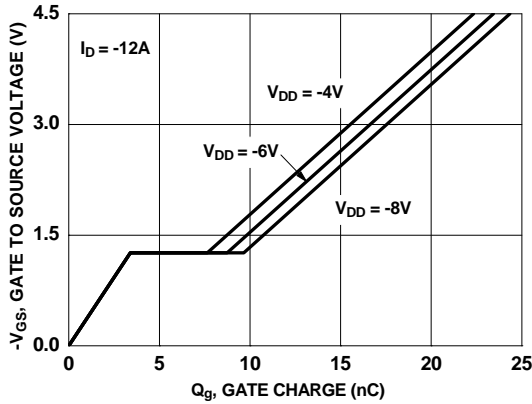
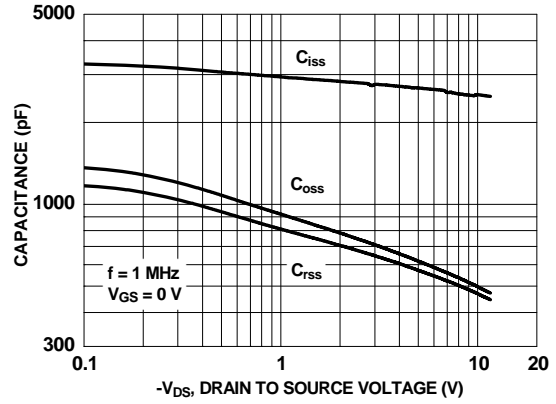


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

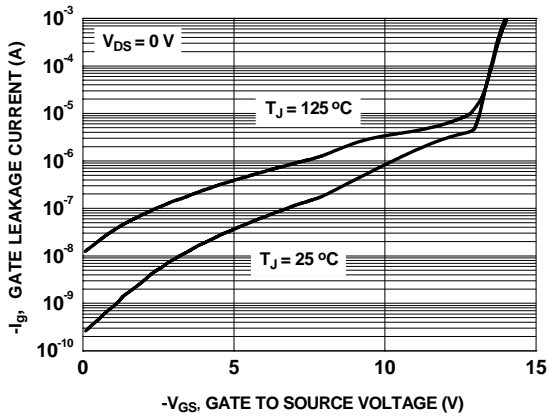
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



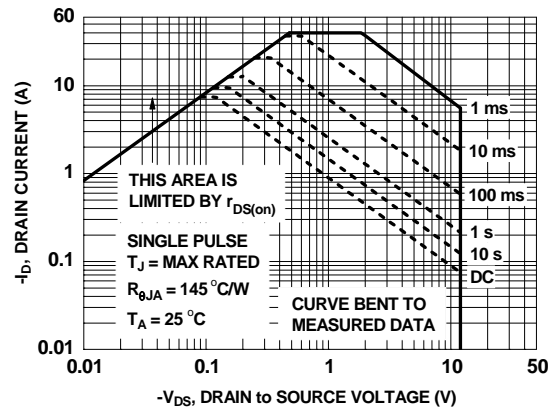
**Figure 7. Gate Charge Characteristics**



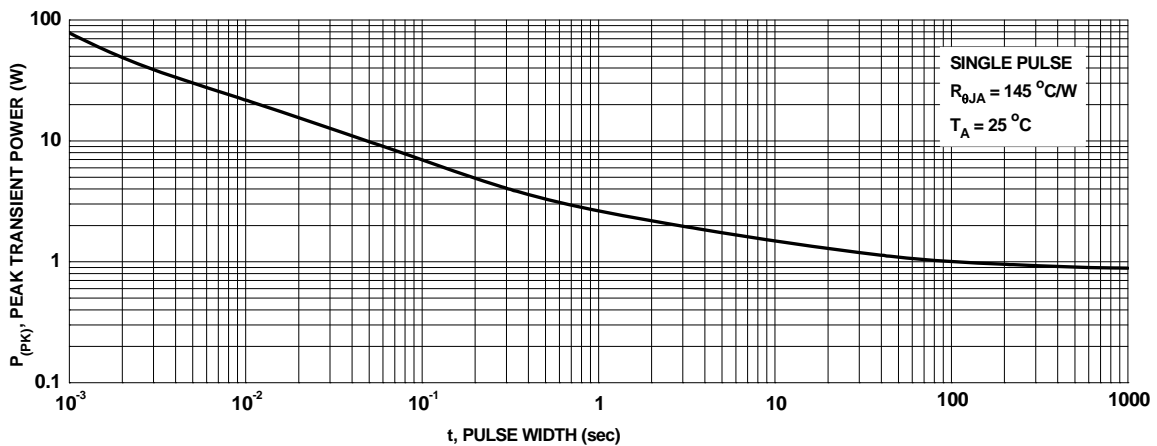
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Gate Leakage Current vs Gate to Source Voltage**

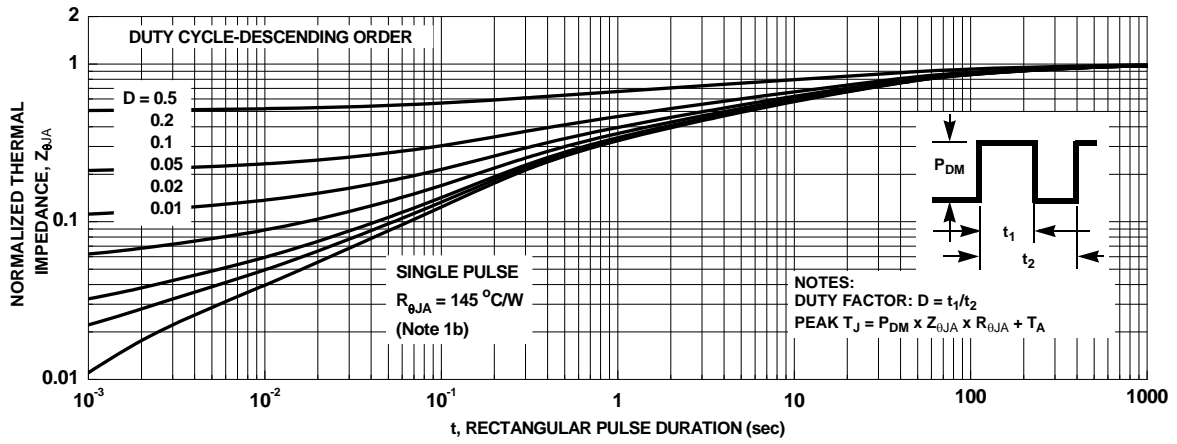


**Figure 10. Gate Leakage Current vs Gate to Source Voltage**

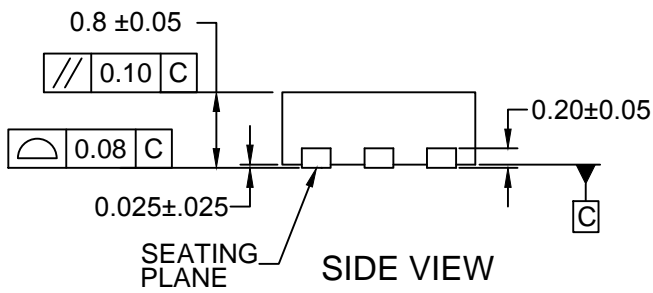
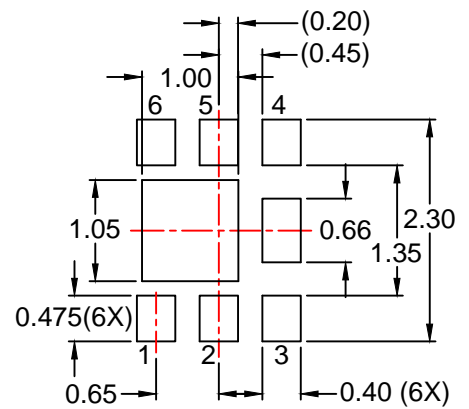
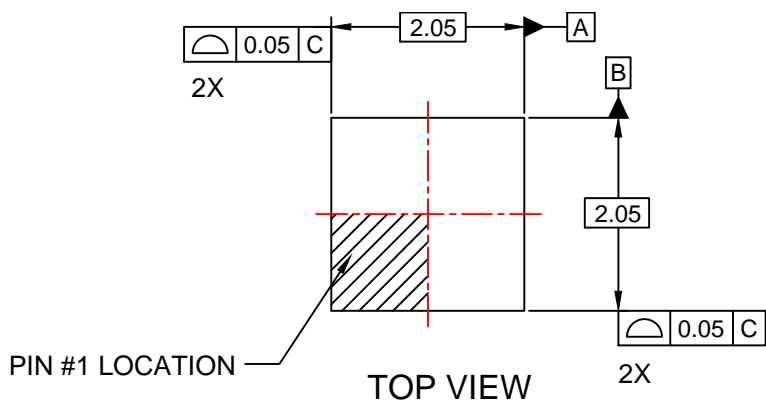


**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

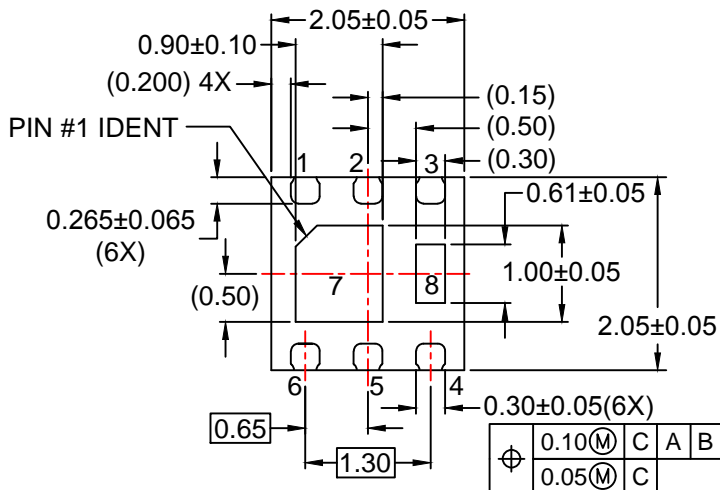


**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**



### RECOMMENDED LAND PATTERN

Pin #	Function
1	Drain
2	Drain
3	Gate
4	Source
5	Drain
6	Drain
7	Drain
8	Source



### NOTES:

- PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
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- REFERENCE DRAWING NO : MKT-MLP06Prev1.



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