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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

February 2014

FDMA908PZ

Single P-Channel PowerTrench® MOSFET

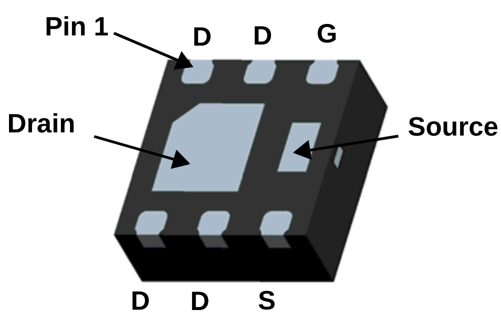
-12 V, -12 A, 12.5 mΩ

Features

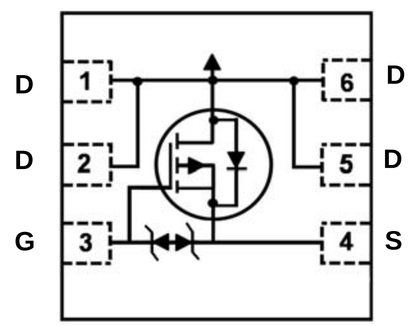
- Max $r_{DS(on)}$ = 12.5 mΩ at V_{GS} = -4.5 V, I_D = -12 A
- Max $r_{DS(on)}$ = 18 mΩ at V_{GS} = -2.5 V, I_D = -10 A
- Max $r_{DS(on)}$ = 28 mΩ at V_{GS} = -1.8 V, I_D = -8 A
- Low Profile - 0.8 mm maximum in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2.8 kV typical (Note 3)
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance and zener diode protection against ESD. The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.



MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-12	V
V_{GS}	Gate to Source Voltage			±8	V
I_D	Drain Curre -Continuous	T_A = 25 °C	(Note 1a)	-12	A
	-Pulsed			-40	
P_D	Power Dissipation	T_A = 25 °C	(Note 1a)	2.4	W
	Power Dissipation	T_A = 25 °C	(Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	145	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
908	FDMA908PZ	MicroFET 2X2	7 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-10		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -9.6 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±10	μA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-0.4	-0.6	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		2.8		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -4.5 V, I_D = -12 A		10	12.5	mΩ
		V_{GS} = -2.5 V, I_D = -10 A		13	18	
		V_{GS} = -1.8 V, I_D = -8 A		18	28	
		V_{GS} = -4.5 V, I_D = -12 A, T_J = 125 °C		13	16	
g_{FS}	Forward Transconductance	V_{DD} = -5 V, I_D = -12 A		63		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = -6 V, V_{GS} = 0 V, f = 1 MHz		2638	3957	pF
C_{oss}	Output Capacitance			649	974	pF
C_{rss}	Reverse Transfer Capacitance			602	903	pF

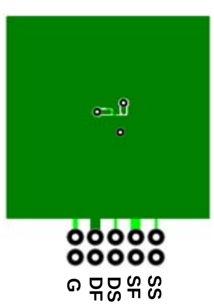
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -6 V, I_D = -12 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		11	21	ns
t_r	Rise Time			12	23	ns
$t_{d(off)}$	Turn-Off Delay Time			131	223	ns
t_f	Fall Time			71	121	ns
Q_g	Total Gate Charge	V_{GS} = -4.5 V, V_{DD} = -6 V, I_D = -12 A		24	34	nC
Q_{gs}	Gate to Source Charge			3.4		nC
Q_{gd}	Gate to Drain “Miller” Charge			5.3		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -2 A (Note 2)		-0.6	-1.2	V
		V_{GS} = 0 V, I_S = -12 A (Note 2)		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -12 A, di/dt = 100 A/μs		26	42	ns
Q_{rr}	Reverse Recovery Charge			8.5	17	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 52 °C/W when mounted on a 1 in^2 pad of 2 oz copper.

b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

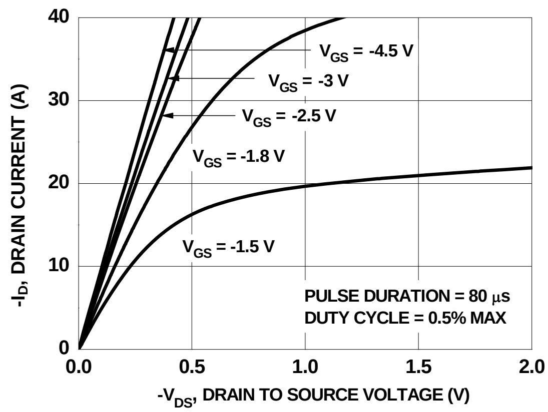


Figure 1. On-Region Characteristics

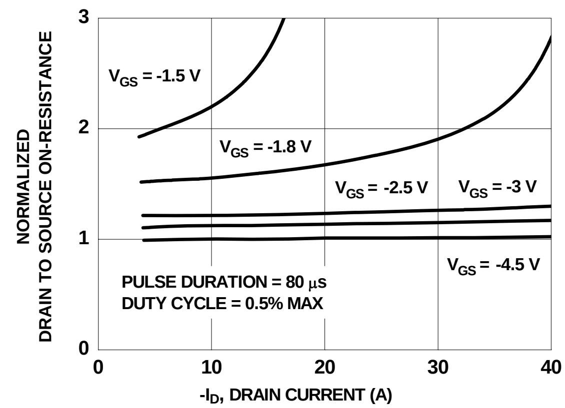


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

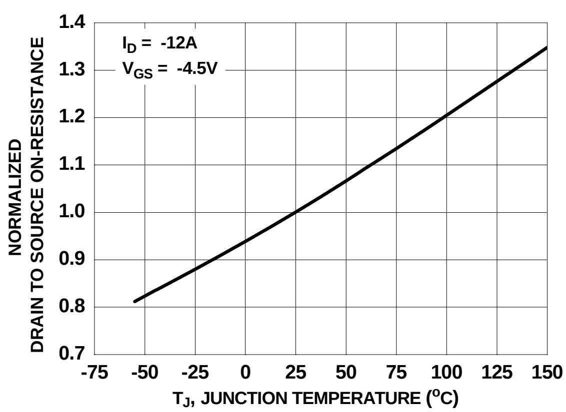


Figure 3. Normalized On-Resistance vs Junction Temperature

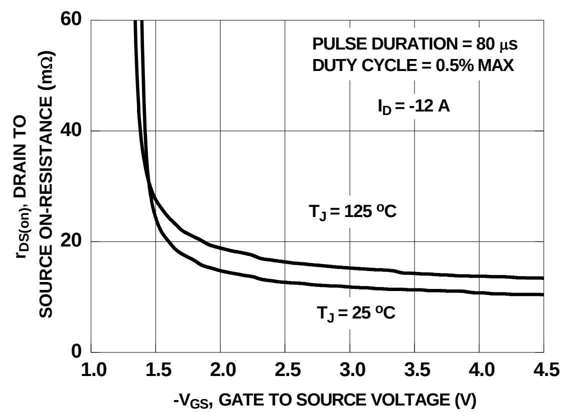


Figure 4. On-Resistance vs Gate to Source Voltage

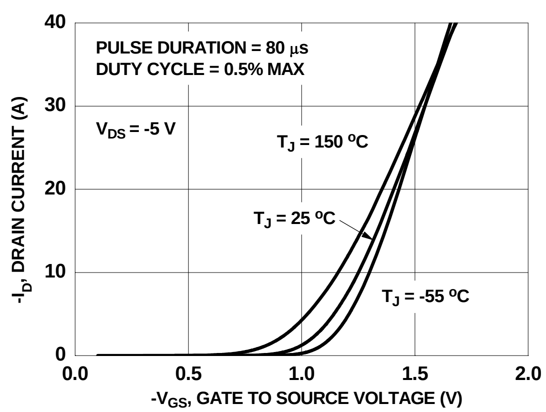


Figure 5. Transfer Characteristics

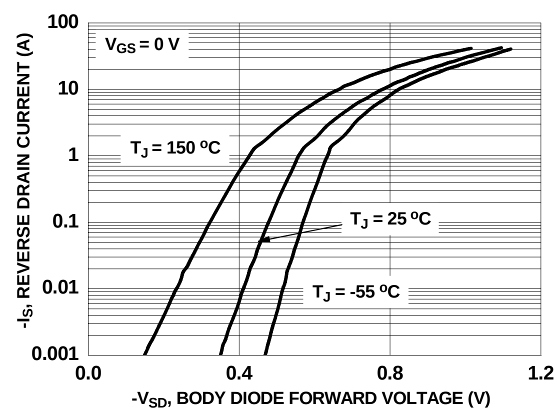


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

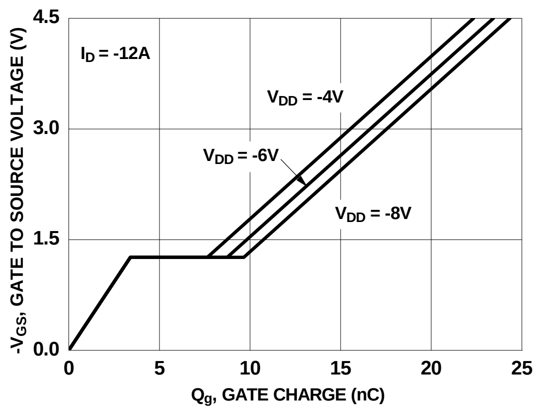


Figure 7. Gate Charge Characteristics

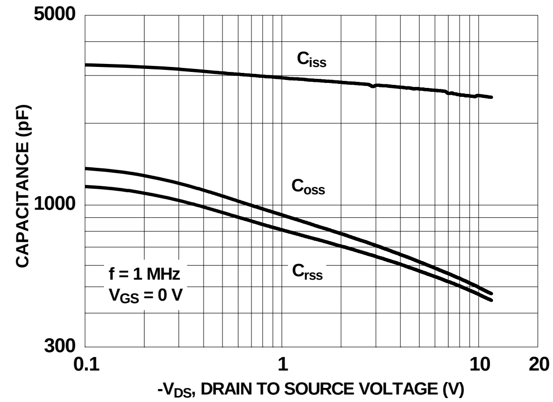


Figure 8. Capacitance vs Drain to Source Voltage

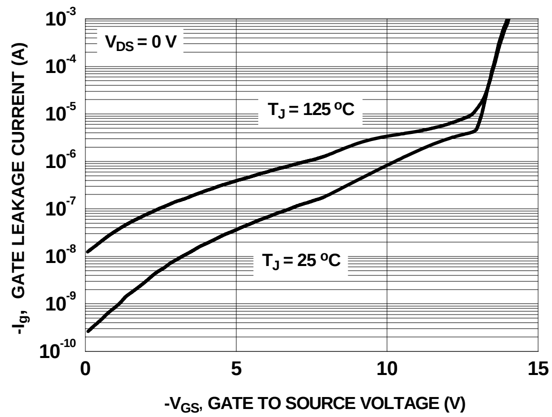


Figure 9. Gate Leakage Current vs Gate to Source Voltage

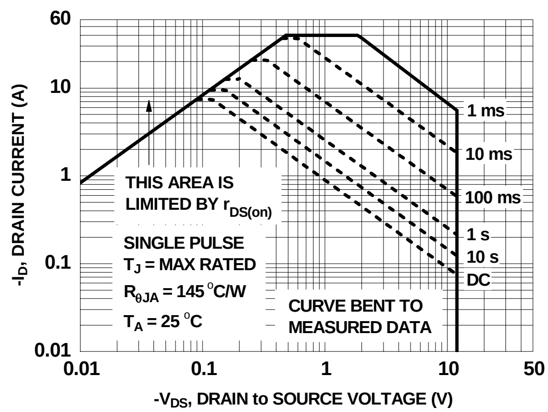


Figure 10. Gate Leakage Current vs Gate to Source Voltage

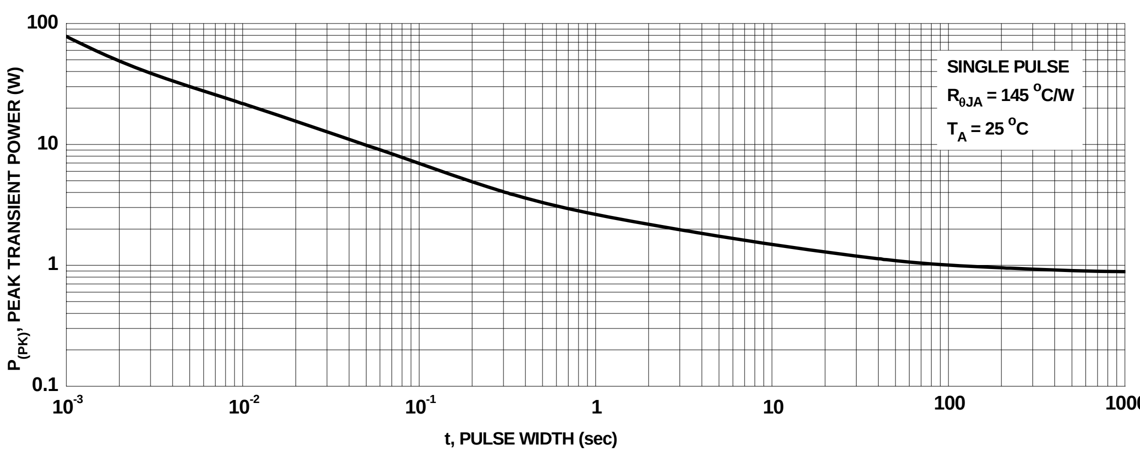


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

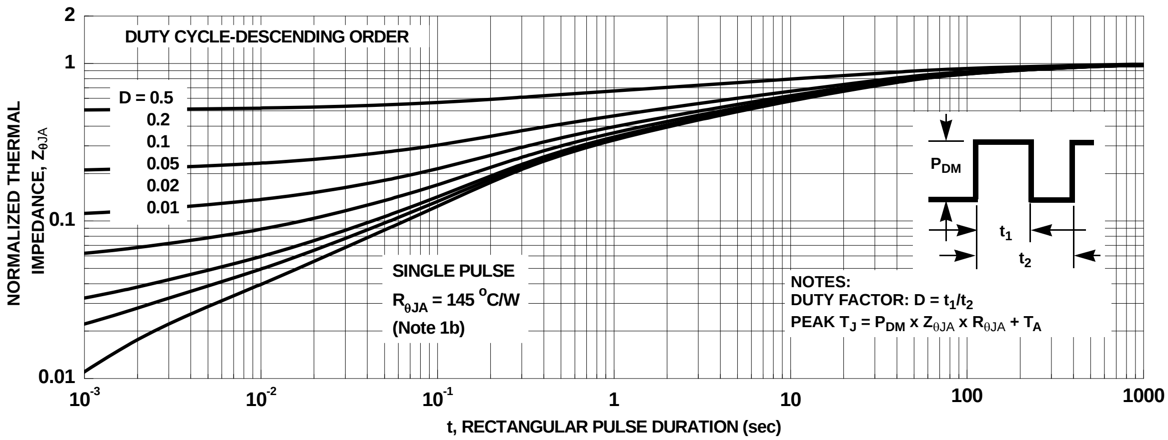
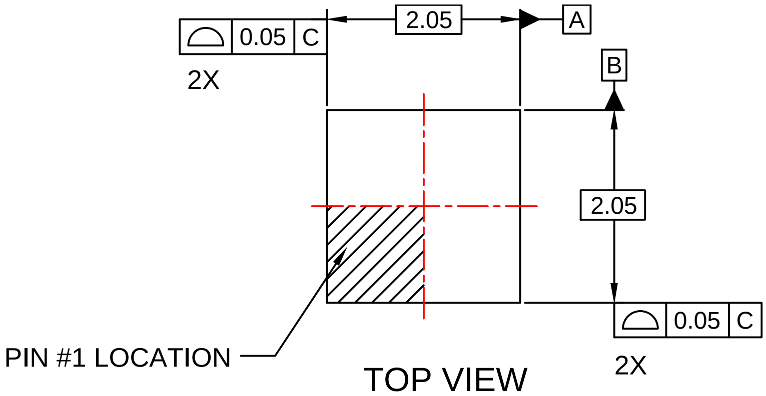
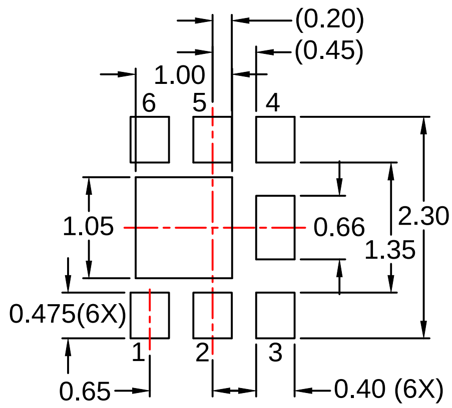


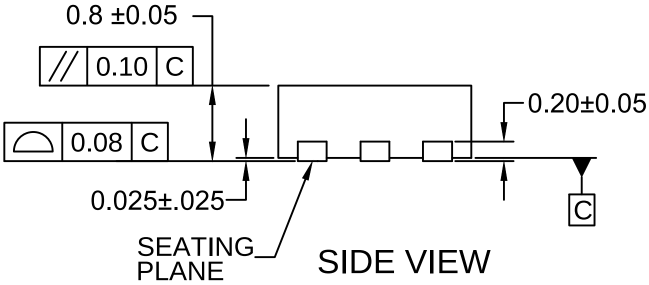
Figure 12. Junction-to-Ambient Transient Thermal Response Curve



TOP VIEW

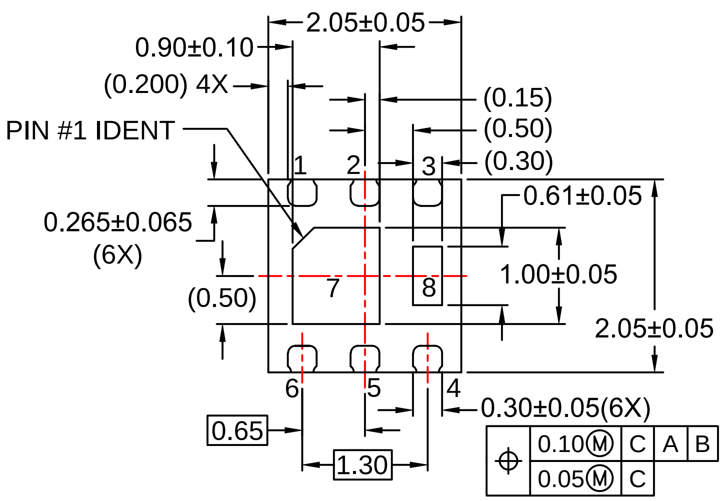


RECOMMENDED LAND PATTERN



SIDE VIEW

Pin #	Function
1	Drain
2	Drain
3	Gate
4	Source
5	Drain
6	Drain
7	Drain
8	Source



BOTTOM VIEW

NOTES:

A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-FDMA908Prev1.

F. REFERENCE DRAWING NO : MKT-MLP06Prev1.

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