MOSFET – Power, N-Channel, SMPS

500 V, 44 A, 120 mΩ

FDH44N50

Description

UniFET ™ MOSFET is ON Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on−state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- Low Gate Charge Q_g Results in Simple Drive Requirement (Typ. 90 nC)
- Improved Gate, Avalanche and High Reapplied dv/dt Ruggedness
- Reduced $R_{DS(on)}$ (110 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 22 A)
- Reduced Miller Capacitance and Low Input Capacitance (Typ. C_{rss} = 40 pF)
- Improved Switching Speed with Low EMI
- 175°C Rated Junction Temperature
- This Device is Pb−Free and is RoHS Compliant

Applications

- Lighting
- Uninterruptible Power Supply
- AC−DC Power Supply

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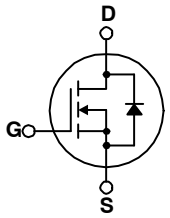
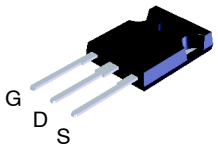
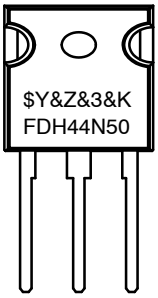
V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
500 V	120 mΩ @ 10 V	44 A





TO−247−3LD
CASE 340CK

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDH44N50	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	FDH44N50	Unit
V_{DSS}	Drain to Source Voltage	500	V
V_{GS}	Gate−Source Voltage	±30	V
I_D	Drain Current – – Continuous (T_C = 25°C, V_{GS} = 10 V) – Continuous (T_C = 100°C, V_{GS} = 10 V) – Pulsed (Note 1)	44 32 176	A
P_D	Power Dissipation	750	W
	Derate Above 25°C	5	W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to + 175	°C
	Soldering Temperature for 10 Seconds	300 (1.6 mm from Case)	°C
	Mounting Torque, 8−32 or M3 Screw	10 ibf*in (1.1 N*m)	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

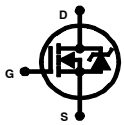
PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Package Method	Reel Size	Tape Width	Quantity
FDH44N50	FDH44N50	TO−247−3	Tube	N/A	N/A	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FDH44N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
STATICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		500	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C		–	0.61	–	V/°C
$r_{DS(ON)}$	Drain to Source On−Resistance	V_{GS} = 10 V, I_D = 22 A		–	0.11	0.12	Ω
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA		2	3.15	4	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	T_C = 25°C	–	–	25	μA
			T_C = 150°C	–	–	250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V		–	–	±100	nA
DYNAMICS							
gf_S	Forward Transconductance	V_{DS} = 50 V, I_D = 22 A		11	–	–	S
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 10 V, V_{DS} = 400 V, I_D = 44 A		–	90	108	nC
Q_{gs}	Gate to Source Gate Charge			–	24	29	nC
Q_{gd}	Gate to Drain “Miller” Charge			–	31	37	nC
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 44 A, R_D = 5.68 Ω, R_G = 2.15 Ω		–	16	–	ns
t_r	Turn−On Rise Time			–	84	–	ns
$t_{d(off)}$	Turn-Off Delay Time			–	45	–	ns
t_f	Turn−Off Fall Time			–	79	–	ns
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		–	5335	–	pF
C_{oss}	Output Capacitance			–	645	–	pF
C_{rss}	Reverse Transfer Capacitance			–	40	–	pF
AVALANCHE CHARACTERISTICS							
E_{AS}	Single Pulse Avalanche Energy (Note 2)			1500	–	–	mJ
I_{AR}	Avalanche Current			–	–	44	A
DRAIN-SOURCE DIODE CHARACTERISTICS							
I_S	Continuous Source Current (Body Diode)	MOSFET symbol Showing the integral reverse p−n junction diode. 		–	–	44	A
I_{SM}	Pulsed Source Current (Body Diode) (Note 1)			–	–	176	A
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 44 A		–	0.900	1.2	V
t_{rr}	Reverse Recovery Time	I_{SD} = 44 A, dI_{SD}/dt = 100 A/μs		–	920	1100	ns
Q_{rr}	Reverse Recovery Charge	I_{SD} = 44 A, dI_{SD}/dt = 100 A/μs		–	14	18	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Starting T_J = 25°C, L = 1.61 mH, I_{AS} = 44 A

TYPICAL CHARACTERISTICS

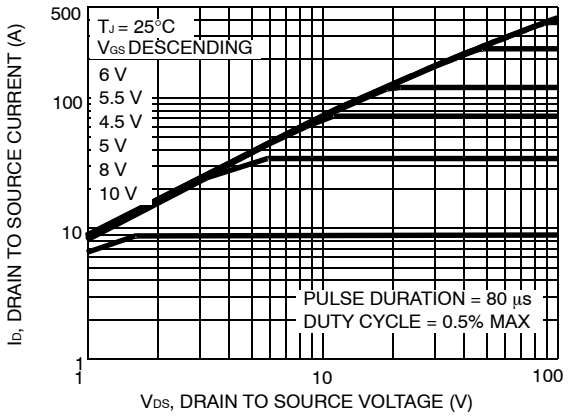


Figure 1. Output Characteristics

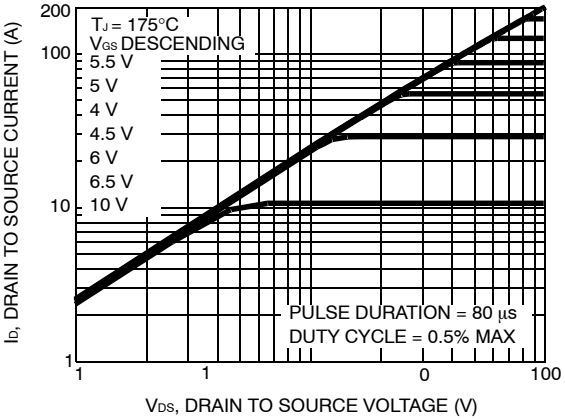


Figure 2. Output Characteristics

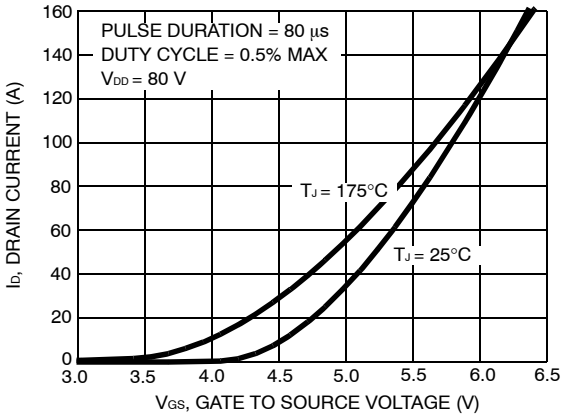


Figure 3. Transfer Characteristics

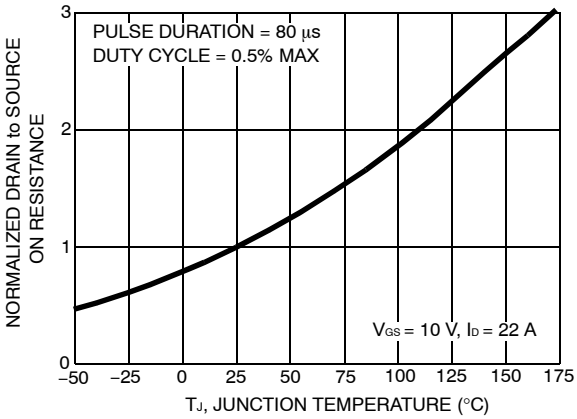


Figure 4. Normalized Drain to Source On Resistance vs. Junction Temperature

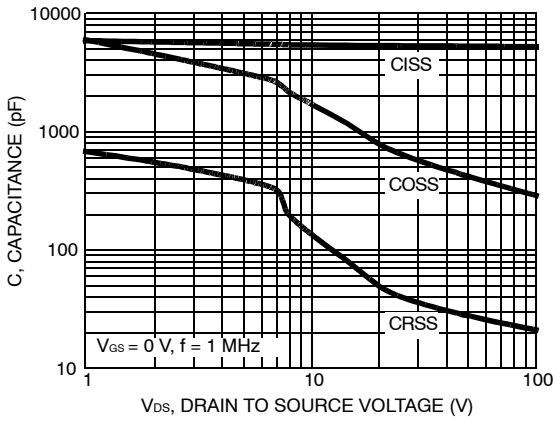


Figure 5. Capacitance vs. Drain to Source Voltage

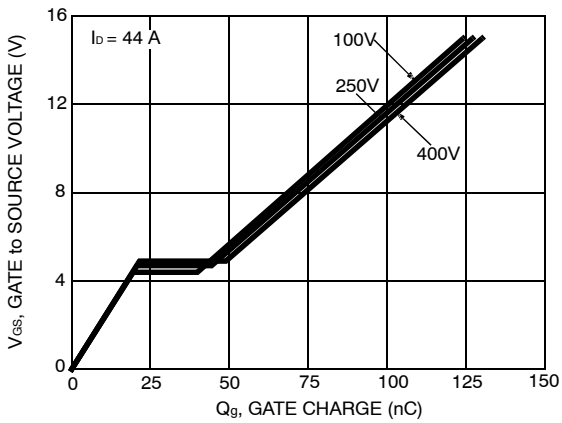


Figure 6. Gate Charge Waveforms for Constant Gate Current

TYPICAL CHARACTERISTICS

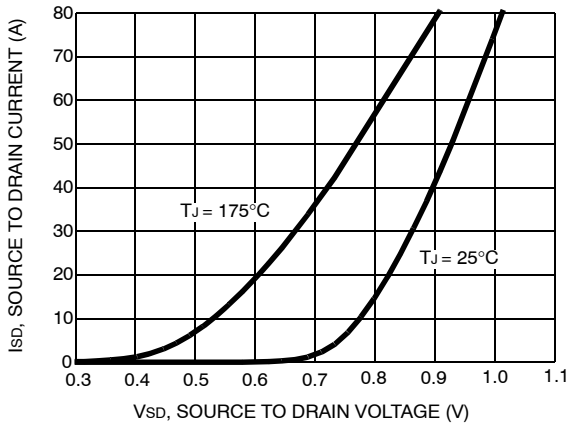


Figure 7. Body Diode Forward Voltage vs. Body Diode Current

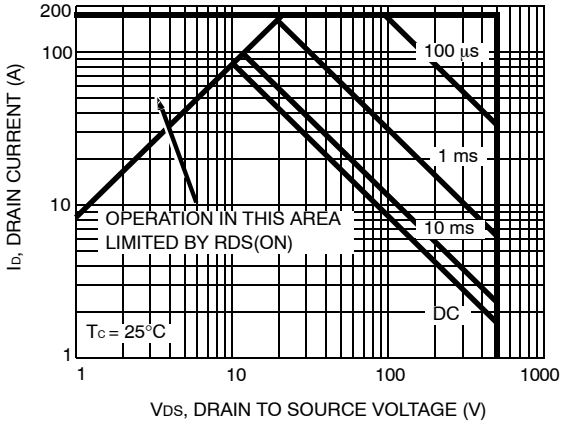


Figure 8. Maximum Safe Operating Area

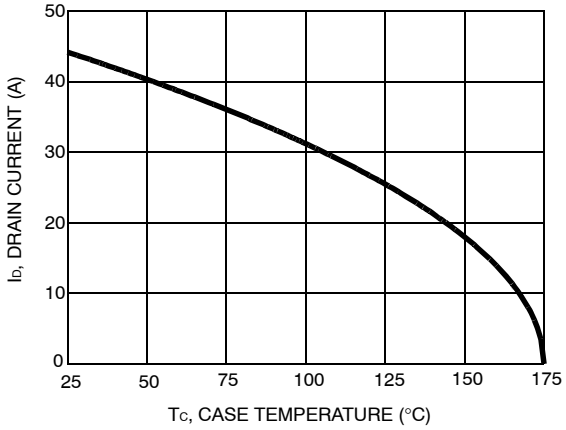


Figure 9. Maximum Drain Current vs. Case Temperature

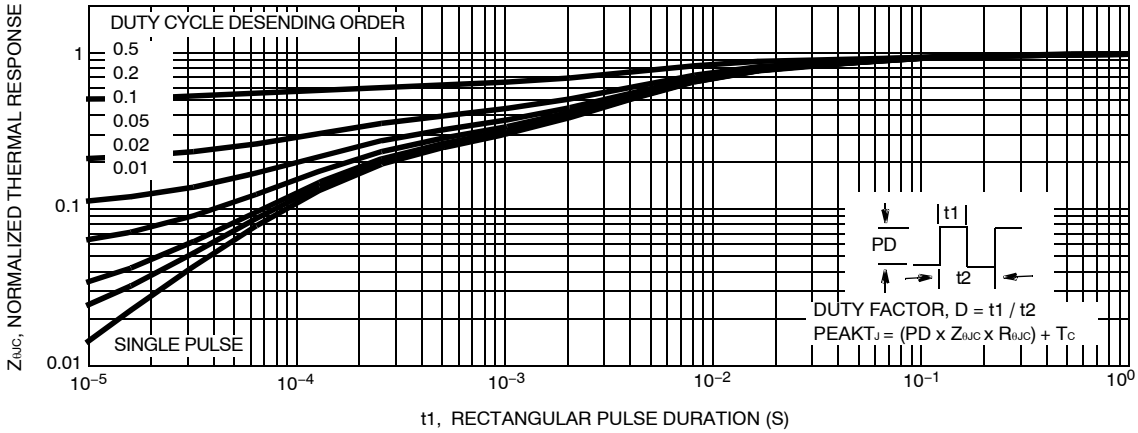


Figure 10. Normalized Transient Thermal Impedance, Junction to Case

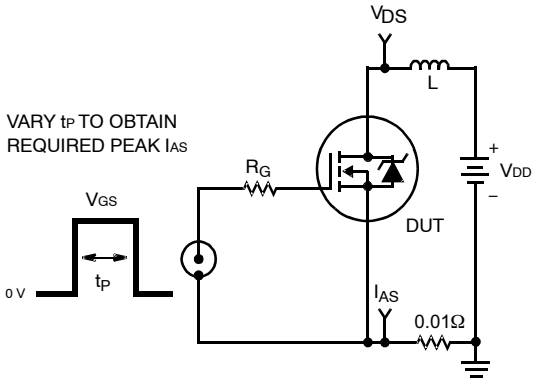


Figure 11. Unclamped Energy Test Circuit

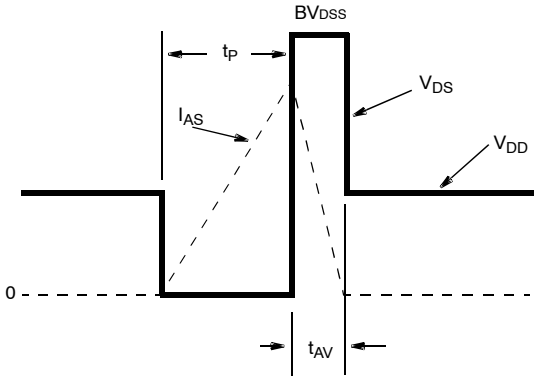


Figure 12. Unclamped Energy Waveforms

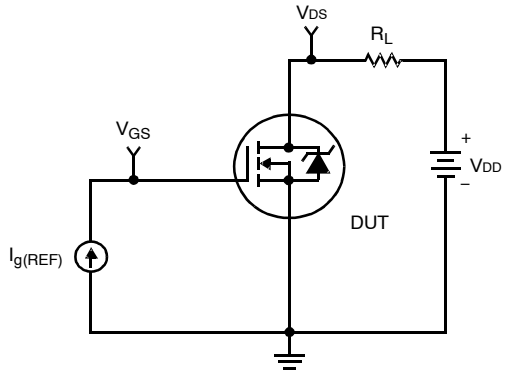


Figure 13. Gate Charge Test Circuit

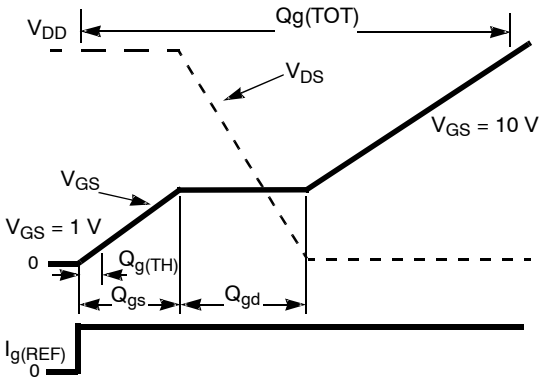


Figure 14. Gate Charge Waveforms

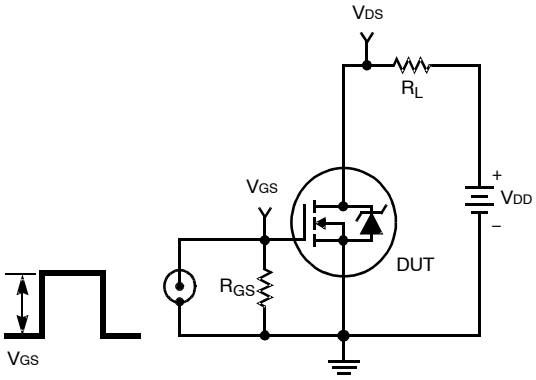


Figure 15. Switching Time Test Circuit

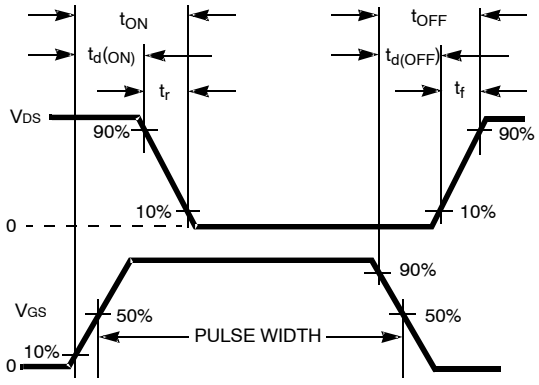


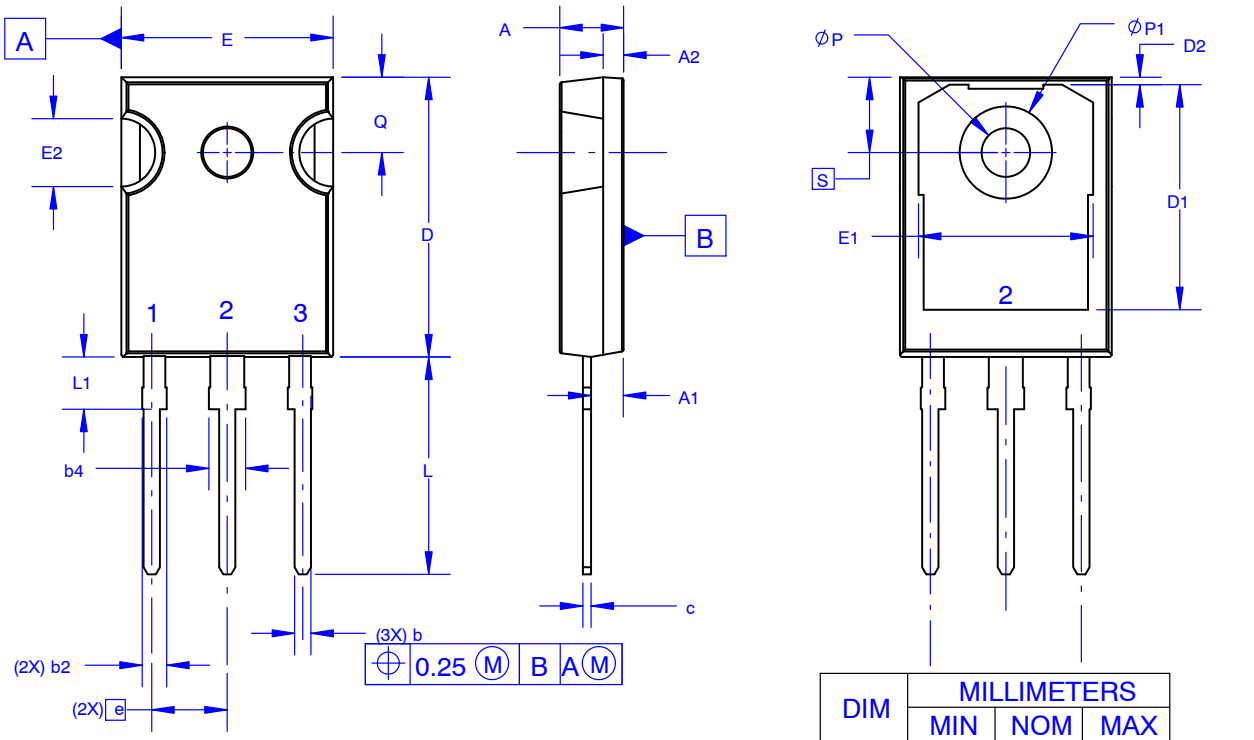
Figure 16. Switching Time Waveform

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019

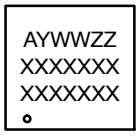


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TO−247−3LD SHORT LEAD**	**PAGE 1 OF 1**

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Phone: 011 421 33 790 2910

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