DESCRIPTION

This document describes the specifications for the F0552 1710MHz to 2050MHz dual path Sampling Intermediate Frequency (SIF) Receiver ideal for Multi-mode, Multi-carrier BaseStation Receivers. Refer to the Part # Matrix below describing the frequency coverage of the complete series. This series of devices covers all UTRA bands up to 2.7GHz and offers significantly better Noise and Distortion performance than currently available solutions. IF frequencies up to 450 MHz are supported.

The F0552 SIF provides 29dB gain and offers 47dB gain adjustment in 1dB steps designed to operate with a single 5V supply. Nominally, the device offers +45 dBm Output IP3 using 450mA of I_{CC}. Alternately one can configure the device in low current (LC) mode to reduce power consumption to < 1.9 Watts.

This device is packaged in a 10 x 10 mm 68-pin Thin QFN with 50 ohm single-ended RF input and 200 ohm differential IF output impedances for ease of integration into the receiver lineup. The EvKit is configured to match the 200 ohm differential IF output to 100 ohms differential for a broad range of IF center frequencies per the application drawings.

COMPETITIVE ADVANTAGE

Renesas' Zero-Distortion™ mixer in combination with interstage filtering and Renesas' proprietary FlatNoise™ DVGA improves system SNR to the point where the external SAW filter can be eliminated. Both $IP3_O$ and NF are kept virtually flat while gain is backed off, enhancing SNR significantly under high level interferer conditions, and greatly benefiting 2G/3G/4G Multi-Carrier IF sampling receivers. In addition, total power consumption is reduced by ~35% compared to conventional solutions.

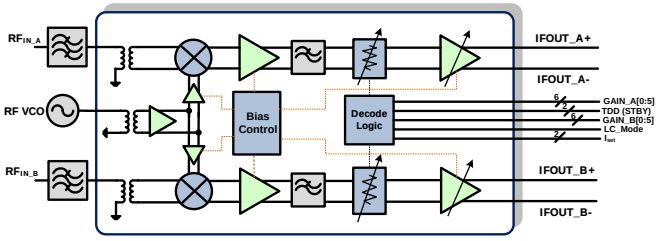
- ✓ No external SAW is needed
- ✓ Reduced Power Consumption by 35%
- ✓ NF and OIP3 virtually flat for first 17 dB gain reduction

The fast-settling, parallel mode gain step of 1.0dB coupled with the excellent differential non-linearity allow for SNR to be maximized further by targeting the minimum necessary gain in small, accurate increments. The matched output does not require a terminating resistor, thus the gain and distortion performance are preserved when driving Bandpass Anti-Alias filters.

FEATURES

- Dual Channel for Diversity / MIMO Systems
- Combines FlatNoise™ and Zero-Distortion™ technology
- 29dB Total Power Gain
- 47dB gain control range
- 1 dB Gain Steps
- Ultra linear +45dBm $IP3_O$
- Low NF: 9.6dB at G_{MAX}
- 50Ω input impedance
- Matched to 100Ω differential output impedance
- Ultra high +19.8dBm P1dBo
- Independent channel standby mode
- Constant LO impedance in STBY mode
- 6-bit parallel control
- 60MHz to 450MHz IF frequency range
- Excellent 2x2, 3x3, IM2, 2nd Harmonic Rejection
- I_{CC} = 450mA STD Mode, 375mA LC Mode
- 10 x 10 mm 68-pin VFQFPN package

DEVICE BLOCK DIAGRAM



PART# MATRIX

Part#	RF freq range	UTRA bands	IF freq range	Typ. Gain	Injection
F0502	698 - 915	5,6,8,12,13,14,17 18,19,20	60 – 300	29	Low & High Side
F0552	**1710 - 2050**	**1,2,3,4,9,10,23, 25,33,34,35,36, 37,39**	**60 – 450**	**29**	**Low & High Side**
F0562	2300 – 2700	7,38,40,41	60 – 450	29	Low & High Side

CONTENTS

ABSOLUTE MAXIMUM RATINGS

VCC to GND	-0.3V to +5.5V
A[5:0], B[5:0], TDD_A, TDD_B (STBY), LCMode	-0.3V to (VCC + 0.25V)
MX_IFA+, MX_IFA-, MX_IFB+, MX_IFB-	-0.3V to (VCC + 0.25V)
IFOUT_A+, IFOUT_A-, IFOUT_B+, IFOUT_B-	1V to (Vcc + 0.3V)
LO1_ADJ	+1V to +3V
LO2_ADJ	+2.1V to +4V
MX_IF_BiasA, MX_IF_BiasB	-0.3V to +0.3V
LO_IN, RFIN_A, RFIN_B	-0.3V to +0.3V
RF Input Power (RFIN_A, RFIN_B)	+20dBm
ISET_A, ISET_B to GND	-0.3V to +2.2V
Continuous Power Dissipation	2.5W
θ_{JA} (Junction – Ambient)	+25°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+3°C/W
Operating Temperature Range (Case Temperature)	T_C = -40°C to +105°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+260°C

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE – CHANNEL A AND B

Gain Set Target	Gain CodeWord	Code Name	Gain Set Target	Gain CodeWord	Code Name	Gain Set Target	Gain CodeWord	Code Name
27	000000	G_{27}	5	010110	G_{5}	-17	101100	G_{-17}
26	000001	G_{26}	4	010111	G_{4}	-18	101101	G_{-18}
25	000010	G_{25}	3	011000	G_{3}	-19	101110	G_{-19}
24	000011	G_{24}	2	011001	G_{2}	-20	101111	G_{-20}
23	000100	G_{23}	1	011010	G_{1}	-20	110000	G_{-20}
22	000101	G_{22}	0	011011	G_{0}	-20	110001	G_{-20}
21	000110	G_{21}	-1	011100	G_{-1}	-20	110010	G_{-20}
20	000111	G_{20}	-2	011101	G_{-2}	-20	110011	G_{-20}
19	001000	G_{19}	-3	011110	G_{-3}	-20	110100	G_{-20}
18	001001	G_{18}	-4	011111	G_{-4}	-20	110101	G_{-20}
17	001010	G_{17}	-5	100000	G_{-5}	-20	110110	G_{-20}
16	001011	G_{16}	-6	100001	G_{-6}	-20	110111	G_{-20}
15	001100	G_{15}	-7	100010	G_{-7}	-20	111000	G_{-20}
14	001101	G_{14}	-8	100011	G_{-8}	-20	111001	G_{-20}
13	001110	G_{13}	-9	100100	G_{-9}	-20	111010	G_{-20}
12	001111	G_{12}	-10	100101	G_{-10}	-20	111011	G_{-20}
11	010000	G_{11}	-11	100110	G_{-11}	-20	111100	G_{-20}
10	010001	G_{10}	-12	100111	G_{-12}	-20	111101	G_{-20}
9	010010	G_{9}	-13	101000	G_{-13}	-20	111110	G_{-20}
8	010011	G_{8}	-14	101001	G_{-14}	-20	111111	G_{-20}
7	010100	G_{7}	-15	101010	G_{-15}			
6	010101	G_{6}	-16	101011	G_{-16}			

F0552 RECOMMENDED OPERATING CONDITIONS

Parameter	Comment	Symbol	Min	Typ	Max	Units
Supply Voltage(s)	All V_{CC} pins	V_{CC}	4.75		5.25	V
LO Power		P_{LO}	-3		+3	dBm
Operating Temperature Range	Case Temperature	T_{CASE}	-40		+105	°C
RF Freq Range	For Cellular Applications	F_{RF}	1710		2050	MHz
LO Freq Range		F_{LOLS}	1345		2330	
IF Range		F_{IF}	60		450	

F0552 SPECIFICATION

F0552 Typical Application Circuit, when operated as a Sampling IF Receiver, V_{CC} = +5.00V, T_C = +25°C, F_{RF} = 1880 MHz, F_{IF} = 184MHz, F_{LO} = 1696MHz, P_{LO} = 0dBm, Output power = +3dBm per tone unless otherwise noted, TDD_A, TDD_B = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted.

Parameter	Comment	Symbol	Min	Typ	Max	Units
Logic Input High	For all control pins	V_{IH}	***1.07***			V
Logic Input Low	For all control pins	V_{IL}			***0.68***	V
Logic Current	For all control pins	I_{IH}, I_{IL}	***-150***		***10***	µA
Supply Current	Total V_{CC}, STD Mode	I_{STD}		***450***	***510***	mA
Supply Current	Total V_{CC}, LC Mode	I_{LC}		***375***	***420***	mA
Supply Current	▪ Standby Mode ▪ STBY = V_{IH} ▪ Total Both Channels	I_{STBY}		***21***	***28***	mA
Gain STD Mode	Conversion Power Gain Minimum attenuation	G_{STDMAX}	***27***	***29***[1]	***31***	dB
Gain LC Mode	Conversion Power Gain Minimum attenuation	G_{LC}	***26.5***	***28.5***	***30.5***	dB
Gain control range		G_{RANGE}		47[2]		dB
Gain STD mode min gain setting	Maximum attenuation	G_{STDMIN}		-18		dB
Step size		G_{STEP}		1		dB
Differential Gain Error	Between any two adjacent 1dB steps	DNL		0.1	0.2	dB
Integral Gain Error	Error vs. line (G_{27} Ref)	INL		***0.2***	***0.8***	dB
Phase Error	Maximum phase change between G_{MAX} and any state down to G_{-14}	IPE		2.5	4	degree
NF STD Mode	Noise Figure (@ +25C)	NF_{STD}		9.6	10.6	dB
NF STD Mode 10dB reduced gain		NF_{STD_G-10}		9.6	10.6	dB
NF LC Mode	Noise Figure (@ +25C)	NF_{LC}		9.3	10.3	dB
NF LC Mode 10dB reduced gain		NF_{LC_G-10}		9.5	10.5	dB
NF w/Blocker	▪ +100 MHz offset blocker ▪ P_{IN} = +4dBm ▪ 28dB gain reduced	NF_{BLK}		19.7	21	dB

F0552 Specification (Continued)

F0552 Typical Application Circuit, when operated as a Sampling IF Receiver, V_{CC} = +5.00V, T_C = +25°C, F_{RF} = 1880 MHz, F_{IF} = 184MHz, F_{LO} = 1696MHz, P_{LO} = 0dBm, Output power = +3dBm per tone unless otherwise noted, TDD_A, TDD_B = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted.

Parameter	Comment	Symbol	Min	Typ	Max	Units
Turn-on time	▪ Gate STBY from V_{IH} to V_{IL} ▪ Time for IF Signal to settle to within 0.1 dB of final value	T_{SETTL}		0.17	0.20	µsec
Attenuator adjustment settling time	▪ Any two Adjacent 1dB Steps ▪ +/-0.10 dB Pout settling	T_{1dB}		17.5	25	nsec
Output IP3 Max Gain, STD_{MODE}	▪ Set G_{MAX}, ▪ 800 KHz Tone Separation	$IP3_{O1}$	***40***	***45***		dBm
Output IP3 10dB reduced gain, STD_{MODE}	▪ From $G_{MAX\ to}$ G_{MAX-10}, ▪ Pout = +1dBm per tone ▪ 800 KHz Tone Separation	$IP3_{O2}$	40	45		dBm
Output IP3 10dB reduced gain, STD_{MODE}	▪ From $G_{MAX\ to}$ G_{MAX-10}, ▪ Pout = +1dBm per tone ▪ 800 KHz Tone Separation ▪ -40C ≤ Tcase ≤ +105C ▪ IF = 138MHz, LO = 1742MHz ▪ IF = 184MHz, LO = 1696MHz ▪ IF = 276MHz[3], LO = 1604MHz	$IP3_{O3}$		44		dBm
Output IP3 Max Gain, LC_{MODE}	▪ Set G_{MAX}, ▪ 800 KHz Tone Separation	$IP3_{O4}$	40	45		dBm
Input IP3 22dB reduced gain, STD_{MODE}	▪ Set $G_{MAX-22dB}$, ▪ Pin = - 5dBm per tone ▪ 800 KHz Tone Separation	$IP3_{ISTD}$	28	31.5		dBm
Input IP3 22dB reduced gain, LC_{MODE}	▪ Set $G_{MAX-22dB}$, ▪ Pin = -10dBm per tone ▪ 800 KHz Tone Separation	$IP3_{ILC}$		24.5		dBm
1 dB Compression Max Gain, STD_{MODE}	Output referred	$P1dB_{O1}$	***17***	19.8		dBm
1 dB Compression 30dB reduced gain, STD_{MODE}	▪ Input referred ▪ Set $G_{MAX-30dB}$	$P1dB_{I1}$	8.2	9.2		dBm
1 dB Compression Max Gain, LC_{MODE}	Output referred	$P1dB_{O2}$	***17***	19.8		dBm
1 dB Compression 30dB reduced gain, LC_{MODE}	▪ Input referred ▪ Set $G_{MAX-30dB}$	$P1dB_{I2}$	6.5	7		dBm
2RF – 2LO rejection Max Gain, STD_{MODE}	▪ Frequency = F_{RF} - ½ F_{IF} ▪ P_{RF} = -27dBm	$2x2_1$		-75	-65	dBc
2RF – 2LO rejection 22dB reduced gain, STD_{MODE}	▪ Frequency = F_{RF} - ½ F_{IF} ▪ P_{RF} = -5dBm	$2x2_2$		-72	-62	dBc

F0552 Specification (Continued)

F0552 Typical Application Circuit, when operated as a Sampling IF Receiver, V_{CC} = +5.00V, T_C = +25°C, F_{RF} = 1880 MHz, F_{IF} = 184MHz, F_{LO} = 1696MHz, P_{LO} = 0dBm, Output power = +3dBm per tone unless otherwise noted, TDD_A, TDD_B = LOW. EVkit IF transformer losses are de-embedded unless otherwise noted.

Parameter	Comment	Symbol	Min	Typ	Max	Units
2RF – 2LO rejection Max Gain, LC_{MODE}	▪ Frequency = F_{RF} - ½ F_{IF} ▪ P_{RF} = -27dBm	$2x2_3$		-74	-60	dBc
2RF – 2LO rejection 22dB reduced gain, LC_{MODE}	▪ Frequency = F_{RF} - ½ F_{IF} ▪ P_{RF} = -5dBm	$2x2_4$		-71	-60	dBc
2nd Harmonic Max Gain, STD_{MODE}	P_{RF} = -27 dBm	$HD2_1$		-77	-70	dBc
2nd Harmonic Max Gain, LC_{MODE}	P_{RF} = -27 dBm	$HD2_3$		-76	-70	dBc
3rd Harmonic – Max Gain, STD_{MODE}	P_{RF} = -27 dBm	$HD3_1$		-100	-80	dBc
3rd Harmonic Max Gain, LC_{MODE}	P_{RF} = -27 dBm	$HD3_3$		-100	-82	dBc
Channel Isolation Max Gain, STD_{MODE}	IF_B Pout vs. IF_A w/ RF_A input	ISO_{C_STD}	40	43		dB
Channel Isolation Max Gain, LC_{MODE}	IF_B Pout vs. IF_A w/ RF_A input	ISO_{C_LC}	40	43		dB
LO to IF leakage Max Gain, STD_{MODE}		ISO_{LI-1}		-53	-45	dBm
LO to IF leakage Max Gain, LC_{MODE}		ISO_{LI-3}		-54	-45	dBm
RF to IF leakage Max Gain, STD_{MODE}	P_{RF} = -27 dBm	ISO_{RI-1}		-84	-75	dBc
RF to IF leakage Max Gain, LC_{MODE}	P_{RF} = -27 dBm	ISO_{RI-2}		-85	-75	dBc
LO to RF leakage, STD_{MODE}		ISO_{LR}		-37		dBm
RFIN Impedance	Single Ended	Z_{RFIN}		50		Ω
LO Port Impedance	Single Ended	Z_{LO}		50		
IF Output Impedance	Differential	Z_{IF}		200		

Specification Notes:

1 – Items in min/max columns in ***bold italics*** are confirmed by Test using BOM1 components supporting 4:1 output impedance transformation to 50 ohms.
2 – All other Items in min/max columns are confirmed by Design Characterization using BOM2 components supporting 2:1 output impedance transformation to 100 ohms.
3 – Matching network changed for 276MHz IF per BOM table values.

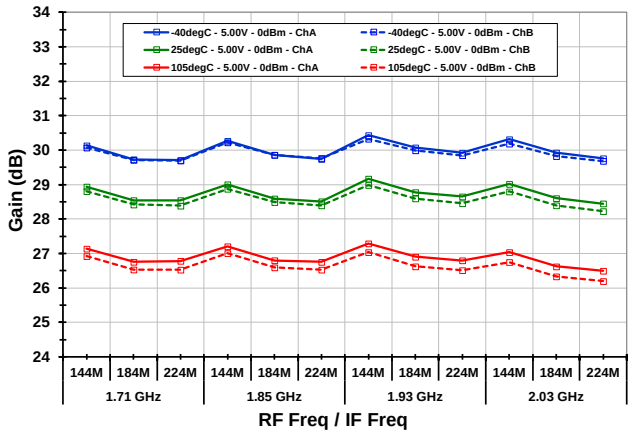
TYPICAL OPERATING CONDITIONS (STD MODE, 184MHZ IF)

Unless otherwise noted, the following conditions apply to the 184MHz Typ Ops Graphs:

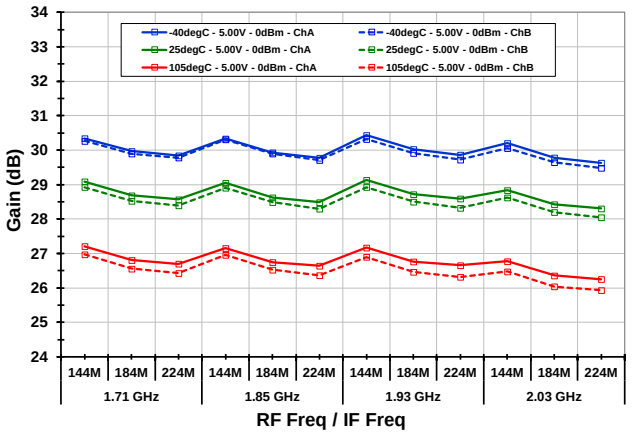
- BOM2 Applications circuit with 184MHz IF Center +/- 40 MHz bandwidth network to provide matching to 100 ohm differential load provided by 2:1 transformer (see page 51)
- Pout ~ +1 dBm
- P_{IN} from -27 to -6dBm (Gain Setting Adjusted to yield Pout ~ +1 dBm without exceeding -6dBm P_{IN})
- Tone Spacing = 800kHz
- Device configured in Standard Mode with Low Side Injection
- T_{CASE} = 25°C, V_{CC} = 5.00 V, LO Power = 0 dBm
- RF Frequency: 1.88GHz
- IF Frequency: 184MHz
- Gain Setting Sweep points: 27dB (G_{MAX})
- Transformer Losses are de-embedded
- Input RF trace Losses are not de-embedded
- Listed Temperatures are Case Temperature (T_C = Case Temperature)
- Where noted, T_A or T_{AMB} = Ambient Temperature

TOCs [MAX GAIN, STD MODE, IF = 184M] GAIN (-1-)

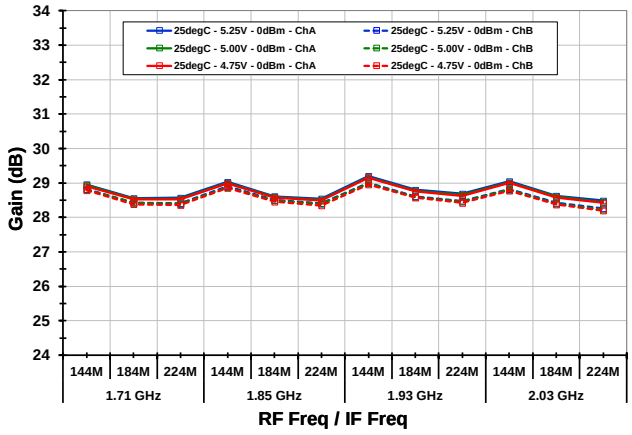
Gain vs. TCASE [low side inj.]



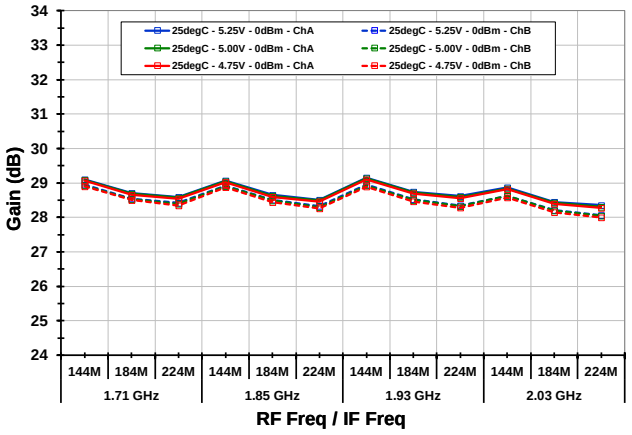
Gain vs. T_{CASE} [high side inj.]



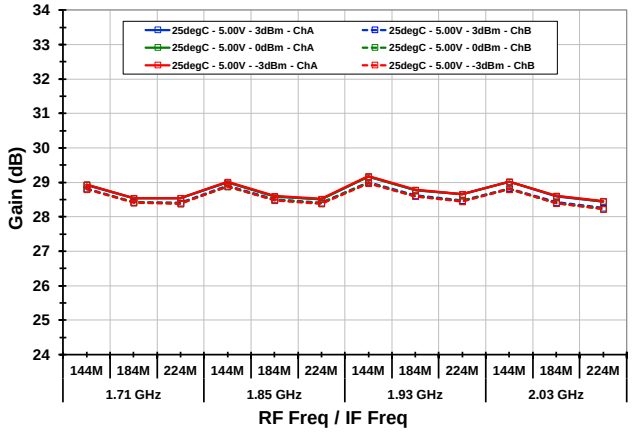
Gain vs. V_{CC} [low side inj.]



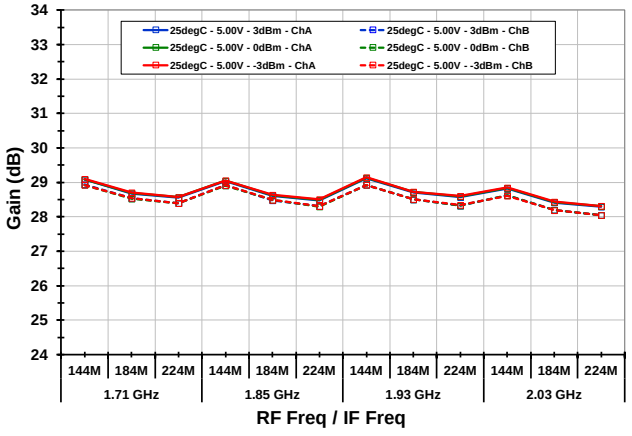
Gain vs. V_{CC} [high side inj.]



Gain vs. LO level [low side inj.]

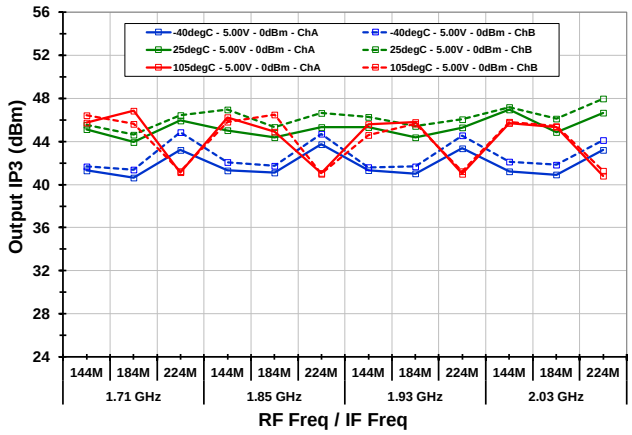


Gain vs. LO level [high side inj.]

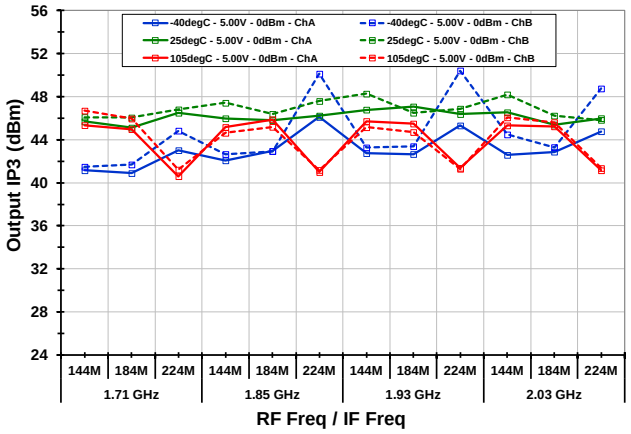


TOCs [MAX GAIN, STD MODE, IF = 184M] OIP3 (-2-)

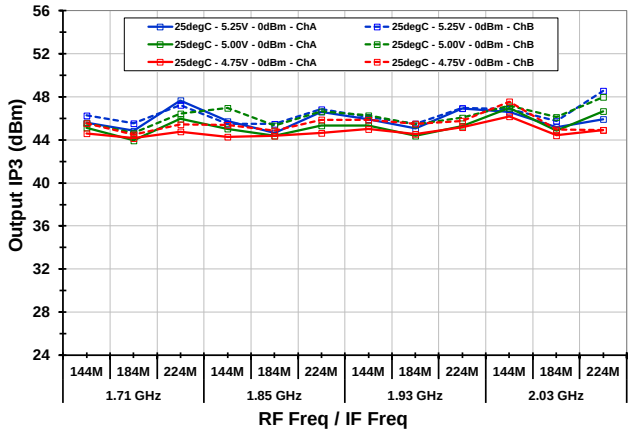
Output IP3 vs. T_{CASE} [low side inj.]



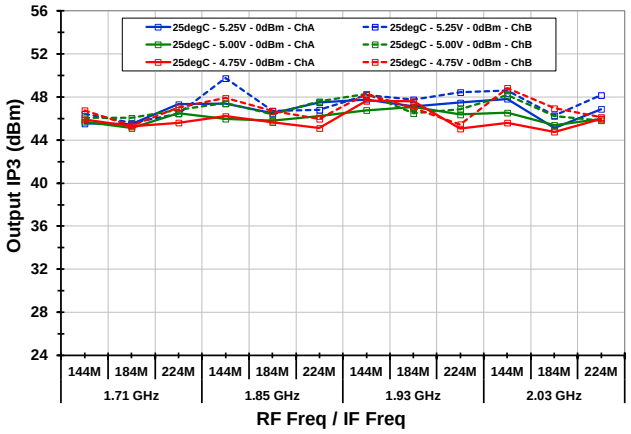
Output IP3 vs. T_{CASE} [high side inj.]



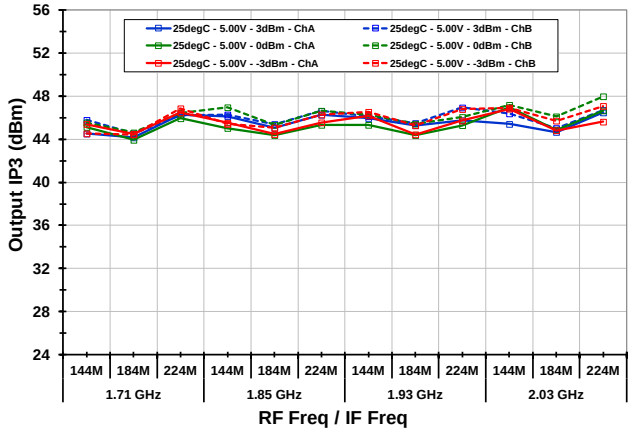
Output IP3 vs. V_{CC} [low side inj.]



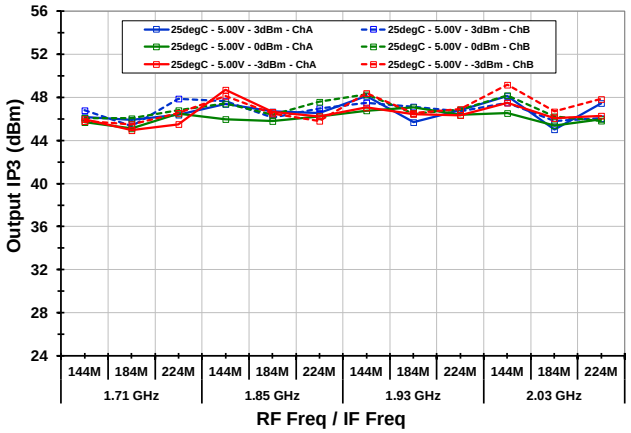
Output IP3 vs. V_{CC} [high side inj.]



Output IP3 vs. LO level [low side inj.]

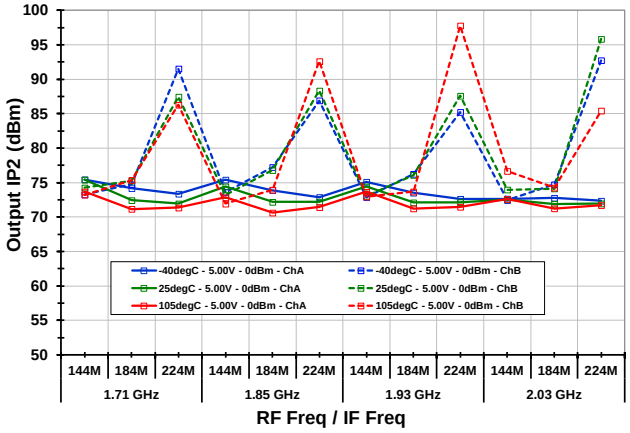


Output IP3 vs. LO level [high side inj.]

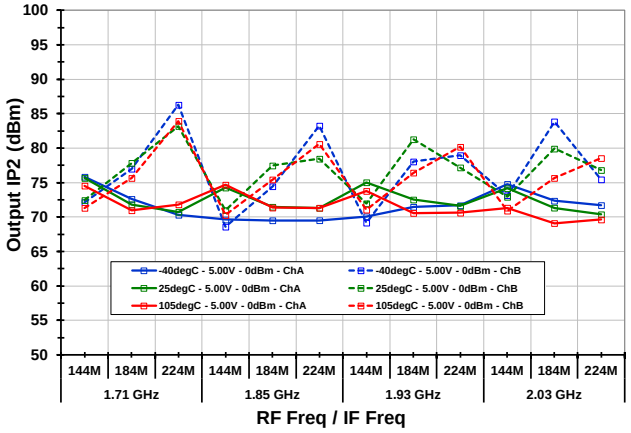


TOCs [MAX GAIN, STD MODE, IF = 184M] OIP2 (-3-)

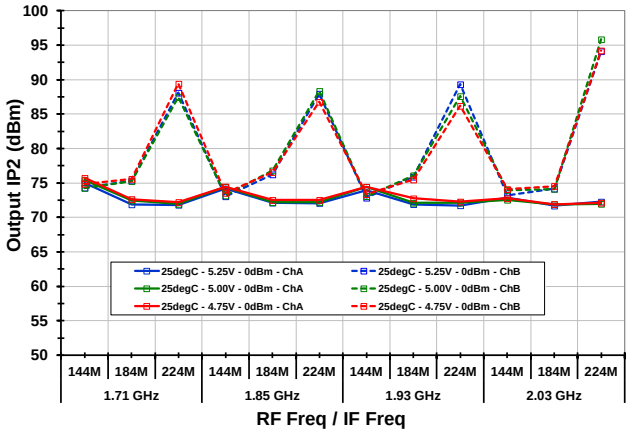
Output IP2 vs. T_{CASE} [low side inj.]



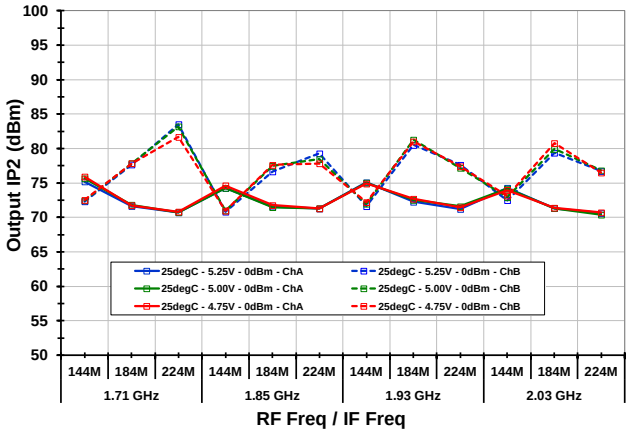
Output IP2 vs. T_{CASE} [high side inj.]



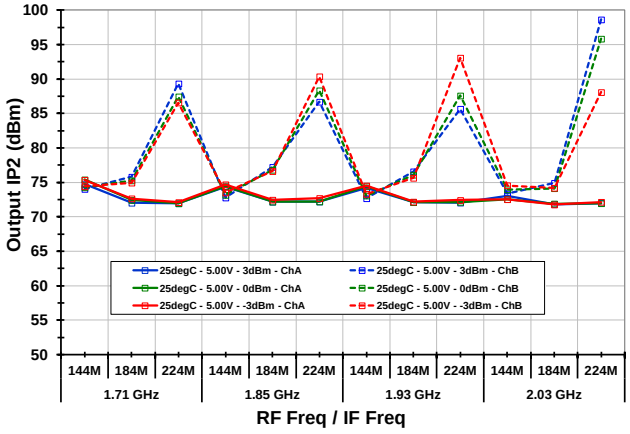
Output IP2 vs. V_{CC} [low side inj.]



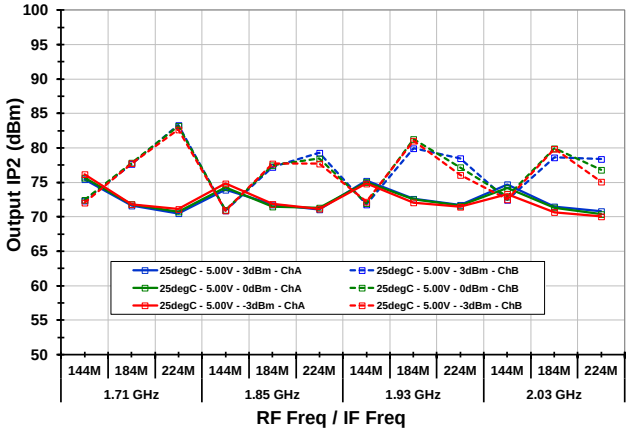
Output IP2 vs. V_{CC} [high side inj.]



Output IP2 vs. LO level [low side inj.]

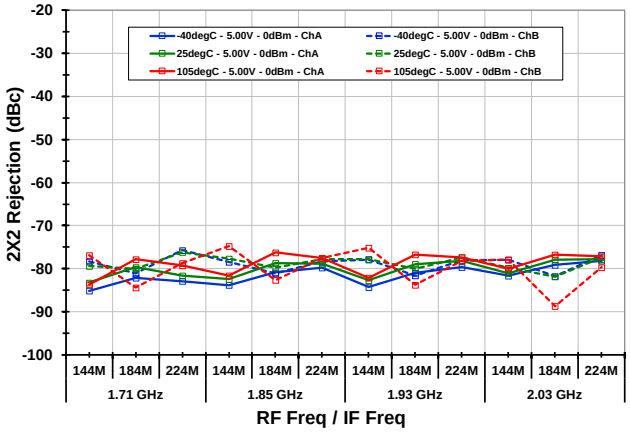


Output IP2 vs. LO level [high side inj.]

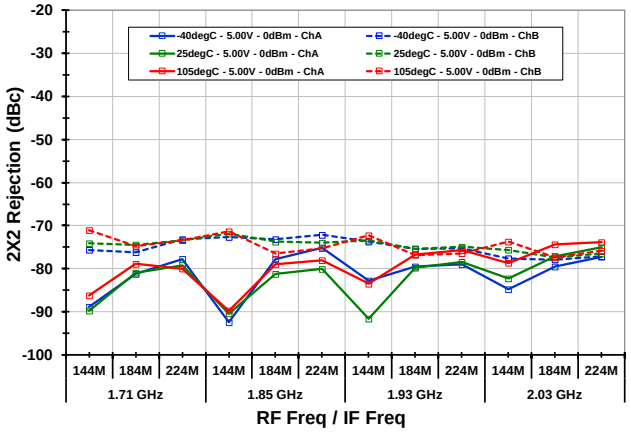


TOCs [MAX GAIN, STD MODE, IF = 184M] 2X2 (-4-)

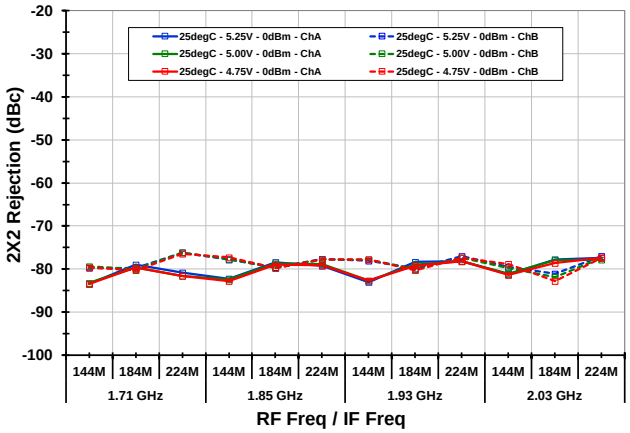
2x2 Rejection vs. T_{CASE} [low side inj.]



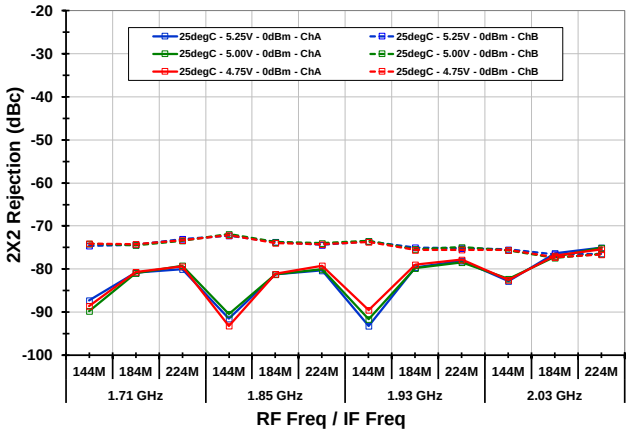
2x2 Rejection vs. T_{CASE} [high side inj.]



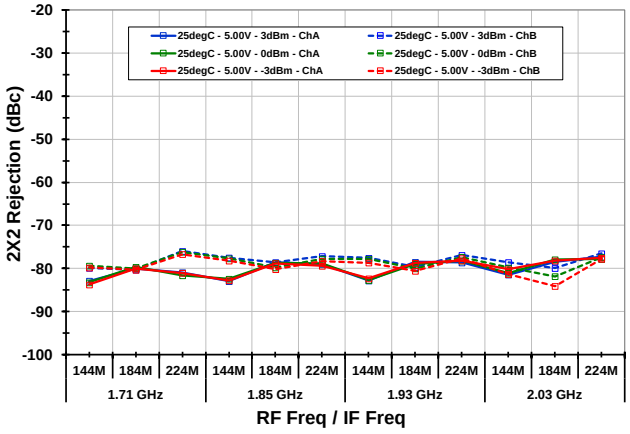
2x2 Rejection vs. V_{CC} [low side inj.]



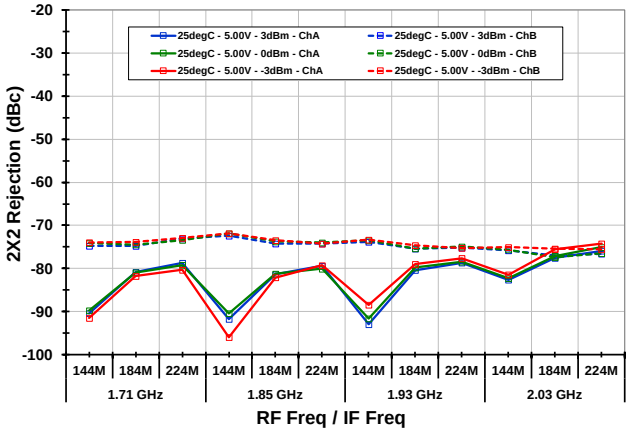
2x2 Rejection vs. V_{CC} [high side inj.]



2x2 Rejection vs. LO level [low side inj.]

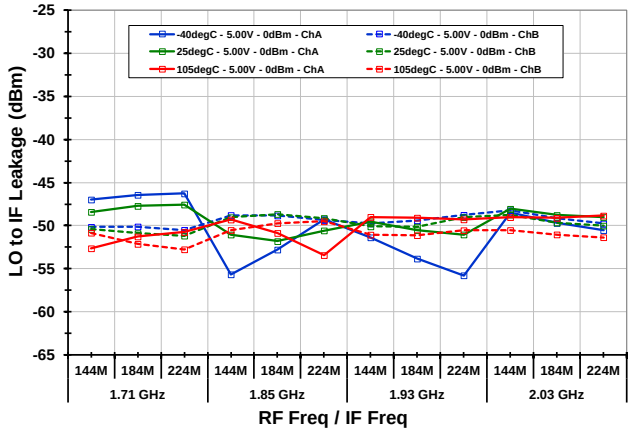


2x2 Rejection vs. LO level [high side inj.]

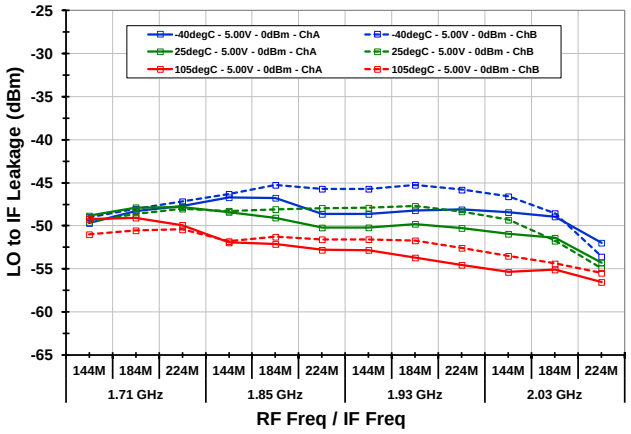


TOCs [Max Gain, STD Mode, IF = 184M] Leakage (-5-)

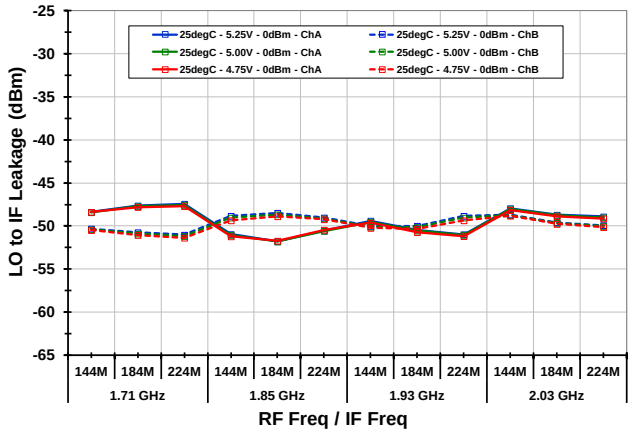
LO to IF Leakage vs. T_{CASE} [low side inj.]



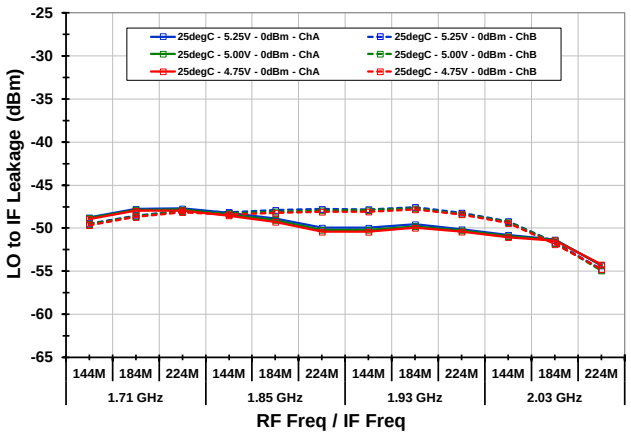
LO to IF Leakage vs. T_{CASE} [high side inj.]



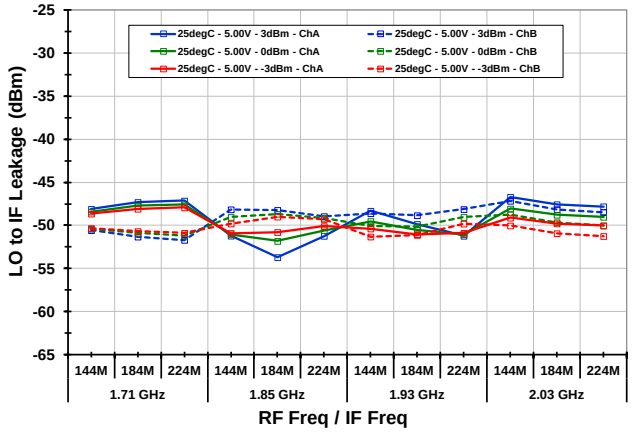
LO to IF Leakage vs. V_{CC} [low side inj.]



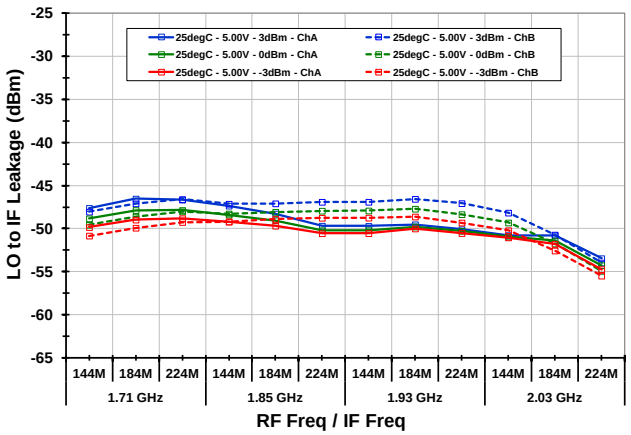
LO to IF Leakage vs. V_{CC} [high side inj.]



LO to IF Leakage vs. LO level [low side inj.]

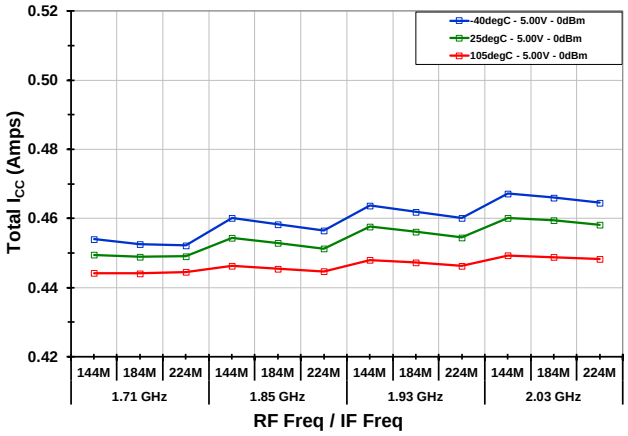


LO to IF Leakage vs. LO level [high side inj.]

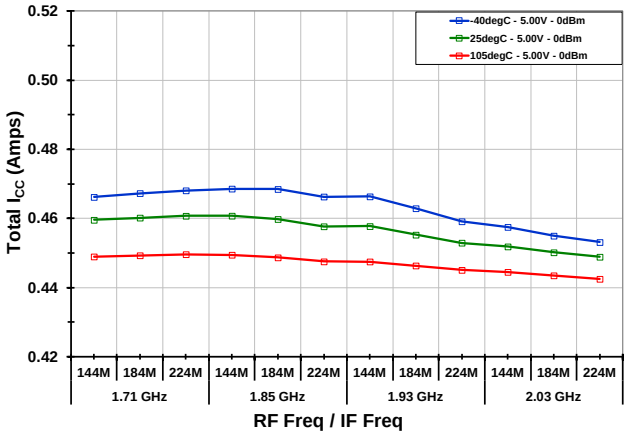


TOCs [MAX GAIN, STD MODE, IF = 184M] DC CURRENT (-6-)

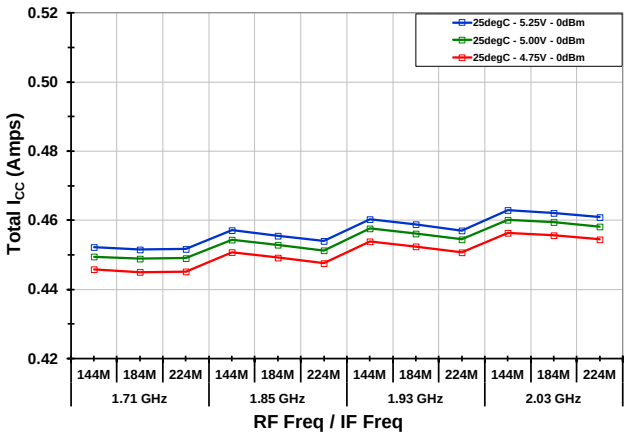
Total Current Drain vs. T_{CASE} [low side inj.]



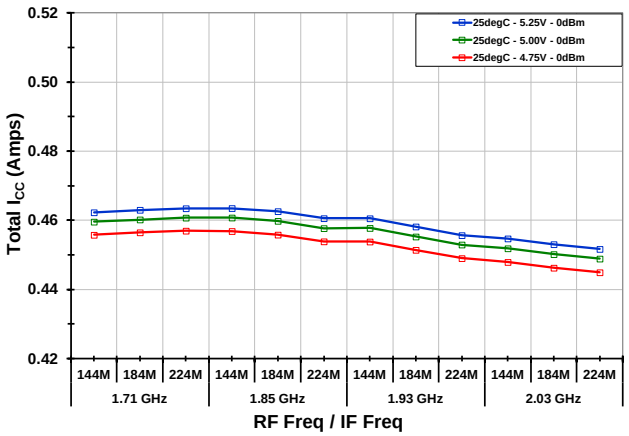
Total Current Drain vs. T_{CASE} [high side inj.]



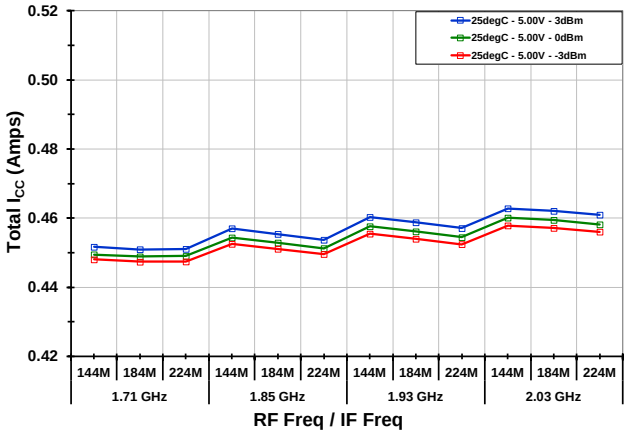
Total Current Drain vs. V_{CC} [low side inj.]



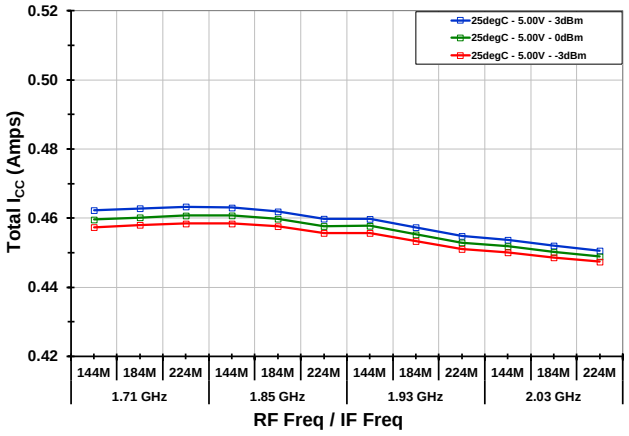
Total Current Drain vs. V_{CC} [high side inj.]



Total Current Drain vs. LO level [low side inj.]

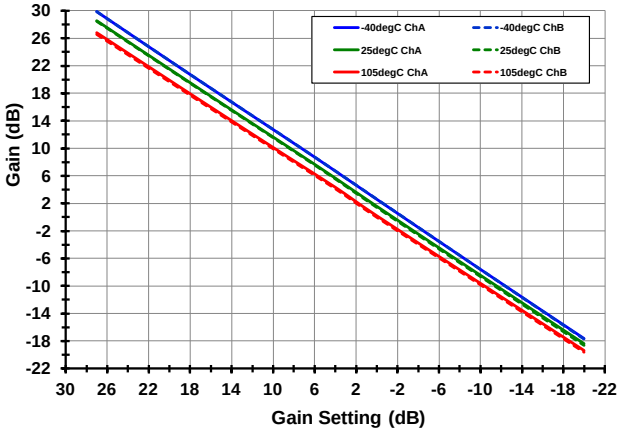


Total Current Drain vs. LO level [high side inj.]

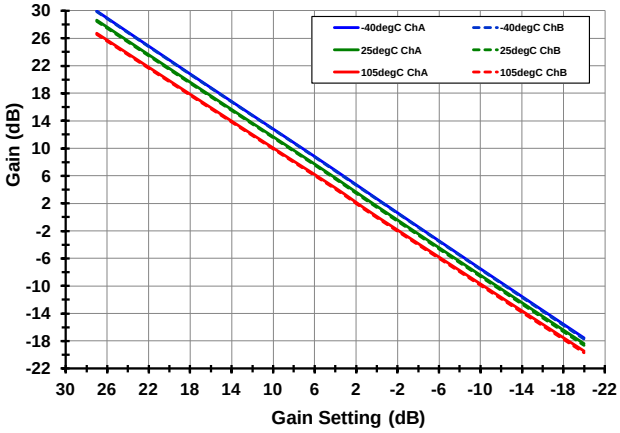


TOCs Swept Gain Setting [STD Mode, IF =184M, LS Injection] Gain, OIP3, IIP3 (-7-)

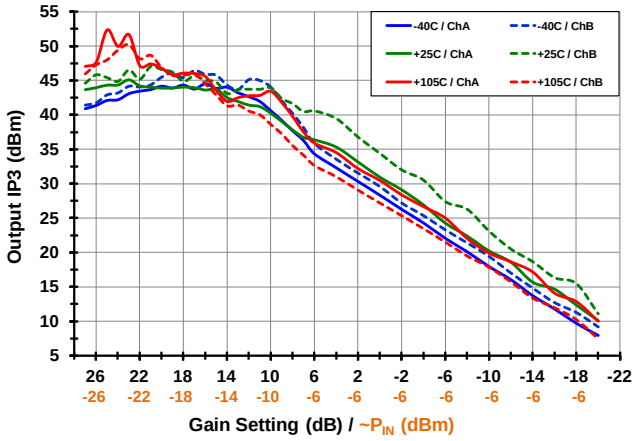
Gain [1.71 GHz]



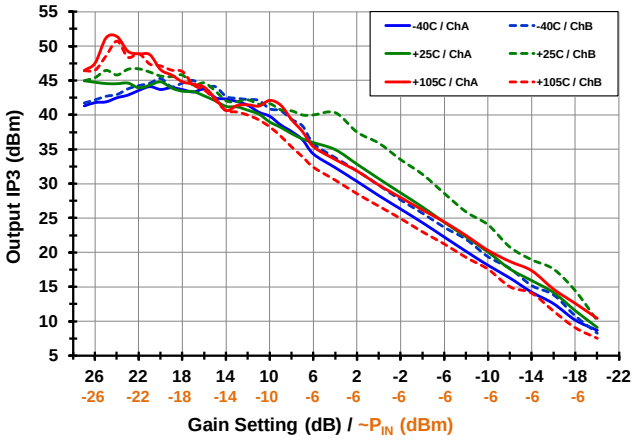
Gain [1.88 GHz]



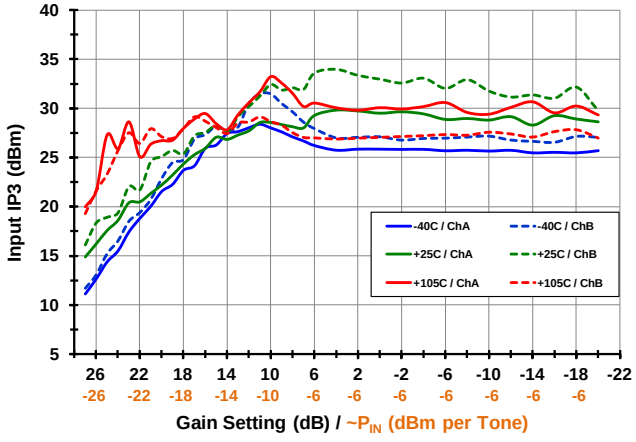
Output IP3 [1.71 GHz]



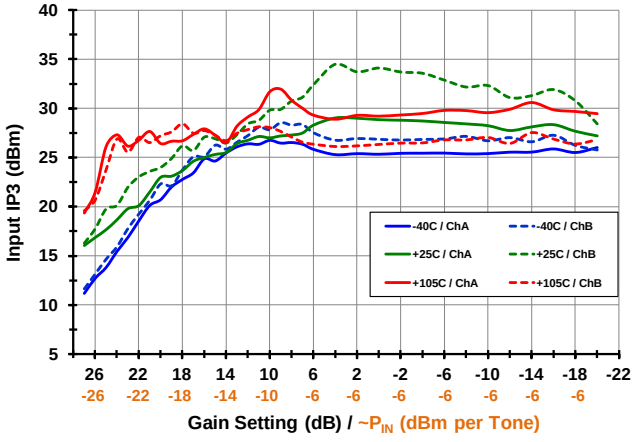
Output IP3 [1.88 GHz]



Input IP3 [1.71 GHz]

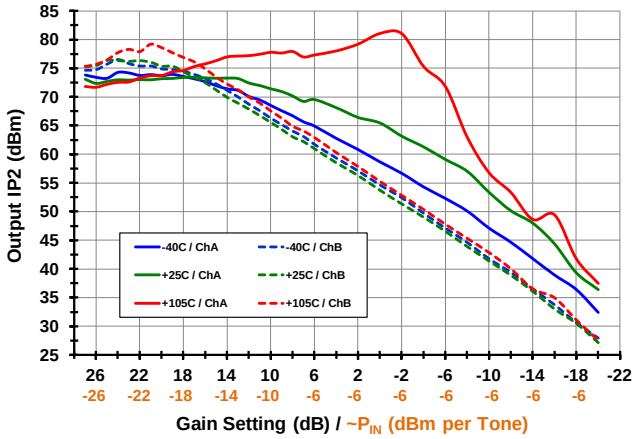


Input IP3 [1.88 GHz]

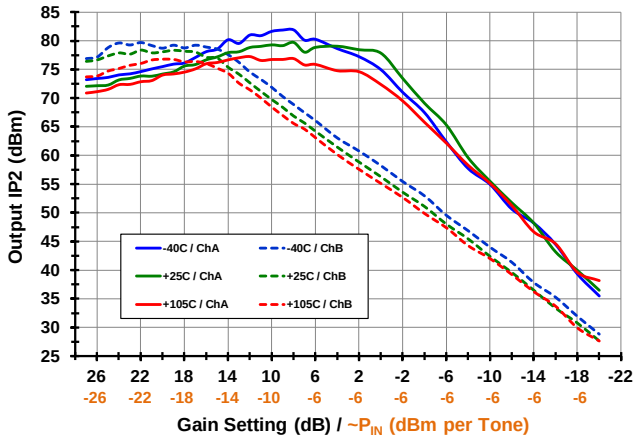


TOCs Swept Gain Setting [STD Mode, IF =184M, LS Injection] OIP2, IIP2, 2X2 (-8-)

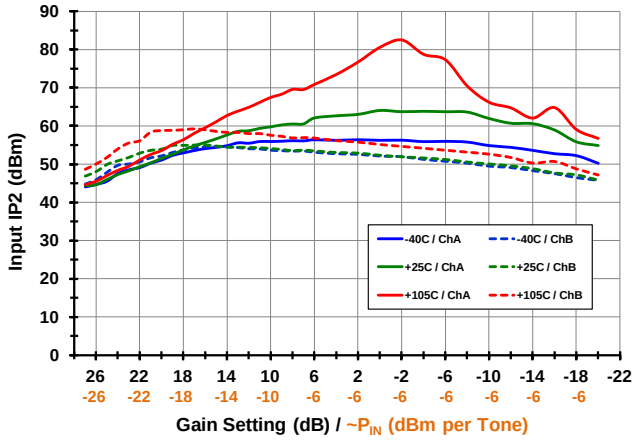
Output IP2 [1.71 GHz]



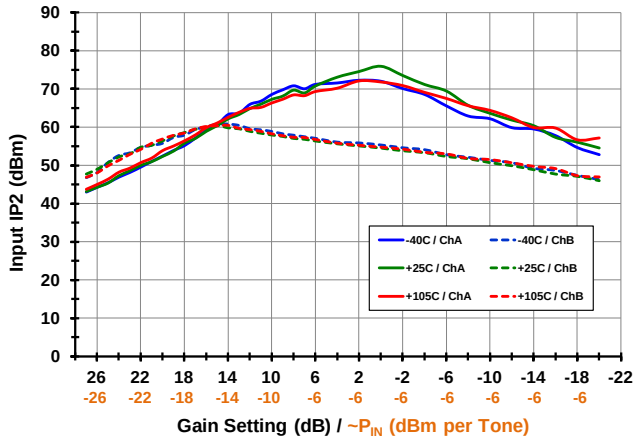
Output IP2 [1.88 GHz]



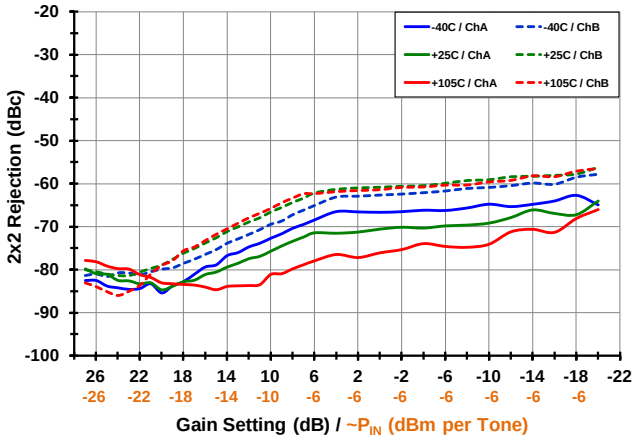
Input IP2 [1.71 GHz]



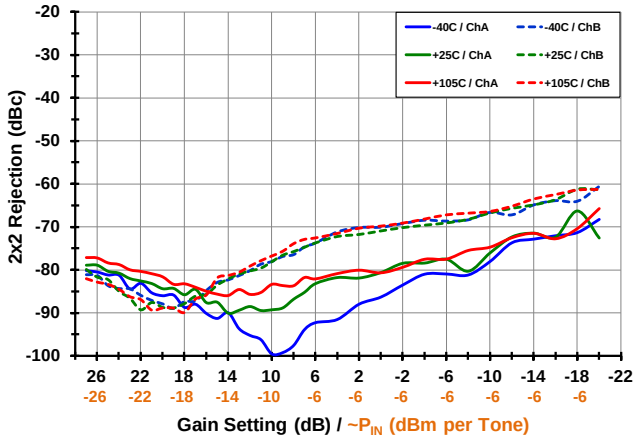
Input IP2 [1.88 GHz]



2x2 Rejection [1.71 GHz]

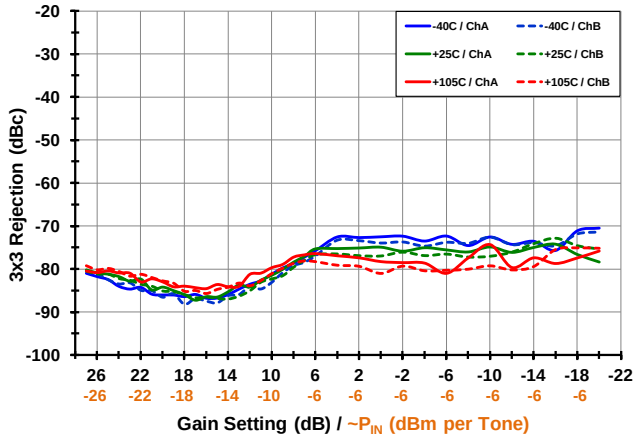


2x2 Rejection [1.88 GHz]

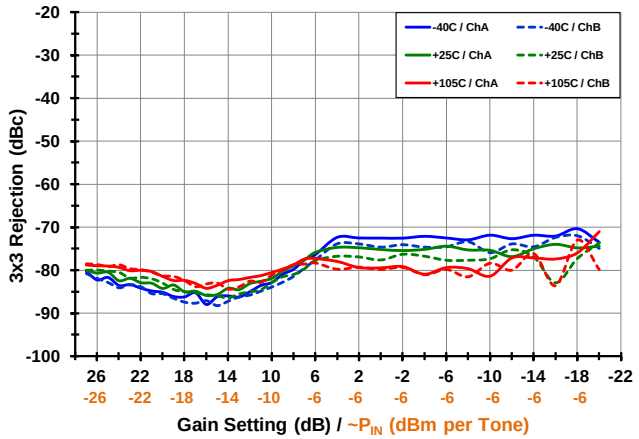


TOCs Swept Gain Setting [STD Mode, IF =184M, LS Injection] 3X3, Leakage (-9-)

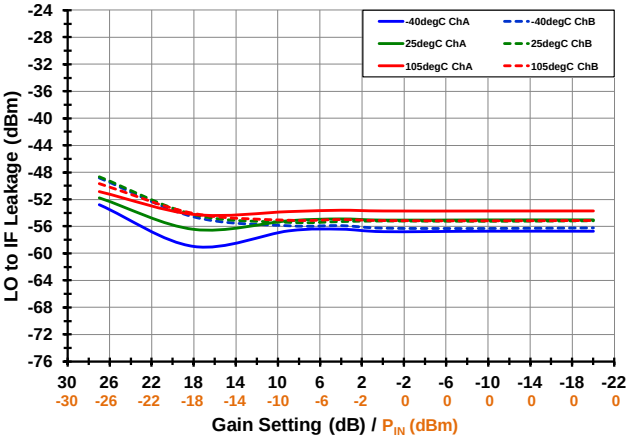
3x3 Rejection [1.71 GHz]



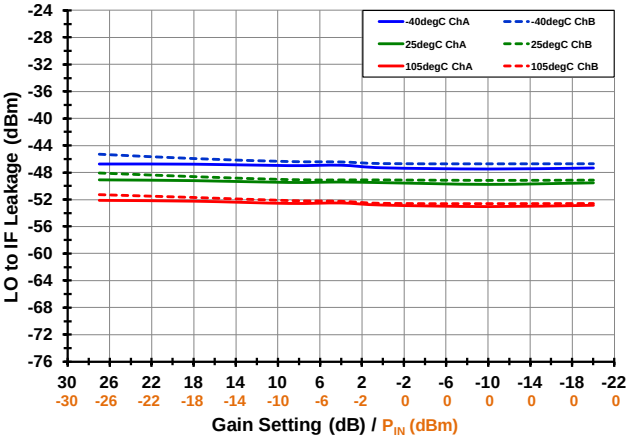
3x3 Rejection [1.88 GHz]



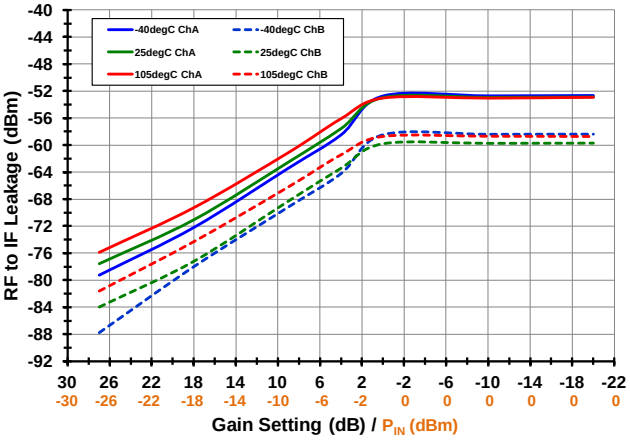
LO to IF Leakage [low side inj, 1.85 GHz]



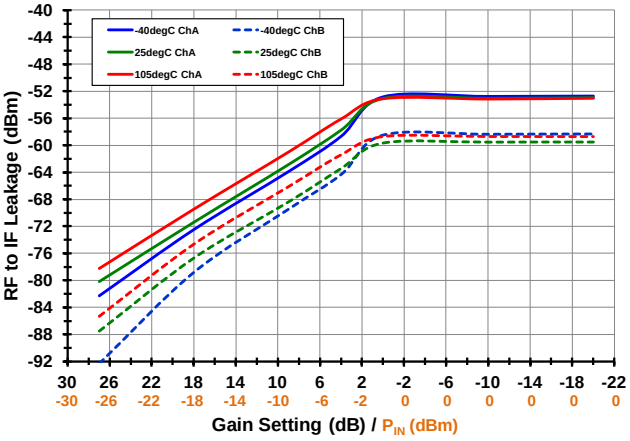
LO to IF Leakage [high side inj., 1.85 GHz]



RF to IF Leakage [low side inj., 1.85 GHz]

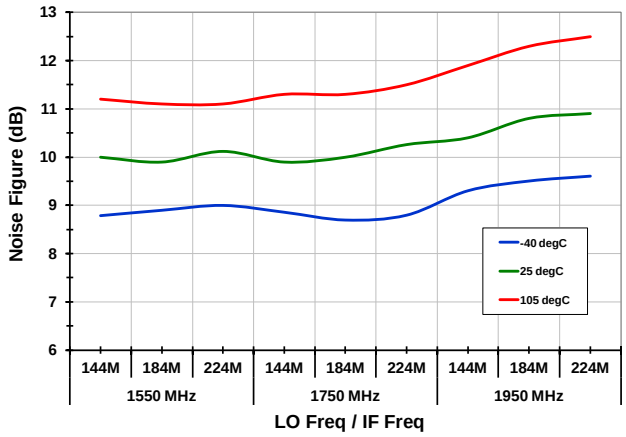


RF to IF Leakage [high side inj., 1.85 GHz]

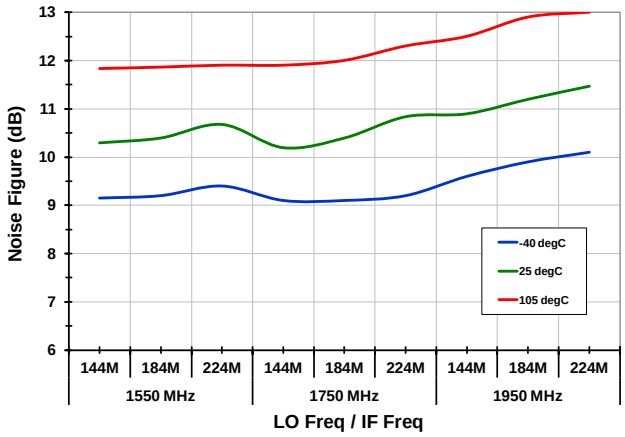


TOCs Noise Figure [STD Mode, CHA only] (-10-)

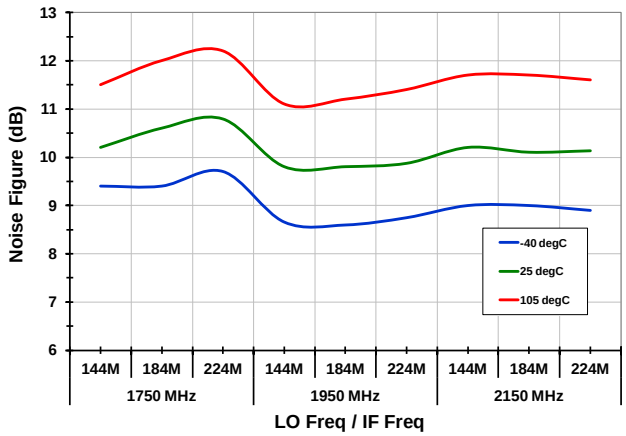
RF & IF Freq Sweep [G_{MAX}, Low Side inj.]



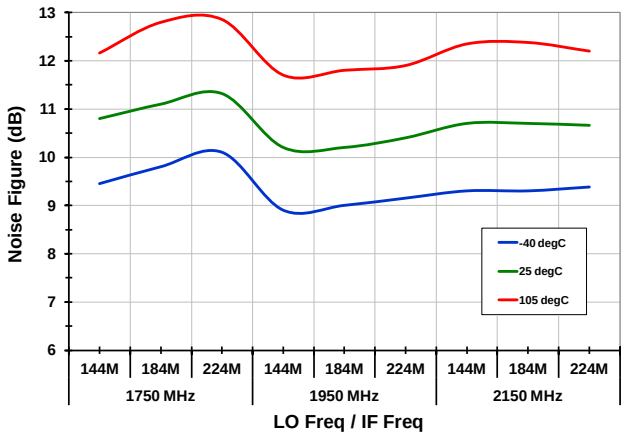
RF & IF Freq Sweep [G_{10dB}, Low Side inj.]



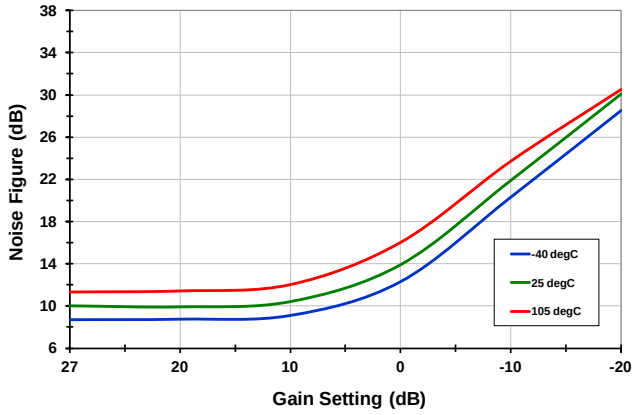
RF & IF Freq Sweep [G_{MAX}, High Side inj.]



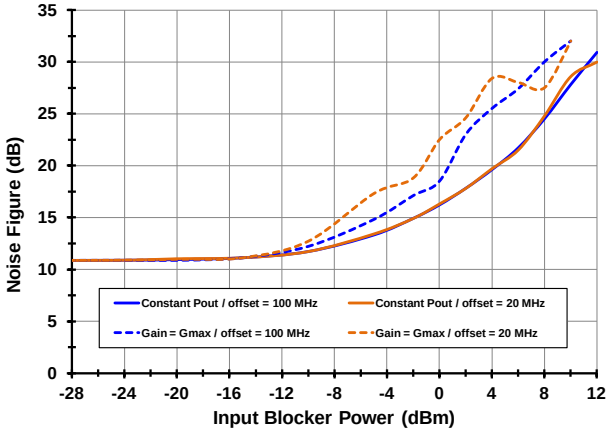
RF & IF Freq Sweep [G_{10dB}, High Side inj.]



Gain Setting Sweep [LO = 1.75 GHz, IF = 184 MHz]

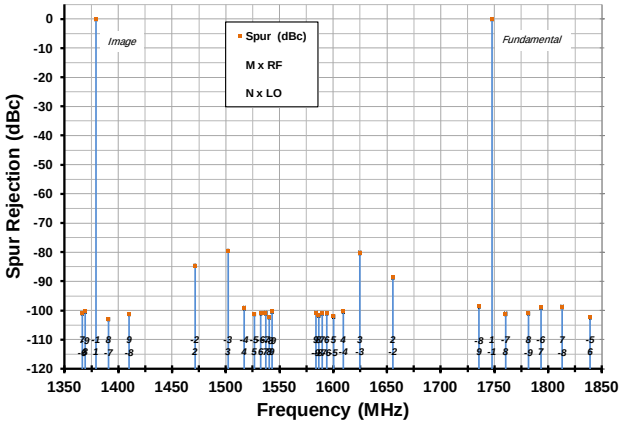


Blocker Power Sweep [LO = 2.15 GHz, T_A = 25C]

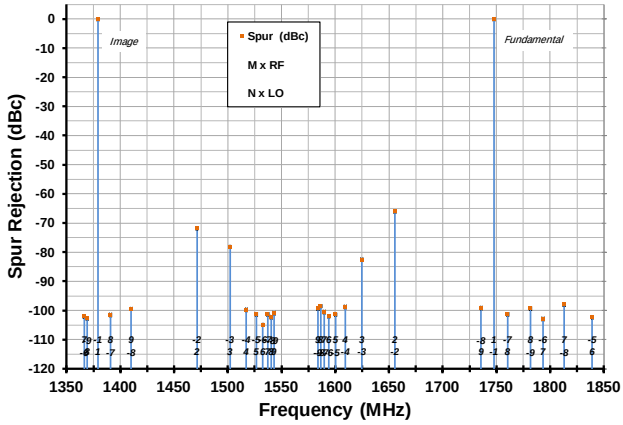


TOCs SPURS [STD MODE, IF MATCH 184M, LO = 1.563 GHz, GAIN = 0 dB, T_A = 25C] (-11-)

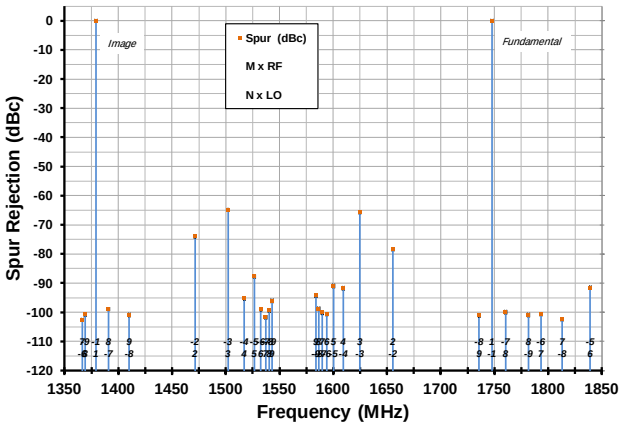
Close-In Spurs [ChA, P_{RF} = -5 dBm]



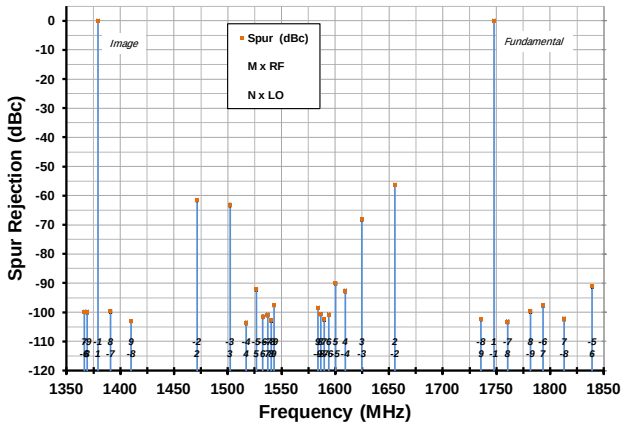
Close-In Spurs [ChB, P_{RF} = -5 dBm]



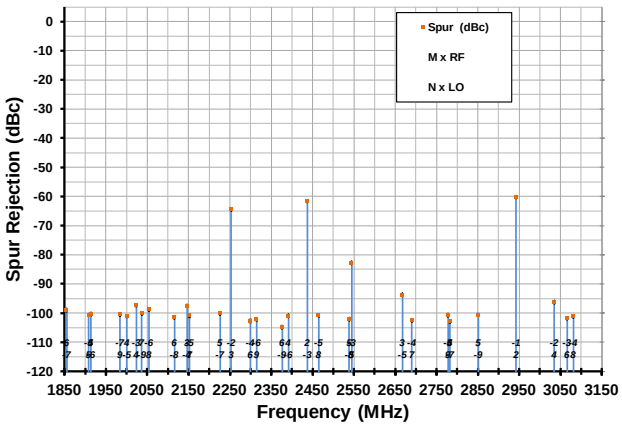
Close-In Spurs [ChA, P_{RF} = 0 dBm]



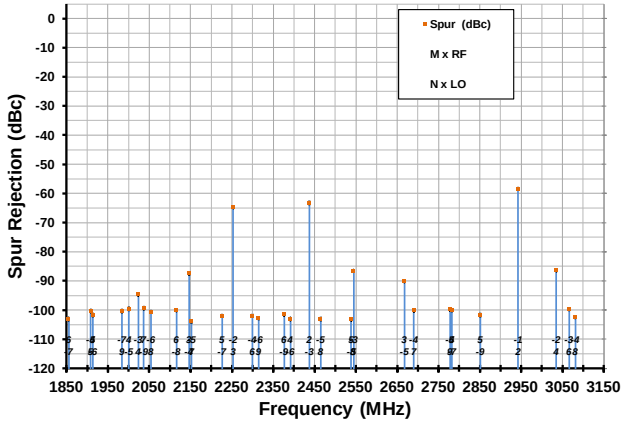
Close-In Spurs [ChB, P_{RF} = 0 dBm]



Other Spurs [ChA, P_{RF} = -5 dBm]

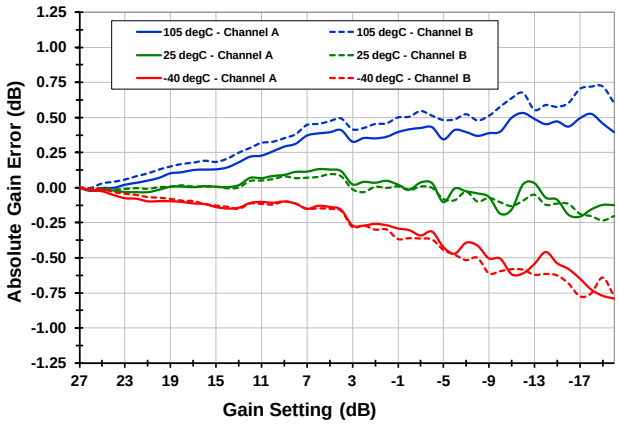


Other Spurs [ChB, P_{RF} = -5 dBm]

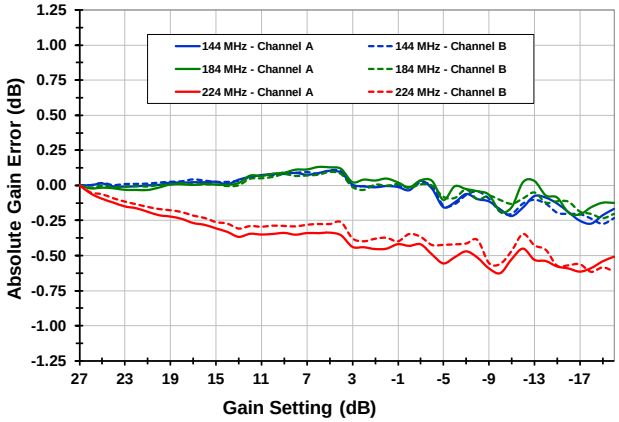


GAIN ACCURACY, BOARD LOSSES (-12-)

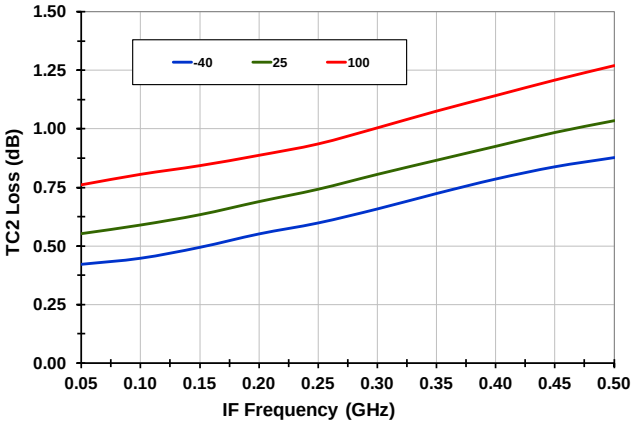
Accuracy vs. T_{CASE} [RF = 1.85 GHz, IF = 184 MHz]



Accuracy vs. IF Freq [RF = 1.85 GHz, T_{CASE} = 25C]

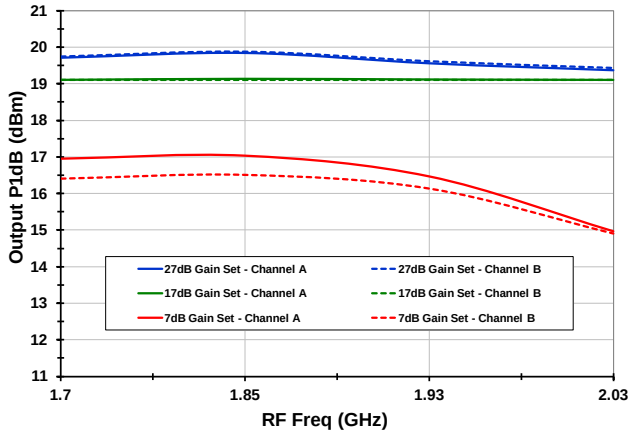


Transformer TC2-7T Loss vs. Temperature

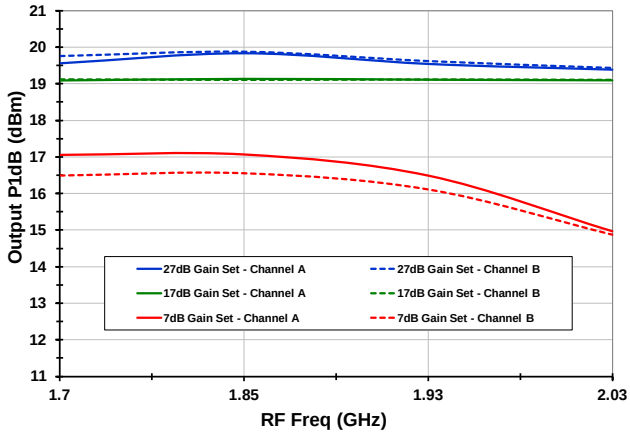


TOCs P1dB [STD Mode] (-13-)

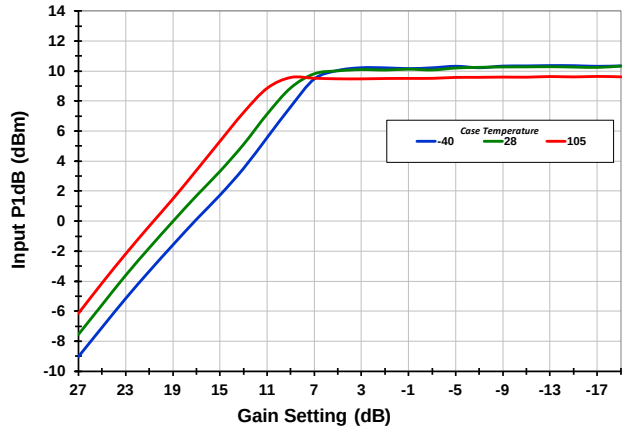
P1dB RF Sweep [IF = 184 MHz, Low Side inj.]



P1dB RF Sweep [IF = 184 MHz, High Side inj.]



P1dB Gain Set Sweep [RF = 1.88 GHz IF = 184 MHz]



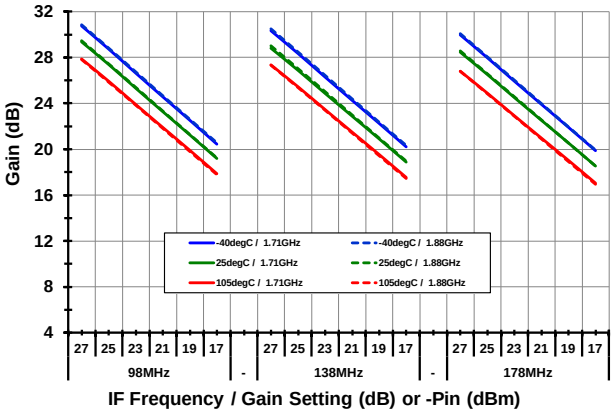
TYPICAL OPERATING CONDITIONS (STD MODE, 138MHZ IF)

Unless otherwise noted, the following conditions apply to the 138MHz Typ Ops Graphs:

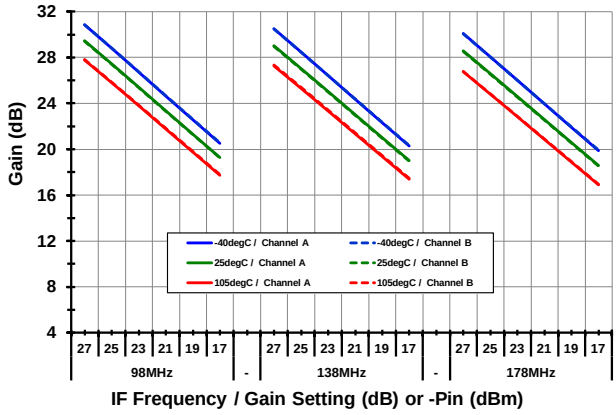
- BOM2 Applications circuit with 138MHz IF Center +/- 40 MHz bandwidth network to provide matching to 100 ohm differential load provided by 2:1 transformer (see page 51)
- Pout ~ +1dBm
- P_{IN} from -27 to -6 dBm (Gain Setting Adjusted to yield Pout ~ +1 dBm without exceeding -6dBm P_{IN})
- Tone Spacing = 800kHz
- Device configured in Standard Mode with Low Side Injection
- T_{CASE} = 25°C, V_{CC} = 5.00V, LO Power = 0dBm
- RF Frequency: 1.88GHz
- IF Frequency: 138MHz
- Transformer Losses are de-embedded
- Input RF trace Losses are not de-embedded

TOCs [STD Mode, IF = 138M, LS Injection] Gain, OIP3, OIP2 (-14-)

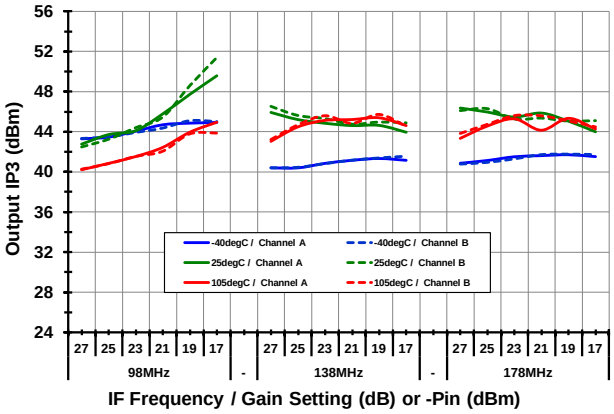
Gain vs. T_{CASE} [1.71 GHz RF]



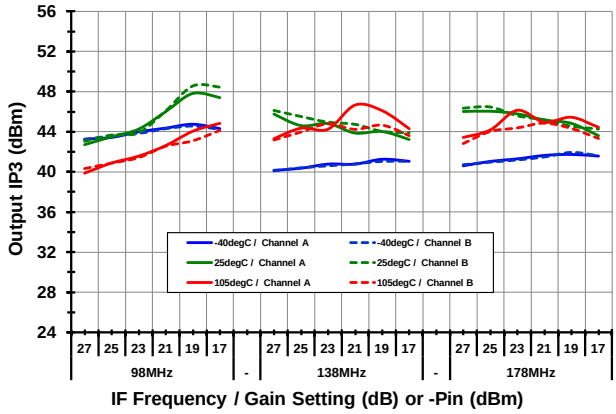
Gain vs. T_{CASE} [1.88 GHz RF]



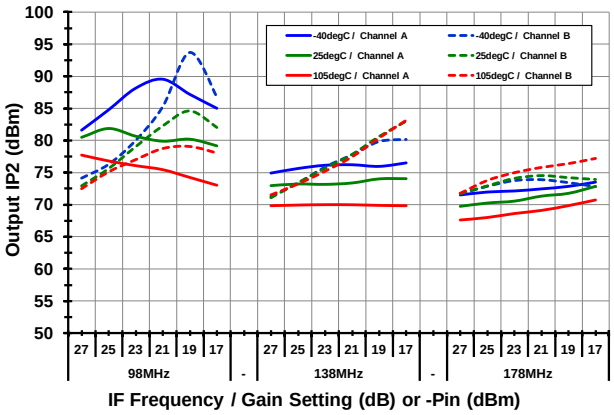
Output IP3 vs. T_{CASE} [1.71 GHz RF]



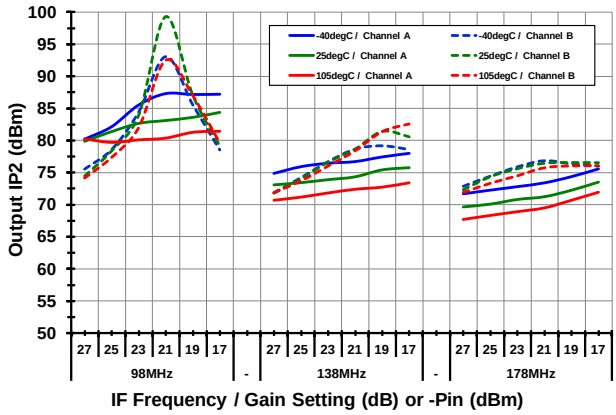
Output IP3 vs. T_{CASE} [1.88 GHz RF]



Output IP2 vs. T_{CASE} [1.71 GHz RF]

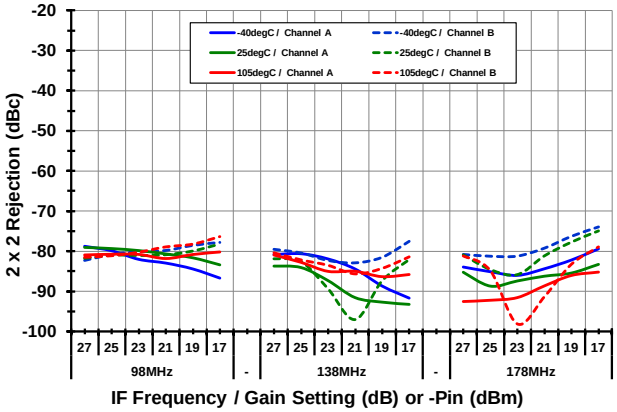


Output IP2 vs. T_{CASE} [1.88 GHz RF]

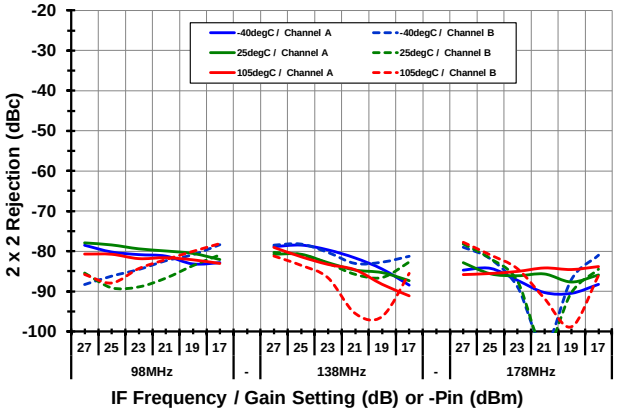


TOCs [STD Mode, IF = 138M, LS Injection] 2X2, 3X3, Leakage (-15-)

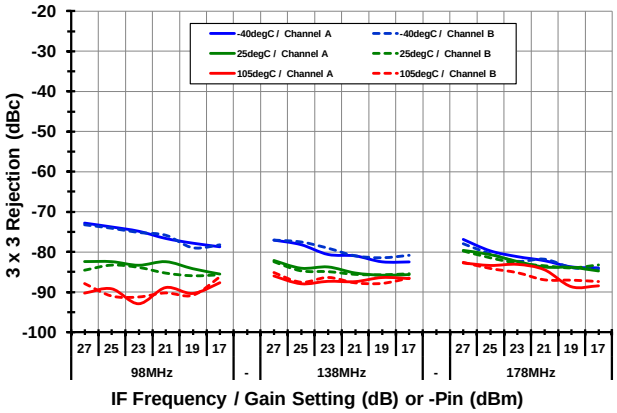
2 X 2 vs. T_{CASE} [1.71 GHz RF]



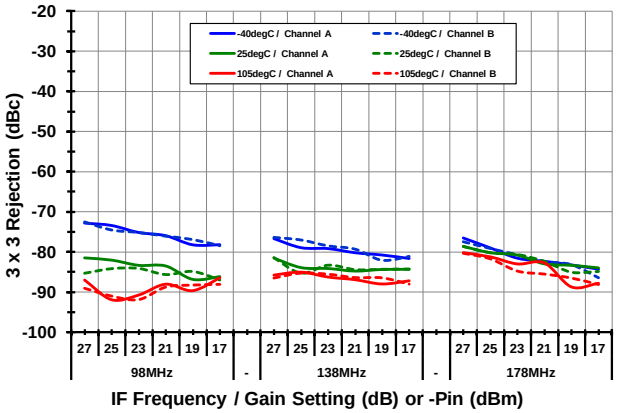
2 X 2 vs. T_{CASE} [1.88 GHz RF]



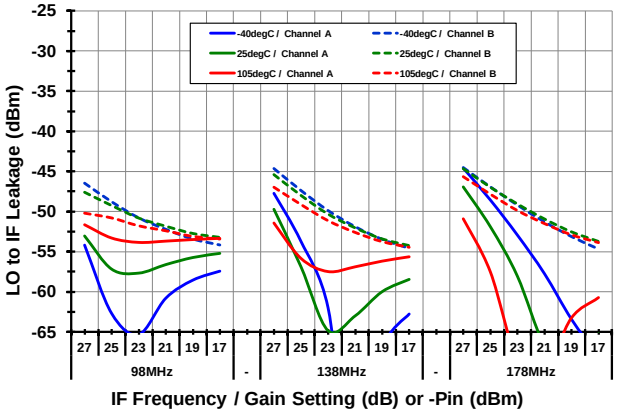
3 x 3 vs. T_{CASE} [1.71 GHz RF]



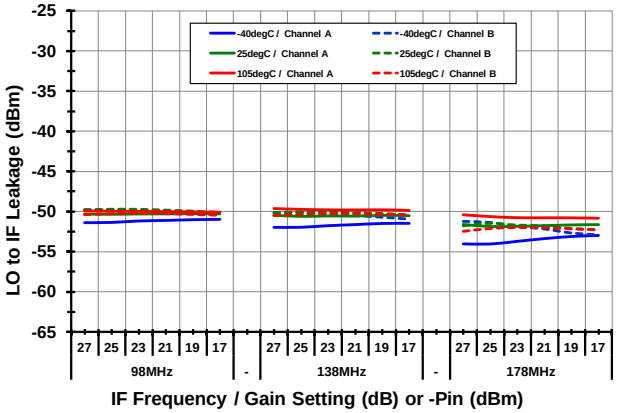
3 x 3 vs. T_{CASE} [1.88 GHz RF]



LO to IF Leakage vs. T_{CASE} [1.71 GHz RF]

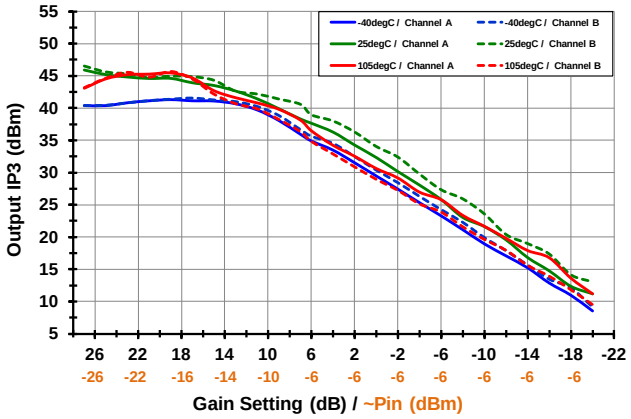


LO to IF Leakage vs. T_{CASE} [1.88 GHz RF]

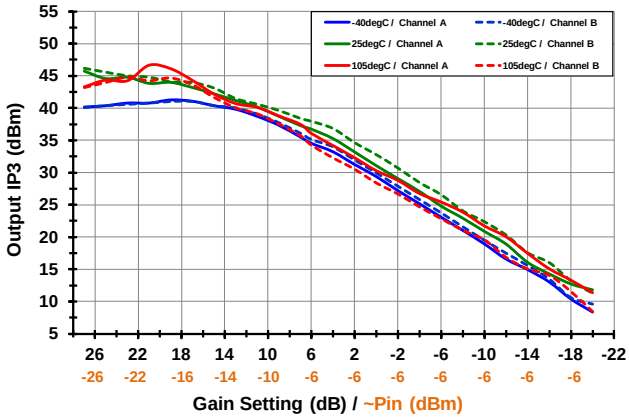


TOCs [STD MODE, IF = 138M, LS INJECTION] OIP3, OIP3, 2X2 (-16-)

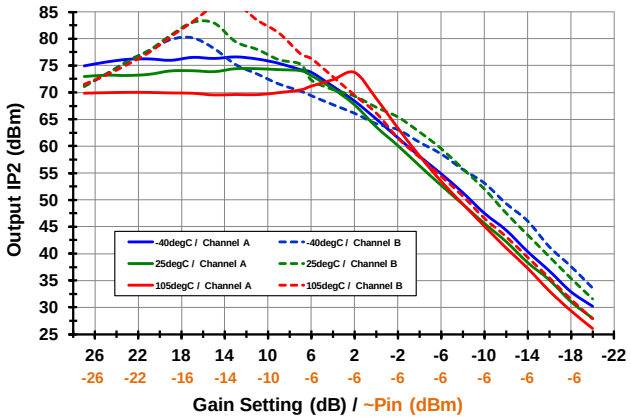
Output IP3 [1.71 GHz RF]



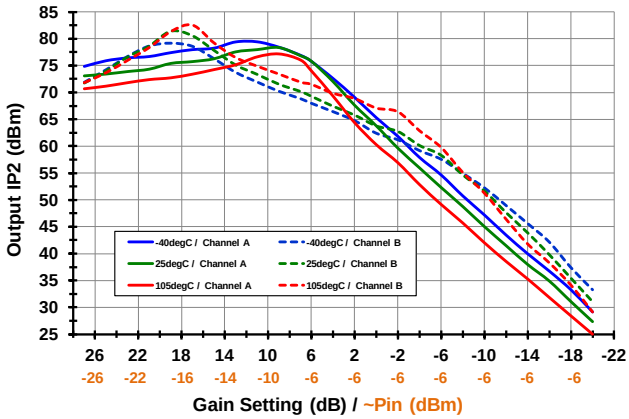
Output IP3 [1.88 GHz RF]



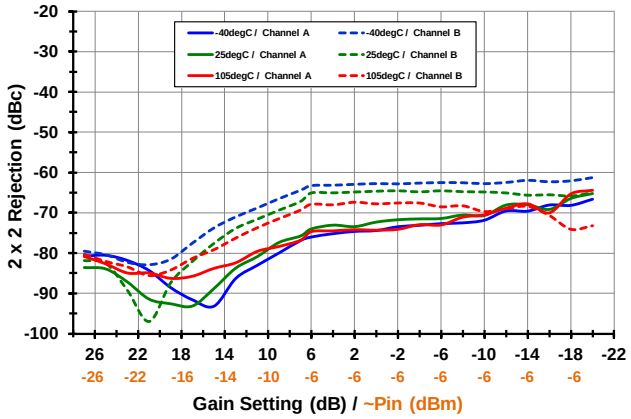
Output IP2 [1.71 GHz RF]



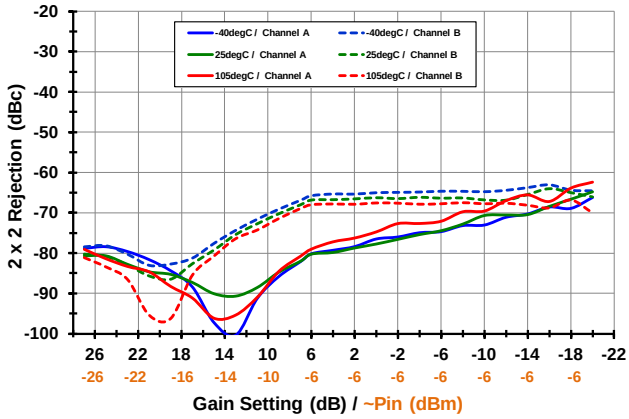
Output IP2 [1.88 GHz RF]



2x2 Rejection [1.71 GHz RF]

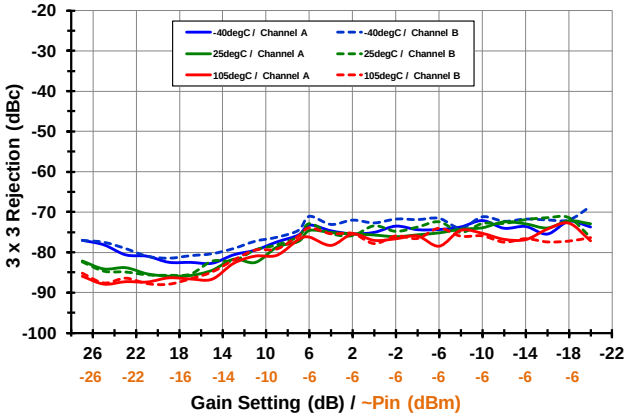


2x2 Rejection [1.88 GHz RF]

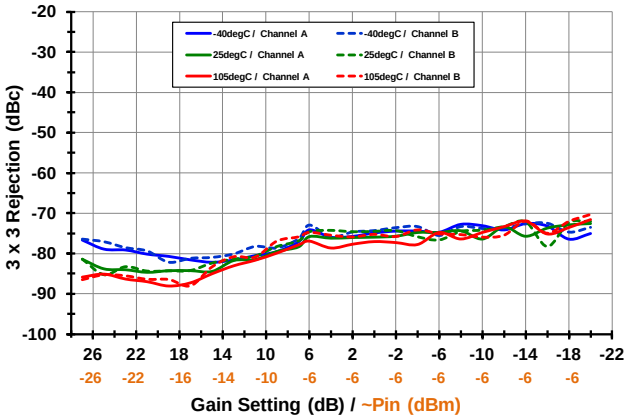


TOCs [STD Mode, IF = 138M, LS Injection] 3X3, Leakage (-17-)

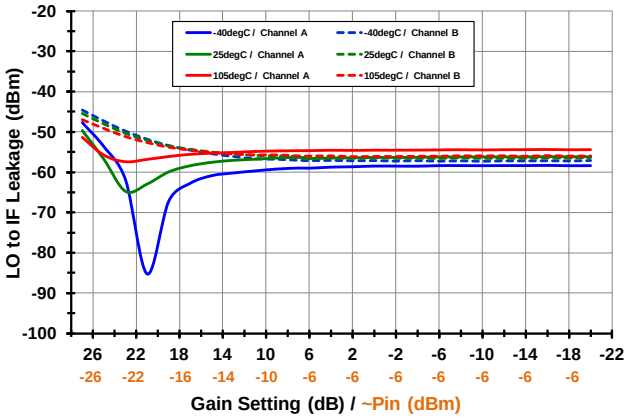
3x3 Rejection [1.71 GHz RF]



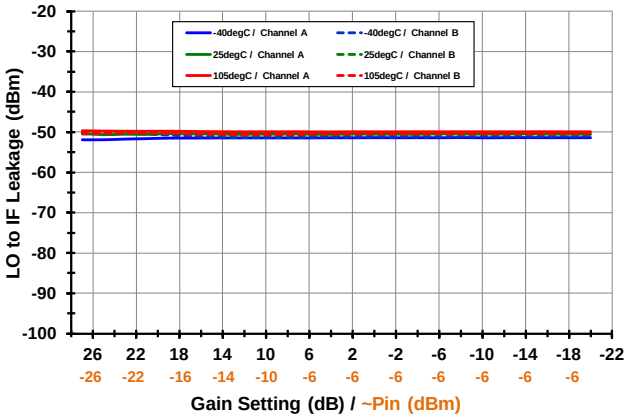
3x3 Rejection [1.88 GHz RF]



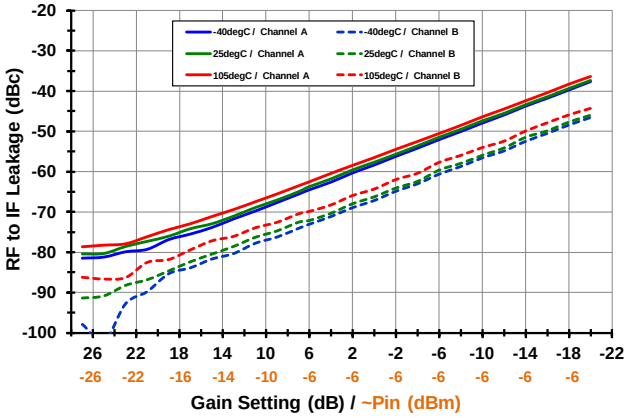
LO to IF Leakage [1.71 GHz RF]



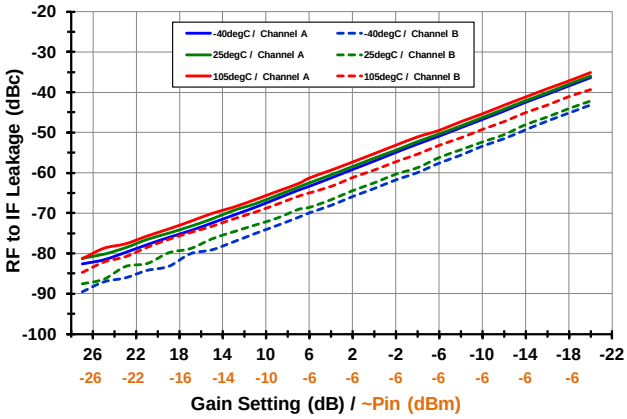
LO to IF Leakage [1.88 GHz RF]



RF to IF Leakage [1.71 GHz RF]



RF to IF Leakage [1.88 GHz RF]



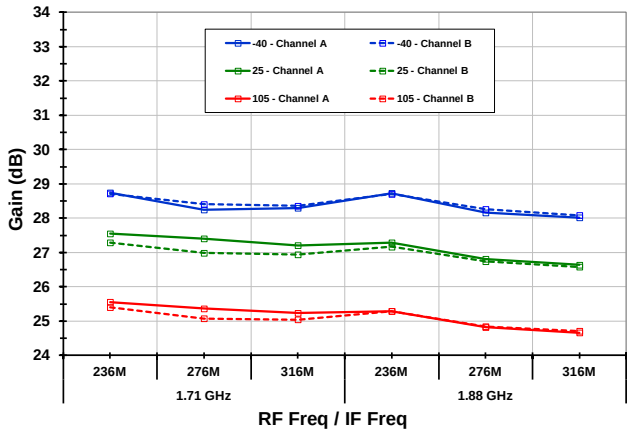
TYPICAL OPERATING CONDITIONS (STD MODE, 276MHZ IF)

Unless otherwise noted, the following conditions apply to the 276MHz Typ Ops Graphs:

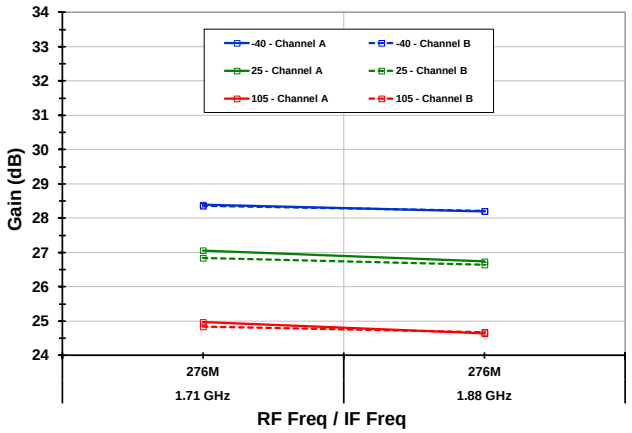
- BOM2 Applications circuit with 276MHz IF Center +/- 40 MHz bandwidth network to provide matching to 100 ohm differential load provided by 2:1 transformer (see page 51)
- Pout ~ +1dBm
- P_{IN} from -27 to -6 dBm (Gain Setting Adjusted to yield Pout ~ +1 dBm without exceeding -6dBm P_{IN})
- Tone Spacing = 800kHz
- Device configured in Standard Mode with Low Side Injection
- T_{CASE} = 25C, V_{CC} = 5.00V, LO Power = 0dBm
- RF Frequency: 1.88GHz
- IF Frequency: 276MHz
- Transformer Losses are de-embedded
- Input RF trace Losses are not de-embedded

TOCs [MAX GAIN, IF = 276M, STD MODE] GAIN, OIP3, OIP2 (-18-)

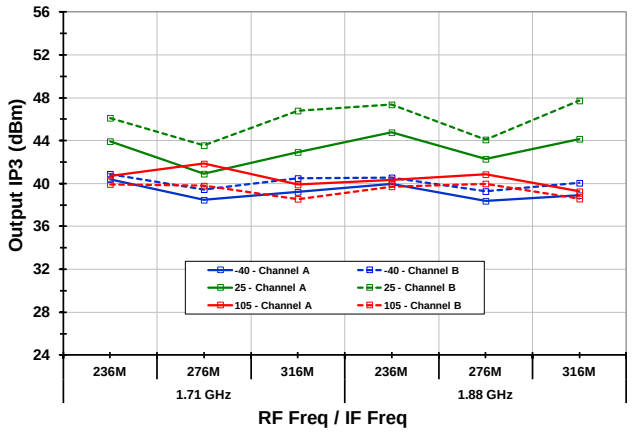
Gain vs. T_{CASE} [low side inj.]



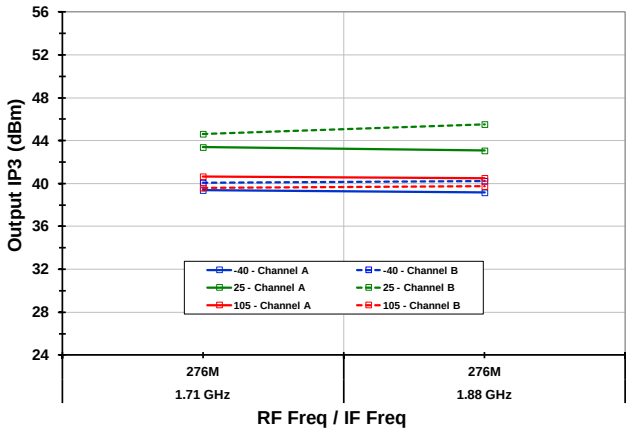
Gain vs. T_{CASE} [high side inj.]



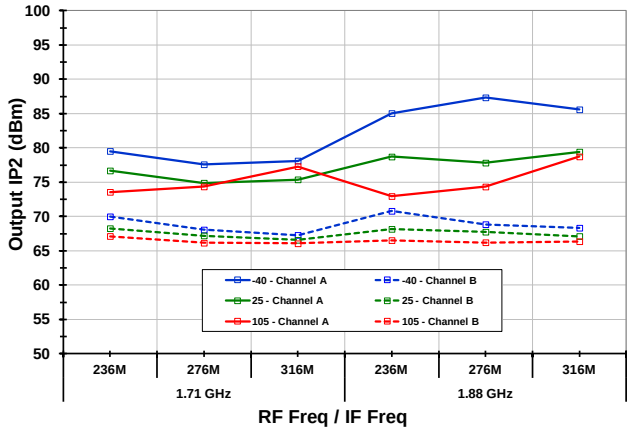
Output IP3 vs. T_{CASE} [low side inj.]



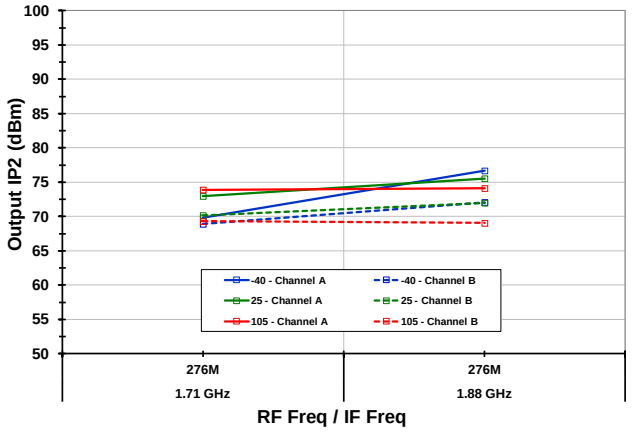
Output IP3 vs. T_{CASE} [high side inj.]



Output IP2 vs. T_{CASE} [low side inj.]

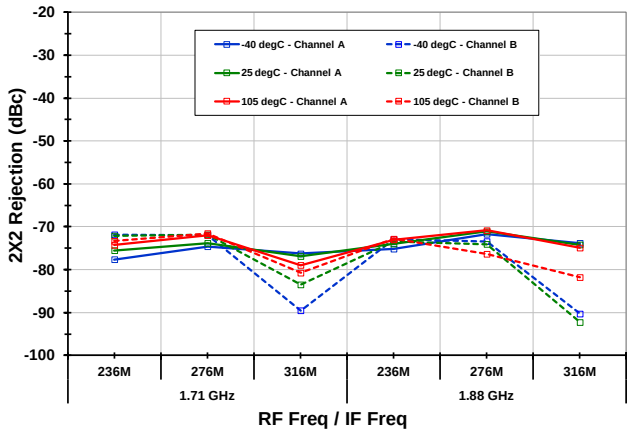


Output IP2 vs. T_{CASE} [high side inj.]

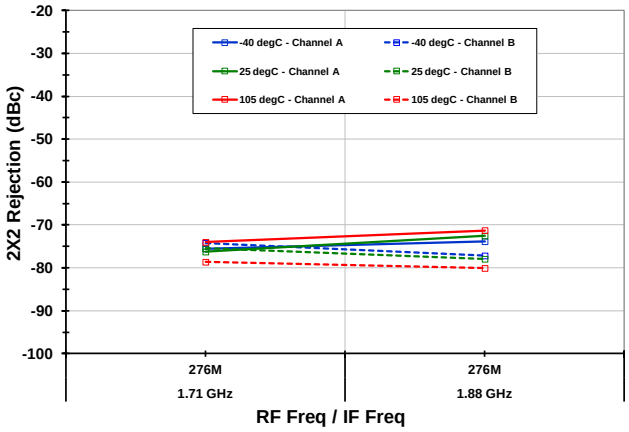


TOCs [MAX GAIN, IF = 276M, STD MODE] 2X2, 3X3, LEAKAGE (-19-)

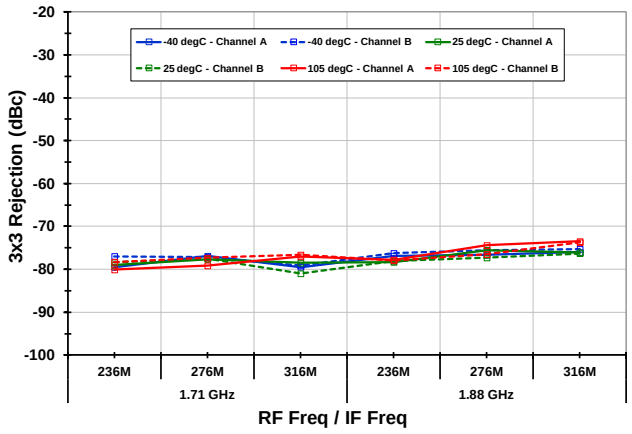
2 X 2 vs. T_{CASE} [low side inj.]



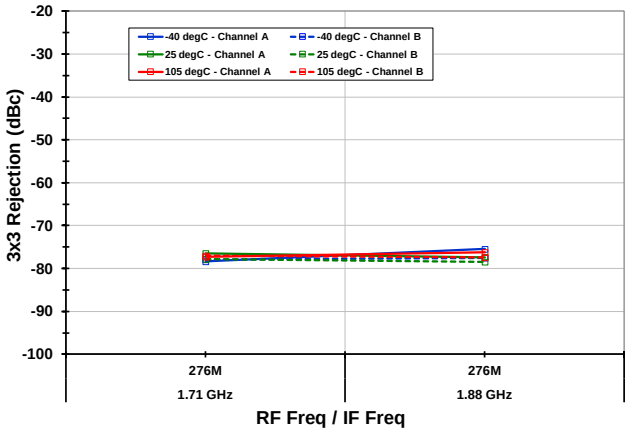
2 X 2 vs. T_{CASE} [high side inj.]



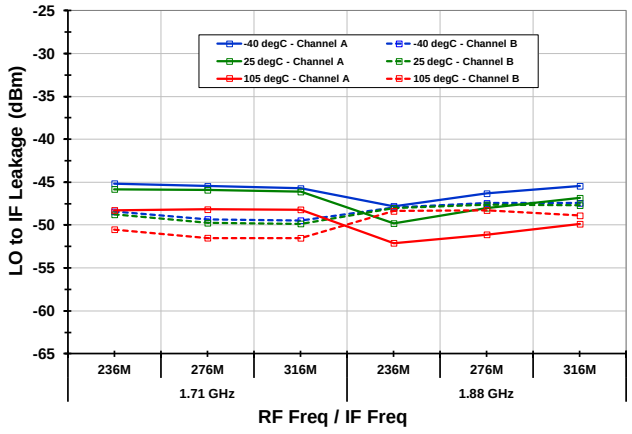
3 x 3 vs. TCASE [low side inj.]



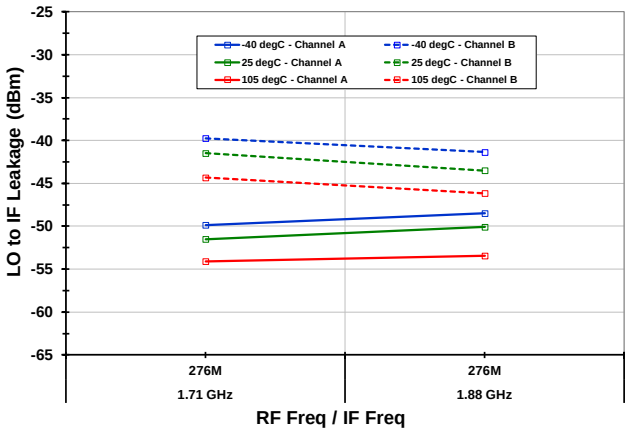
3 x 3 vs. T_{CASE} [high side inj.]



LO to IF Leakage vs. T_{CASE} [low side inj.]

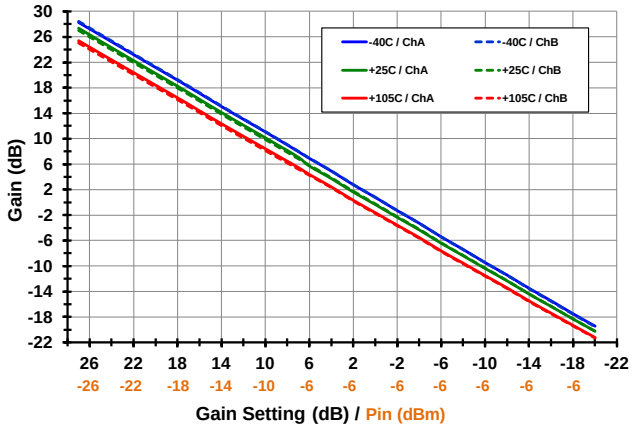


LO to IF Leakage vs. T_{CASE} [high side inj.]

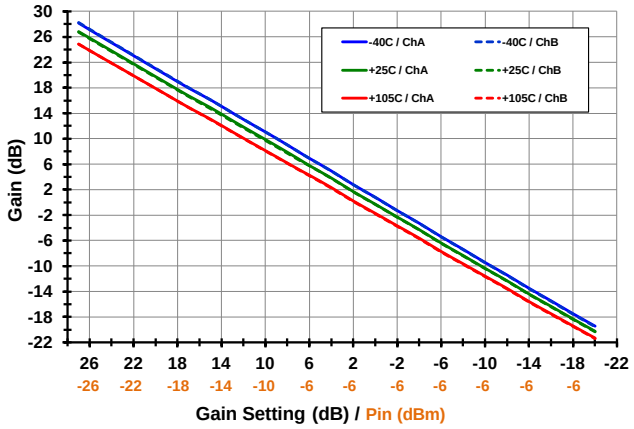


TOCs Swept Gain Setting [STD Mode, IF =276M, LS Injection] Gain, OIP3, IIP3 (-20-)

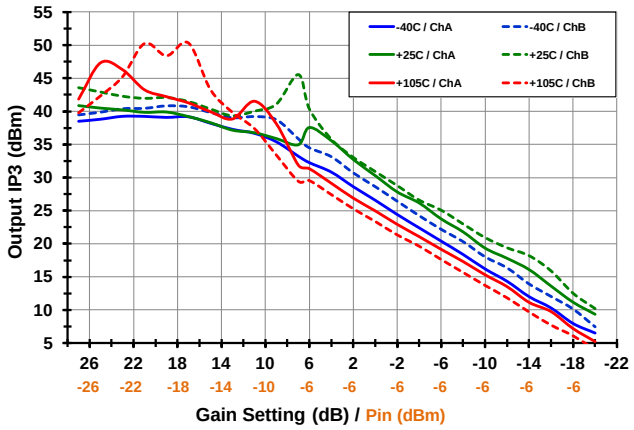
Gain [1.71 GHz]



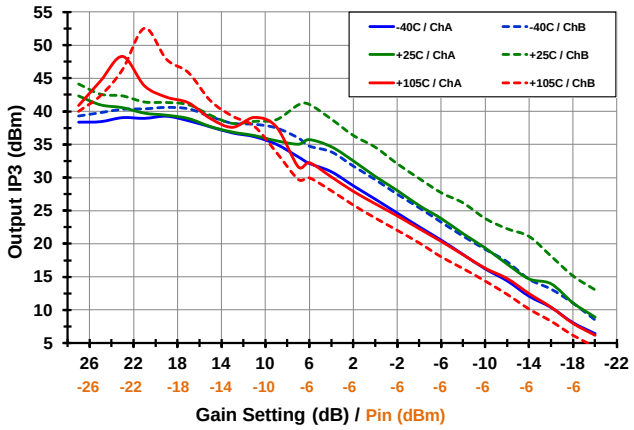
Gain [1.88 GHz]



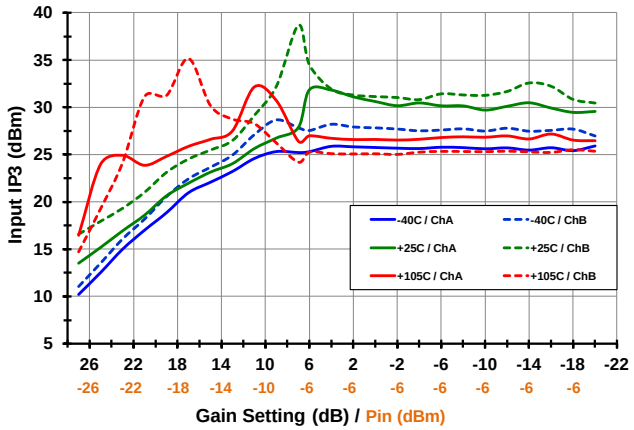
Output IP3 [1.71 GHz]



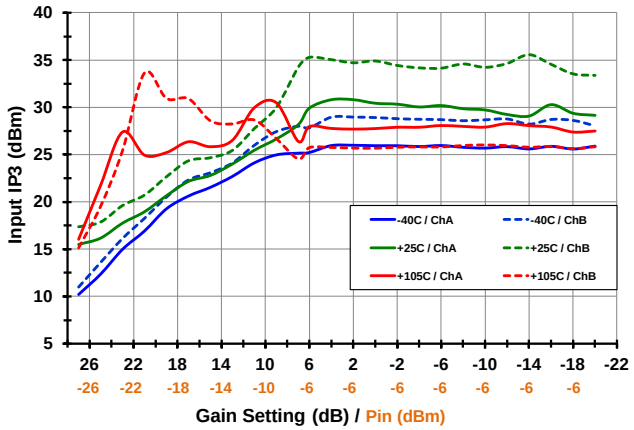
Output IP3 [1.88 GHz]



Input IP3 [1.71 GHz]

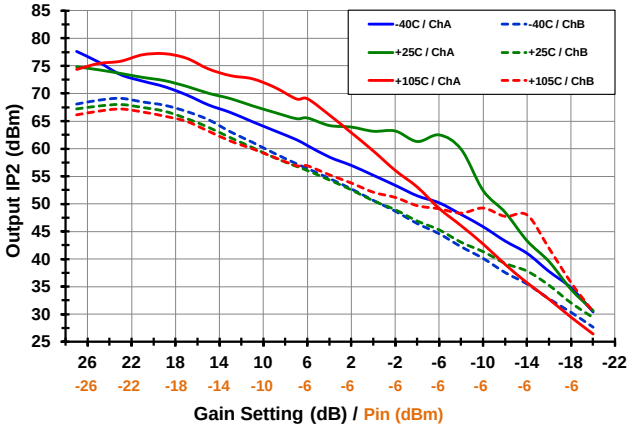


Input IP3 [1.88 GHz]

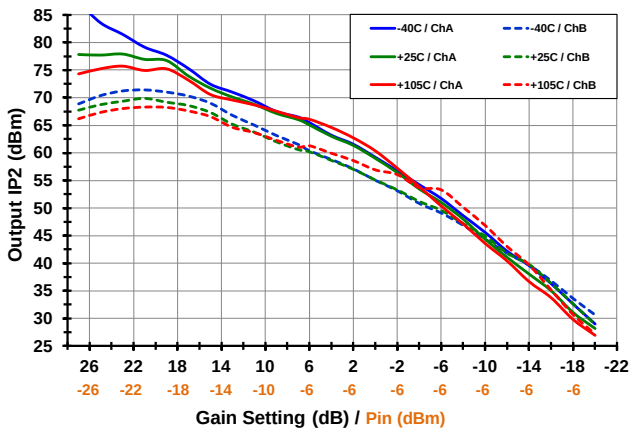


TOCs Swept Gain Setting [STD Mode, IF =276M, LS Injection] OIP2, IIP2, 2X2 (-21-)

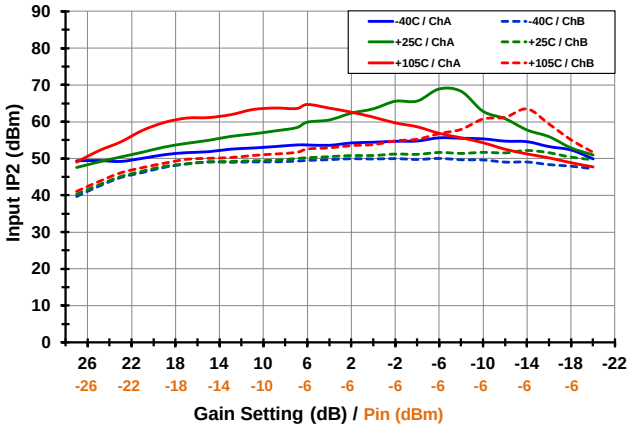
Output IP2 [1.71 GHz]



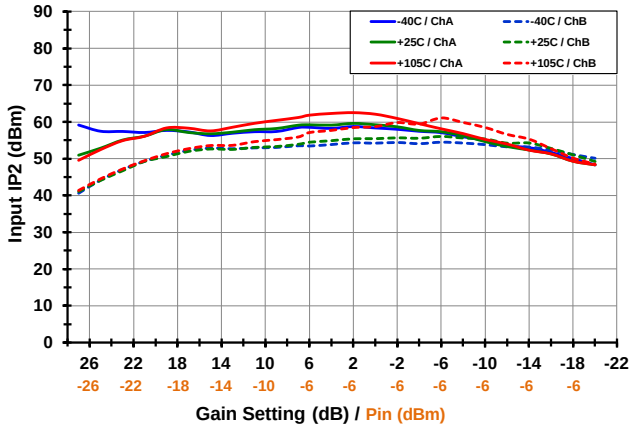
Output IP2 [1.88 GHz]



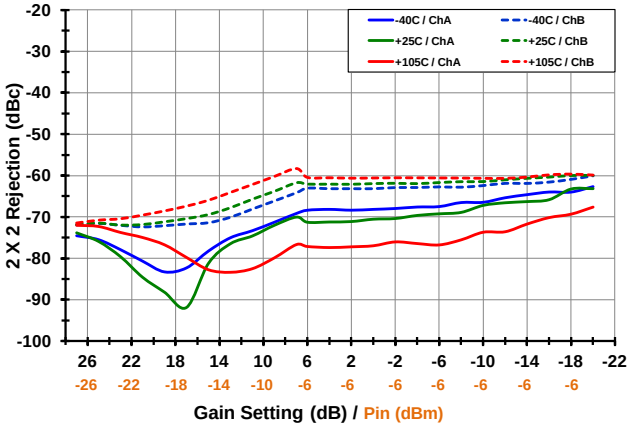
Input IP2 [1.71 GHz]



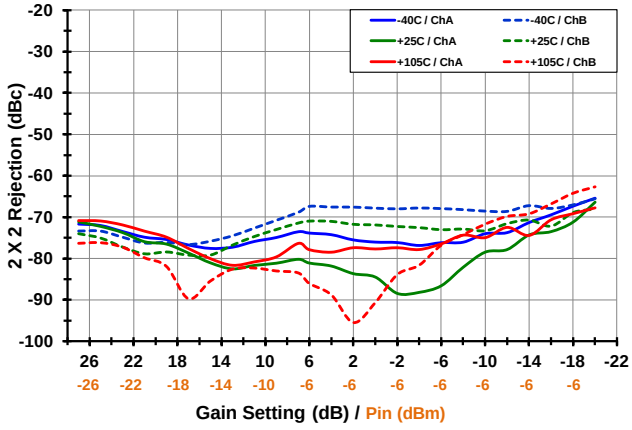
Input IP2 [1.88 GHz]



2x2 Rejection [1.71 GHz]

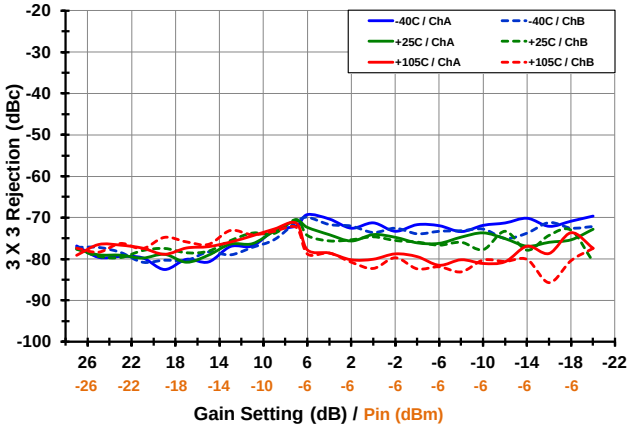


2x2 Rejection [1.88 GHz]

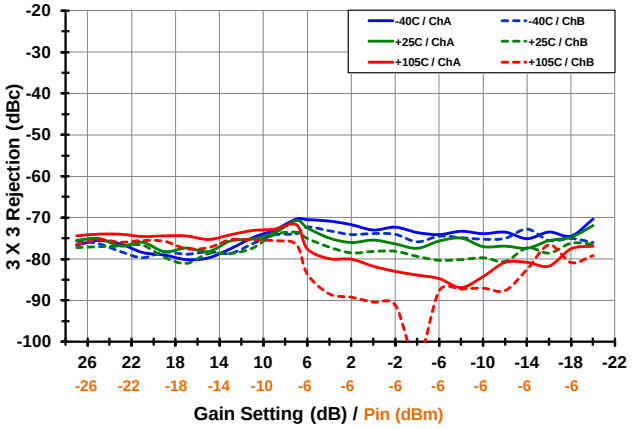


TOCs Swept Gain Setting [STD Mode, IF =276M, LS Injection] 3X3, Leakage (-22-)

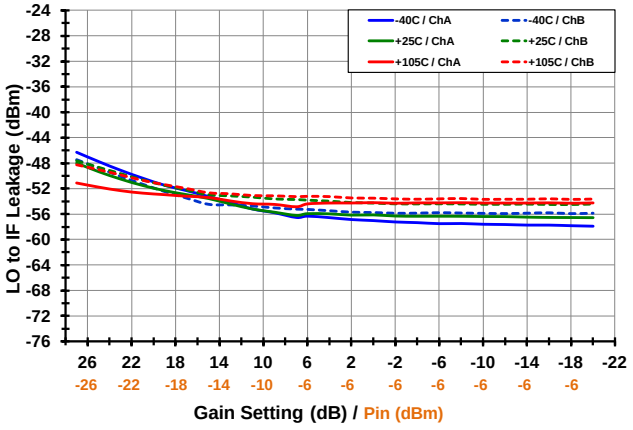
3x3 Rejection [1.71 GHz]



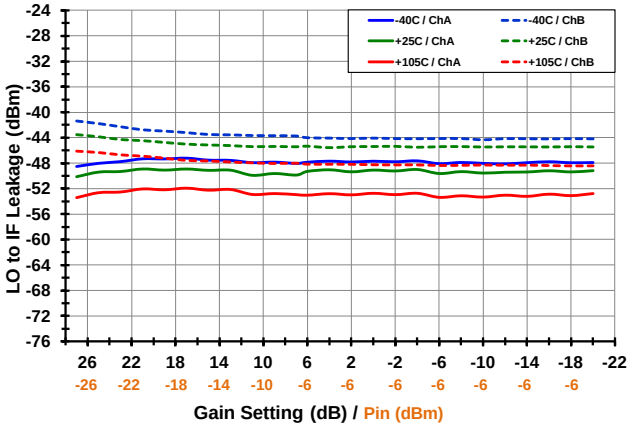
3x3 Rejection [1.88 GHz]



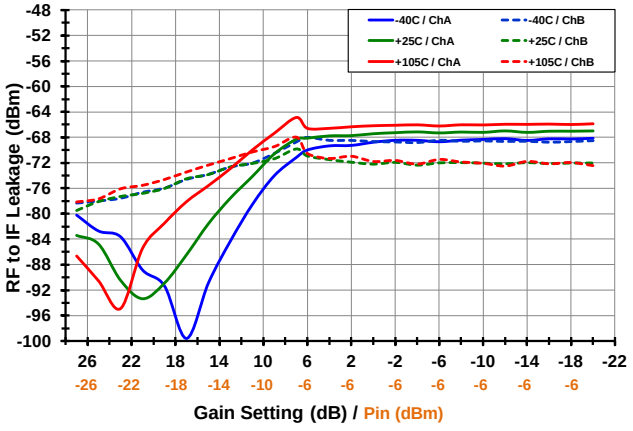
LO to IF Leakage [low side inj, 1.88 GHz]



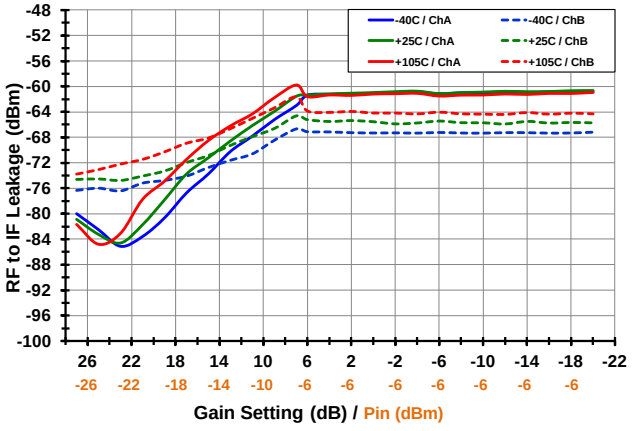
LO to IF Leakage [high side inj., 1.88 GHz]



RF to IF Leakage [1.71 GHz]



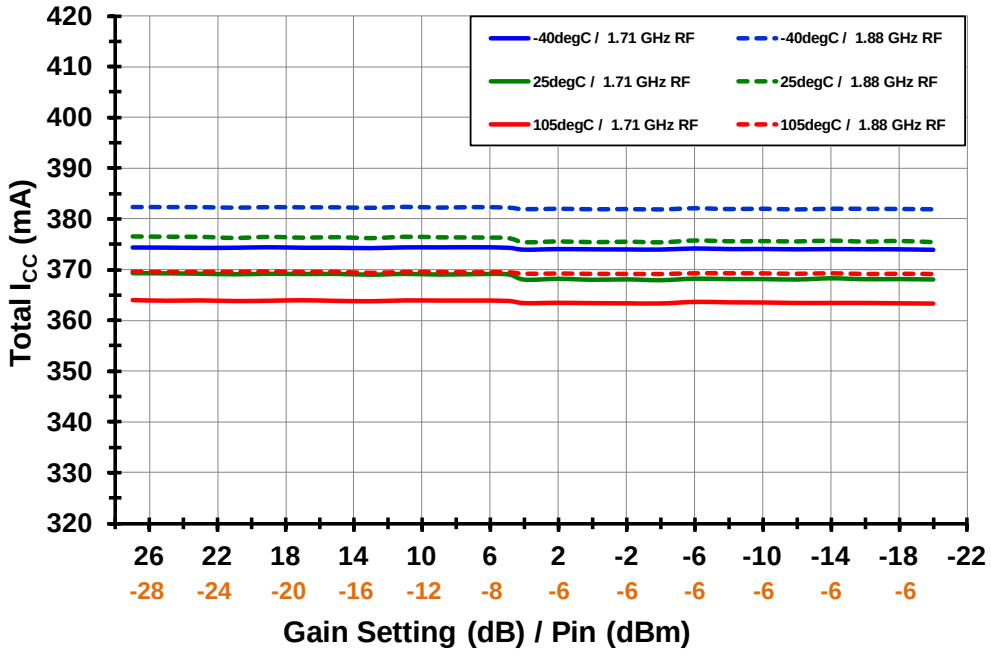
RF to IF Leakage [1.88 GHz]



TYPICAL OPERATING CONDITIONS (LC MODE, 184MHZ)

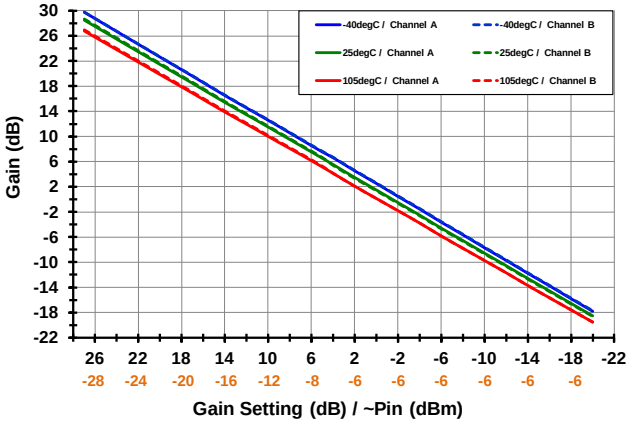
Unless otherwise noted, the following conditions apply to the 184MHz LC Mode Typ Ops Graphs:

- BOM2 Applications circuit for 100 ohm differential load with 184MHz IF Center +/- 40 MHz BW into 2:1 Transformer (see page 51)
- Pout ~ +1dBm
- P_{IN} from -29 to -6 dBm (Gain Setting Adjusted to yield Pout ~ +1dBm without exceeding -6dBm P_{IN})
- Tone Spacing = 800kHz
- Device configured in Standard Mode with Low Side Injection
- T_{CASE} = 25°C, V_{CC} = 5.00V, LO Power = 0dBm
- RF Frequency: 1.88GHz
- IF Frequency: 184MHz
- Transformer Losses are de-embedded
- Input RF trace Losses are not de-embedded

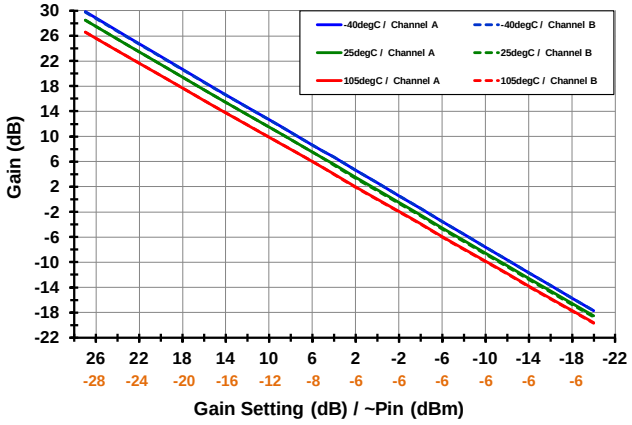


TOCs Swept Gain Setting [LC Mode, IF =184M, LS Injection] Gain, OIP3, IIP3 (-23-)

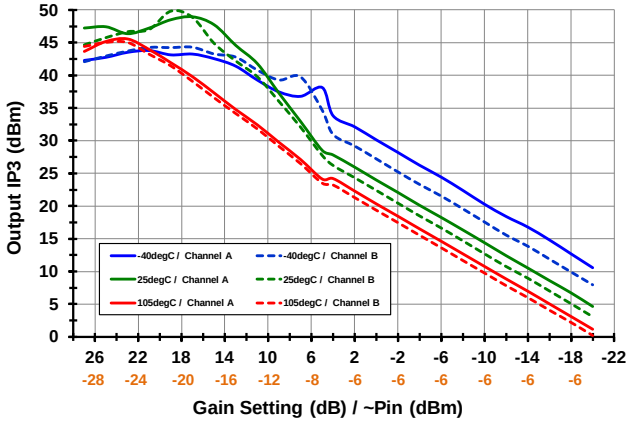
Gain [1.71 GHz]



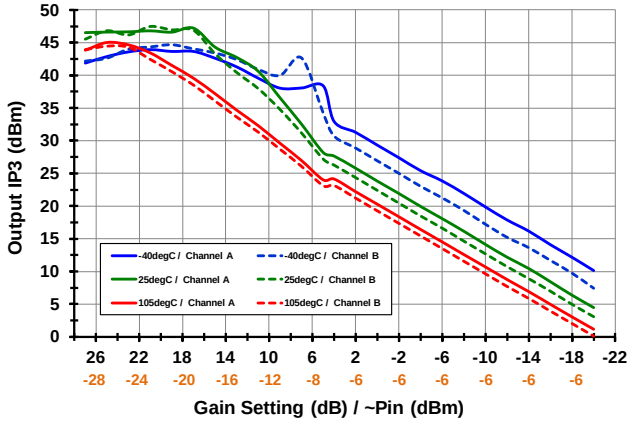
Gain [1.88 GHz]



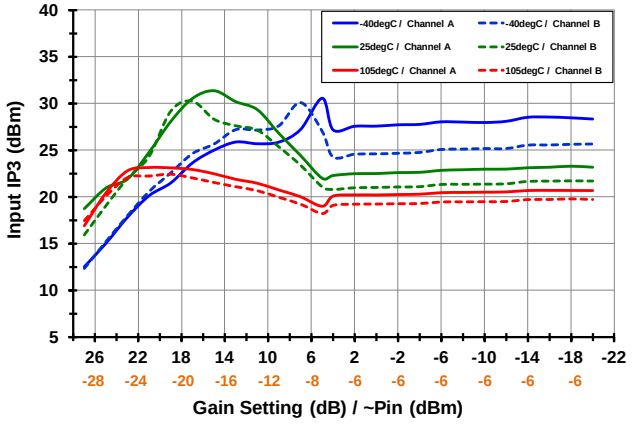
Output IP3 [1.71 GHz]



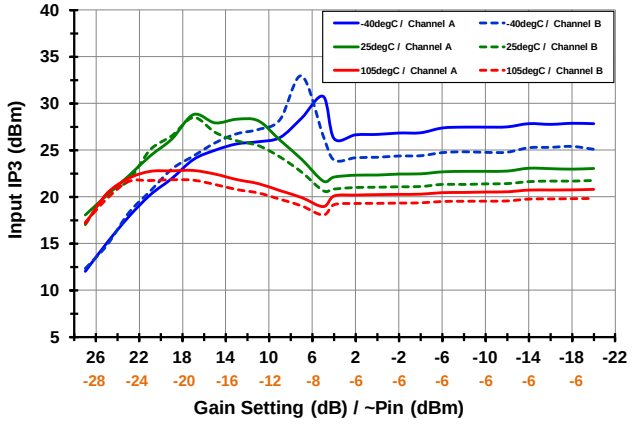
Output IP3 [1.88 GHz]



Input IP3 [1.71 GHz]

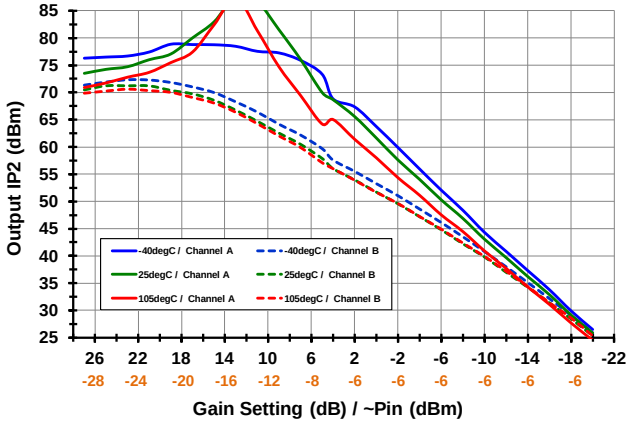


Input IP3 [1.88 GHz]

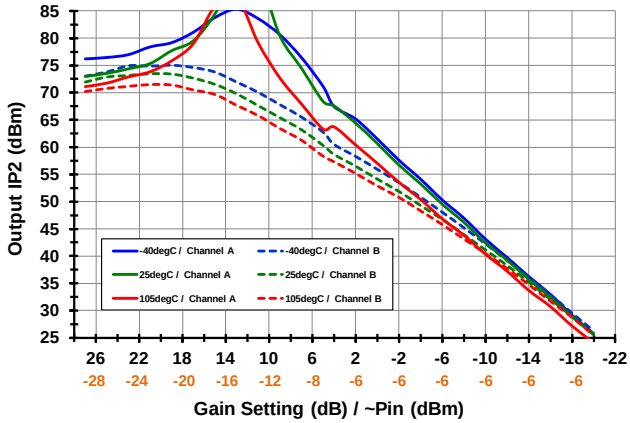


TOCs Swept Gain Setting [LC Mode, IF =184M, LS Injection] OIP2, IIP2, 2X2 (-24-)

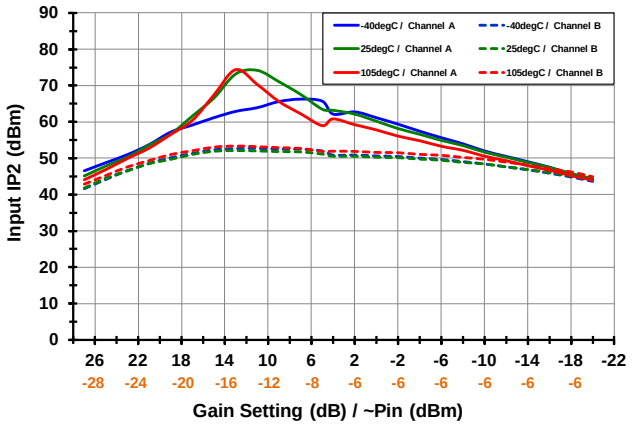
Output IP2 [1.71 GHz]



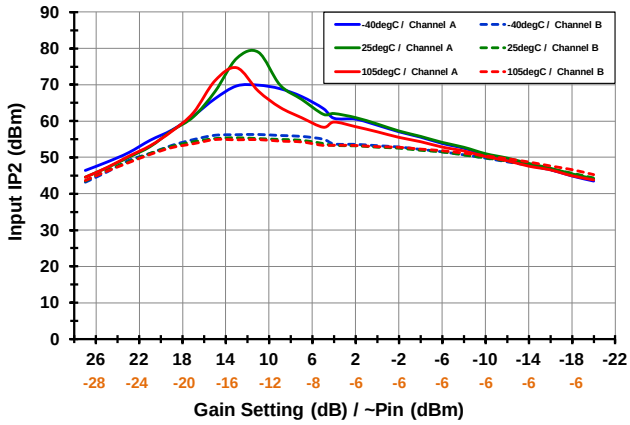
Output IP2 [1.88 GHz]



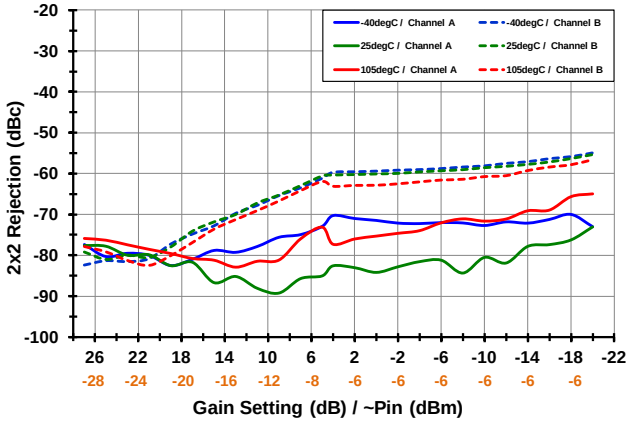
Input IP2 [1.71 GHz]



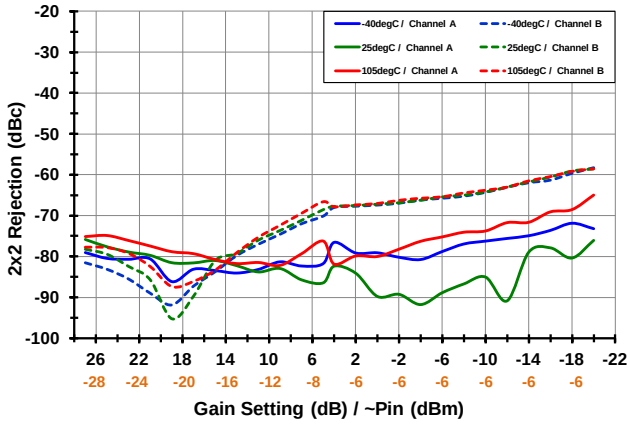
Input IP2 [1.88 GHz]



2x2 Rejection [1.71 GHz]

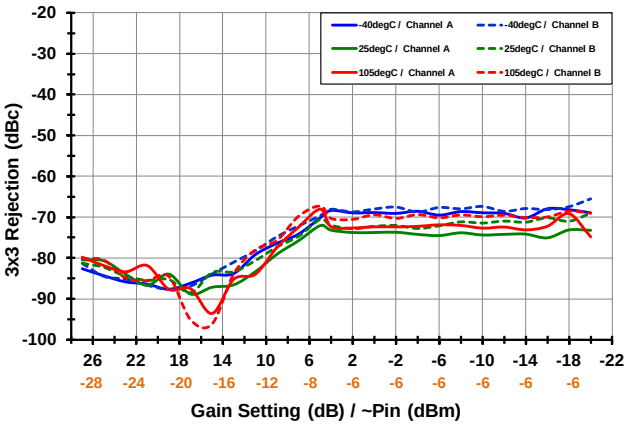


2x2 Rejection [1.88 GHz]

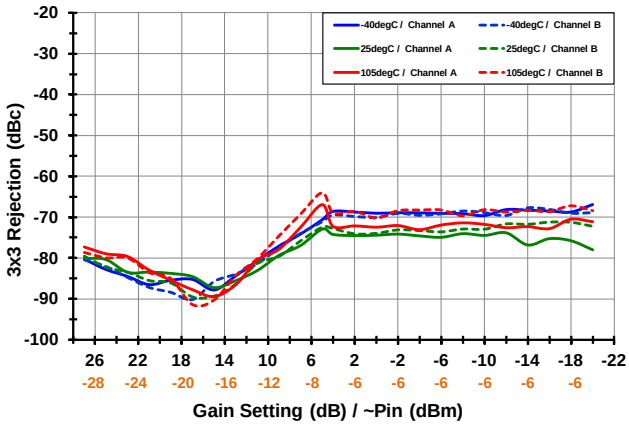


TOCs Swept Gain Setting [LC Mode, IF =184M, LS Injection] 3X3, Leakage (-25-)

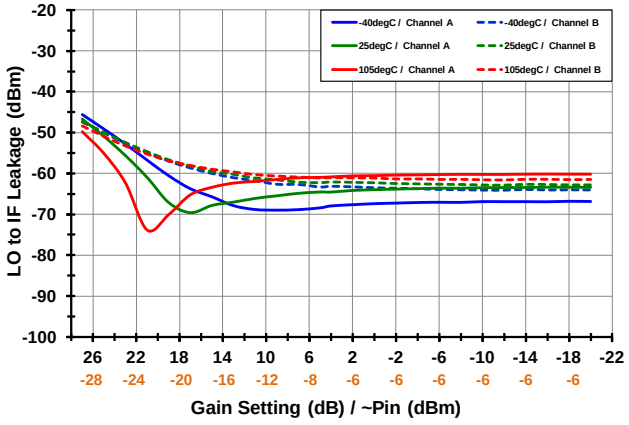
3x3 Rejection [1.71 GHz]



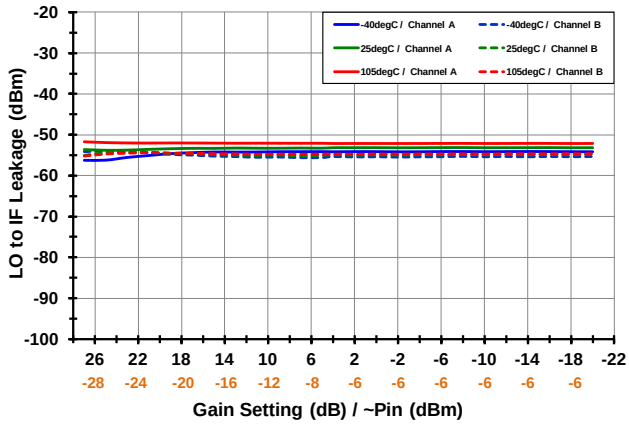
3x3 Rejection [1.88 GHz]



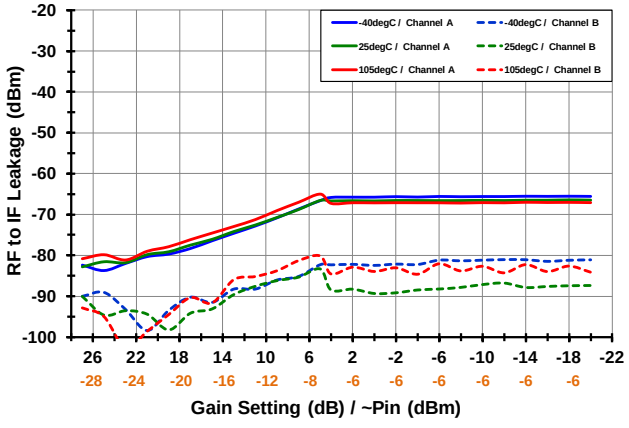
LO to IF Leakage [low side inj, 1.88 GHz]



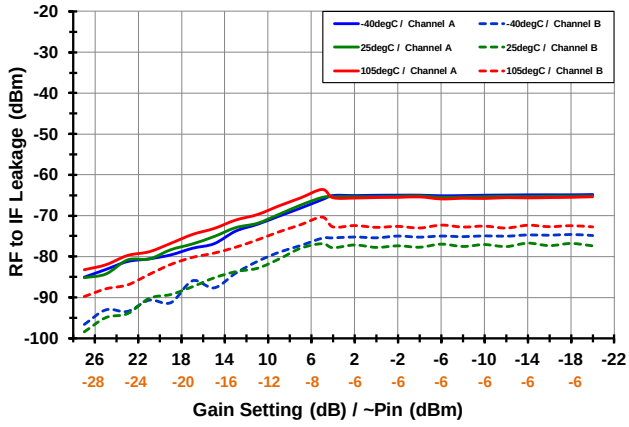
LO to IF Leakage [high side inj., 1.88 GHz]



RF to IF Leakage [1.71 GHz]

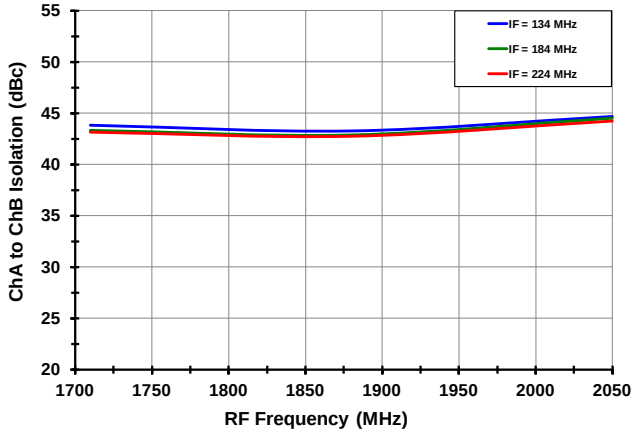


RF to IF Leakage [1.88 GHz]

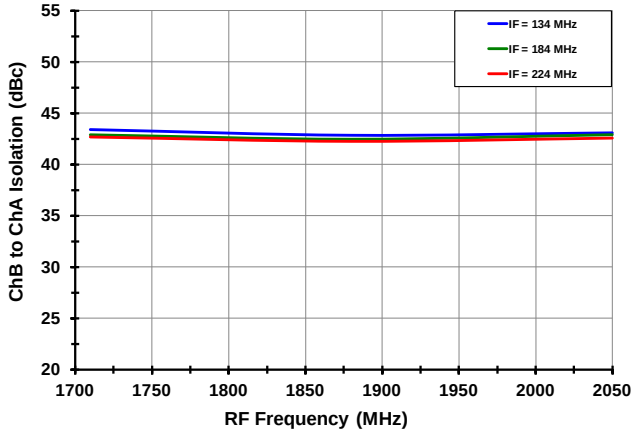


TOCs Swept Gain Setting [LC Mode, IF =184M, LS Injection] ChA Iso (-26-)

Channel Isolation [ChA to ChB]

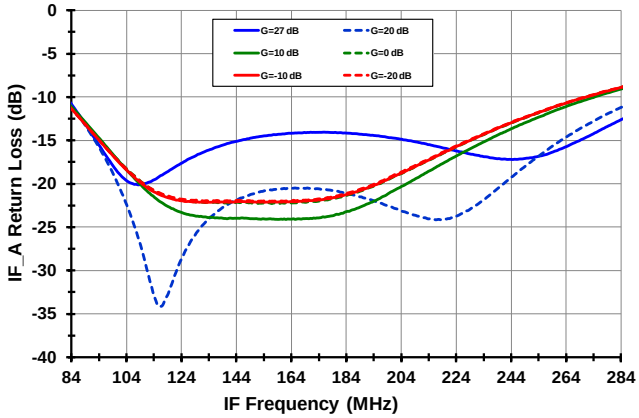


Channel Isolation [ChB to ChA]

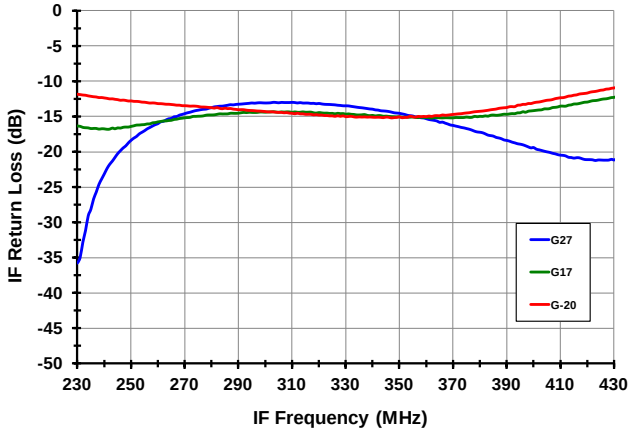


TOCs Return Loss [STD Mode] (-27-)

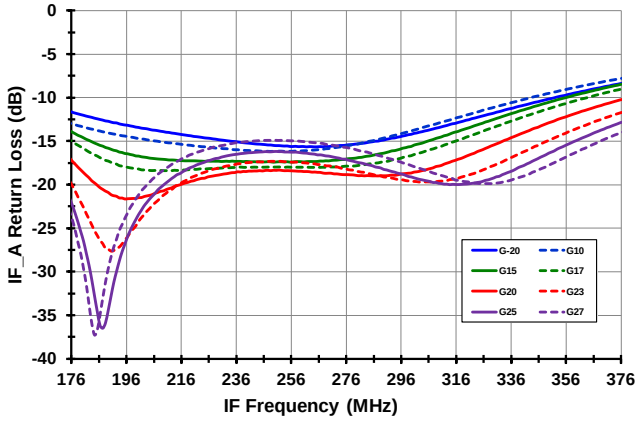
IF_A Output Return Loss 138M, 184M match



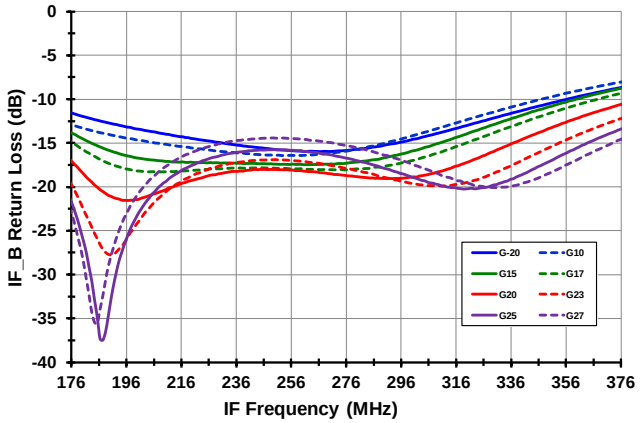
IF_A Output Return Loss 330MHz match



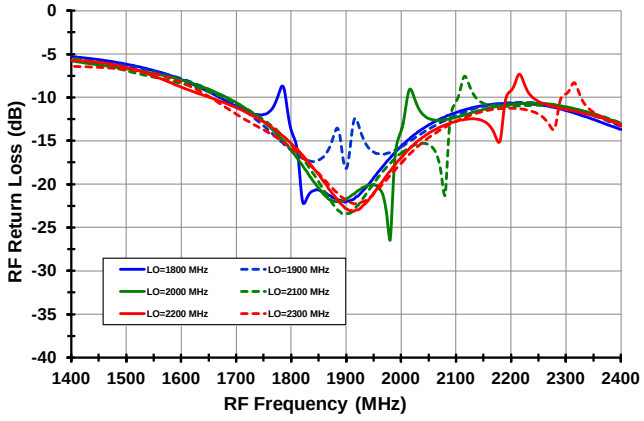
IF_A Return Loss 276MHz match



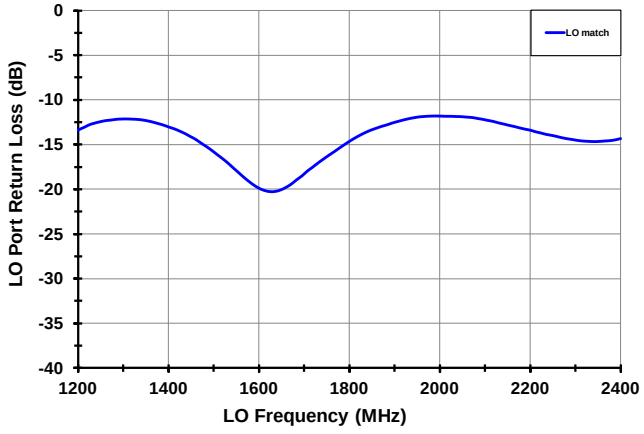
IF_B Return Loss 276MHz match



RF Input Return Loss

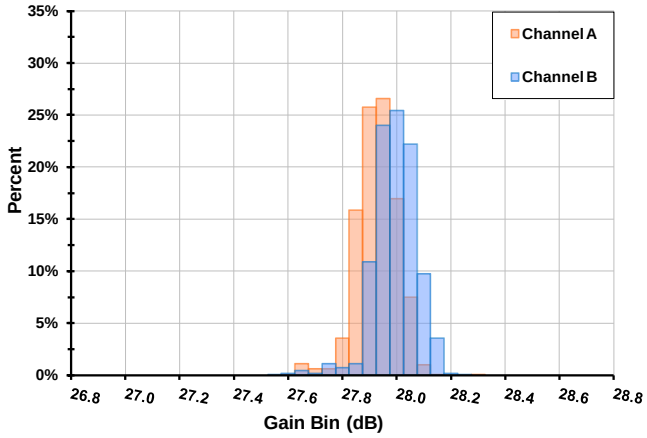


LO Input Return Loss

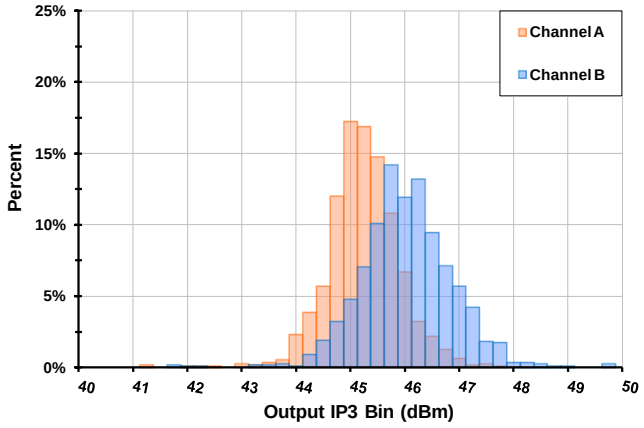


TOCs Histograms [N= 1090, T_{CASE} = 25C] (-28-)

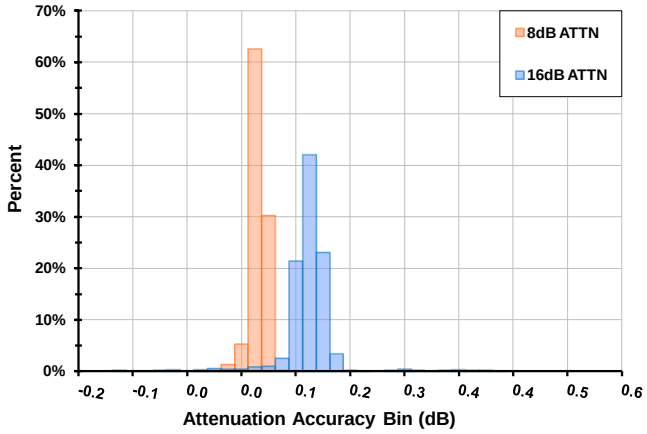
Gain [RF = 1880M, LO =1696M, G_{MAX}]



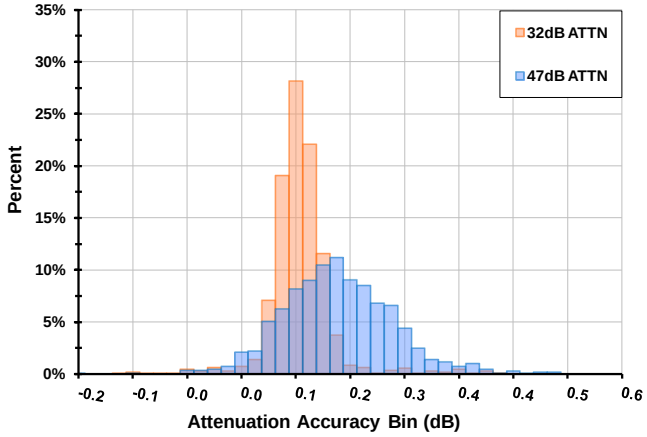
Output IP3 [RF = 1880M, LO =1696M, G_{MAX}]



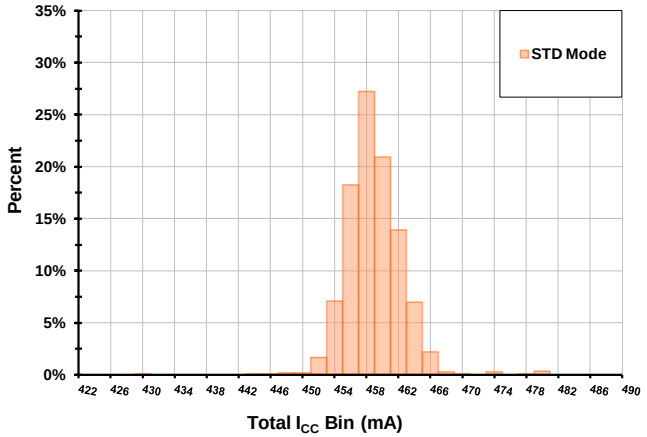
ATTN Accuracy1 [RF = 1880M, LO =1696, ChA]



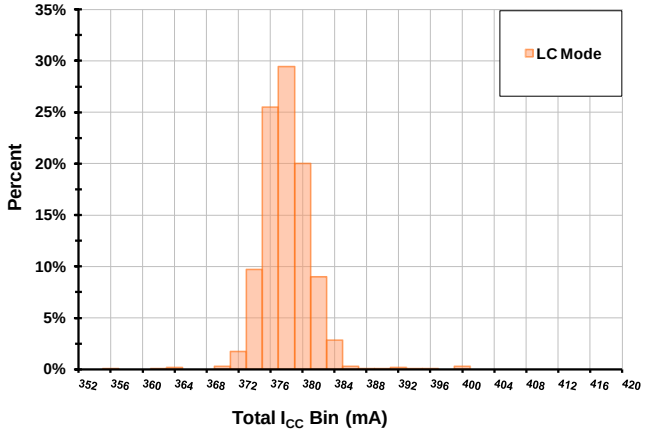
ATTN Accuracy2 [RF = 1880M, LO =1696, ChA]



I_{CC} STD Mode [LO =1696M, V_{CC} = 5.00 V]



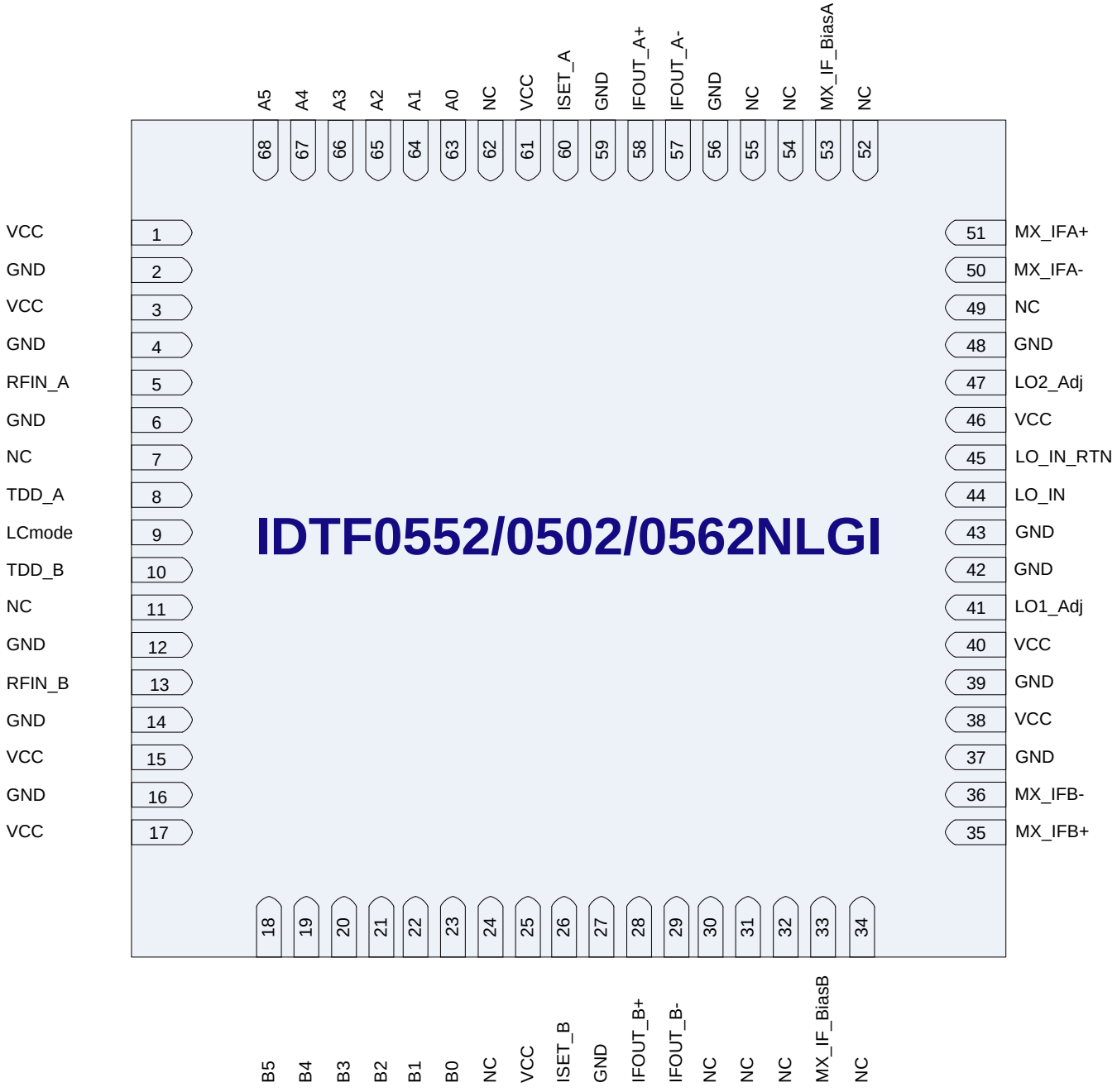
I_{CC} LC Mode [LO =1696M, V_{CC} = 5.00 V]



PACKAGE OUTLINE DRAWINGS

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

F0552 PINOUT



F0552 PIN DESCRIPTION TABLE

Pin	Name	Function
1, 3, 15, 17, 25, 38, 40, 46, 61	VCC	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
2, 4, 6, 12, 14, 16, 27, 37, 39, 42, 43, 48, 56, 59	GND	Ground these pins.
5	RFIN_A	Main Channel RF Input. Internally matched to 50Ω. DO NOT apply DC to these pins
7, 11, 24, 30, 31, 32, 34, 49, 52, 54, 55, 62	NC	No Connection. Not internally connected. OK to connect to VCC, OK to connect to GND
8	TDD_A	Standby control for Channel A. Includes an internal pull-up resistor so leave as NC for Standby mode. Set this pin to low or GND for normal operation.
9	LCmode	Low_Current Mode. Includes an internal pull-up resistor so leave as NC for LC mode. Set this pin to low or GND for STD mode.
10	TDD_B	Standby control for Channel B. Includes an internal pull-up resistor so leave as NC for Standby mode. Set this pin to low or GND for normal operation.
13	RFIN_B	Diversity Channel RF Input. Internally matched to 50Ω
18	B5	Parallel Gain Control Input – MSB. Includes an internal pull-up resistor.
19	B4	Parallel Gain Control Input. Includes an internal pull-up resistor.
20	B3	Parallel Gain Control Input. Includes an internal pull-up resistor.
21	B2	Parallel Gain Control Input. Includes an internal pull-up resistor.
22	B1	Parallel Gain Control Input. Includes an internal pull-up resistor.
23	B0	Parallel Gain Control Input – LSB (1 dB step). Includes an internal pull-up resistor.
26	ISET_B	ChB VGA Icc set: Recommended resistor value = 3.83K
28	IFOUT_B+	Channel B Differential Output +. Pull up to Vcc through an inductor
29	IFOUT_B-	Channel B Differential Output -. Pull up to Vcc through an inductor
33	MX_IF_BiasB	Connect the specified resistor for either Standard mode (41ohm) or LC mode (62ohm) from this pin to ground to set the bias for the Diversity IF amplifier. This is NOT a current set resistor.
35	MX_IFB+	Diversity Mixer Differential IF (+) Output. Connect a pullup inductor from this pin to VCC.
36	MX_IFB-	Diversity Mixer Differential IF (-) Output. Connect a pullup inductor from this pin to VCC.

F0552 PIN DESCRIPTION TABLE (CONTINUED)

41	LO1_ADJ	Connect the specified resistor for either Standard mode (220ohm) or LC mode (240ohm) from this pin to ground to set the LO common buffer Icc.
44	LO_IN	Local Oscillator Input. Connect the LO to this port through the recommended coupling capacitor.
45	LO_IN_RTN	Transformer ground return. Ground this pin.
47	LO2_ADJ	Connect the specified resistor for either Standard mode (1.3K) or LC mode (2.15K) from this pin to ground to set the LO drive buffers Icc.
50	MX_IFA-	Diversity Mixer Differential IF (-) Output. Connect a pullup inductor from this pin to VCC.
51	MX_IFA+	Diversity Mixer Differential IF (+) Output. Connect a pullup inductor from this pin to VCC.
53	MX_IF_BiasA	Connect the specified resistor for either Standard mode (41ohm) or LC mode (62ohm) from this pin to ground to set the bias for the Diversity IF amplifier. This is NOT a current set resistor.
57	IFOUT_A-	Channel A Differential Output -. Pull up to Vcc through an inductor
58	IFOUT_A+	Channel A Differential Output +. Pull up to Vcc through an inductor
60	ISET_A	ChA VGA Icc set: Recommended resistor value = 3.83K
63	A0	Parallel Gain Control Input – LSB (1dB step). Includes an internal pull-up resistor.
64	A1	Parallel Gain Control Input. Includes an internal pull-up resistor.
65	A2	Parallel Gain Control Input. Includes an internal pull-up resistor.
66	A3	Parallel Gain Control Input. Includes an internal pull-up resistor.
67	A4	Parallel Gain Control Input. Includes an internal pull-up resistor.
68	A5	Parallel Gain Control Input – MSB. Includes an internal pull-up resistor.
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance.

F0552 Digital Pin Voltage and Resistance Values

The following table provides open-circuit DC voltage and resistance values referenced to ground for each of the control pins listed.

Pin	Name	DC Voltage (volts)	Pull-up Resistance (ohms)
8	TDD_A	5	50k
9	LC_MODE	5	50k
10	TDD_B	5	50k
18 – 23	B0-B5	5	50k
63 - 68	A0-A5	5	50k

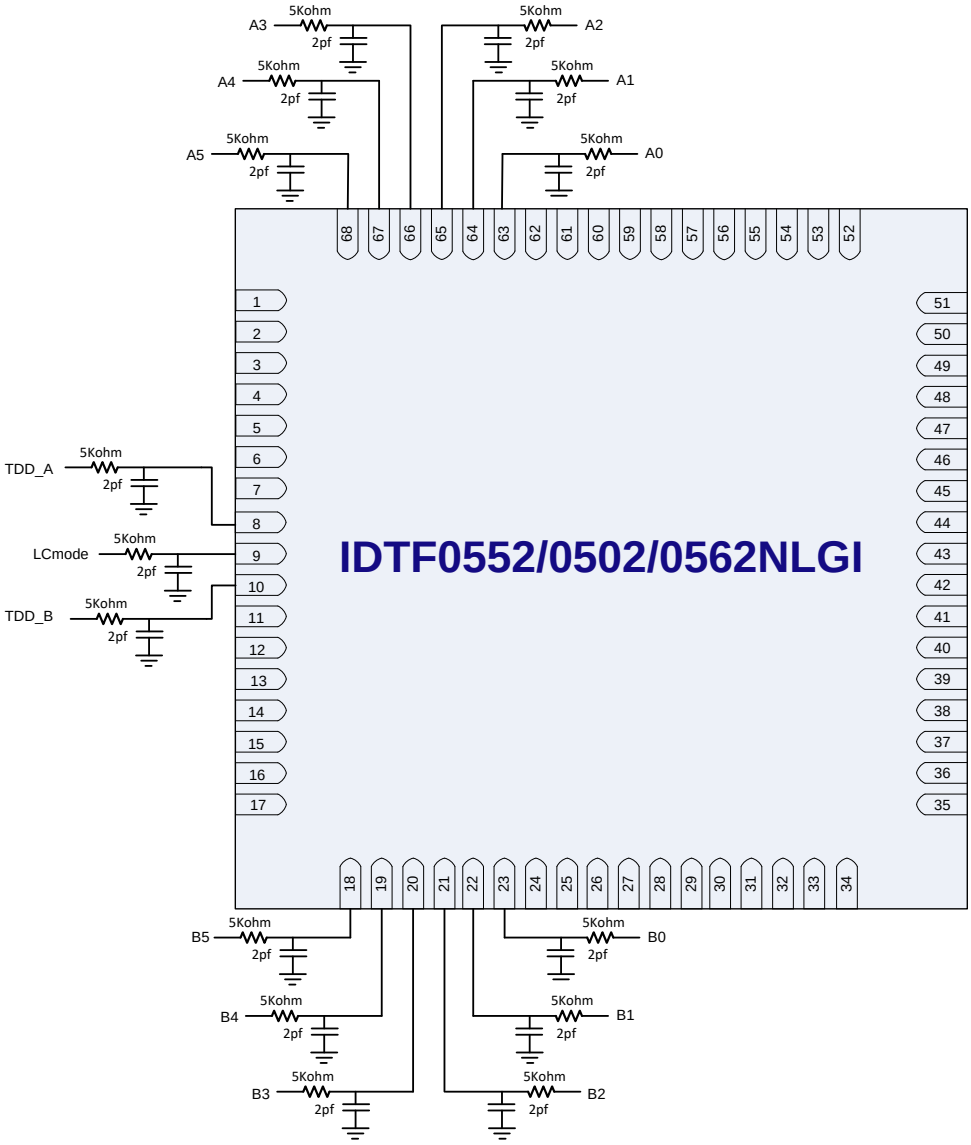
APPLICATIONS INFORMATION

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µs. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

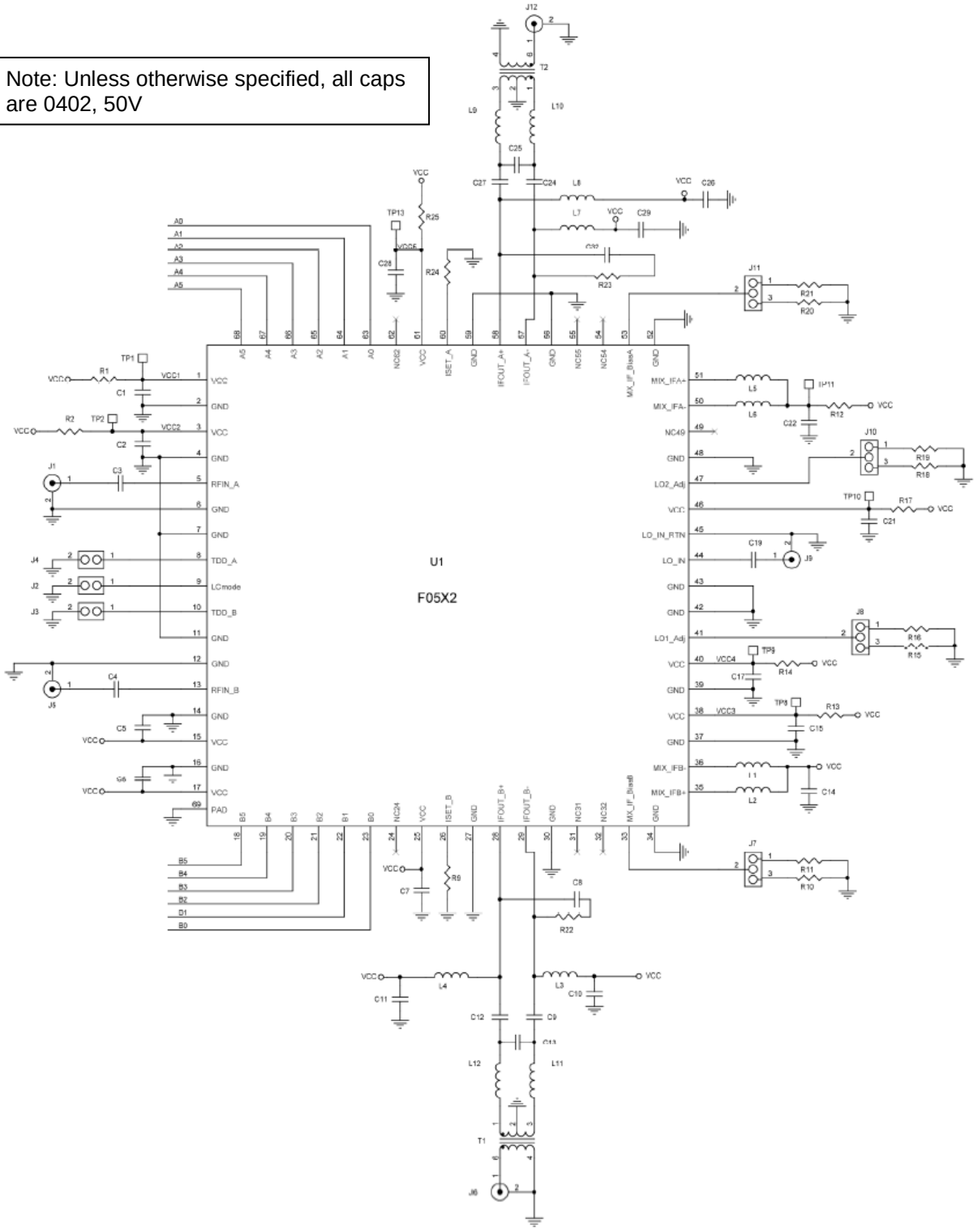
If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., provisions for an R-C circuit at the input of each control and data pin is recommended. This applies to pins 8, 9, 10, 18 - 23, and 63 - 68 as shown below.



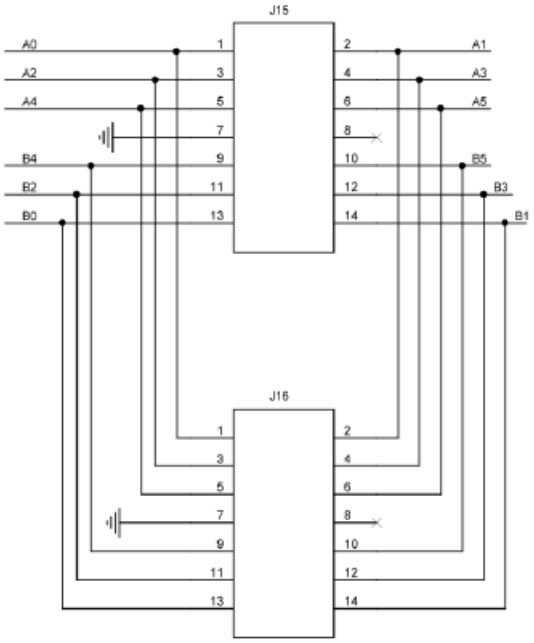
EVKIT AND TYPICAL APPLICATION SCHEMATIC

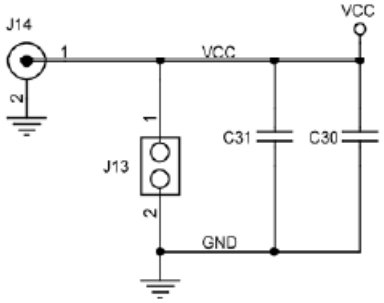
The following schematic describes the recommended EVkit and applications circuit.

Note: Unless otherwise specified, all caps are 0402, 50V

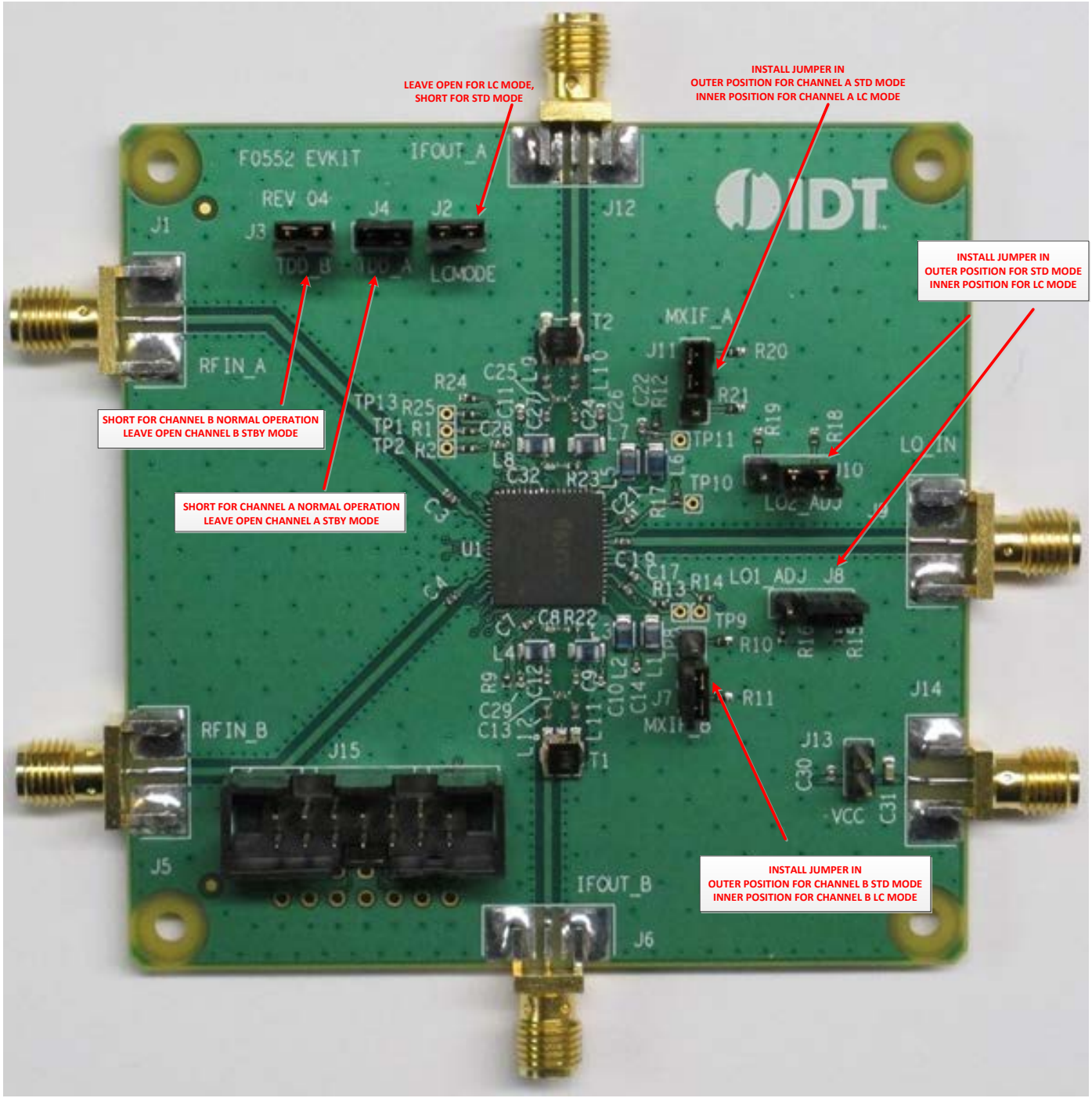


SCHEMATIC CONTINUED FROM PREVIOUS PAGE





EVKIT PICTURE



F0552 BOM 1 AND 2

Two EV Kit BOMs are included: BOM1 supports the 4:1 output transformation from 200 ohms to 50 ohms used for production test and BOM2 supports the 2:1 output transformation from 200 ohms to 100 ohms used to generate the typical operating curve graphs.

BOM1 includes components for 4:1 output transformation supporting production test (IF center frequency 184MHz)

F0552 BOM For 4:1 IF=184Mhz for Correlation

5/24/2013

Item #	Value	Size	Desc	Mfr. Part #	Mfr.	Supplier Part #	Supplier	Part Reference	Qty
1	18pF	0402	CAP CER 18pF 50V 5% C0G 0402	GRM1555C1H180JZ01[	MURATA	490-1281-1-ND	Digikey	C3,4	2
2	39pF	0402	CAP CER 39pF 50V 5% C0G 0402	GRM1555C1H390JZ01[	MURATA	490-1286-1-ND	Digikey	C19	1
3	1000pF	0402	CAP CER 1000PF 50V C0G 0402	GRM1555C1H102JA01[	MURATA	490-3244-1-ND	Digikey	C9,12,24,27	4
4	10nF	0402	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01[	MURATA	490-1313-1-ND	Digikey	C1,2,5,6,7,10,11,14,15, 17,21,22,26,28,29,30	16
5	10uF	0603	CAP CER 10UF 6.3V X5R 0603	GRM188R60J106ME47[	MURATA	490-3896-1-ND	Digikey	C31	1
6	220	0402	RES 220 OHM 1/10W 1% 0402 SMD	ERJ-2RKF2200X	Panasonic	P220LCT-ND	Digikey	R15	1
7	240	0402	RES 240 OHM 1/10W 1% 0402 SMD	ERJ-2RKF2400X	Panasonic	P240LCT-ND	Digikey	R16	1
8	1.3K	0402	RES 1.30K OHM 1/10W 1% 0402 SMD	ERJ-2RKF1301X	Panasonic	P1.30KLCT-ND	Digikey	R18	1
9	2.15k	0402	RES 2.15K OHM 1/10W 1% 0402 SMD	ERJ-2RKF2151X	Panasonic	P2.15KLCT-ND	Digikey	R19	1
10	62	0402	RES 62.0 OHM 1/10W 1% 0402 SMD	ERJ-2RKF62R0X	Panasonic	P62.0LCT-ND	Digikey	R10,21	2
11	3.83K	0402	RES 3.83K OHM 1/10W 1% 0402 SMD	ERJ-2RKF3831X	Panasonic	P3.83KLCT-ND	Digikey	R9,24	2
12	40.2	0402	RES 40.2 OHM 1/10W 1% 0402 SMD	ERJ-2RKF40R2X	Panasonic	P40.2LCT-ND	Digikey	R11,20	2
13	0	0402	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic	P0.0JCT-ND	Digikey	R1,2,12,13,14,17,25, L9	11
14	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (small)	142-0711-821	Emerson Johnson	530-142-0711-82[	Mouser	J6,12,14	3
15	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Big)	142-0701-851	Emerson Johnson	530-142-0701-85[	Mouser	J1,5,9	3
16	Header 14 Pin	TH 14	CONN HEADER VERT SGL 14POS GOLD	N2514-6002-RB	3M	MHC14K-ND	Digikey	J15	1
17	Header 2 Pin	TH 2	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M	3M9447-ND	Digikey	J2,3,4,13	4
18	Header 3 Pin	TH 3	CONN HEADER VERT SGL 3POS GOLD	961103-6404-AR	3M	3M9448-ND	Digikey	J7,8,10,11	4
19	1:4 Balun	SM-22	4:1 Center Tap Balun	TC4-1WG2+	Mini Circuits	TC4-1WG2+	Mini Circuits	T1,2	2
20	390 nH	0805	0805CS (2012) Ceramic Chip Inductor	0805CS-391XJLB	COILCRAFT	0805CS-391XJLB	COILCRAFT	L1-8	8
21	F0552 / Socket	TQFN-68	Sampling IF receiver / Socket	F0552	IDT	F0552	IDT	U1	1
22	Not populated							C13,25	
23	PCB	Rev 02	PCB Rev 02	F0552 EV Kit Rev 02			SBC		1
24	BOM	Rev 04	F0552 BOM Rev 04						
								Total	72

BOM2 includes components for 2:1 output transformation used for TOCs (IF center frequency 184MHz +/ - 40MHz)

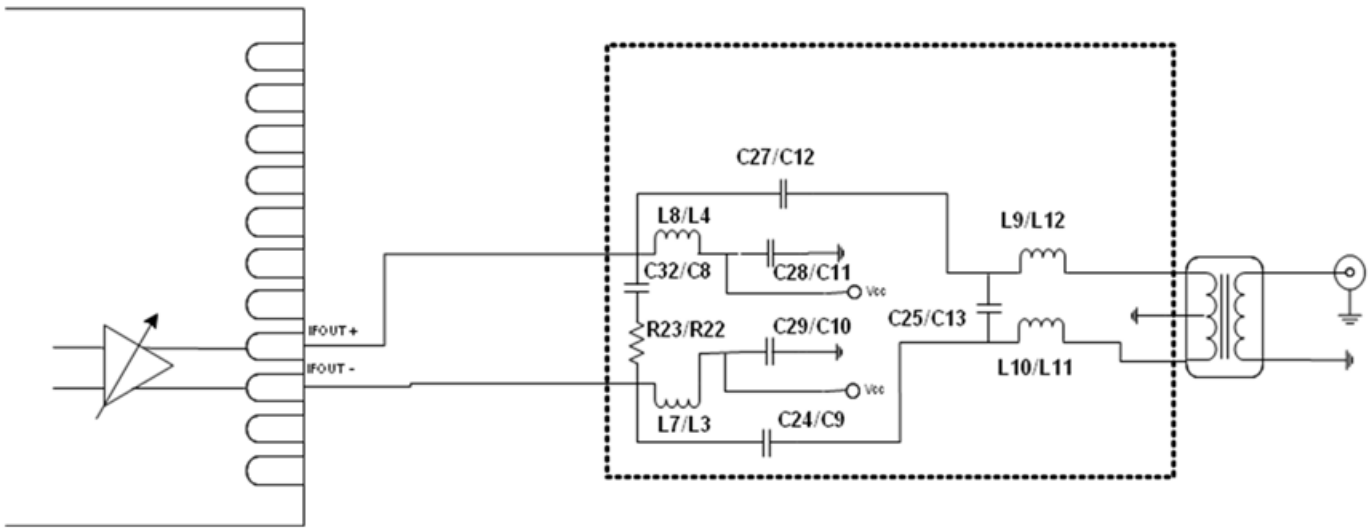
F0552 BOM For 2:1 IF=184Mhz

6/10/2013

Item #	Value	Size	Desc	Mfr. Part #	Mfr.	Supplier Part #	Supplier	Part Reference	Qty
1	18pF	0402	CAP CER 18pF 50V 5% C0G 0402	GRM1555C1H180JZ01[	MURATA	490-1281-1-ND	Digikey	C3,4	2
2	39pF	0402	CAP CER 39pF 50V 5% C0G 0402	GRM1555C1H390JZ01[	MURATA	490-1286-1-ND	Digikey	C19	1
3	20pF	0402	CAP CER 20pF 50V C0G 0402	GRM1555C1H200JZ01[	MURATA	490-1282-1-ND	Digikey	C9,12,24,27	4
4	3pF	0402	CAP CER 3pF 50V C0G 0402	GRM1555C1H3R0CZ01[	MURATA	490-3205-1-ND	Digikey	C13,25	2
5	10nF	0402	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01[	MURATA	490-1313-1-ND	Digikey	C1,2,5,6,7,10,11,14 ,15,	16
6	10uF	0603	CAP CER 10UF 6.3V X5R 0603	GRM188R60J106ME47[	MURATA	490-3896-1-ND	Digikey	C31	1
7	220	0402	RES 220 OHM 1/10W 1% 0402 SMD	ERJ-2RKF2200X	Panasonic	P220LCT-ND	Digikey	R15	1
8	240	0402	RES 240 OHM 1/10W 1% 0402 SMD	ERJ-2RKF2400X	Panasonic	P240LCT-ND	Digikey	R16	1
9	1.3K	0402	RES 1.30K OHM 1/10W 1% 0402 SMD	ERJ-2RKF1301X	Panasonic	P1.30KLCT-ND	Digikey	R18	1
10	2.15k	0402	RES 2.15K OHM 1/10W 1% 0402 SMD	ERJ-2RKF2151X	Panasonic	P2.15KLCT-ND	Digikey	R19	1
11	62	0402	RES 62.0 OHM 1/10W 1% 0402 SMD	ERJ-2RKF62R0X	Panasonic	P62.0LCT-ND	Digikey	R10,21	2
12	3.83K	0402	RES 3.83K OHM 1/10W 1% 0402 SMD	ERJ-2RKF3831X	Panasonic	P3.83KLCT-ND	Digikey	R9,24	2
13	40.2	0402	RES 40.2 OHM 1/10W 1% 0402 SMD	ERJ-2RKF40R2X	Panasonic	P40.2LCT-ND	Digikey	R11,20	2
14	0	0402	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic	P0.0JCT-ND	Digikey	R1,2,12,13,14,17,25	7
15	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (small)	142-0711-821	Emerson Johnson	530-142-0711-821	Mouser	J6,12,14	3
16	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Big)	142-0701-851	Emerson Johnson	530-142-0701-851	Mouser	J1,5,9	3
17	Header 14 Pin	TH 14	CONN HEADER VERT SGL 14POS GOLD	N2514-6002-RB	3M	MHC14K-ND	Digikey	J15	1
18	Header 2 Pin	TH 2	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M	3M9447-ND	Digikey	J2,3,4,13	4
19	Header 3 Pin	TH 3	CONN HEADER VERT SGL 3POS GOLD	961103-6404-AR	3M	3M9448-ND	Digikey	J7,8,10,11	4
20	2:1 Balun	SM-22	2:1 Center Tap Balun	TC2-72T+	Mini Circuits	TC2-72T+	Mini Circuits	T1,2	2
21	390 nH	0805	0805CS (2012) Ceramic Chip Inductor	0805CS-391XJLB	COILCRAFT	0805CS-391XJLB	COILCRAFT	L1,2,5,6	4
22	150nH	0805	0805CS (2012) Ceramic Chip Inductor	0805CS-151XJLB	COILCRAFT	0805CS-151XJLB	COILCRAFT	L3,4,7,8	4
23	30nH	0402	0402CS Ceramic Chip Inductor	0402CS-30NXJLU	COILCRAFT	0402CS-30NXJLU	COILCRAFT	L9-12	4
24	F0552	TQFN-68	Sampling IF receiver	F0552	IDT	F0552	IDT	U1	1
25	PCB	Rev 02	PCB Rev 02	F0552 EV Kit Rev 02			SBC		1
26	BOM	Rev 04	F0552 BOM Rev 04						
								Total	74

For the complete list of matching values for IF frequencies other than 184MHz, see the following table.

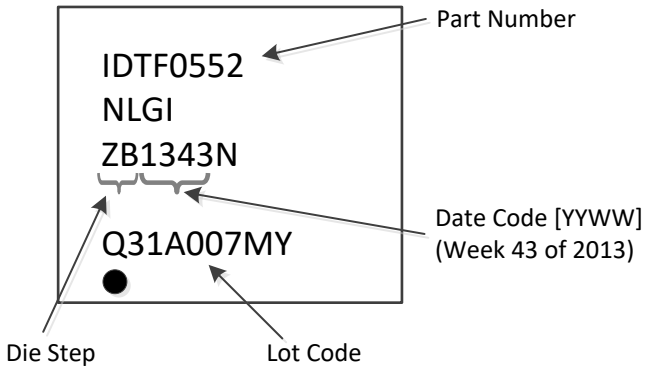
IF BIAS AND OUTPUT MATCHING CIRCUIT AND BOM FOR VARIOUS IFS



IF NETWORK BOM FOR DIFFERENT FREQUENCIES

Item #	Part Reference	Value				Unit
		IF frequency				
		80 (60-100)	138, 184 (98-240)	276 (190-316)	330 (250-410)	MHz
1	C9,12,24,27	75	20	8	6	pF
2	C13,25	11	3	1.2	0.7	pF
3	C8,C32	0.6	0.6	0.6	0.6	pF
4	R23, R22	100	100	100	100	ohm
5	L3,4,7,8	220	150	82	56	nH
6	L9-12	36	30	24	18	nH

TOP MARKINGS



ORDERING INFORMATION

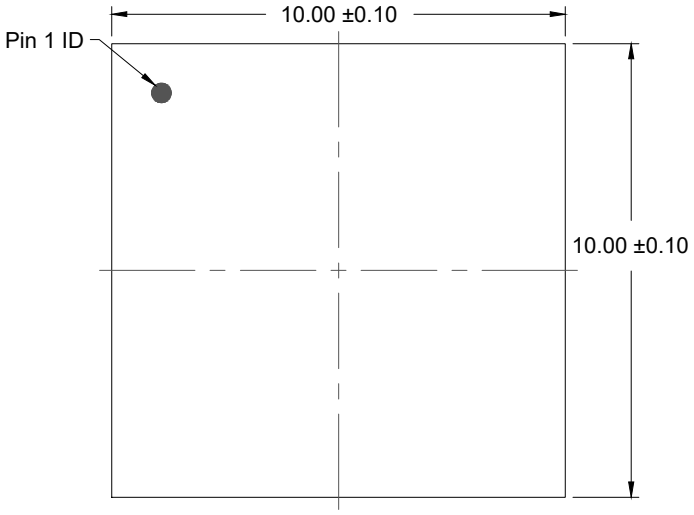
Part Number	Package Description	Carrier Type	Temperature Range
F0552NLGI	68-VFQFPN, 10 × 10 mm	Tape and Reel	-40°C to +85°C
F0552NLGI8		Tray	

REVISION HISTORY

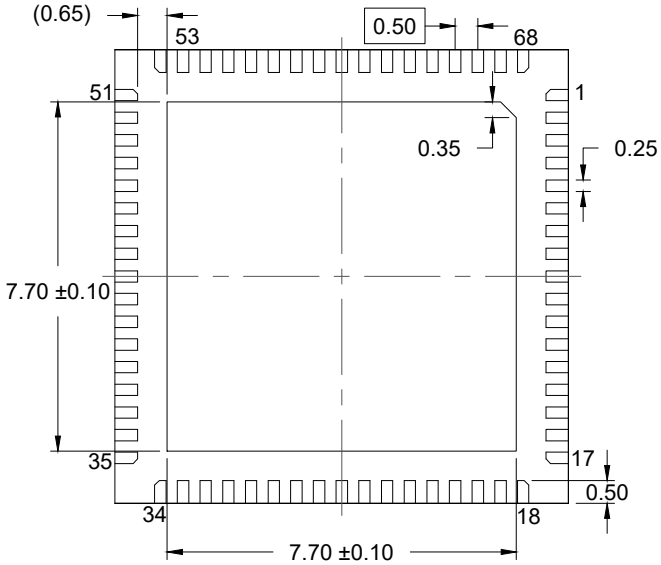
Revision Date	Description
February 9, 2022	Rebranded to Renesas.
January 27, 2014	Initial release.

Package Outline Drawing

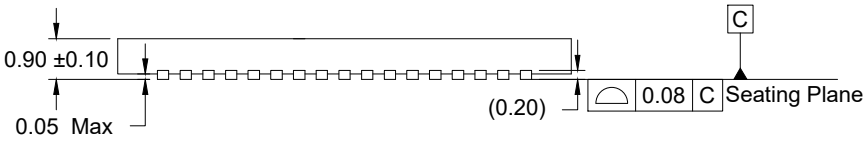
Package Code: NLG68P1
68-VFQFPN 10.0 x 10.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4111-01, Revision: 02, Date Created: Mar 28, 2024



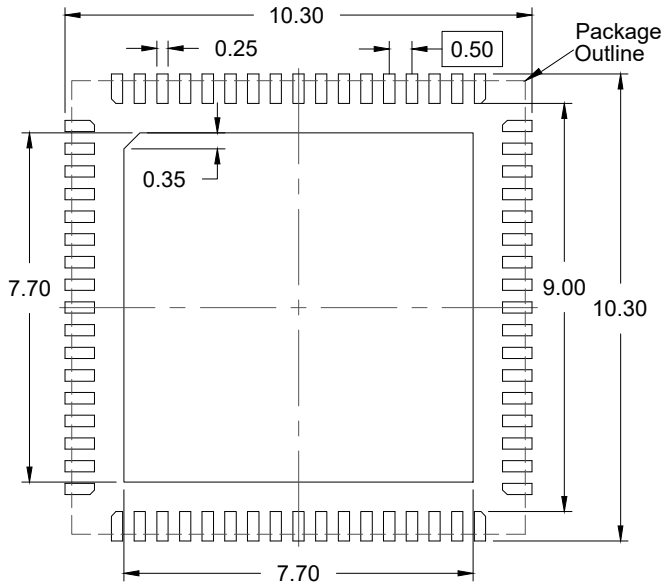
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.