



EVL28167-A-Q-00A

3A, 22V, Synchronous Buck-Boost Converter with I²C Interface for Power Delivery Evaluation Board

DESCRIPTION

The EVL28167-A-Q-00A is an evaluation board for the MP28167-A, a high-efficiency, synchronous buck-boost converter with four integrated power switches and an I²C interface. The device can regulate output voltages across a wide input voltage supply range (2.8V to 22V).

The MP28167-A's integrated output voltage scaling and configurable output current limit functions are ideal for USB power delivery (PD) applications.

In buck mode, the MP28167-A uses constant-on-time (COT) control. In boost mode, it uses constant-off-time control. This provides fast load transient response and a smooth buck-boost mode transient. The MP28167-A features automatic pulse-frequency modulation (PFM) and pulse-width modulation (PWM) modes, forced PWM mode, as well as configurable constant current (CC) limiting and soft start (SS). These features provide flexible design options for different applications.

The MP28167-A's fault protections include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), short-circuit protection (SCP), and thermal shutdown (TSD).

The MP28167-A requires a minimal number of readily available, standard external components, and is available in a QFN-16 (3mmx3mm) package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Operating input voltage	V _{IN}	12	V
Switching frequency	f _{SW}	500	kHz
Output voltage	V _{OUT}	5	V
Output current	I _{OUT}	3	A

FEATURES

- Configurable Output Voltage via the FB Pin
- Wide 2.8V to 22V Operating Input Range
- 0.08V to 1.637V Reference Voltage (V_{REF}) Range with 0.8mV Resolution via the I²C (Default V_{REF} is 1V)
- 3A Output Current or 4A Input Current
- Four Internal, Low R_{DS(ON)} Power MOSFETs
- Accurate Constant Current (CC) Output Current Limit with Internal Sensing
- 500kHz/750kHz Configurable Switching Frequency
- Line Drop Compensation
- Over-Voltage Protection (OVP) with Hiccup Mode
- Short-Circuit Protection (SCP) with Hiccup Mode
- Over-Temperature Protection
- I²C Interface and One-Time Programmable (OTP) Non-Volatile Memory:
 - Pulse-Frequency Modulation (PFM)
 - Pulse-Width Modulation (PWM) Modes, Line Drop Compensation, Soft Start, OCP, OVP, etc.
- Configurable EN Shutdown Discharge
- Available in a QFN-16 (3mmx3mm) Package

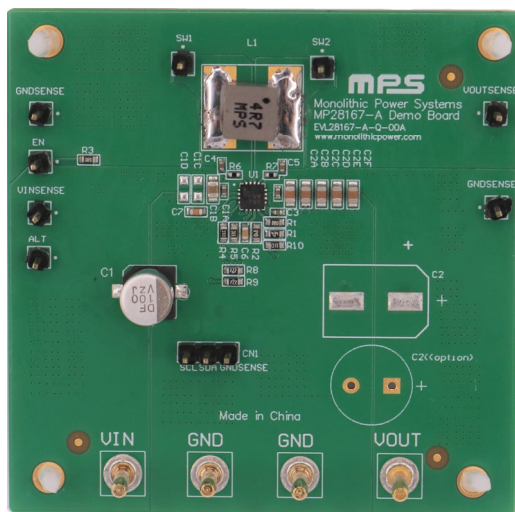
 Optimized Performance with MPS Inductor MPL-AL6050 Series

APPLICATIONS

- USB Power Delivery (PD) for Sourcing Ports
- Buck-Boost Bus Voltage (V_{BUS}) Supplies

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

EVL28167-A-Q-00A EVALUATION BOARD

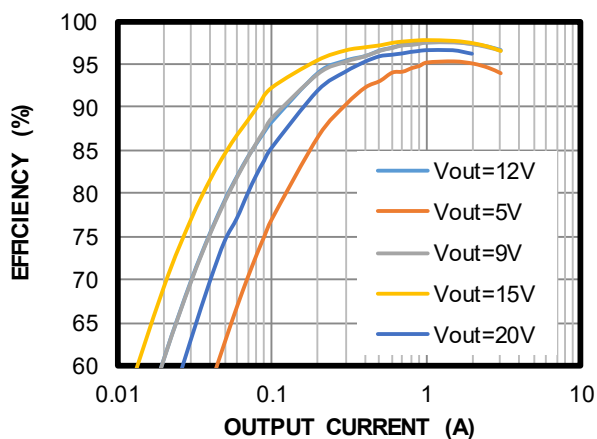


LxW (6.35cmx6.35cm)

Board Number	MPS IC Number	MPS Inductor
EVL28167-A-Q-00A	MP28167GQ-A	MPL-AL6050-4R7

Efficiency vs. Output Current

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 500kHz$,
 $L = 4.7\mu H$, $RDC = 16.5m\Omega$



QUICK START GUIDE

1. Connect the load terminals to:
 - a. Positive (+): VOUT
 - b. Negative (-): GND
2. Preset the power supply output to 12V.
3. Turn off the power supply.
4. Connect the power supply terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND
5. After making the connections, turn on the power supply. The board automatically should start up with its default settings. The related parameters can be changed by the I²C. ⁽¹⁾

Note:

- 1) Refer to the MP28167-A datasheet for how to change the parameters via the I²C.

EVALUATION BOARD SCHEMATIC

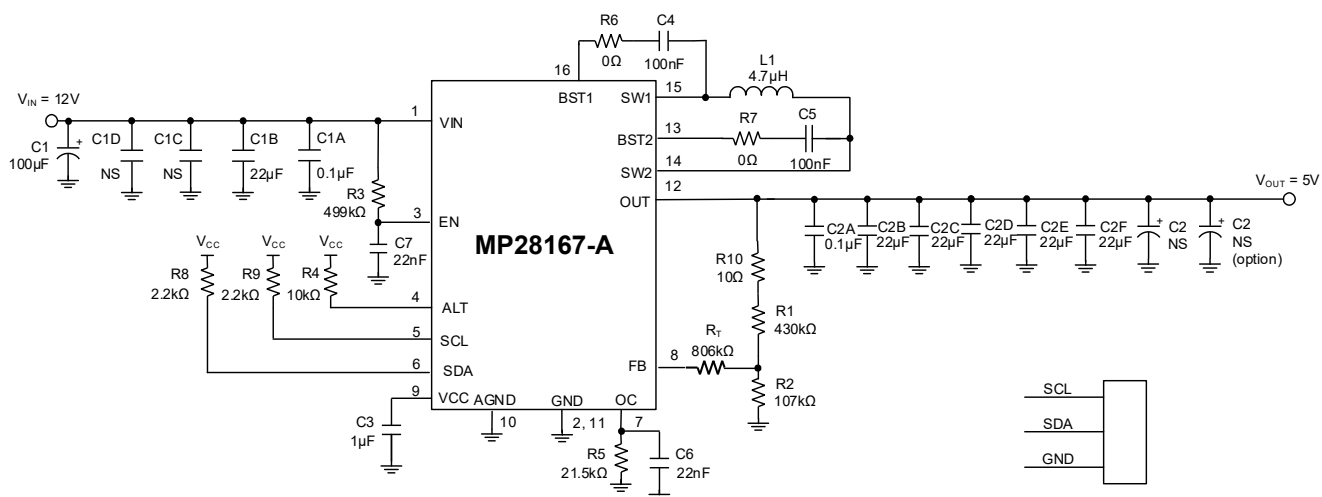


Figure 1: Evaluation Board Schematic

EVL28167-A-Q-00A BILL OF MATERIALS

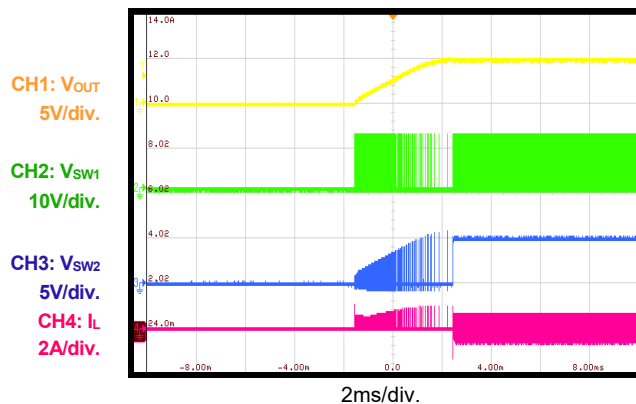
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	U1	MP28167-A	Synchronous buck-boost converter	QFN-16 (3mmx3mm)	MPS	MP28167GQ-A
1	L1	4.7 μ H	Inductor, RDC = 16.5m Ω , I _{SAT} = 11A	SMD	MPS	MPL-AL6050-4R7
1	C1	100 μ F	Electrolytic capacitor, 35V	SMD	Chemicon	EMZJ350ADA101MF80G
6	C1B, C2B, C2C, C2D, C2E, C2F	22 μ F	Ceramic capacitor 25V, X5R	0805	TDK	C2012X5R1E226M
1	C3	1 μ F	Ceramic capacitor, 16V, X6S	0402	Murata	GRM155C81C105KE11D
4	C1A, C2A, C4, C5	100nF	Ceramic capacitor, 50V, X7R	0402	Samsung	CL05B104KB5NNNC
2	C6, C7	22nF	Ceramic capacitor, 50V, X5R	0603	Murata	GRM188R71H223KA01D
0	C1C, C1D, C2, C2 (option)	NS	NA	NA	NA	NA
1	R1	430k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07430KL
1	R2	107k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07107KL
1	R3	499k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07499KL
1	R4	10k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R5	21.5k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0721K5RL
2	R6, R7	0 Ω	Film resistor, 1%	0402	Yageo	RC0402FR-070RL
2	R8, R9	2.2k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-072K2L
1	R10	10 Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0710RL
1	R _T	806k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07806KL
1	CN1	2.54mm	Test pin	DIP	Würth	61300311121

EVB TEST RESULTS

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 4.7\mu H$, $f_{SW} = 500kHz$, $T_A = 25^\circ C$, unless otherwise noted.

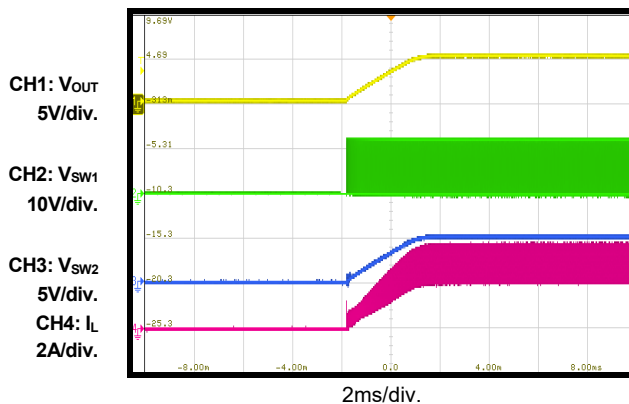
Start-Up through EN via I²C Command

Load = 0A



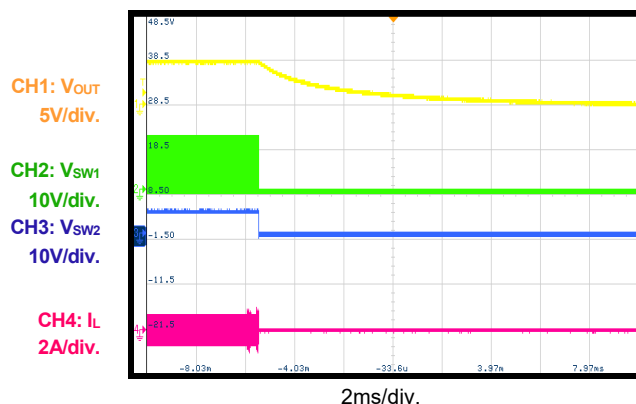
Start-Up through EN via I²C Command

Load = 3A



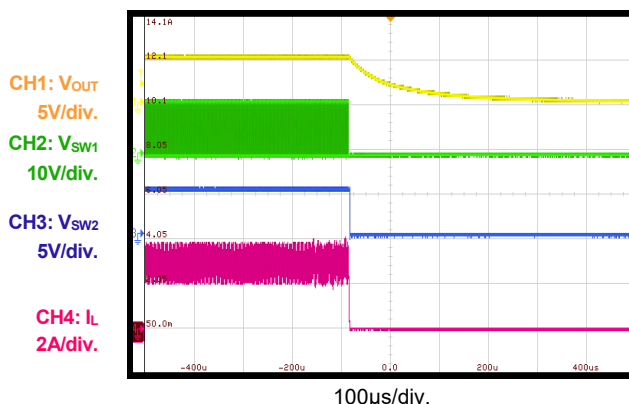
Shutdown through EN via I²C Command

Load = 0A



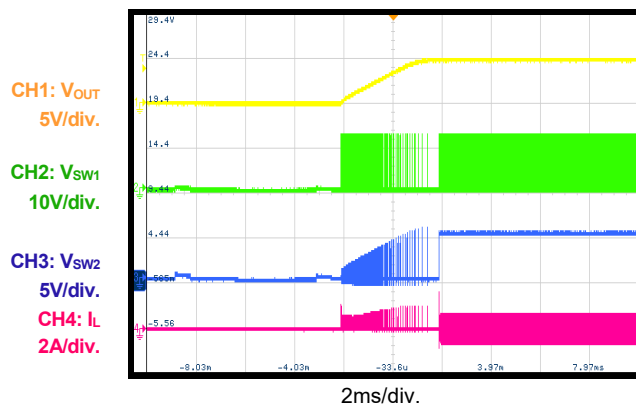
Shutdown through EN via I²C Command

Load = 3A



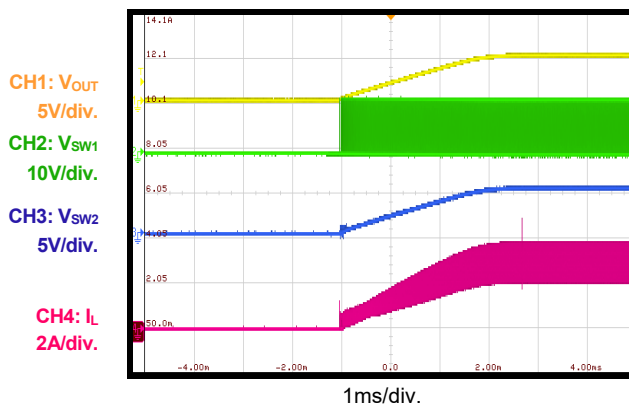
Start-Up through EN

Load = 0A



Start-Up through EN

Load = 3A

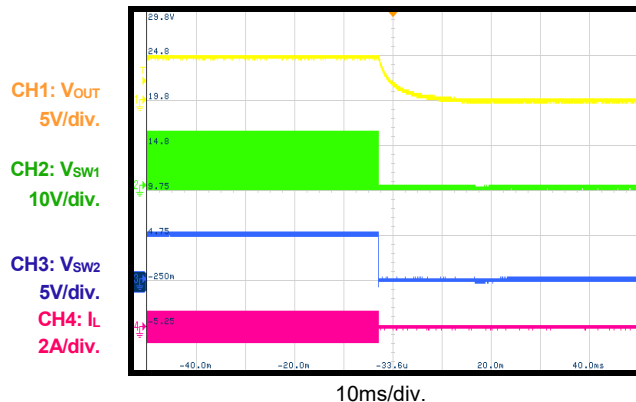


EVB TEST RESULTS *(continued)*

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 4.7\mu H$, $f_{SW} = 500kHz$, $T_A = 25^\circ C$, unless otherwise noted.

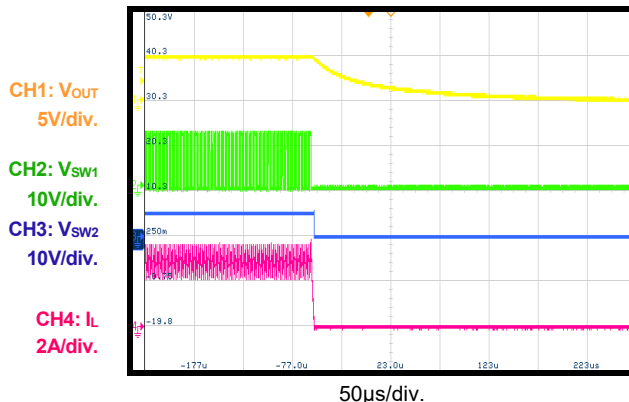
Shutdown through EN

Load = 0A



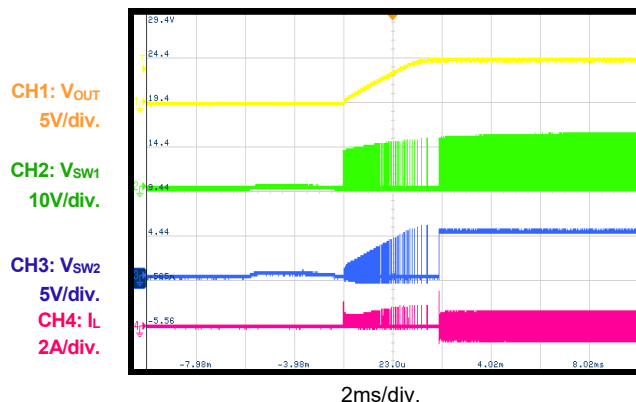
Shutdown through EN

Load = 3A



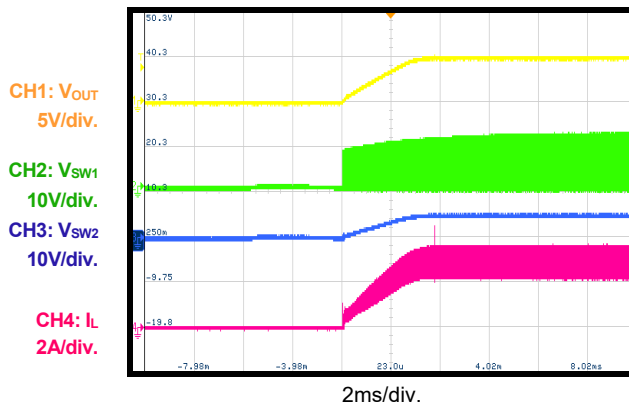
Start-Up through VIN

Load = 0A



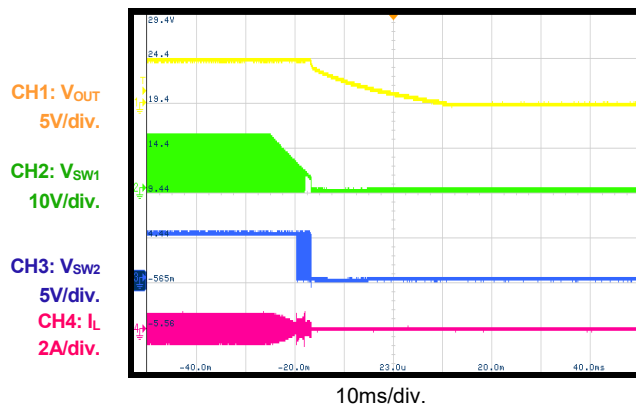
Start-Up through VIN

Load = 3A



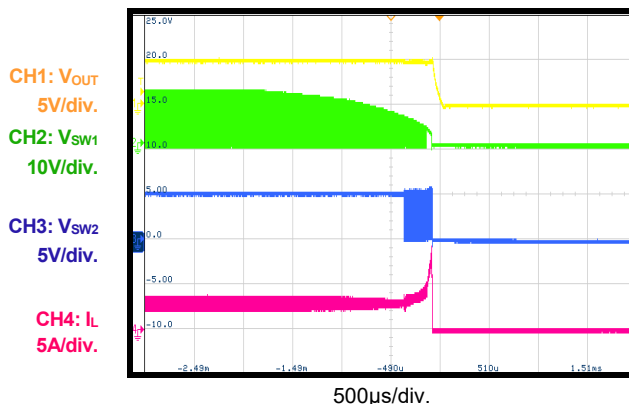
Shutdown through VIN

Load = 0A



Shutdown through VIN

Load = 3A

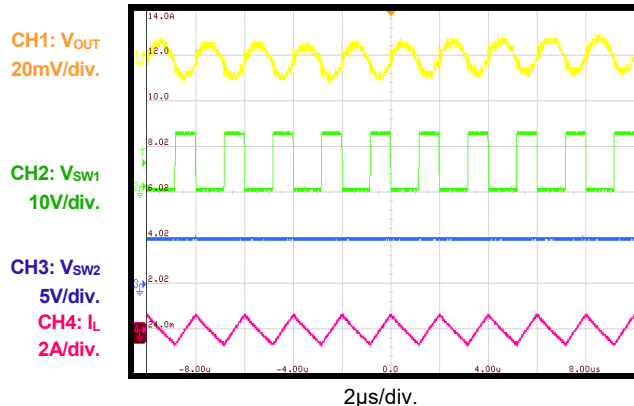


EVB TEST RESULTS (continued)

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 4.7\mu H$, $f_{SW} = 500kHz$, $T_A = 25^\circ C$, unless otherwise noted.

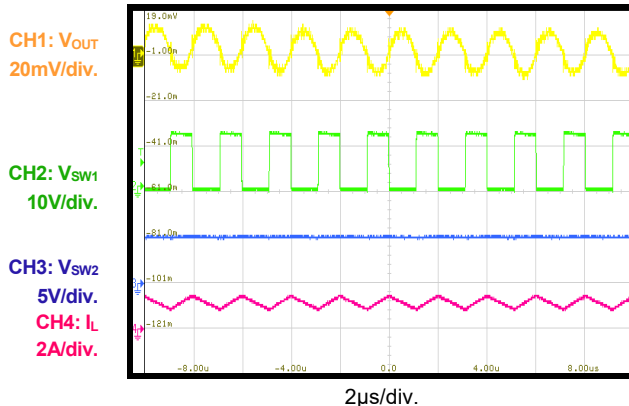
Steady State

$V_{OUT} = 5V$, load = 0A, $f_{SW} = 500kHz$



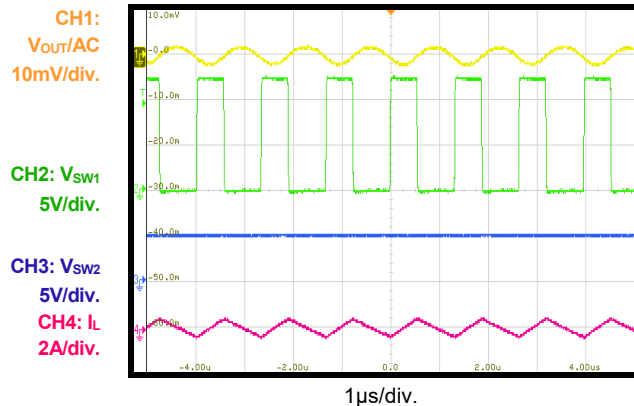
Steady State

$V_{OUT} = 5V$, load = 3A, $f_{SW} = 500kHz$



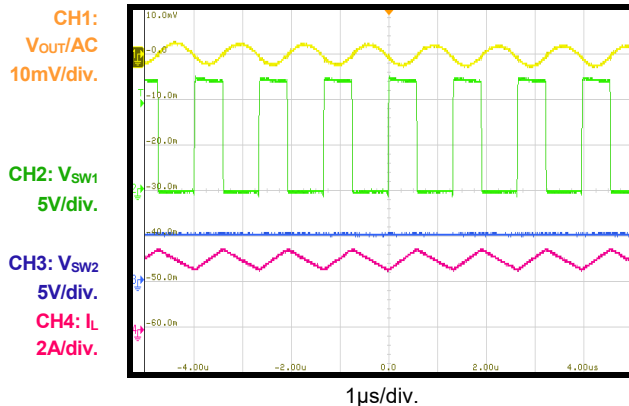
Steady State

$V_{OUT} = 5V$, load = 0A, $f_{SW} = 750kHz$



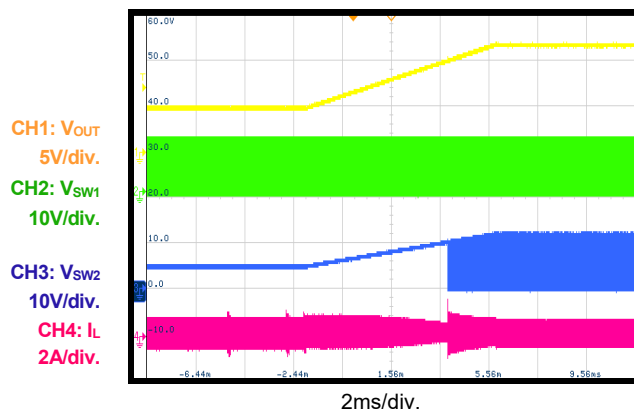
Steady State

$V_{OUT} = 5V$, load = 3A, $f_{SW} = 750kHz$



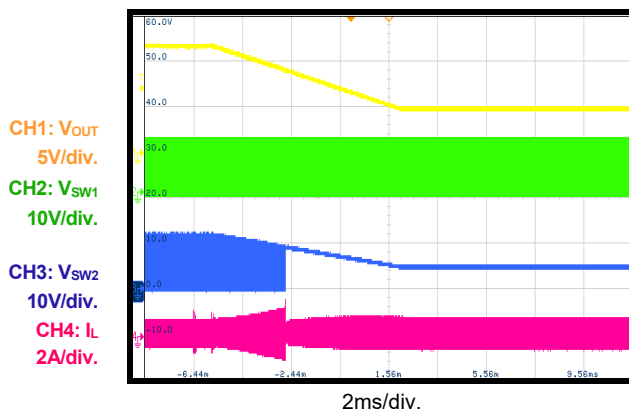
I²C VID

$V_{OUT} = 5V$ to 12V, $I_{OUT} = 0A$, $R_1 = 430k\Omega$, $R_2 = 53.6k\Omega$



I²C VID

$V_{OUT} = 5V$ to 12V, $I_{OUT} = 0A$, $R_1 = 430k\Omega$, $R_2 = 53.6k\Omega$

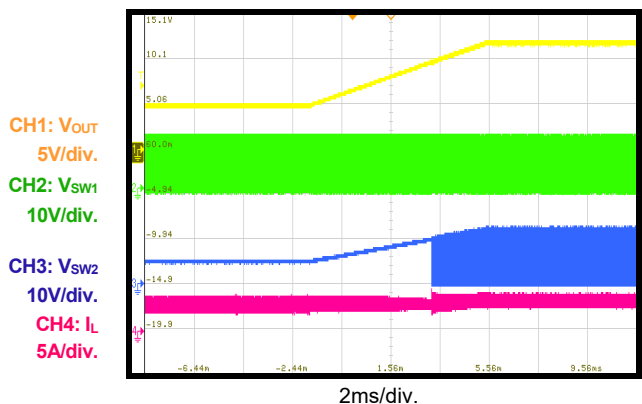


EVB TEST RESULTS (continued)

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 4.7\mu H$, $f_{SW} = 500kHz$, $T_A = 25^\circ C$, unless otherwise noted.

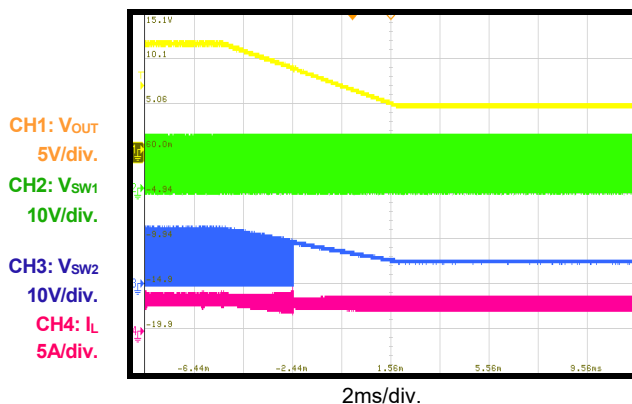
I^2C VID

$V_{OUT} = 5V$ to $12V$, $I_{OUT} = 3A$, $R_1 = 430k\Omega$, $R_2 = 53.6k\Omega$



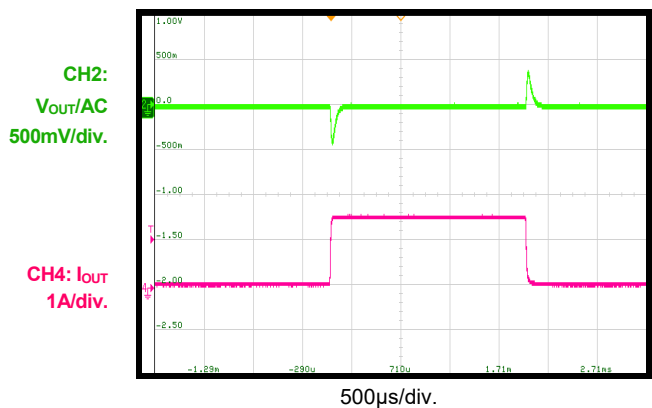
I^2C VID

$V_{OUT} = 5V$ to $12V$, $I_{OUT} = 3A$, $R_1 = 430k\Omega$, $R_2 = 53.6k\Omega$



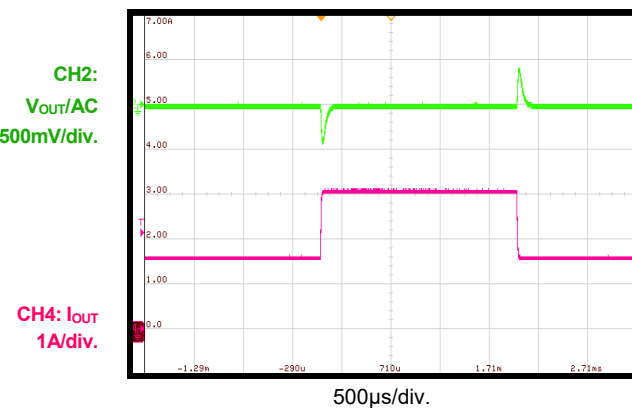
Load Transient

$V_{IN} = 12V$, $V_{OUT} = 5V$, no line drop compensation, $0A$ to $1.5A$, $150mA/\mu s$

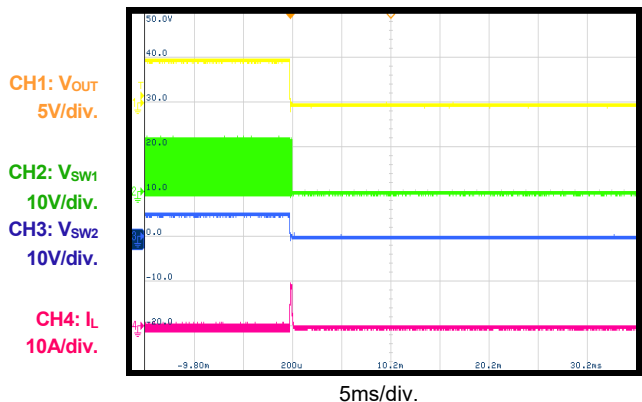


Load Transient

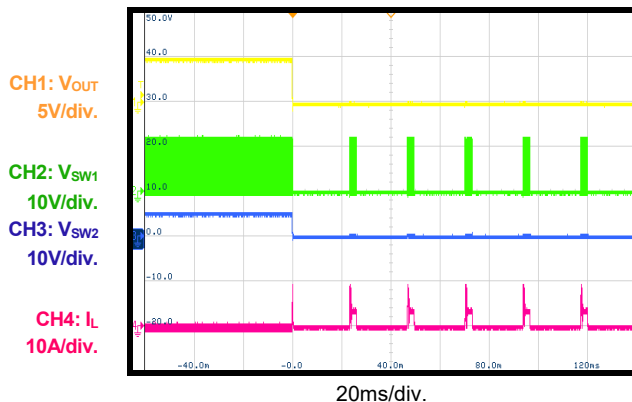
$V_{IN} = 12V$, $V_{OUT} = 5V$, no line drop compensation, $1.5A$ to $3A$, $150mA/\mu s$



SCP Entry in Latch-Off Mode



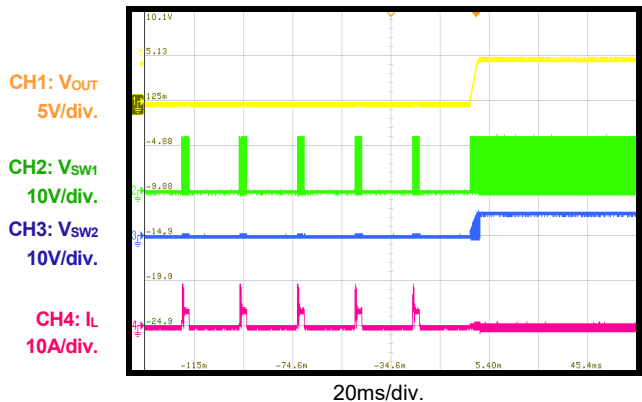
SCP Entry in Hiccup Mode



EVB TEST RESULTS *(continued)*

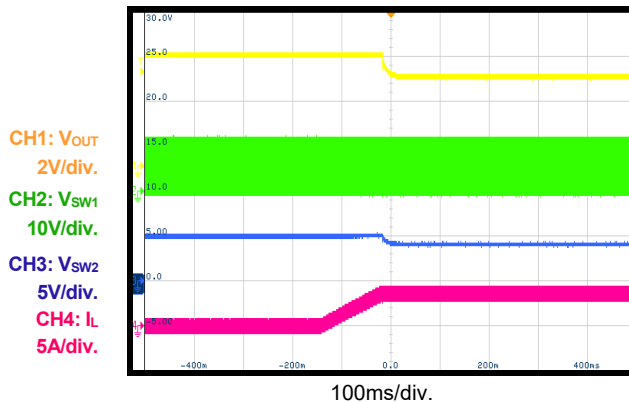
Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 4.7\mu H$, $f_{SW} = 500kHz$, $T_A = 25^{\circ}C$, unless otherwise noted.

SCP Recovery in Hiccup Mode

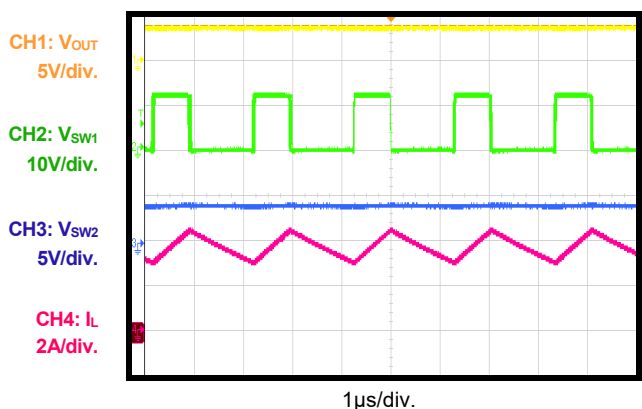


CC Limit Entry

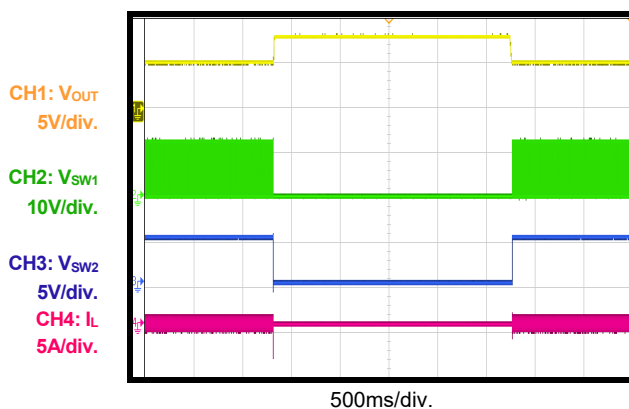
Tested in CV mode on an electronic load



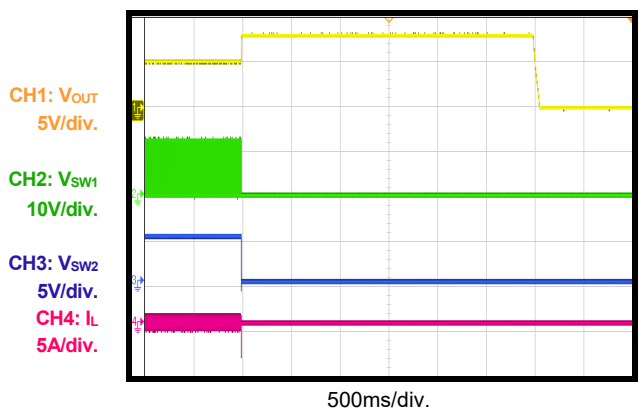
CC Limit Steady State



V_{OUT} OVP in Hiccup Mode



V_{OUT} OVP in Latch-Off Mode



PCB LAYOUT

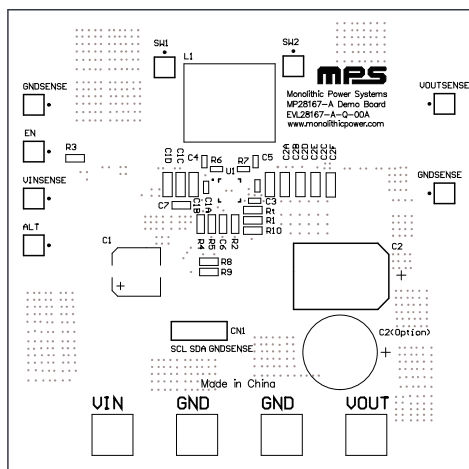


Figure 2: Top Silk

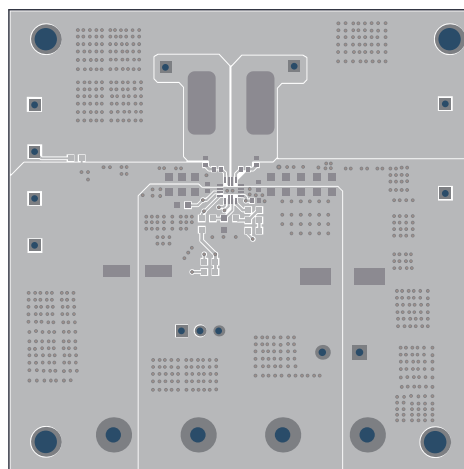


Figure 3: Top Layer

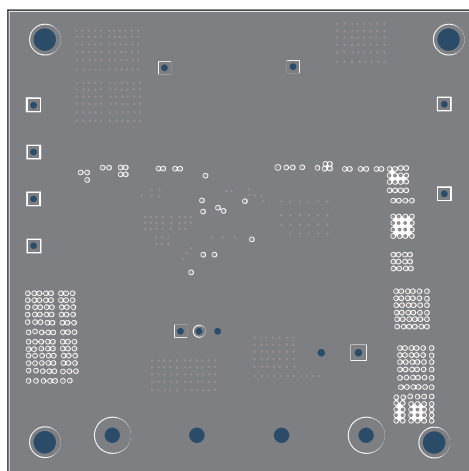


Figure 4: Mid-Layer 1

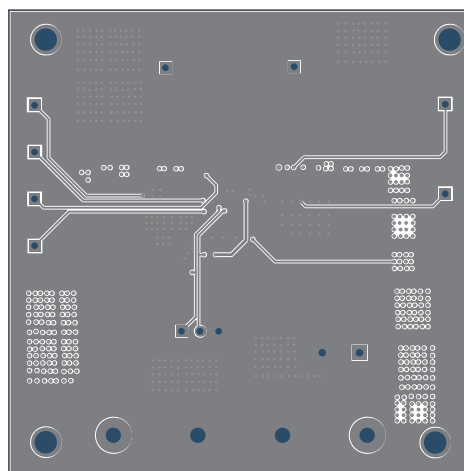


Figure 5: Mid-Layer 2

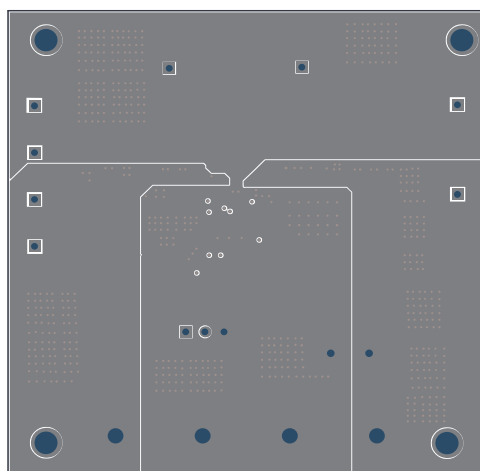


Figure 6: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/25/2021	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.