



EV2760-VT-00A

I²C-Controlled, 1-Cell to 4-Cell, Buck-Boost NVDC Charger with Reverse Source Mode Evaluation Board

DESCRIPTION

The EV2760-VT-00A evaluation board is designed to demonstrate the capabilities of the MP2760, a buck-boost, narrow voltage DC (NVDC) charger IC designed for applications with 1-cell to 4-cell series battery packs.

The MP2760 can accept a wide 4V to 22V operating input voltage (V_{IN}) range to charge the battery and power the load connected on SYS. The device also supplies a wide 3V to 21V voltage at the IN pin in source mode, which

is compliant with USB powered device (PD) specifications.

When input power is present, the EV2760-VT-00A charges the battery with a maximum 6A charge current. It can also supply voltage at the input when source mode is enabled. In source mode, the output current (I_{OUT}) is limited to 6A.

The MP2760 is available in a TQFN-30 (4mmx5mm) package.

PERFORMANCE SUMMARY ⁽¹⁾

Specifications are at $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		4V to 22V
Battery charge regulation voltage (V_{BATT_REG})	2 cells	8.4V (I ² C-configurable)
Fast charge current (I_{CC})	$V_{IN} = 9\text{V to } 22\text{V}$	2A (I ² C-configurable)
System voltage ($V_{SYS_MIN_REG}$)	2 cells	6.5V (I ² C-configurable)
Output voltage in source mode (V_{IN_SRC}) range		3V to 21V
Output voltage in source mode (V_{IN_SRC})		4.98V (I ² C-configurable)
Output current limit in source mode (I_{IN_SRC})		2A (I ² C-configurable)
Charge typical efficiency	$V_{IN} = 20\text{V}$, $V_{BATT} = 8\text{V}$, $I_{CC} = 5\text{A}$	93.49%
Charge peak efficiency	$V_{IN} = 12\text{V}$, $V_{BATT} = 8\text{V}$, $I_{CC} = 3\text{A}$	96%
Source mode typical efficiency	$V_{BATT} = 7.4\text{V}$, $V_{IN_SRC} = 20\text{V}$, $I_{IN_SRC} = 1.5\text{A}$	93.5%
Source mode peak efficiency	$V_{BATT} = 8.4\text{V}$, $V_{IN_SRC} = 12\text{V}$, $I_{IN_SRC} = 1.5\text{A}$	96.37%
Switching frequency (f_{SW})		600kHz (I ² C-configurable)

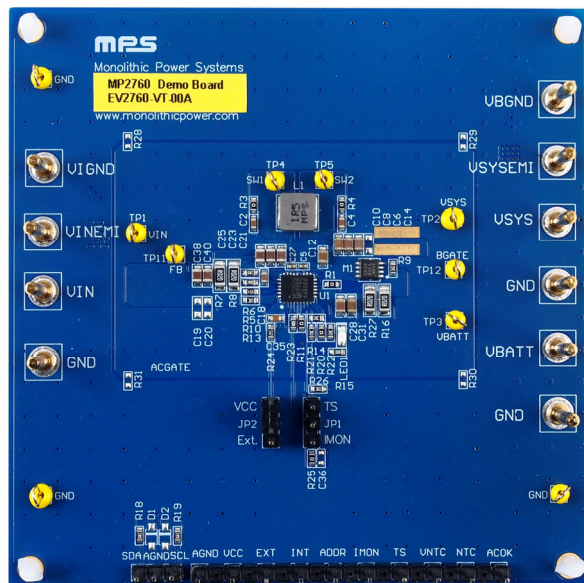
Note:

1) Refer to the MP2760 datasheet for details.



Optimized Performance with MPS Inductor MPL-AL5030-1R5

EVALUATION BOARD



LxWxH (8.9cmx8.9cmx0.8cm)

Board Number	MPS IC Number
EV2760-VT-00A	MP2760GVT-0000

QUICK START GUIDE

The EV2760-VT-00A evaluation board is designed for the MP2760, a buck-boost NVDC charger, when the device is used to charge a 2-cell battery. The board layout accommodates most commonly used resistors and capacitors. The board's default function is preset for charger mode, and the full charge voltage is preset to 8.4V. In charge mode, the MP2760 can work automatically in buck or buck-boost mode according to the input and battery voltages.

Follow the steps below to prepare the evaluation board.

1. Ensure that the computer has at least one USB port and a USB cable. The MP2760 evaluation software must be properly installed.
2. Connect the USB-to-I²C communication kit (EVKT-USBI2C-02) (see Figure 1).



Figure 1: USB-to-I²C Communication Kit

3. To enable the software, double-click on the “MP2651 Evaluation Kit” .exe file to run the MP2651 evaluation software. The software supports Windows 7 and Windows 10 operating systems.

The MP2760 evaluation kit.exe file can be downloaded from the MPS website.

Original Test Set-Up for the MP2760

1. Connect the battery terminals to:
 - a. Positive (+): VBATT
 - b. Negative (-) GND
2. If using a battery simulator, preset the battery voltage between 0V and 8.4V, then turn off the battery voltage.
3. Connect the battery simulator output to the VBATT and GND pins, respectively.
4. Turn on the battery simulator before starting the test.
5. For charge mode testing, connect the input terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND

Figure 2 on page 4 shows the charge mode testing set-up.

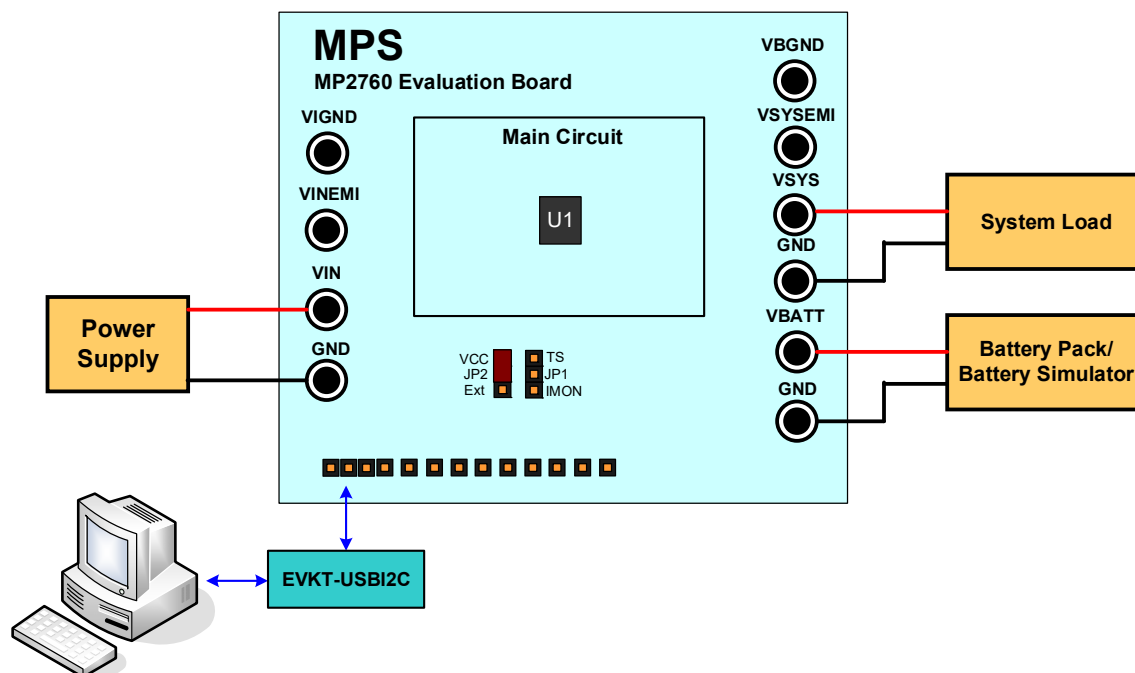


Figure 2: Charge Mode Test Set-Up

6. Connect the system load terminals to:
 - a. Positive (+): VSYS
 - b. Negative (-): GND
7. For source mode testing, connect the load terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND

Table 1 shows the jumper connection settings.

Table 1: Jumper Connections

Jack	Description	Default Setting
JP1 ⁽²⁾	To select the pull-voltage, pull JP1 up to VCC or an external power source.	Pull up JP1 to VCC
JP2 ⁽³⁾	For the TS/IMON pin's connection, connect TS/IMON to different external circuitry depending on the TS/IMON selection.	Open

Notes:

- 2) If EXT is selected, add an external power source (e.g. 3.3V) at EXT to AGND. If VCC is selected, no other action is required.
- 3) TS/IMON has different external circuits. Connect TS/IMON to the corresponding circuit using the I²C.

8. Launch the MP2760 evaluation software (see Figure 3).



Figure 3: MP2760 Evaluation Software

- Turn on the input voltage (V_{IN}) to charge the battery and power the system load with the default settings.

Modifying Parameters via the GUI

To use MPS's GUI, ensure that all connections are successful, such as the connections between the computer, USB-to-I²C communication kit, and the evaluation board.

Figure 4 shows the MP2760's basic settings.

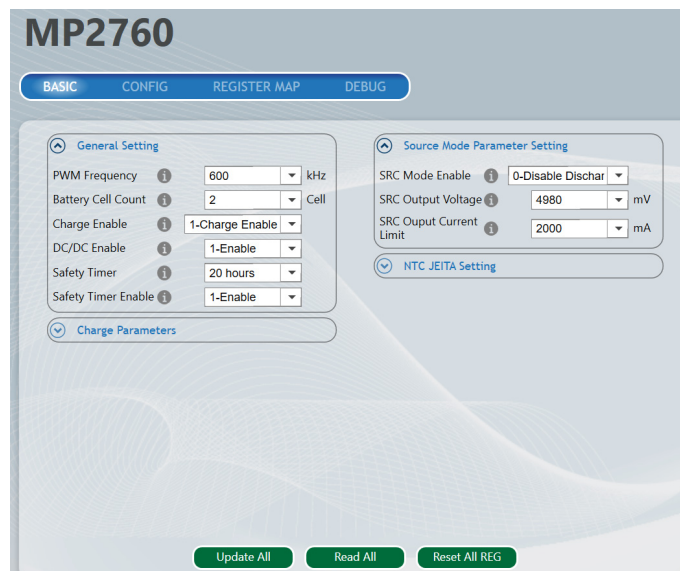
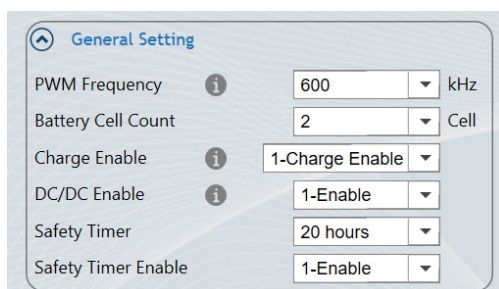


Figure 4: Basic Settings

Figure 5 on page 6 shows how to configure the general settings. These settings include the pulse-width modulation (PWM) frequency, battery cell count, safety timer, basic controls in charge mode (such as enabling the DC/DC converter), and charge enabling.

Note that the recommended PWM frequency is between 500kHz and 800kHz.

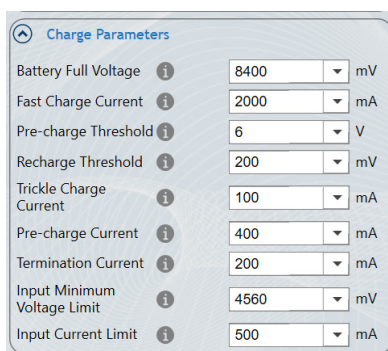


General Setting	
PWM Frequency	600 kHz
Battery Cell Count	2 Cell
Charge Enable	1-Charge Enable
DC/DC Enable	1-Enable
Safety Timer	20 hours
Safety Timer Enable	1-Enable

Figure 5: General Settings

Figure 6 shows how to configure the charge parameters, including the battery-full voltage, fast charge current, pre-charge threshold, recharge threshold, trickle charge current, pre-charge current, and termination current.

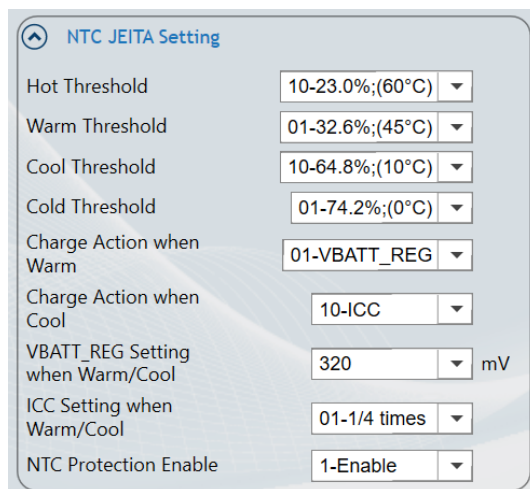
The charge parameters also provide the parameters for power path management, including the input minimum voltage limit and input current limit. All the parameters can be input directly by keyboard.



Charge Parameters	
Battery Full Voltage	8400 mV
Fast Charge Current	2000 mA
Pre-charge Threshold	6 V
Recharge Threshold	200 mV
Trickle Charge Current	100 mA
Pre-charge Current	400 mA
Termination Current	200 mA
Input Minimum Voltage Limit	4560 mV
Input Current Limit	500 mA

Figure 6: Charge Parameters

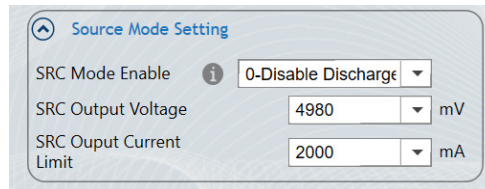
Figure 7 shows how to configure the negative temperature coefficient (NTC) JEITA settings for battery thermal protection.



NTC JEITA Setting	
Hot Threshold	10-23.0%;(60°C)
Warm Threshold	01-32.6%;(45°C)
Cool Threshold	10-64.8%;(10°C)
Cold Threshold	01-74.2%;(0°C)
Charge Action when Warm	01-VBATT_REG
Charge Action when Cool	10-ICC
VBATT_REG Setting when Warm/Cool	320 mV
ICC Setting when Warm/Cool	01-1/4 times
NTC Protection Enable	1-Enable

Figure 7: NTC JEITA Settings

Figure 8 on page 7 shows how to configure the source mode settings. In source mode, the battery supplies power to the IN pin. The discharge parameters include the SRC mode (enabled or disabled), SRC output voltage, and SRC output current limit.



Source Mode Setting

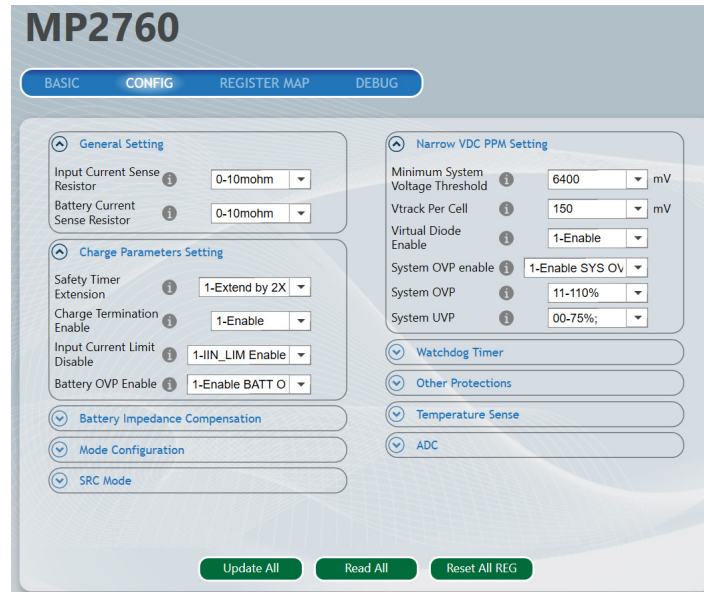
SRC Mode Enable ⓘ 0-Disable Discharge ▼

SRC Output Voltage 4980 ▼ mV

SRC Output Current Limit 2000 ▼ mA

Figure 8: Source Mode Settings

Figure 9 shows the MP2760's configuration settings.



MP2760

BASIC CONFIG REGISTER MAP DEBUG

General Setting

Input Current Sense Resistor ⓘ 0-10mohm ▼

Battery Current Sense Resistor ⓘ 0-10mohm ▼

Charge Parameters Setting

Safety Timer Extension ⓘ 1-Extend by 2X ▼

Charge Termination Enable ⓘ 1-Enable ▼

Input Current Limit Disable ⓘ 1-IIN_LIM Enable ▼

Battery OVP Enable ⓘ 1-Enable BATT O' ▼

Battery Impedance Compensation

Mode Configuration

SRC Mode

Narrow VDC PPM Setting

Minimum System Voltage Threshold ⓘ 6400 ▼ mV

Vtrack Per Cell ⓘ 150 ▼ mV

Virtual Diode Enable ⓘ 1-Enable ▼

System OVP enable ⓘ 1-Enable SYS OV ▼

System OVP ⓘ 11-110% ▼

System UVP ⓘ 00-75% ▼

Watchdog Timer

Other Protections

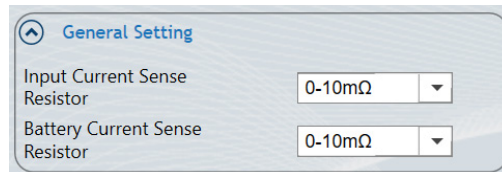
Temperature Sense

ADC

Update All Read All Reset All REG

Figure 9: Configuration Settings

Figure 10 shows how to configure and select the current-sense resistors.



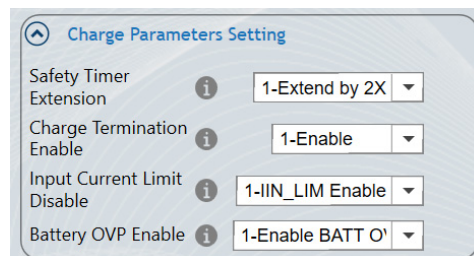
General Setting

Input Current Sense Resistor 0-10mΩ ▼

Battery Current Sense Resistor 0-10mΩ ▼

Figure 10: Current-Sense Resistor Settings

Figure 11 shows how to configure the charge protection parameters. These parameters include the safety timer extension, as well as options to enable charge termination, the input current limit, and battery over-voltage protection (OVP).



Charge Parameters Setting

Safety Timer Extension ⓘ 1-Extend by 2X ▼

Charge Termination Enable ⓘ 1-Enable ▼

Input Current Limit Disable ⓘ 1-IIN_LIM Enable ▼

Battery OVP Enable ⓘ 1-Enable BATT O' ▼

Figure 11: Charge Parameters Setting

Figure 12 on page 8 shows how to configure the battery impedance compensation, including the battery impedance and voltage compensation limit.

Batter Impedance Compensation

Battery Impedance: 0 mΩ

Voltage Compensation Limit: 0 mV

Figure 12: Battery Impedance Compensation

Figure 13 shows how to configure the external MOSFET control. ACGATE can be set to drive the input MOSFET between the ADP pin and the input current-sense resistor. BGATE can be set to control the battery MOSFET between the SYS pin and the battery current-sense resistor.

Mode Configuration

BGATE Driver Enable: 1-Enable BGATE

BGATE Force Off: 0-Not force BGAT

ACGATE Force On: 0-Not force ACGA

ACGATE Driver Enable: 1-Enable ACGAE

Figure 13: External MOSFET Configuration

Figure 14 shows how to configure the SRC mode control, which includes the SRC output voltage configuration and protections.

SRC Mode

SRC Output Voltage Configuration: 0-By register bit

SRC Output Voltage Offset: 0 V

Battery Low Voltage Protection Enable: 1-Enable

Battery Low Voltage Threshold: 6 V

DC/DC Action when Battery Low Voltage: 0-INT

Battery Discharge Current Limit: 6400 mA

Battery Discharge Current Limit Enable: 0-Disable

Figure 14: SRC Mode Configuration

Figure 15 shows how to configure the NVDC power path management (PPM).

Narrow VDC PPM Setting

Minimum System Voltage Threshold: 6400 mV

Vtrack Per Cell: 100 mV

Virtual Diode Enable: 1-Enable

System OVP enable: 1-Enable SYS OV

System OVP: 11-110%

System UVP: 00-75%;

Figure 15: NVDC PPM Settings

Figure 16 on page 9 shows how to configure the watchdog timer.

Watchdog Timer

Watchdog Timer: 00-Disable Tim

Watchdog Feed Bit: 0-Normal

Watchdog Timer Setting when Input Absent: 1-Enable

Figure 16: Watchdog Timer

Figure 17 shows how to configure additional protections, including the input under-voltage (UV) threshold, input over-voltage (OV) threshold, and input OV deglitch time.

Other Protections

Input Under Voltage Threshold: 3.2 V

Input Over Voltage Threshold: 22.4 V

Input Over Voltage Deglitch Time: 0-100ns

Figure 17: Additional Protections

Figure 18 shows how to configure temperature-sense control. The TS/IMON pin can be set as either the temperature-sense pin (TS) or the battery current monitor pin (IMON).

Temperature Sense

TS/IMON Pin Function: 0-TS

TS Sense Point: 1-Battery FET

TS Function Enable: 1-Enable

TS Function Action Enable when Fault: 1-INT and TS a

TS Temperature Threshold: 100-14.3%;(80°

Thermal loop Enable: 1-Enable

Thermal Loop Temperature Threshold: 111-120°C

Figure 18: Temperature Sense

Figure 19 shows how to configure the ADC operation mode.

ADC

ADC Conversion Behavior: 0-One-shot Cor

ADC Conversion One-shot Enable: 1-Enable ADC

Figure 19: ADC Operation Mode

Figure 20 on page 10 shows the register map, which matches all the register results displayed on the BASIC and CONFIG pages.

MP2760

BASIC CONFIG REGISTER MAP DEBUG

Command code	Command name	Register
05H	Device Address Setting	0209
06H	Input Minimum Voltage Limit Setting	0039
07H	System Minimum Voltage Setting	002C
08H	Input Current Limit Setting	003C
09H	Output Voltage Setting	00F9
0AH	Battery Impedance Compensation and Output Current Limit Setting	0028
0BH	Battery Low Voltage Setting and Battery Discharge Current Regulation	308C
0CH	JEITA Action Setting	341C
0DH	Temperature Protection Setting	F399
0EH	Configuration Register 0	001C
0FH	Configuration Register 1	F244
10H	Configuration Register 2	0A7E
11H	Configuration Register 3	60EE
12H	Configuration Register 4	3C7E
14H	Charge Current Setting	0A0C

Figure 20: MP2760 Register Map

Figure 21 shows the monitor view.

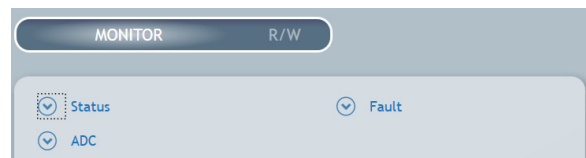


Figure 21: Monitor View

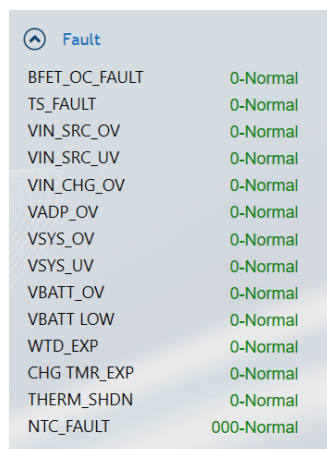
Figure 22 shows how to configure the status.

↑ Status

MD_STAT	01-Operation Mode
PG_STAT	1-Power Good
SWITCH_STAT	11-BOOST
BATTMISS_STAT	0-Normal
Address Setting STAT	0-Single port
CHG_STAT	011-CC charge
VIN_MIN_STAT	0-Not in input voltage limit
IIN_LIM_STAT	1-In input current limit
TJREG_STAT	0-Not in thermal regulation loop
IIN_DPM	500 mA

Figure 22: Status Setting

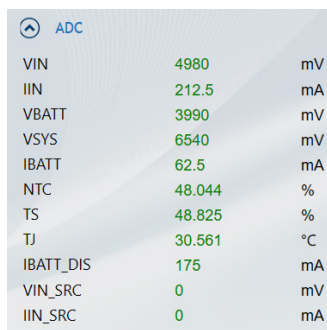
Figure 23 shows how the fault statuses are displayed.



Fault	
BFET_OC_FAULT	0-Normal
TS_FAULT	0-Normal
VIN_SRC_OV	0-Normal
VIN_SRC_UV	0-Normal
VIN_CHG_OV	0-Normal
VADP_OV	0-Normal
VSYS_OV	0-Normal
VSYS_UV	0-Normal
VBATT_OV	0-Normal
VBATT_LOW	0-Normal
WTD_EXP	0-Normal
CHG_TMR_EXP	0-Normal
THERM_SHDN	0-Normal
NTC_FAULT	000-Normal

Figure 23: Fault Settings

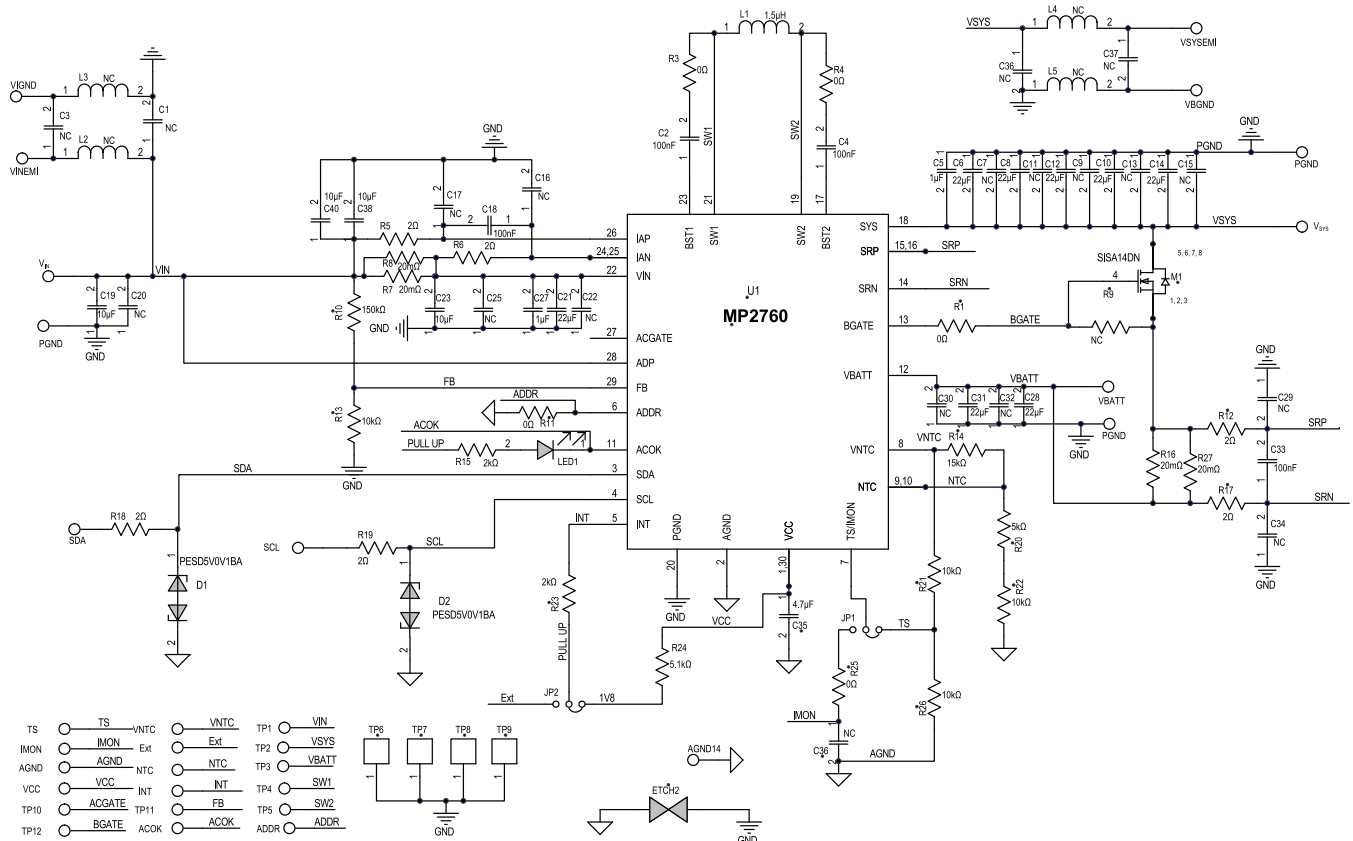
Figure 24 shows how to configure the analog-to-digital converter (ADC).



ADC		
VIN	4980	mV
IIN	212.5	mA
VBATT	3990	mV
VSYS	6540	mV
IBATT	62.5	mA
NTC	48.044	%
TS	48.825	%
TJ	30.561	°C
IBATT_DIS	175	mA
VIN_SRC	0	mV
IIN_SRC	0	mA

Figure 24: ADC Settings

EVALUATION BOARD SCHEMATIC



EV2760-VT-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	L2, L3, L4, L5	NC				
6	R1, R3, R4, R11, R20, R25	0	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
6	R5, R6, R12, R17, R18, R19	2Ω	Film resistor, 5%	0603	Liz	CR0603JA02R0G
4	R7, R8, R16, R27	20mΩ	Film resistor, 1%, 1/4W	1206	Cyntec	RL1632H-R020-FN
1	R9	1mΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071ML
1	R10	150kΩ	Film resistor, 5%, 1/10W	0603	Yageo	RC0603JR-07150KL
5	R13, R14, R21, R22, R26	10kΩ	Film resistor, 1%, 1/10W	0603	Yageo	RC0603FR-0710KL
2	R15, R23	2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072KL
1	R24	5.1kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-075K1L
4	R28, R29, R30, R31	NC				
11	C1, C3, C15, C16, C17, C22, C29, C34, C36, C37, C39	NC				
4	C2, C4, C18, C33	100nF	Ceramic capacitor, 25V, X7R	0603	Wurth	885012206071
2	C5, C27	1μF	Ceramic capacitor, 25V, X5R	0402	Murata	GRM155R61E105KA12
6	C6, C8, C10, C12, C28, C31	22μF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
9	C7, C9, C11, C13, C14, C19, C20, C30, C32	NC				
5	C21, C23, C25, C38, C40	10μF	Ceramic capacitor, 25V, X7S	0805	Murata	GRM21BC7E106KE11L
1	C35	4.7μF	Ceramic capacitor, 25V, X5R	0603	Murata	GRM188R61E475KE11D
1	LED1	Red	Red LED	0805	Bright LED	BL-HUE35A-AV-TRB
2	D1, D2	NC				
1	M1	8.5mΩ	N-channel MOSFET, 30V, 20A	PowerPAK 1212-8	Vishay	SISA14DN-T1-GE3
13	ACOK, ADDR, AGND, AGND, EXT, IMON, INT, NTC, TS, VCC, VNTC, SCL, SDA	2.54mm	Pin header	DIP	Any	

EV2760-VT-00A BILL OF MATERIALS *(continued)*

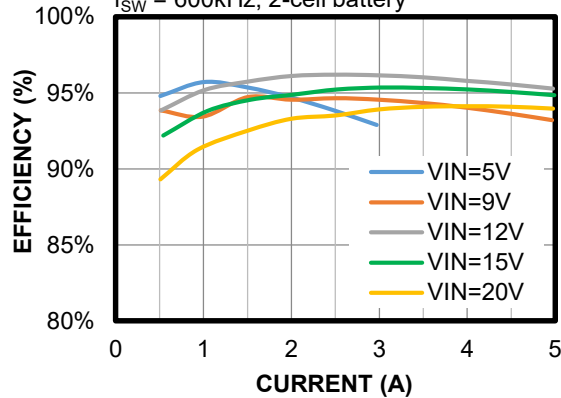
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
11	TP1, TP2, TP3, TP4, TP5, TP6 (GND), TP7 (GND), TP8 (GND), TP9 (GND), TP11, TP12	1mm	Test point, $\phi = 1\text{mm}$	DIP	Any	
10	VIN, VINEMI, VBATT, VSYS, VSYSSEMI, GND, GND, GND, VIGND, VBGND	2mm	Test point, $\phi = 2\text{mm}$	DIP	Any	
2	JP1, JP2	2.54mm	Pin header	DIP	Any	
1	JP1	2.54mm	Jumper	DIP	Any	
1	L1	1.5 μH	Inductor, 9.7m Ω , 9A	SMD	MPS	MPL-AL5030-1R5
1	U1	MP2760	1-cell to 4-cell buck- boost charger	TQFN-30 (4mmx 5mm)	MPS	MP2760GVT-0000

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. Default setting is for a 2-cell battery, $C_{IN} = 10\mu F \times 5 + 1\mu F \times 1$, $C_{SYS} = 22\mu F \times 4 + 1\mu F \times 1$, $C_{BATT} = 22\mu F \times 2$, $L = 1.5\mu H$ (10m Ω), $f_{SW} = 600kHz$, 2-cell battery. $T_A = 25^\circ C$, unless otherwise noted.

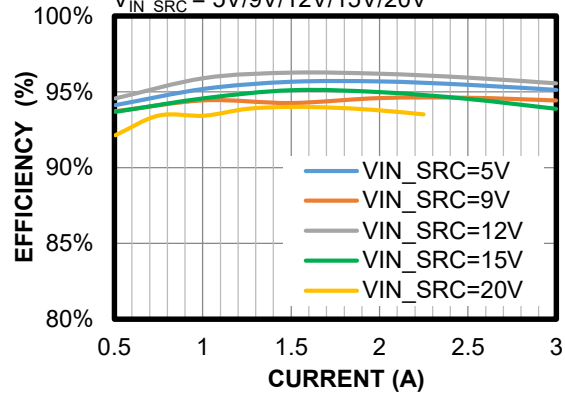
Efficiency vs. Charge Current in Charge Mode

$V_{BATT} = 8V$, $V_{IN} = 5V/9V/12V/15V/20V$,
 $f_{SW} = 600kHz$, 2-cell battery



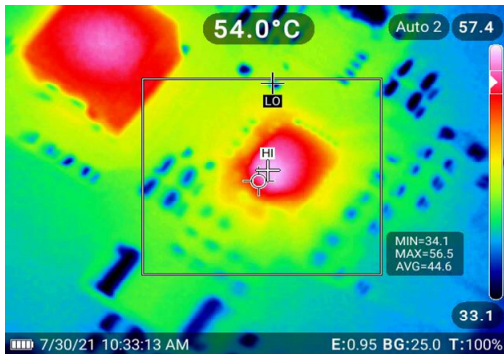
Efficiency vs. Source Current in Source Mode

$V_{BATT} = 8.4V$, $f_{SW} = 600kHz$, 2-cell battery,
 $V_{IN_SRC} = 5V/9V/12V/15V/20V$



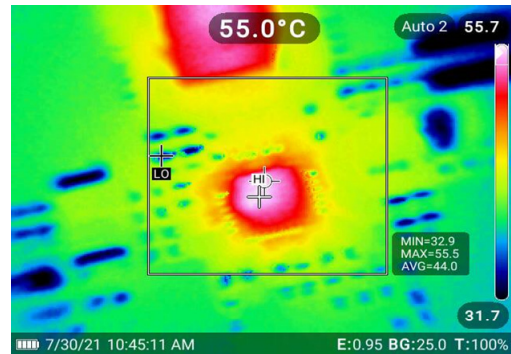
Thermal Performance

Charge mode, $V_{IN} = 20V$, $I_{NLIMIT} = 3A$,
 $V_{BATT} = 8.2V$, $I_{CC} = 5A$



Thermal Performance

Source mode, $V_{BATT} = 8.4V$, $V_{IN_SRC} = 20V$,
 $I_{IN_SRC} = 1.8A$

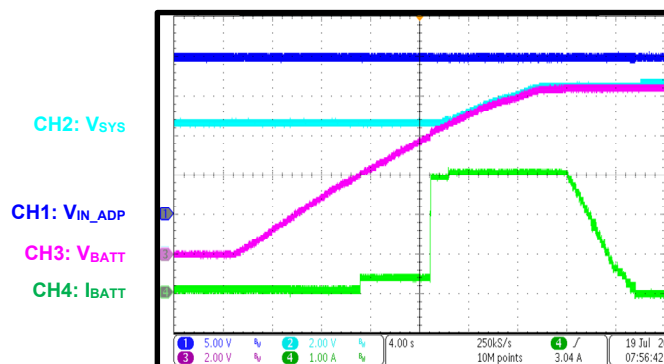


EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. Default setting is for a 2-cell battery, $C_{IN} = 10\mu F \times 5 + 1\mu F \times 1$, $C_{SYS} = 22\mu F \times 4 + 1\mu F \times 1$, $C_{BATT} = 22\mu F \times 2$, $L = 1.5\mu H$ (10m Ω), $f_{SW} = 600kHz$, 2-cell battery. $T_A = 25^\circ C$, unless otherwise noted.

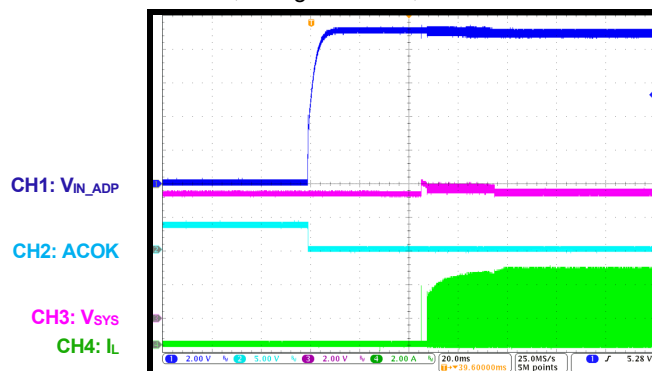
Charge Profile Curves

$V_{IN_ADP} = 20V$, $V_{BATT} = 0V$ to $8.4V$, $I_{IN_MIN} = 3A$,
 $I_{CC} = 2A$, $V_{SYS_MIN} = 6.4V$, $V_{TRACK} = 100mV$



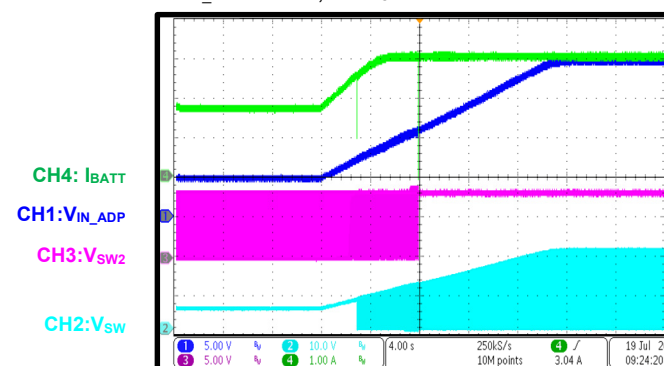
Start-Up through VIN in Charge Mode

9V input power on, $V_{BATT} = 7.4V$ (2 cells),
 $I_{CC} = 2A$, charge enabled, $I_{SYS} = 0A$



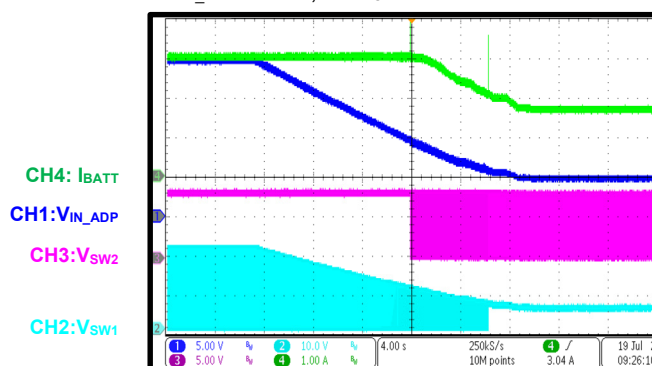
V_{IN_ADP} Step from 5V to 20V

$I_{IN_MIN} = 3A$, $V_{BATT} = 8V$, $I_{CC} = 3A$,
 $V_{SYS_MIN} = 6.4V$, $V_{TRACK} = 100mV$



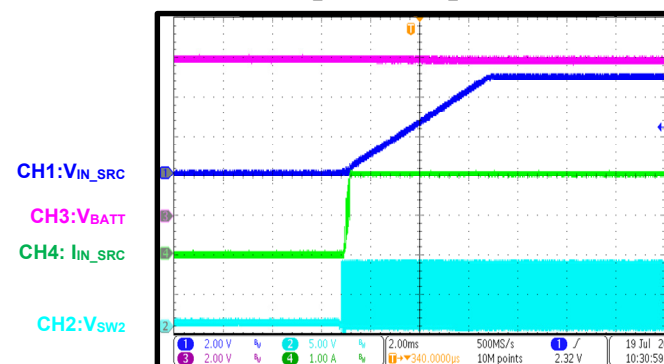
V_{IN_ADP} Step from 20V to 5V

$I_{IN_MIN} = 3A$, $V_{BATT} = 8V$, $I_{CC} = 3A$,
 $V_{SYS_MIN} = 6.4V$, $V_{TRACK} = 100mV$



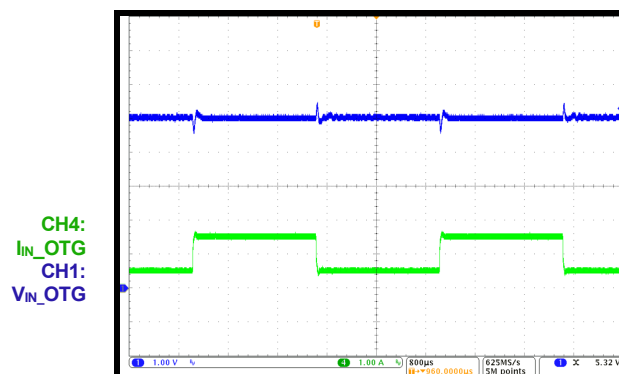
Start-Up through V_{IN_SRC} in Source Mode

$V_{BATT} = 8V$, $V_{IN_SRC} = 5V$, $I_{IN_SRC} = 2A$



Load Transient in Source Mode

$V_{BATT} = 7.4V$ (2 cells), $V_{IN_SRC} = 5V$, load current
 between 0.5A and 1.5A

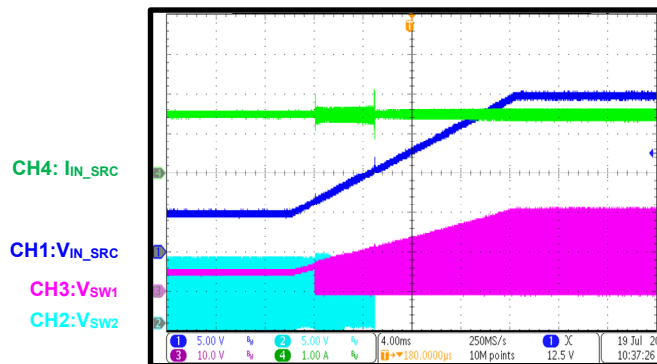


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. Default setting is for a 2-cell battery, $C_{IN} = 10\mu F \times 5 + 1\mu F \times 1$, $C_{SYS} = 22\mu F \times 4 + 1\mu F \times 1$, $C_{BATT} = 22\mu F \times 2$, $L = 1.5\mu H$ (10m Ω), $f_{SW} = 600kHz$, 2-cell battery. $T_A = 25^\circ C$, unless otherwise noted.

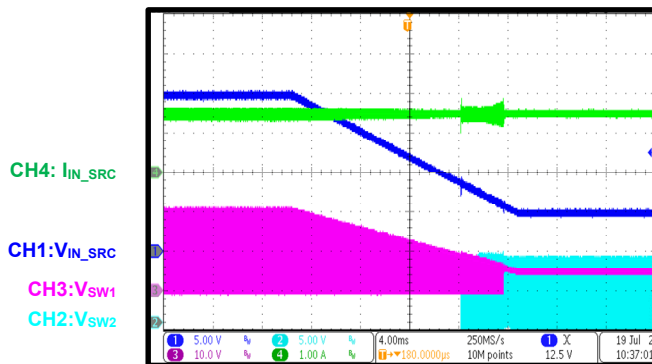
V_{IN_SRC} Step from 5V to 20V in Source Mode

$V_{BATT} = 8V$, $V_{IN_SRC} = 5V$ to $20V$, $I_{IN_SRC} = 1.5A$



V_{IN_SRC} Step from 20V to 5V in Source Mode

$V_{BATT} = 8V$, $V_{IN_SRC} = 20V$ to $5V$, $I_{IN_SRC} = 1.5A$



PCB LAYOUT

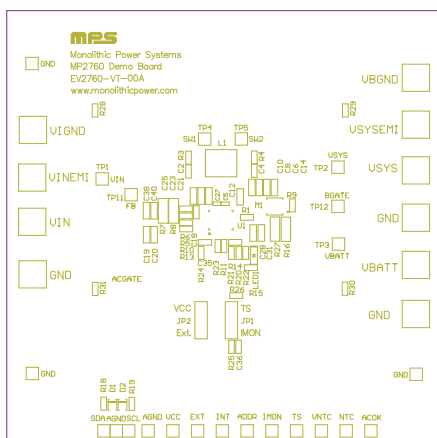


Figure 26: Top Silk

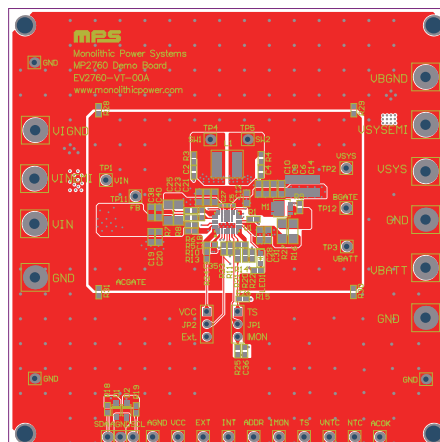


Figure 27: Top Layer

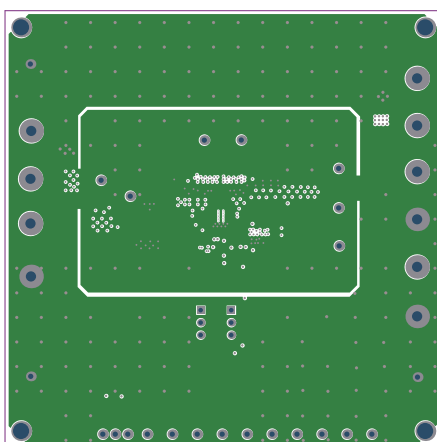


Figure 28: Mid-Layer 1

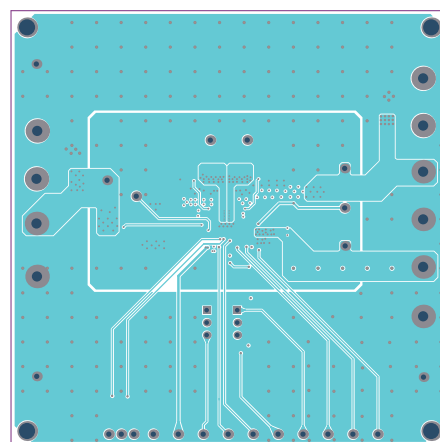


Figure 29: Mid-Layer 2

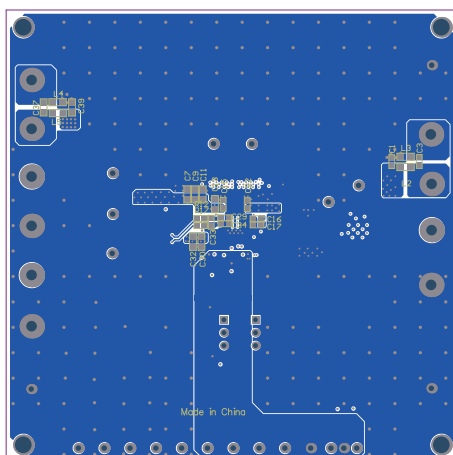


Figure 30: Bottom Layer

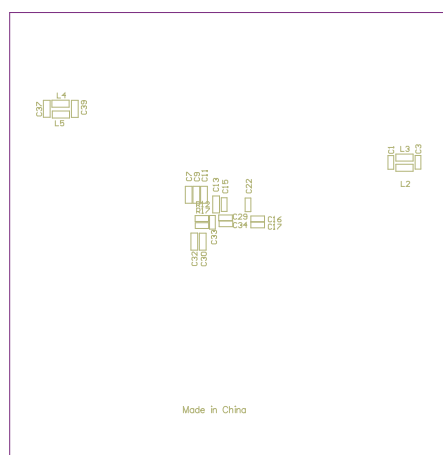


Figure 31: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/11/2022	Initial Release	-

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