8xC251TB/TQ

HIGH-PERFORMANCE CHMOS MICROCONTROLLER

Commercial/Express

- Real-time and Programmed Wait State Bus Operation
- Binary-code Compatible with MCS® 51
- Pin Compatible with 44-pin PLCC and 40-pin PDIP MCS 51 Sockets
- Register-based MCS® 251 Architecture
  - 40-byte Register File
  - Registers Accessible as Bytes, Words, or Double Words
- Enriched MCS 51 Instruction Set
  - 16-bit and 32-bit Arithmetic and Logic Instructions
  - Compare and Conditional Jump Instructions
  - Expanded Set of Move Instructions
- Linear Addressing
- 256-Kbyte Expanded External Code/Data Memory Space
- ROM Options: 16 Kbytes or without ROM
- 16-bit Internal Code Fetch
- 64-Kbyte Extended Stack Space
- On-chip Data RAM Options: 512-Byte
- 8-bit, 2-clock External Code Fetch in Page Mode
- Fast MCS 251 Instruction Pipeline
- User-selectable Configurations:
  - External Wait States (0-3 wait states)
  - Address Range & Memory Mapping
  - Page Mode
  - Extended Data Float Timings or 8xC251Sx Compatible AC Timings
- 32 Programmable I/O Lines
- Eight Maskable Interrupt Sources with Four Programmable Priority Levels
- Three Flexible 16-bit Timer/counters
- Hardware Watchdog Timer
- Programmable Counter Array
  - High-speed Output
  - Compare/Capture Operation
  - Pulse Width Modulator
  - Watchdog Timer
- Two Programmable Serial I/O Ports
  - Framing Error Detection
  - Automatic Address Recognition
- High-performance CHMOS Technology
- Static Standby to 24-MHz Operation
- Complete System Development Support
  - Compatible with Existing Tools
  - MCS 251 Tools Available: Compiler, Assembler, Debugger, ICE
- Package Options (PDIP and PLCC)

July 2004 **Order Number:** 273129-003

REVISION HISTORY:

Date	Revision	Description
November 1997	001	Initial release of this document
December 2003	002	Removed references to 8XC251TA, 8XC251TP
July 2004	003	To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

8xC251TB/TQ
HIGH-PERFORMANCE CHMOS Microcontroller

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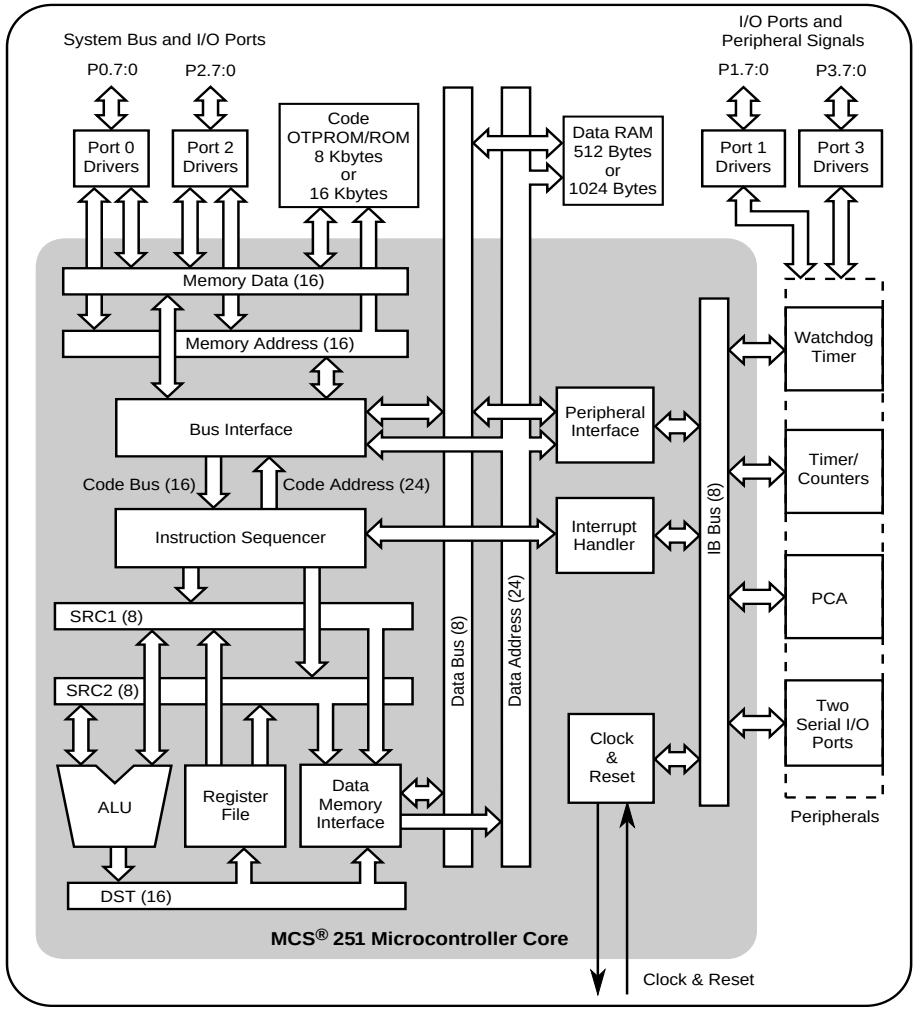
FIGURES

TABLES

1.0 INTRODUCTION

A member of the Intel family of 8-bit MCS 251 microcontrollers, the 8xC251TB/TQ is binary-code compatible with MCS 51 microcontrollers and pin compatible with 40-pin PDIP and 44-pin PLCC MCS 51 microcontrollers. MCS 251 microcontrollers feature an enriched instruction set, linear addressing, and efficient C-language support. The 8xC251TB/TQ has 512 bytes or 1 Kbyte of on-chip RAM and is available with 8 Kbytes or 16 Kbytes of on-chip ROM, or without ROM. A variety of features can be selected by new user-programmable configurations.

Figure 1. 8xC251TB/TQ Block Diagram



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2.0 NOMENCLATURE

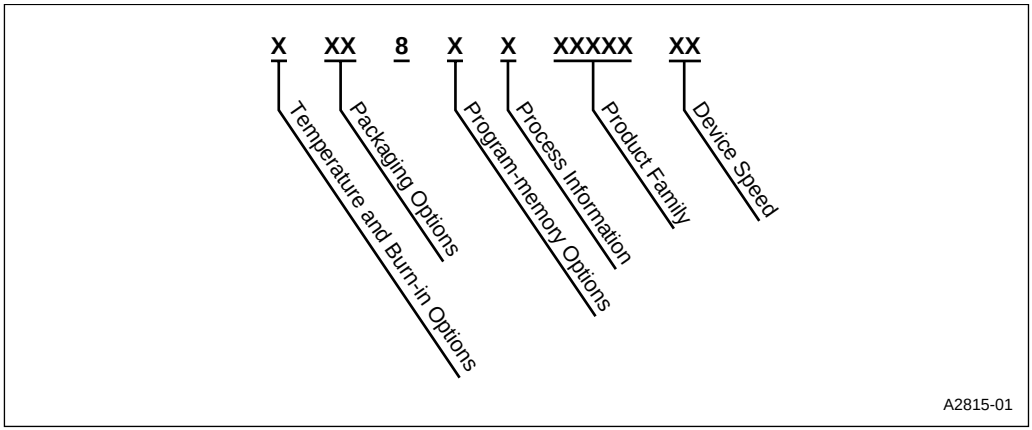


Figure 2. The 8xC251TB/TQ Family Nomenclature

Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
	x	Express operating temperature range (-40°C to 85°C) without Intel standard burn-in.
Packaging Options	x	44-pin Plastic Leaded Chip Carrier (PLCC)
	x	40-pin Plastic Dual In-line Package (PDIP)
	x	40-pin Ceramic Dual In-line Package (Ceramic DIP)
Program Memory Options	0	Without ROM
	3	ROM
Process Information	C	CHMOS
Product Family	251	8-bit control architecture
Device Memory Options	TB	1-Kbyte RAM/16-Kbyte ROM or without ROM
	TQ	512-byte RAM/16-Kbyte ROM or without ROM
Device Speed	24	External clock frequency

NOTE: To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

Table 2 lists the proliferation options. See Figure 2 for the 8xC251TB/TQ family nomenclature.

Table 2. Proliferation Options

8xC251TB/TQ (0 – 24 MHz; 5 V ±10%)	
80C251TB24	CPU-only
80C251TQ24	CPU-only
83C251TB24	ROM

Table lists the 8xC251TB/TQ package definitions.

Table 3. Package Information

Pkg.	Definition	Temperature
x	44 ld. PLCC	0°C to +70°C
x	40 ld. Plastic DIP	0°C to +70°C
x	44 ld. PLCC	-40°C to +85°C

NOTE:

To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

3.0 PINOUT

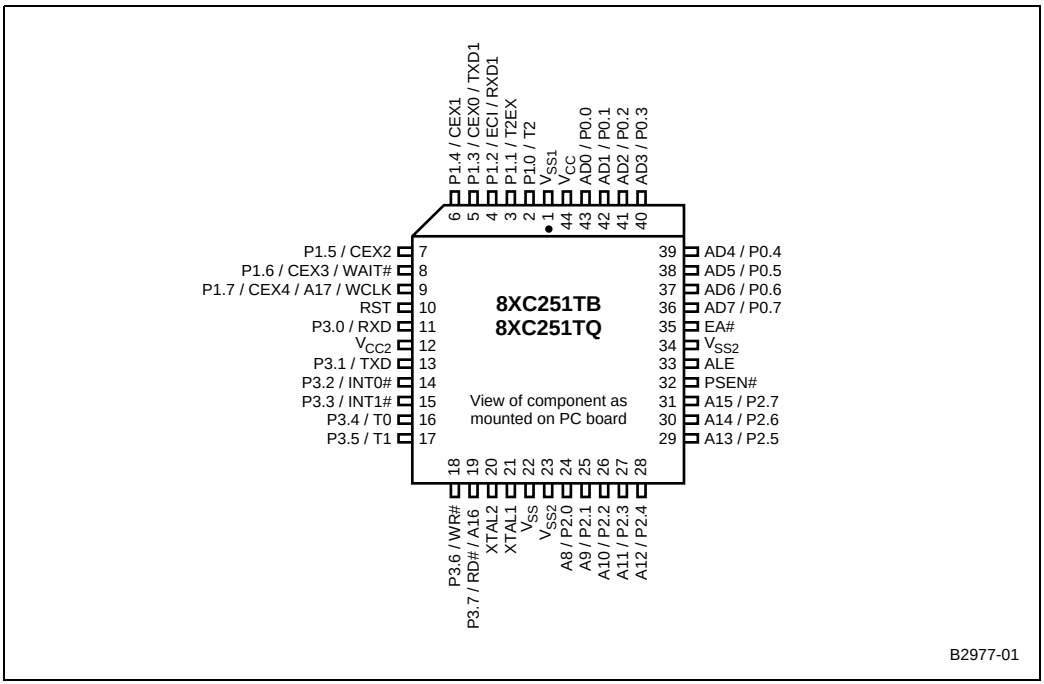


Figure 3. 8xC251TB/TQ 44-pin PLCC Package

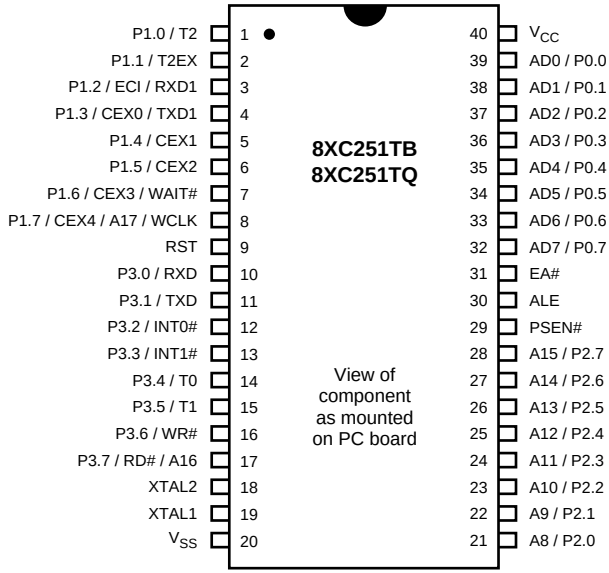


Figure 4. 8xC251TB/TQ 40-pin PDIP Packages

Table 4. 8xC251TB/TQ Pin Assignment

PLCC	DIP	Name
1		V_{SS1}
2	1	P1.0/T2
3	2	P1.1/T2EX
4	3	P1.2/ECI/RXD1
5	4	P1.3/CEX0/TXD1
6	5	P1.4/CEX1
7	6	P1.5/CEX2
8	7	P1.6/CEX3/WAIT#
9	8	P1.7/CEX4/A17/WCLK
10	9	RST
11	10	P3.0/RXD
12		V_{CC2}
13	11	P3.1/TXD
14	12	P3.2/INT0#
15	13	P3.3/INT1#
16	14	P3.4/T0
17	15	P3.5/T1
18	16	P3.6/WR#
19	17	P3.7/RD#/A16
20	18	XTAL2
21	19	XTAL1
22	20	V_{SS}

PLCC	DIP	Name
23		V_{SS2}
24	21	A8/P2.0
25	22	A9/P2.1
26	23	A10/P2.2
27	24	A11/P2.3
28	25	A12/P2.4
29	26	A13/P2.5
30	27	A14/P2.6
31	28	A15/P2.7
32	29	PSEN#
33	30	ALE
34		V_{SS2}
35	31	EA#
36	32	AD7/P0.7
37	33	AD6/P0.6
38	34	AD5/P0.5
39	35	AD4/P0.4
40	36	AD3/P0.3
41	37	AD2/P0.2
42	38	AD1/P0.1
43	39	AD0/P0.0
44	40	V_{CC}

Table 5. 8xC251TB/TQ PLCC/DIP Pin Assignments Arranged by Functional Category

Address & Data		
Name	**PLCC**	**DIP**
AD0/P0.0	43	39
AD1/P0.1	42	38
AD2/P0.2	41	37
AD3/P0.3	40	36
AD4/P0.4	39	35
AD5/P0.5	38	34
AD6/P0.6	37	33
AD7/P0.7	36	32
A8/P2.0	24	21
A9/P2.1	25	22
A10/P2.2	26	23
A11/P2.3	27	24
A12/P2.4	28	25
A13/P2.5	29	26
A14/P2.6	30	27
A15/P2.7	31	28
P3.7/RD#/A16	19	17
P1.7/CEX4/A17/WCLK	9	8

Processor Control		
Name	**PLCC**	**DIP**
P3.2/INT0#	14	12
P3.3/INT1#	15	13
EA#	35	31
RST	10	9
XTAL1	21	18
XTAL2	20	19

Input/Output		
Name	**PLCC**	**DIP**
P1.0/T2	2	1
P1.1/T2EX	3	2
P1.2/ECI/RXD1	4	3
P1.3/CEX0/TXD1	5	4
P1.4/CEX1	6	5
P1.5/CEX2	7	6
P1.6/CEX3/WAIT#	8	7
P1.7/CEX4/A17/WCLK	9	8
P3.0/RXD	11	10
P3.1/TXD	13	11
P3.4/T0	16	14
P3.5/T1	17	15

Power & Ground		
Name	**PLCC**	**DIP**
V_{CC}	44	40
V_{CC2}	12	
V_{SS}	22	20
V_{SS1}	1	
V_{SS2}	23, 34	
EA#	35	31

Bus Control & Status		
Name	**PLCC**	**DIP**
P3.6/WR#	18	16
P3.7/RD#/A16	19	17
ALE	33	30
PSEN#	32	29

4.0 SIGNALS

Table 6. Signal Descriptions (Sheet 1 of 3)

Signal Name	Type	Description	Alternate Function
A17	O	**18th Address Bit (A17).** Output to memory as 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in configuration byte UCONFIG0. See also RD# and PSEN#.	P1.7/CEX4/ WCLK
A16	O	**Address Line 16**. See RD#.	RD#
A15:8[1]	O	**Address Lines**. Upper address lines for the external bus.	P2.7:0
AD7:0[1]	I/O	**Address/Data Lines**. Multiplexed lower address lines and data lines for external memory.	P0.7:0
ALE	O	**Address Latch Enable**. ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	
CEX4:0	I/O	**Programmable Counter Array (PCA) Input/Output Pins**. These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.6:4 P1.7/A17/ WAIT# P1.3/TXD1
EA#	I	**External Access**. Directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is to on-chip ROM if the address is within the range of the on-chip ROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without on-chip ROM, EA# must be strapped to ground.	
ECI	I	**PCA External Clock Input**. External clock input to the 16-bit PCA timer.	P1.2/RXD1
INT1:0#	I	**External Interrupts 0 and 1**. These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#.	P3.3:2
P0.7:0	I/O	**Port 0**. This is an 8-bit, open-drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.7:3	I/O	**Port 1**. This is an 8-bit, bidirectional I/O port with internal pullups.	T2 T2EX ECI/RXD1 CEX3:1 CEX4/A17/ WAIT#/ WCLK CEX0/TXD1
P2.7:0	I/O	**Port 2**. This is an 8-bit, bidirectional I/O port with internal pullups.	A15:8
P3.0 P3.1 P3.3:2 P3.5:4 P3.6 P3.7	I/O	**Port 3**. This is an 8-bit, bidirectional I/O port with internal pullups.	RXD TXD INT1:0# T1:0 WR# RD#/A16

Table 6. Signal Descriptions (Sheet 2 of 3)

Signal Name	Type	Description	Alternate Function
PSEN#	O	**Program Store Enable**. Read signal output. This output is asserted for a memory address range that depends on bits RD0 and RD1 in configuration byte UCONFIG0 (see RD#).	—
RD#	O	**Read or 17th Address Bit (A16).** Read signal output to external data memory or 17th external address bit (A16), depending on the values of bits RD0 and RD1 in configuration byte UCONFIG0. (See PSEN#).	P3.7/A16
RST	I	**Reset**. Reset input to the chip. Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pulldown resistor, which allows the device to be reset by connecting a capacitor between this pin and V_{CC}. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	—
RXD	I/O	**Receive Serial Data**. RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3.	P3.0
RXD1	I/O	**Receive Serial Data 1**. RXD1 sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3 for the 2nd serial port.	P1.2/ECI
T1:0	I	**Timer 1:0 External Clock Inputs**. When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	P3.5:4
T2	I/O	**Timer 2 Clock Input/Output**. For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output.	P1.0
T2EX	I	**Timer 2 External Input**. In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	**Transmit Serial Data**. TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3.	P3.1
TXD1	O	**Transmit Serial Data 1**. TXD1 outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3 for the 2nd serial port.	P1.3/CEX0
V_{CC}	PWR	**Supply Voltage**. Connect this pin to the +5V supply voltage.	—
V_{CC2}	PWR	**Secondary Supply Voltage 2.** This supply voltage connection is provided to reduce power supply noise. Connection of this pin to the +5V supply voltage is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility. (Not available on DIP)	—
V_{SS}	GND	**Circuit Ground**. Connect this pin to ground.	—
V_{SS1}	GND	**Secondary Ground**. This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8xC251TB/TQ as a pin-for-pin replacement for the 8XC51BH, V_{SS1} can be unconnected without loss of compatibility. (Not available on DIP)	—

Table 6. Signal Descriptions (Sheet 3 of 3)

Signal Name	Type	Description	Alternate Function
V_{SS2}	GND	**Secondary Ground 2**. This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8xC251TB/TQ as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility. (Not available on DIP)	—
WAIT#	I	**Real-time Wait State Input.** The real-time WAIT# input is enabled by writing a logical '1' to the WCON.0 (RTWE) bit at S:A7H. During bus cycles, the external memory system can signal 'system ready' to the microcontroller in real time by controlling the WAIT# input signal on the port 1.6 input.	P1.6/CEX3
WCLK	O	Wait Clock Output. The real-time WCLK output is driven at port 1.7 (WCLK) by writing a logical '1' to the WCON.1 (RTWCE) bit at S:A7H. When enabled, the WCLK output produces a square wave signal with a period of one-half the oscillator frequency.	P1.7/CEX4/ A17
WR#	O	Write. Write signal output to external memory.	P3.6
XTAL1	I	**Input to the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.	—
XTAL2	O	**Output of the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	—

NOTE:

The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-pin PLCC and 40-pin DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Memory Signal Selections (RD1:0)

RD1:0	P1.7/CEX/ A17/WCLK	P3.7/RD#/A16	PSEN#	WR#	Features
0 0	A17	A16	Asserted for all addresses	Asserted for writes to all memory locations	256-Kbyte external memory
0 1	P1.7/CEX4/ WCLK	A16	Asserted for all addresses	Asserted for writes to all memory locations	128-Kbyte external memory
1 0	P1.7/CEX4/ WCLK	P3.7 only	Asserted for all addresses	Asserted for writes to all memory locations	64-Kbyte external memory. One additional port pin.
1 1	P1.7/CEX4/ WCLK	RD# asserted for addresses ≤ 7F:FFFFH	Asserted for ≥ 80:0000H	Asserted only for writes to MCS 51 microcontroller data memory locations.	64-Kbyte external memory. Compatible with MCS 51 micro-controllers.

5.0 ADDRESS MAP

Table 8. 8xC251TB/TQ Address Map

Internal Address)	Description	Notes
FF:FFFFH FF:4000H	External Memory except the top eight bytes (FF:FFF8H–FF:FFFFH) which are reserved for the configuration array.	1, 3, 10
FF:3FFFH FF:0000H	External memory or on-chip nonvolatile memory (8Kbytes FF:0000H - FF:1FFFH, 16Kbytes FF:0000H - FF:3FFFH).	3, 4, 5
FE:FFFFH FE:0000H	External Memory	3
FD:FFFFH 02:0000H	Reserved	6
01:FFFFH 01:0000H	External Memory	3
00:FFFFH 00:E000H	External memory or with configuration bit EMAP# = 0, addresses in this range access on-chip code memory in region FF: (16 Kbyte devices only).	5, 7
00:DFFFH 00:0420H	External Memory	7
00:041FH 00:0080H	On-chip RAM (512 bytes 00:0020H - 00:021FH, 1024 bytes 00:0020H - 00:041FH)	7
00:007FH 00:0020H	On-chip RAM	8
00:001FH 00:0000H	Storage for R0–R7 of Register File	2, 9

NOTES:

1. 18 address lines are bonded out (A15:0, A16:0, or A17:0 selected during chip configuration).
2. The special function registers (SFRs) and the register file have separate internal address spaces.
3. Data in this area is accessible by indirect addressing only.
4. Devices reset into internal or external starting locations depending on the state of EA# and configuration byte information See EA#.
5. The 16-Kbyte ROM devices allow internal locations FF:2000H–FF:3FFFH to map into region 00:. In this case, if EA# = 1, a data read to 00:E000H–00:FFFFH is redirected to internal ROM (see bit 1 in UCONFIG0). This is not available for 8-Kbyte ROM devices.
6. This reserved area returns indeterminate values.
7. Data is accessible by direct and indirect addressing.
8. Data is accessible by direct, indirect, and bit addressing.
9. Data is accessible by direct, indirect, and register addressing.
10. Eight addresses at the top of all external memory maps are reserved for current and future device configuration byte information.

6.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65°C to +150°C
Voltage: EA# Pin with respect to V_{SS} ..... 0 V to +13.0 V
Voltage: Any other Pin with respect to V_{SS}... -0.5 V to +6.5 V
I_{OL} per I/O Pin..... 15 mA
Power Dissipation ..... 1.5 W

OPERATING CONDITIONS

T_A (Ambient Temperature Under Bias):
Commercial ..... 0°C to +70°C
Express..... -40°C to +85°C
V_{CC} (Digital Supply Voltage) ..... 4.5 V to 5.5 V
V_{SS} ..... 0 V

NOTE: Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

NOTICE: This document contains information on products being sampled or in the initial production phase of development. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

6.1 D.C. Characteristics

Parameter values apply to all devices unless otherwise indicated.

Table 9. DC Characteristics at V_{CC} = 4.5 – 5.5 V (Sheet 1 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#)	-0.5		0.2 V_{CC} – 0.1	V	
V_{IL1}	Input Low Voltage (EA#)	0		0.2 V_{CC} – 0.3	V	
V_{IH}	Input High Voltage (except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Port 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA I_{OL} = 1.6 mA I_{OL} = 3.5 mA (Note 1, Note 2)
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)			0.3 0.45 1.0	V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA (Note 1, Note 2)
V_{OH}	Output High Voltage (Port 1, 2, 3, ALE, PSEN#)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA (Note 3)

Table 9. DC Characteristics at V_{CC} = 4.5 – 5.5 V (Sheet 2 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Address)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
V_{OH2}	Output High Voltage (Port 2 in External Address during Page Mode)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)			-50	µA	V_{IN} = 0.45 V
I_{LI}	Input Leakage Current (Port 0)			+/-10	µA	0.45 < V_{IN} < V_{CC}
I_{TL}	Logical 1-to-0 Transition Current (Port 1, 2, 3)			-650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pulldown Resistor	40		225	kΩ	
C_{IO}	Pin Capacitance		10 (Note 4)		pF	F_{OSC} = 24 MHz T_A = 25 °C
I_{PD}	Powerdown Current		10 (Note 4)	20	µA	
I_{DL}	Idle Mode Current		35 (Note 4)	44	mA	F_{OSC} = 24 MHz
I_{CC}	Operating Current		70 (Note 4)	83	mA	F_{OSC} = 24 MHz

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:
   - Maximum I_{OL} per port pin:10 mA
   - Maximum I_{OL} per 8-bit port:
     port 0 26 mA
     ports 1–3 15 mA
   - Maximum Total I_{OL} for all output pins 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.

Typical values are obtained using V_{CC} = 5.0, T_A = 25°C and are not guaranteed.

6.2 Definition of AC Symbols

Table 10. AC Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	RD#/PSEN#
W	WR#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

6.3 A.C. Characteristics

Test Conditions: Capacitive load on all pins = 50 pF.

Table 11 lists AC timing parameters for the with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and/or by extending ALE. In the table, Notes 2 and 3 mark parameters affected by an

ALE wait state, and Notes 4 and 5 mark parameters affected by a PSEN#/RD#/WR# wait state.

Figure 6 through Figure 8 show the bus cycles with the timing parameters.

Table 11. AC Characteristics (Sheet 1 of 4)

Symbol	Parameter	@ Max F_{OSC} (1)		F_{OSC} Variable		Units
		Min	Max	Min	Max	
F_{OSC}	XTAL1 Frequency	N/A	N/A	0	24	MHz
T_{OSC}	$1/F_{OSC}$ @ 16MHz @ 24MHz	N/A	N/A	 62.5 41.7		ns
T_{LHLL}	ALE Pulse Width @ 16MHz @ 24MHz	 55.5 34.7		 (0.5+M) $2T_{OSC}$-7		ns (3)
T_{AVLL}	Address Valid to ALE Low @ 16MHz @ 24MHz	 49.5 28.7		 (0.5+M) $2T_{OSC}$-13		ns (3)
T_{LLAX}	Address Hold after ALE Low @ 16MHz @ 24MHz	 10 10		 10		ns (4)
T_{LLAXA}	Address Hold after ALE Low @ 16MHz @ 24MHz	 20 20		 20		ns (5)
T_{RLRH}	RD# or PSEN# Pulse Width @ 16MHz @ 24MHz	 115 73.4		 (1+N) $2T_{OSC}$-10		ns (3,4)
T_{RLRHA}	RD# or PSEN# Pulse Width @ 16MHz @ 24MHz	 93 51.4		 (1+N) $2T_{OSC}$-32		ns (3,5)
T_{WLWH}	WR# Pulse Width @ 16MHz @ 24MHz	 115 73.4		 (1+N) $2T_{OSC}$-10		ns (3,4)
T_{WLWHA}	WR# Pulse Width @ 16MHz @ 24MHz	 93 51.4		 (1+N) $2T_{OSC}$-32		ns (3,5)

Table 11. AC Characteristics (Sheet 2 of 4)

Symbol	Parameter	@ Max F_{OSC} (1)		F_{OSC} Variable		Units
		Min	Max	Min	Max	
T_{LLRL}	ALE Low to RD# or PSEN# Low @ 16MHz @ 24MHz	 10 10		 10		ns (4)
T_{LLRLA}	ALE Low to RD# or PSEN# Low @ 16MHz @ 24MHz	 20 20		 20		ns (5)
T_{LHAX}	ALE High to Address Hold @ 16MHz @ 24MHz	 98 56.4		 (1+M) $2T_{OSC}$-27		ns (3,4)
T_{LHAXA}	ALE High to Address Hold @ 16MHz @ 24MHz	 77.5 56.7		 (0.5+M) $2T_{OSC}$+15		ns (3,5)
T_{RLDV}	RD# or PSEN# Low to Valid Data/Instruction In @ 16MHz @ 24MHz		 95 53.4		 (1+N) $2T_{OSC}$-30	ns (3,4)
T_{RLDVA}	RD# or PSEN# Low to Valid Data/Instruction In @ 16MHz @ 24MHz		 75 33.4		 (1+N) $2T_{OSC}$-50	ns (3,5)
T_{RHDX}	Data/Instruction Hold after RD# or PSEN# High @ 16MHz @ 24MHz	 0 0		 0		ns
T_{RLAZ}	RD#/PSEN# Low to Address Float @ 16MHz @ 24MHz		 10 10		 10	ns
T_{RHDZ1}	Instruction Float after PSEN# or RD# high @ 16MHz @ 24MHz		 10 10		 10	ns (4)
T_{RHDZ1A}	Instruction Float after PSEN# or RD# high @ 16MHz @ 24MHz		 57.5 36.7		 T_{OSC}-5	ns (5)
T_{RHDZ2}	Data Float after PSEN# or RD# high @ 16MHz @ 24MHz		 135 93.4		 $2T_{OSC}$+10	ns (4)
T_{RHDZ2A}	Data Float after PSEN# or RD# high @ 16MHz @ 24MHz		 182.5 120.1		 $3T_{OSC}$-5	ns (5)

Table 11. AC Characteristics (Sheet 3 of 4)

Symbol	Parameter	@ Max F_{OSC} (1)		F_{OSC} Variable		Units
		Min	Max	Min	Max	
T_{RHLH2}	RD# or PSEN# High to ALE High (data) @ 16MHz @ 24MHz	 135 93.4		 $2T_{OSC}$+10		ns (4)
T_{RHLH2A}	RD# or PSEN# High to ALE High (data) @ 16MHz @ 24MHz	 180.5 118.1		 $3T_{OSC}$-7		ns (5)
T_{RHLH1}	RD# or PSEN# High to ALE High (Instruction) @ 16MHz @ 24MHz	 10 10		 10		ns (4)
T_{RHLH1A}	RD# or PSEN# High to ALE High (Instruction) @ 16MHz @ 24MHz	 55.5 34.7		 T_{OSC}-7		ns (5)
T_{WHLH}	WR# High to ALE Low @ 16MHz @ 24MHz	 135 93.4		 $2T_{OSC}$+10		ns (4)
T_{WHLHA}	WR# High to ALE Low @ 16MHz @ 24MHz	 180.5 118.1		 $3T_{OSC}$-7		ns (5)
T_{AVDV1}	Address (mux'd) valid to Valid Data/ Instruction In @ 16MHz @ 24MHz		 190 106.8		 (2+M+N) $2T_{OSC}$-60	ns (3,4)
T_{AVDV1A}	Address (mux'd) valid to Valid Data/ Instruction In @ 16MHz @ 24MHz		 159.5 97.1		 (1.5+M+N) $2T_{OSC}$-28	ns (3,4)
T_{AVDV2}	Address (demux'd) valid to Valid Data/Instruction In @ 16MHz @ 24MHz		 212 128.8		 (2+M+N) $2T_{OSC}$-38	ns (3)
T_{AVDV3}	Address (P0)Valid to Valid Instruction In @ 16MHz @ 24MHz		 65 23.4		 (1+N) $2T_{OSC}$-60	ns (3)
T_{AVRL}	Address Valid to RD# or PSEN# Low @ 16MHz @ 24MHz	 85 43.4		 (1+M) $2T_{OSC}$-40		ns (3,4)
T_{AVRLA}	Address Valid to RD# or PSEN# Low @ 16MHz @ 24MHz	 72.5 51.7		 (0.5+M) $2T_{OSC}$+10		ns (3,5)

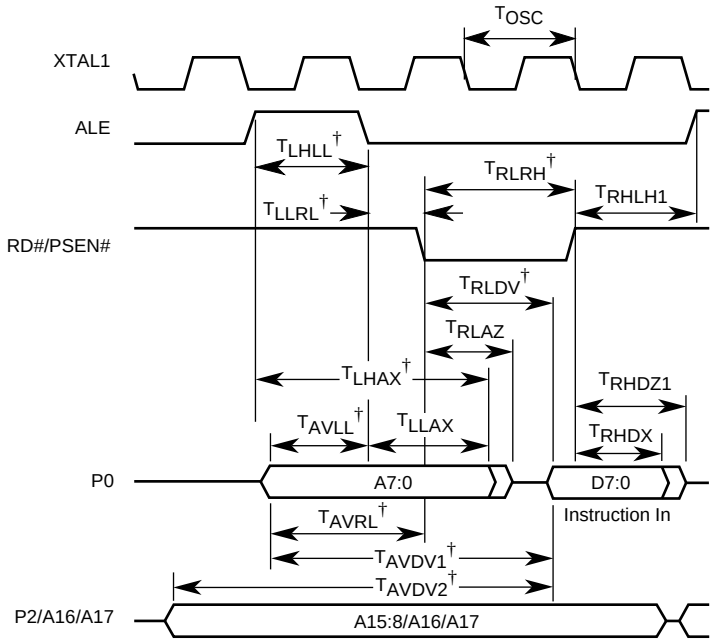
Table 11. AC Characteristics (Sheet 4 of 4)

Symbol	Parameter	@ Max F_{OSC} (1)		F_{OSC} Variable		Units
		Min	Max	Min	Max	
T_{AVWL1}	Address (mux'd) Valid to WR# Low @ 16MHz @ 24MHz	 85 43.4		 (1+M) $2T_{OSC}$-40		ns (3,4)
T_{AVWL1A}	Address (mux'd) Valid to WR# Low @ 16MHz @ 24MHz	 72.5 51.7		 (0.5+M) $2T_{OSC}$+10		ns (3,5)
T_{AVWL2}	Address (demux'd) Valid to WR# Low @ 16MHz @ 24MHz	 108 66.4		 (1+M) $2T_{OSC}$-17		ns (3,4)
T_{AVWL2A}	Address (demux'd) Valid to WR# Low @ 16MHz @ 24MHz	 135 93.4		 (1+M) $2T_{OSC}$+10		ns (3,5)
T_{WHQX}	Data Hold after WR# High @ 16MHz @ 24MHz	 49.5 28.7		 T_{OSC}-13		ns
T_{QVWH}	Data Valid to WR# High @ 16MHz @ 24MHz	 110 68.4		 (1+N) $2T_{OSC}$-15		ns (3)
T_{WHAX}	WR# High to Address Hold @ 16MHz @ 24MHz	 112 70.4		 $2T_{OSC}$-13		ns

NOTES:

1. 24 MHz XTAL Frequency.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M = number of wait states (0 or 1) for ALE and N = Number of wait states (0,1,2 or 3) for RD#/PSEN#/WR#.
4. Device configured with the default data float timing for fast memory interface (EDF# = 1).
5. Device configured with extended data float timing for slow memory interface (EDF# = 0).

6.3.1 External Bus Cycles, Nonpage Mode



† The value of this parameter depends on wait states. See the table of AC characteristics.

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Figure 5. External Bus Cycle: Code Fetch (Nonpage Mode)

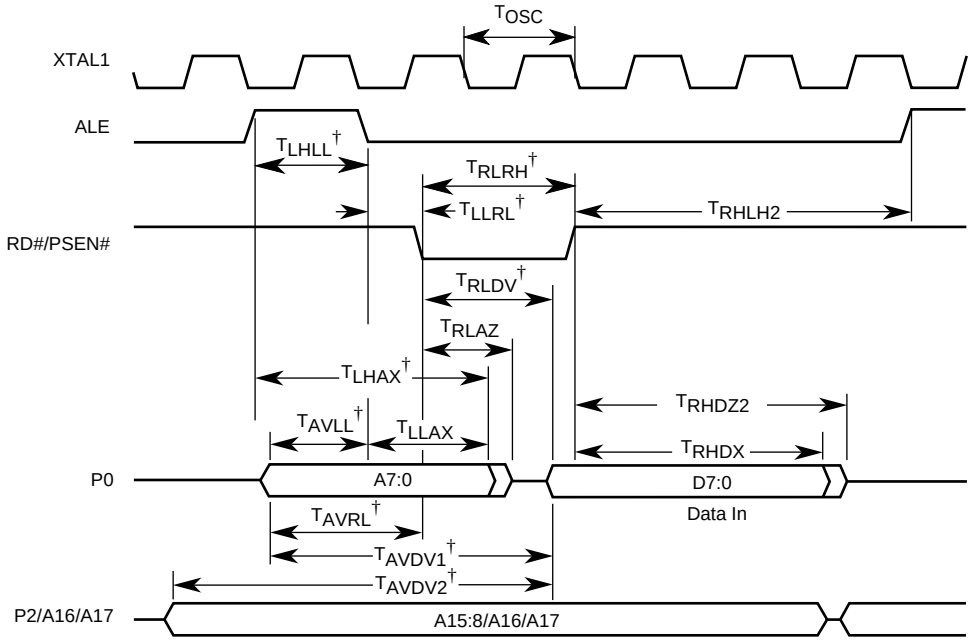


Figure 6. External Bus Cycle: Data Read (Nonpage Mode)

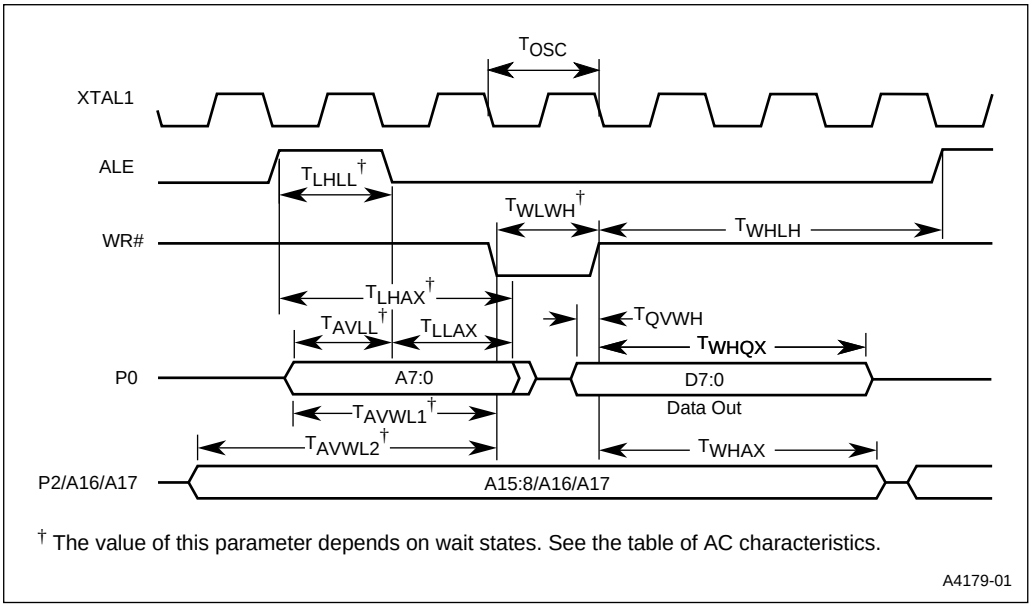
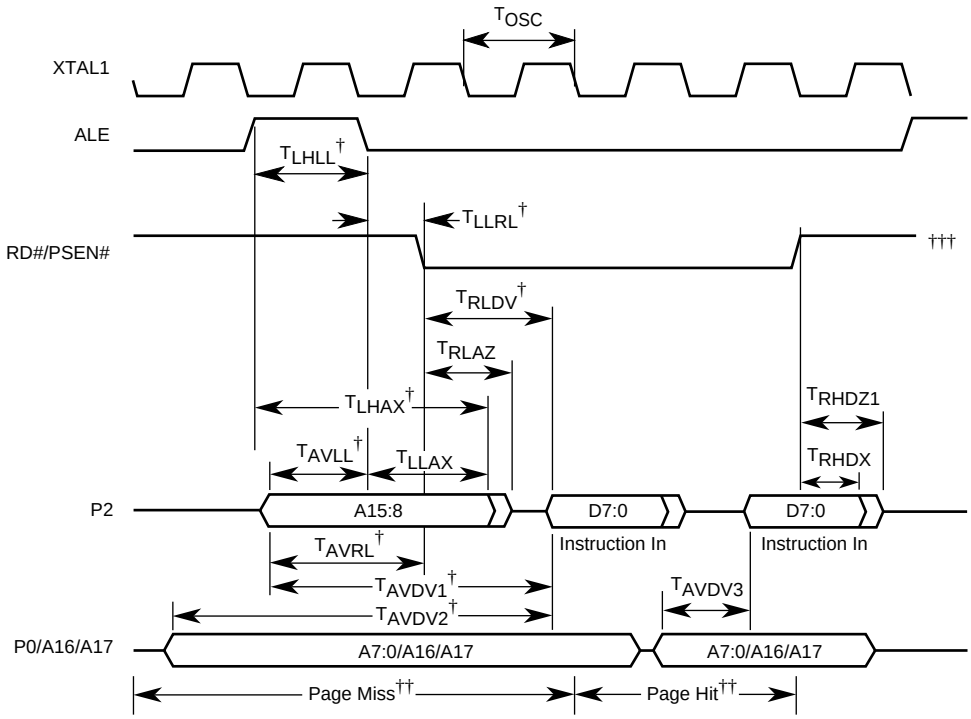


Figure 7. External Bus Cycle: Data Write (Nonpage Mode)

6.3.2 External Bus Cycles, Page Mode



† The value of this parameter depends on wait states. See the table of AC characteristics.

†† A page hit (i.e., a code fetch to the same 256-byte "page" as the previous code fetch) requires one state ($2T_{OSC}$); a page miss requires two states ($4T_{OSC}$).

††† During a sequence of page hits, PSEN# remains low until the end of the last page-hit cycle.

A4213-02

Figure 8. External Bus Cycle: Code Fetch (Page Mode)

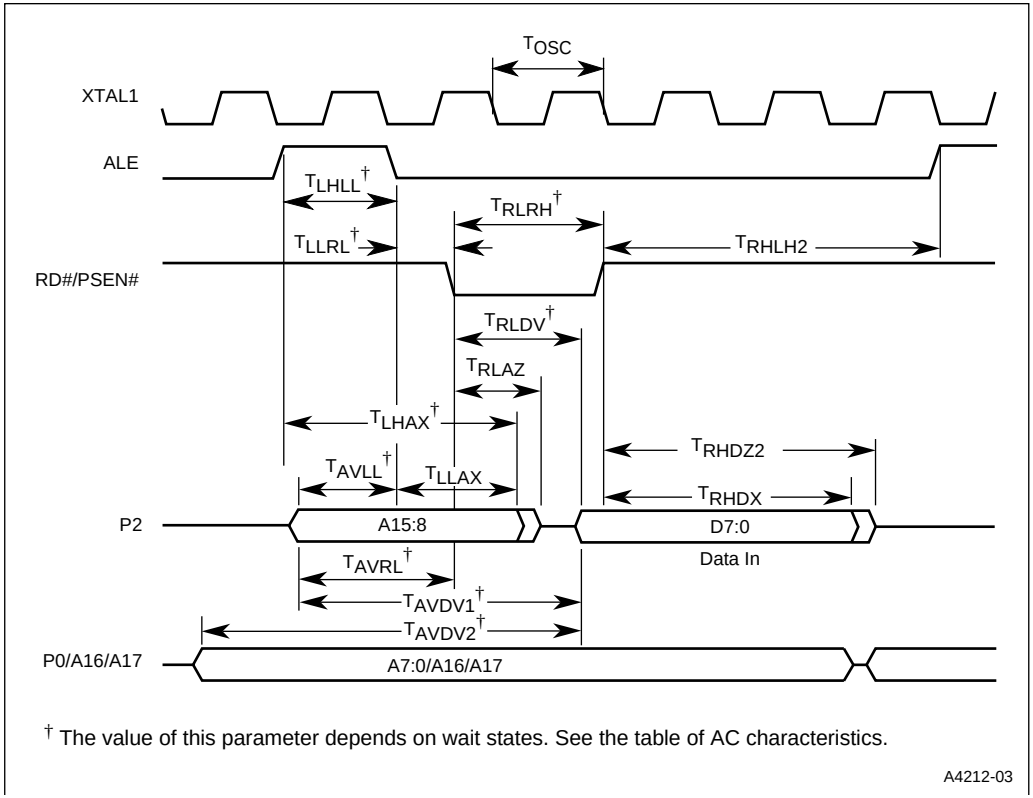


Figure 9. External Bus Cycle: Data Read (Page Mode)

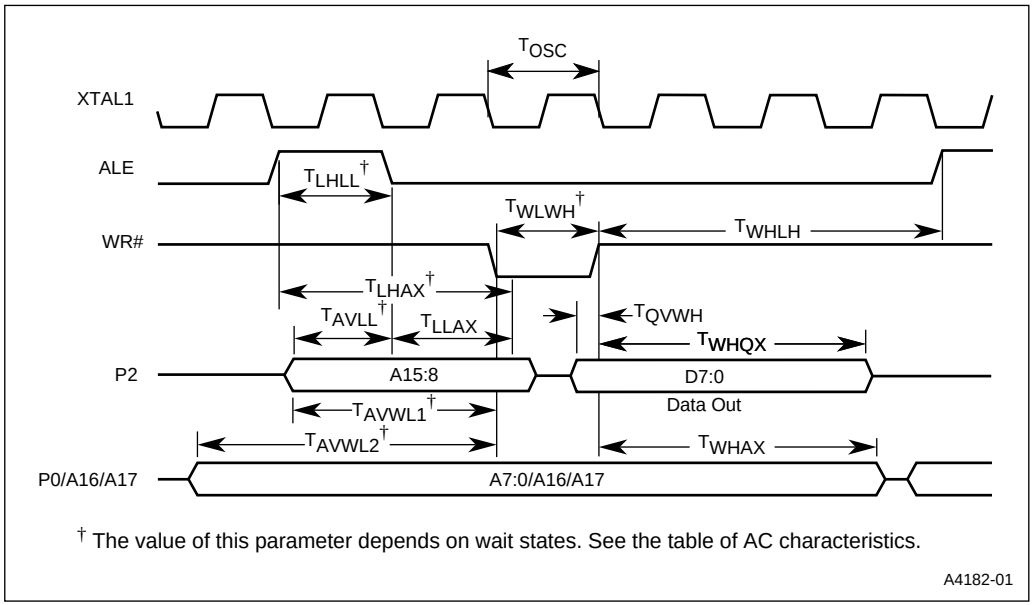


Figure 10. External Bus Cycle: Data Write (Page Mode)

6.3.3 Definition of Real-Time Wait Symbols

Table 12. Real-time Wait Timing Symbol Definitions

Signals	
A	Address
D	Data
C	WCLK
Y	WAIT#
W	WR#
R	RD#/PSEN#

Conditions	
L	Low
X	Hold
V	Setup

6.3.4 External Bus Cycles, Real-Time Wait States

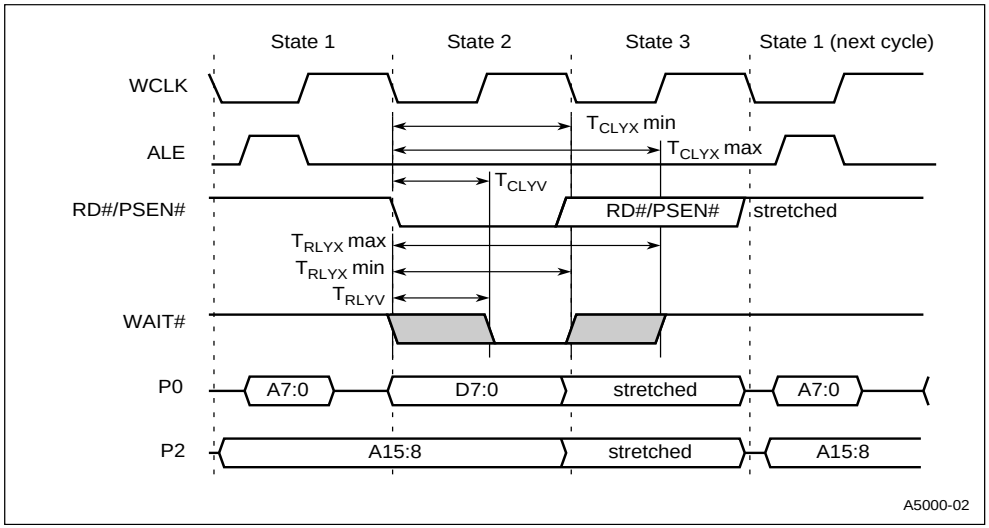


Figure 11. External Bus Cycle: Code Fetch/Data Read (Nonpage Mode)

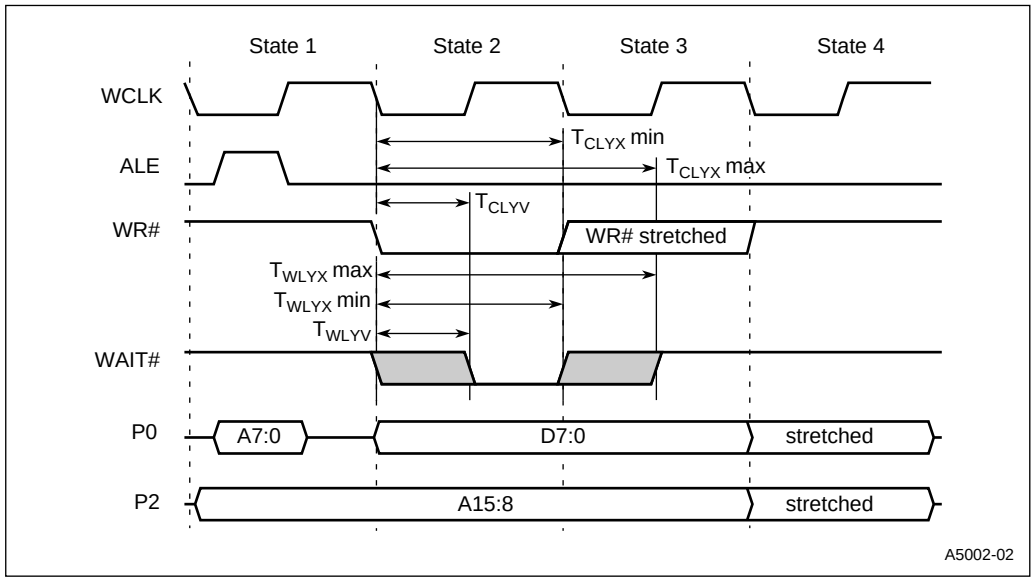


Figure 12. External Bus Cycle: Data Write (Nonpage Mode)

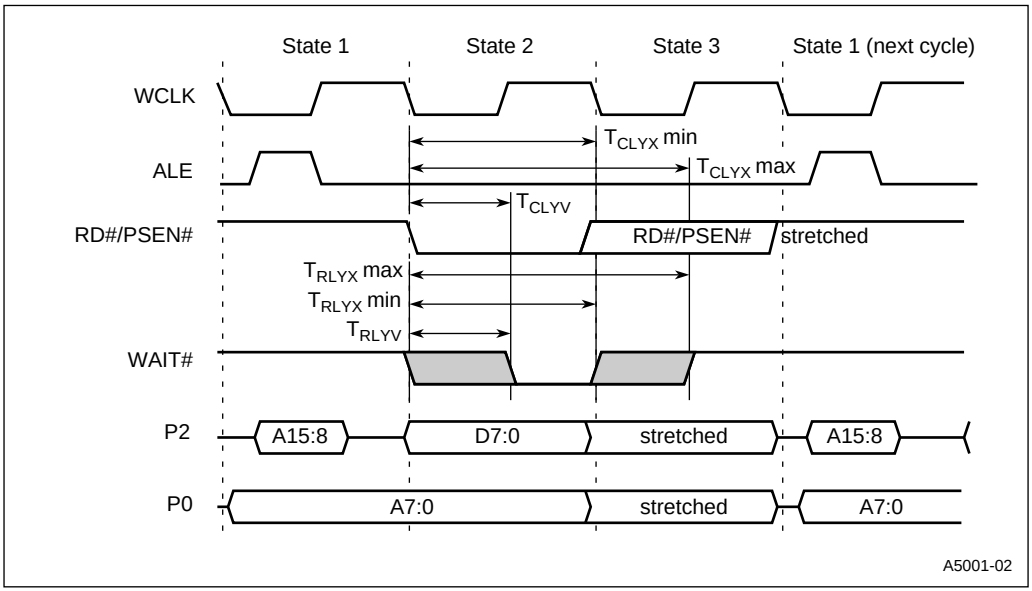


Figure 13. External Bus Cycle: Code Fetch/Data Read (Page Mode)

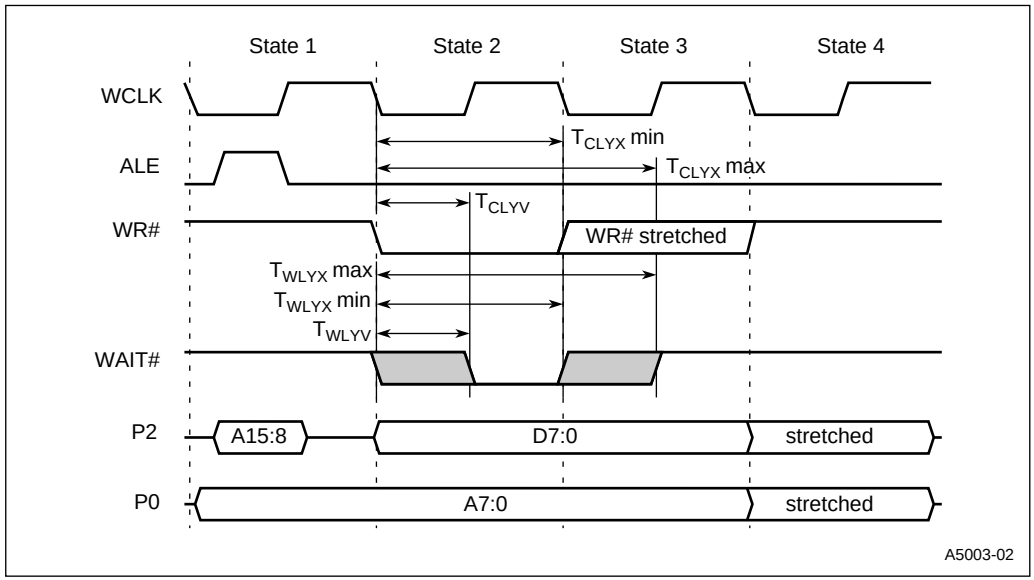


Figure 14. External Bus Cycle: Data Write (Page Mode)

Table 13. Real-Time Wait AC Timing

Symbol	Parameter	Min	Max	Units
T_{CLYV}	Wait Clock Low to Wait Set-up	0	T_{OSC} – 13	ns
T_{CLYX}	Wait Hold after Wait Clock Low	(2W)T_{OSC} + 5	(1+2W)T_{OSC} – 20	ns (1)
T_{RLYV}	PSEN#/RD# Low to Wait Set-up	0	T_{OSC} – 13	ns
T_{RLYVA}	PSEN#/RD# Low to Wait Set-up	0	T_{OSC} – 35	ns (2)
T_{RLYX}	Wait Hold after PSEN#/RD# Low	(2W)T_{OSC} + 5	(1+2W)T_{OSC} – 20	ns (1)
T_{WLYV}	WR# Low to Wait Set-up	0	T_{OSC} – 13	ns
T_{WLYVA}	WR# Low to Wait Set-up	0	T_{OSC} – 35	ns (2)
T_{WLYX}	Wait Hold after WR# Low	(2W)T_{OSC} + 5	(1+2W)T_{OSC} – 20	ns (1)

NOTES:
1. W = 0, 1, 2 — is the number of real time wait states.
2. Device configured with the extended data float timing.

6.4 AC Characteristics — Serial Port, Shift Register Mode

Table 14. Serial Port Timing — Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Cycle Time	$12T_{OSC}$		ns
T_{QVSH}	Output Data Setup to Clock Rising Edge	$10T_{OSC} - 133$		ns
T_{XHQX}	Output Data hold after Clock Rising Edge	$2T_{OSC} - 117$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		$10T_{OSC} - 133$	ns

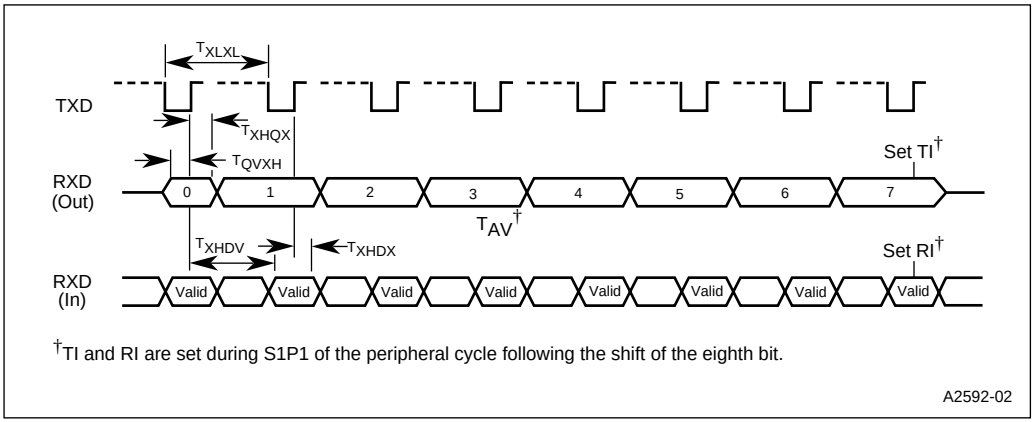


Figure 15. Serial Port Waveform — Shift Register Mode

6.5 External Clock Drive

Table 15. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency (F_{OSC})		24	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		10	ns
T_{CHCL}	Fall Time		10	ns

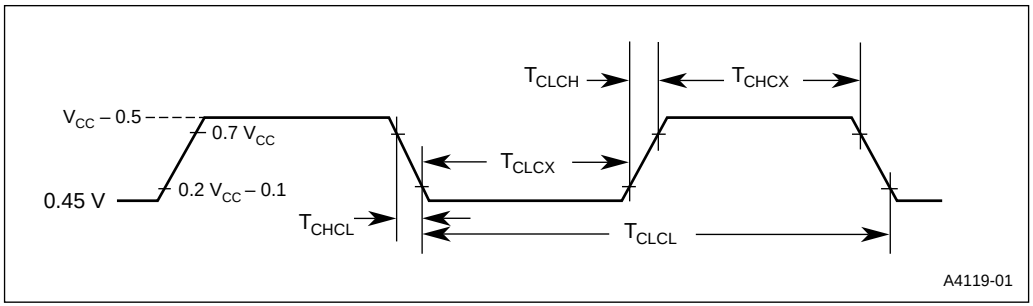


Figure 16. External Clock Drive Waveforms

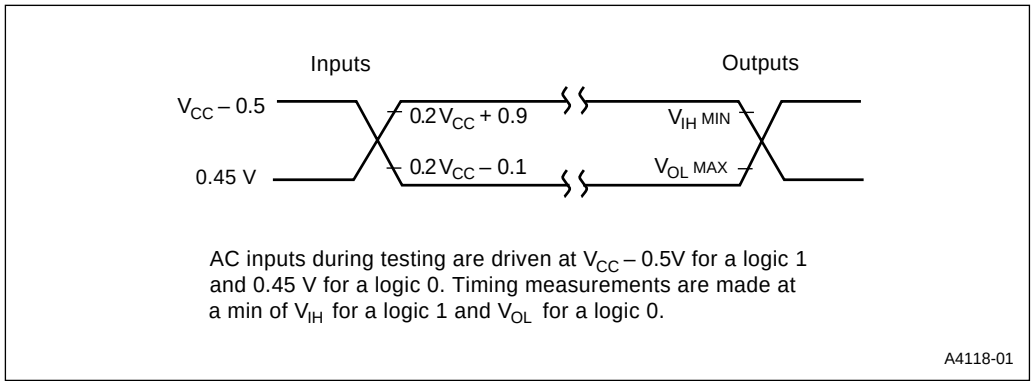
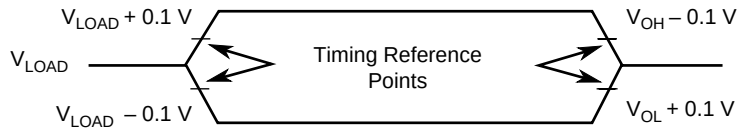


Figure 17. AC Testing Input, Output Waveforms



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with I_{OL}/I_{OH} = ± 20 mA.

A4117-01

Figure 18. Float Waveforms

7.0 THERMAL CHARACTERISTICS

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 16. Thermal Characteristics

Package Type	Θ_{JA}	Θ_{JC}
44-pin PLCC	46°C/W	16°C/W
40-pin PDIP	45°C/W	16°C/W