512Kx32 CMOS High Speed Static RAM

FEATURES

- DSP Memory Solution
  - Motorola DSP96002
  - Analog SHARC DSP
  - Texas Instruments TMS320C3x, TMS320C4x
- Random Access Memory Array
  - Fast Access Times: 12*, 15, 17, and 20ns
  - TTL Compatible I/O
  - Fully Static, No Clocks
- Surface Mount Package
  - 68 Lead PLCC, No. 99 JEDEC M0-47AE
  - Small Footprint, 0.990 Sq. In.
  - Multiple Ground Pins for Maximum Noise Immunity
- Single +5V (±5%) Supply Operation

* This product is subject to change without notice.

DESCRIPTION

The EDI8L32512C is a high speed, 5V, 16Mb SRAM. The device is available with access times of 12, 15, 17 and 20ns allowing the creation of a no wait state DSP memory solution. The high speed, 5v supply voltage and control lines make the divice ideal for creating floating point DSP memory solutions.

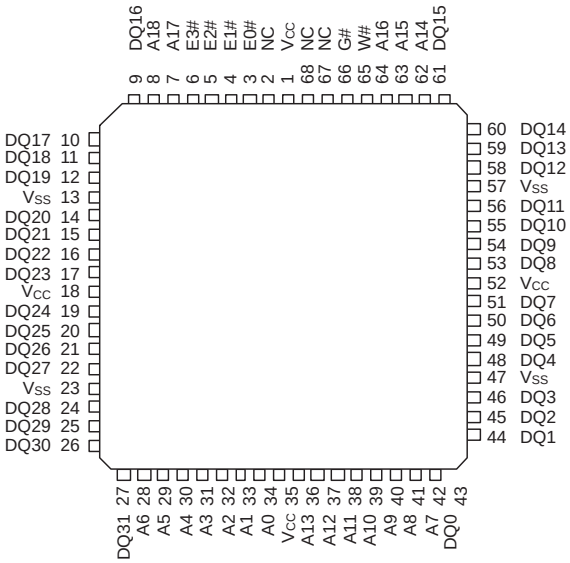
The device can be configured as a 512K x 32 and used to create a single chip external data memory solution for TI's TMS320C30/C31 (Figure 8), TMS320C32 (Figure 9) or TMS320C4x (Figure 10), Motorola's DSP96002 and Analog's SHARC DSP (Figure 11). Alternatively, the device's chip enables can be used to configure it as a 1M x 16. A 1M x 48 program memory array for Analog's SHARC DSP is created using three devices (Figure 12). If this memory is too deep, two 512K x 24s (EDI8L24512C) can be used to create a 512K x 48 array or two 128K x 48 array.

The device provides a 56% space savings when compared to four 512K x 8, 36 pin SOJs. In addition the EDI8L32512C has only a 10pF load on the data lines vs. 32pF for four plastic SOJs.

The device provides a memory upgrade of the EDI8L32256C (256K x 32) or the EDI8L32128C (128K x 32). For additional upgrade information see Figure 13.

Note: Solder Reflow Temperature should not exceed 230°C for 10 seconds.

FIGURE 1 – PIN CONFIGURATION



Note: For memory upgrade information, refer to Pg 8, Fig 13 "EDI MCM-L Upgrade Path"

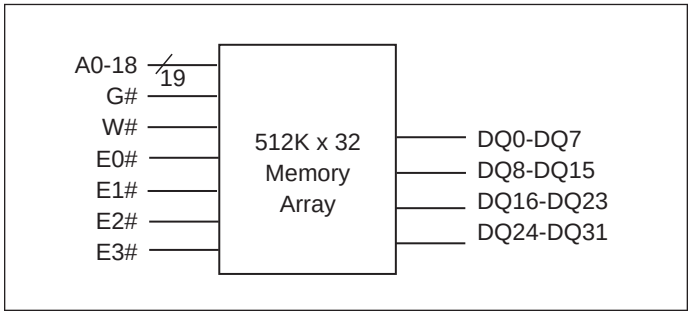
PIN NAMES

A0-A18	Address Inputs
E0#-E3#	Chip Enables
W#	Write Enables
G#	Output Enable
DQ0-DQ31	Common Data Input/Output
V_{CC}	Power (+5V ±10%)
V_{SS}	Ground
NC	No Connection

BYTE CONTROL TABLE

Chip Enable	Byte Control
E0#	DQ0-7
E1#	DQ8-15
E2#	DQ16-23
E3#	DQ24-31

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature t_A (Ambient) Commercial Industrial	 0°C to +70°C -40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	5.0 Watts
Output Current	20 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	--	V_{CC}+0.5V	V
Input Low Voltage	V_{IL}	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 2

Note: For t_{EHQZ},t_{GHQZ} and t_{WLQZ}, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Max		Units
				12-25	17/20	ns
Operating Power Supply Current	I_{CC1}	W# = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle		800	720	mA
Standby (TTL) Power Supply Current	I_{CC2}	E# ≥ V_{IH}, V_{IN} ≤ V_{IL} or V_{IN} ≥V_{IH}, f = 0MHz		200	200	mA
Full Standby Power Supply Current CMOS	I_{CC3}	E# ≥ V_{CC}-0.2V V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V		40	40	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		±10		µA
Output Leakage Current	I_{LO}	V I/O = 0V to V_{CC}		±10		µA
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		0.4		V

TRUTH TABLE

G#	E#	W#	Mode	Output	Power
X	H	X	Standby	HIGH Z	I_{CC2} I_{CC3}
H	L	H	Output Deselect	HIGH Z	I_{CC1}
L	L	H	Read	D_{OUT}	I_{CC1}
X	L	L	Write	D_{IN}	I_{CC1}

CAPACITANCE

(f=1.0MHz, V_{IN}=V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	10	pF
Write & Output Enable Line	W#, G#	30	pF
Chip Enable Line	E0#-E3#	8	pF

FIGURE 2 – AC TEST CONDITIONS

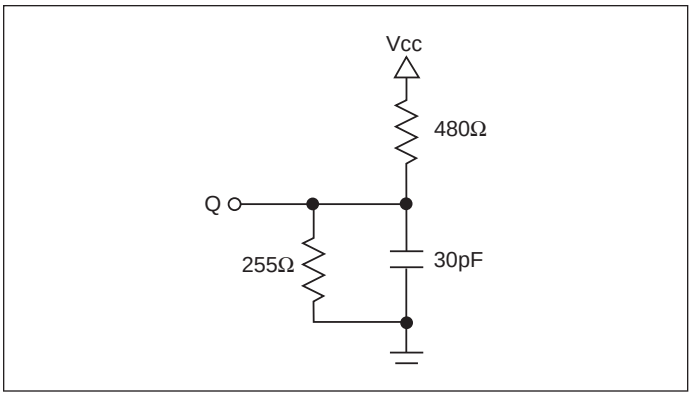
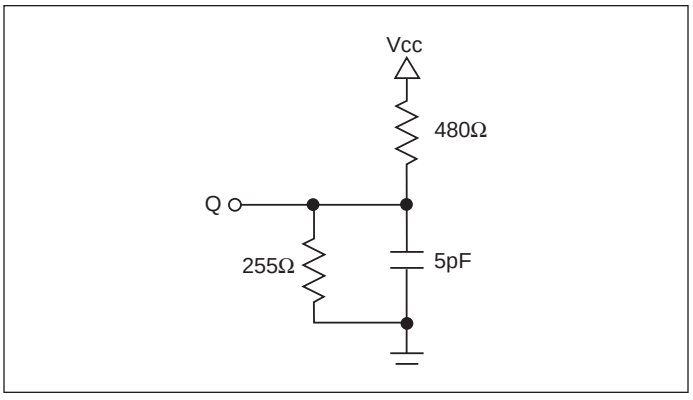


FIGURE 3 – AC TEST CONDITIONS



AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		12ns*		15ns		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	12		15		17		20		ns
Address Access Time	t_{AVQV}	t_{AA}		12		15		17		20	ns
Chip Enable Access	t_{ELQV}	t_{ACS}		12		15		17		20	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		6		7		9		9	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		6		7		9		9	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		0		ns
Output Disable to Output in High Z (1)	t_{GHQZ}	t_{OHZ}		6		7		9		9	ns

*Advanced Information

Note: 1. Parameter guaranteed, but not tested.

FIGURE 4 – READ CYCLE 1 – W# High, G#, E# Low

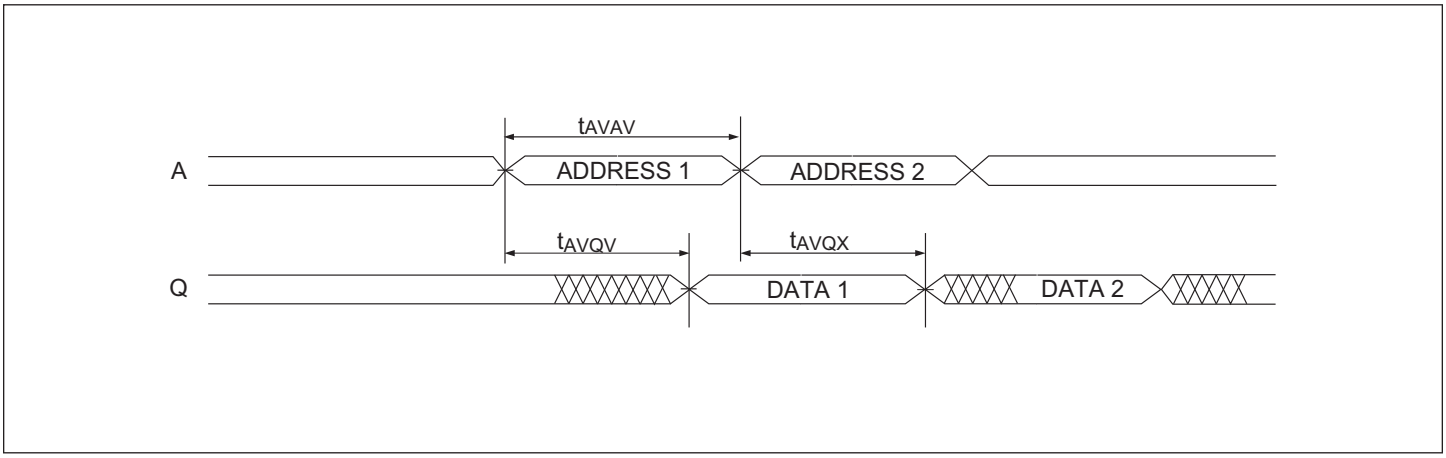
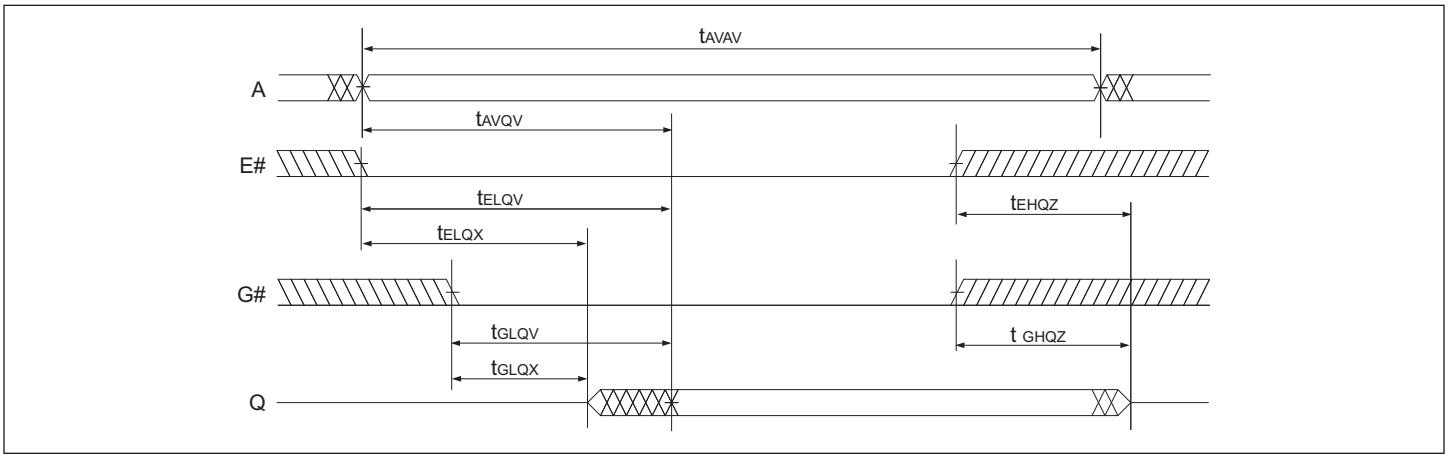


FIGURE 5 – Read Cycle 2 – W# High



AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol		12ns		15ns		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	12		15		17		20		ns
Chip Enable to End of Write	t_{ELWH} t_{ELEH}	t_{CW} t_{CW}	8 8		10 10		11 11		12 12		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AVEH}	t_{AW} t_{AW}	8 8		10 10		11 11		12 12		ns ns
Write Pulse Width	t_{WLWH} t_{ELEH}	t_{WP} t_{WP}	8 10		10 12		11 13		12 14		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} t_{WR}	0 0		0 0		0 0		0 0		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	0 0		0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	6	0	7	0	8	0	9	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	6 6		7 7		8 8		9 9		ns ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		3		ns

*Advanced Information.
Note 1: Parameter guaranteed, but not tested.

FIGURE 6 – WRITE CYCLE 1 – W# CONTROLLED

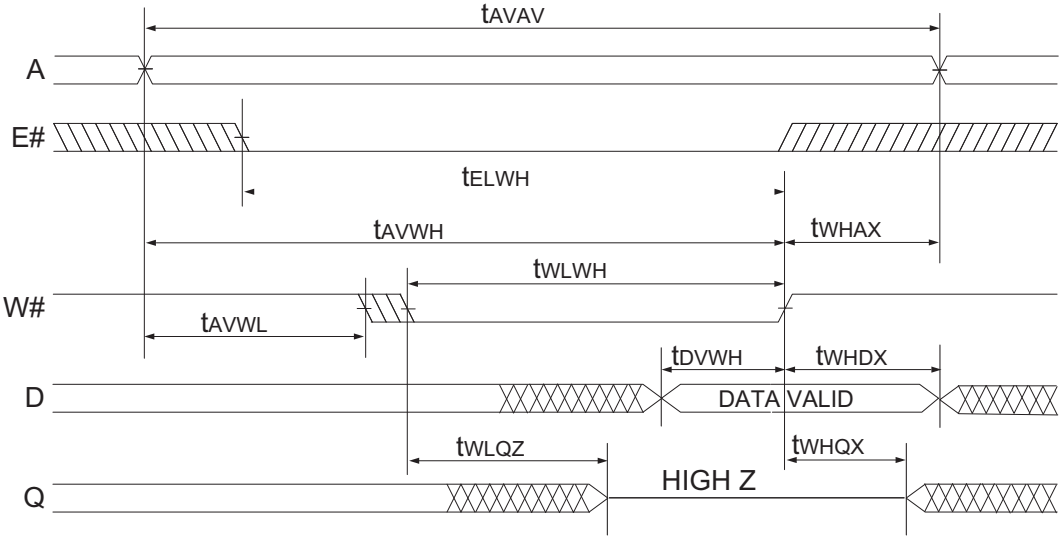
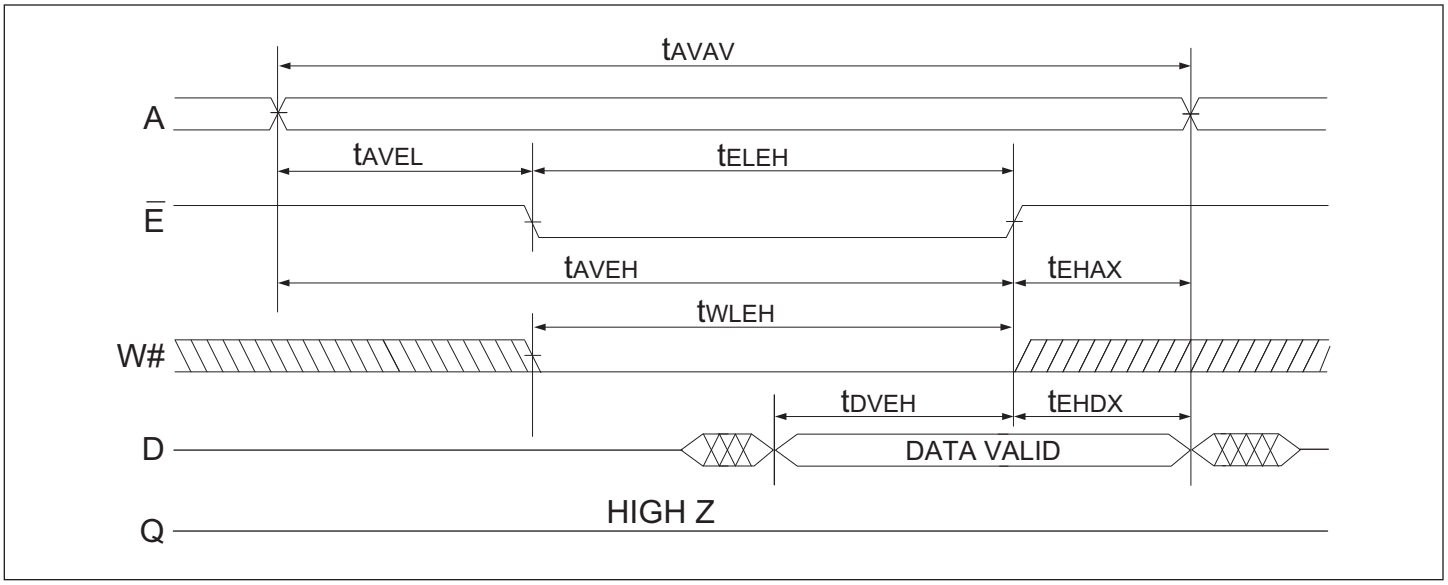


FIGURE 7 – WRITE CYCLE 2 – E# CONTROLLED



ORDERING INFORMATION

Commercial (0°C to +70°C)

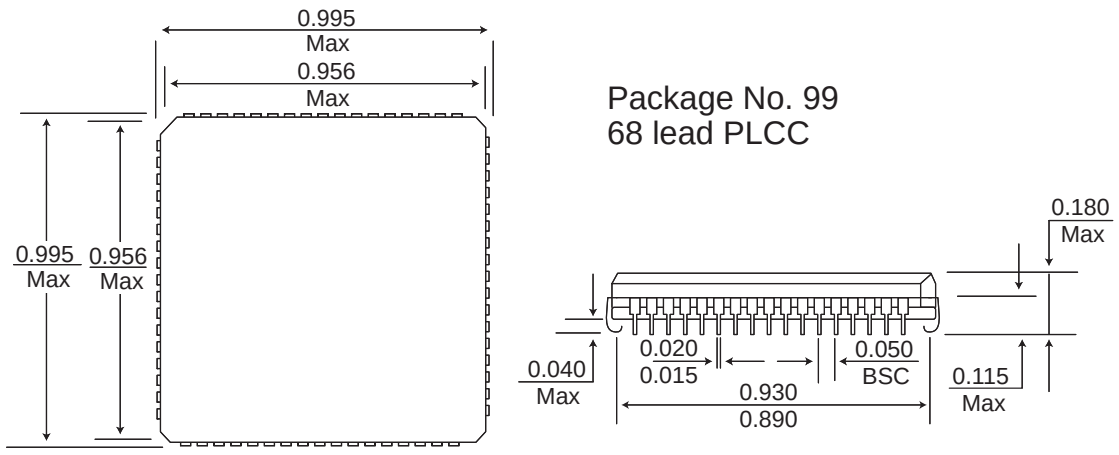
Part Number	Speed (ns)	Package No.
EDI8L32512C12AC*	12	99
EDI8L32512C15AC	15	99
EDI8L32512C17AC	17	99
EDI8L32512C20AC	20	99

Industrial (-40°C to +85°C)

Part Number	Speed (ns)	Package No.
EDI8L32512C15AI*	15	99
EDI8L32512C17AI	17	99
EDI8L32512C20AI	20	99

PACKAGE DRAWING – PACKAGE NO. 99 – 68 LEAD PLCC – JEDEC MO-47AE

Weight = 4.2g – Theta J_A = 40°C/W – Theta J_C = 15°C/W



Coplanarity (lowest lead to highest lead)0.004

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FIGURE 8 – INTERFACING THE TEXAS INSTRUMENT TMS320C 30/31 WITH THE EDI8L32128C (128KX32) OR THE EDI8L32512C (512KX32)

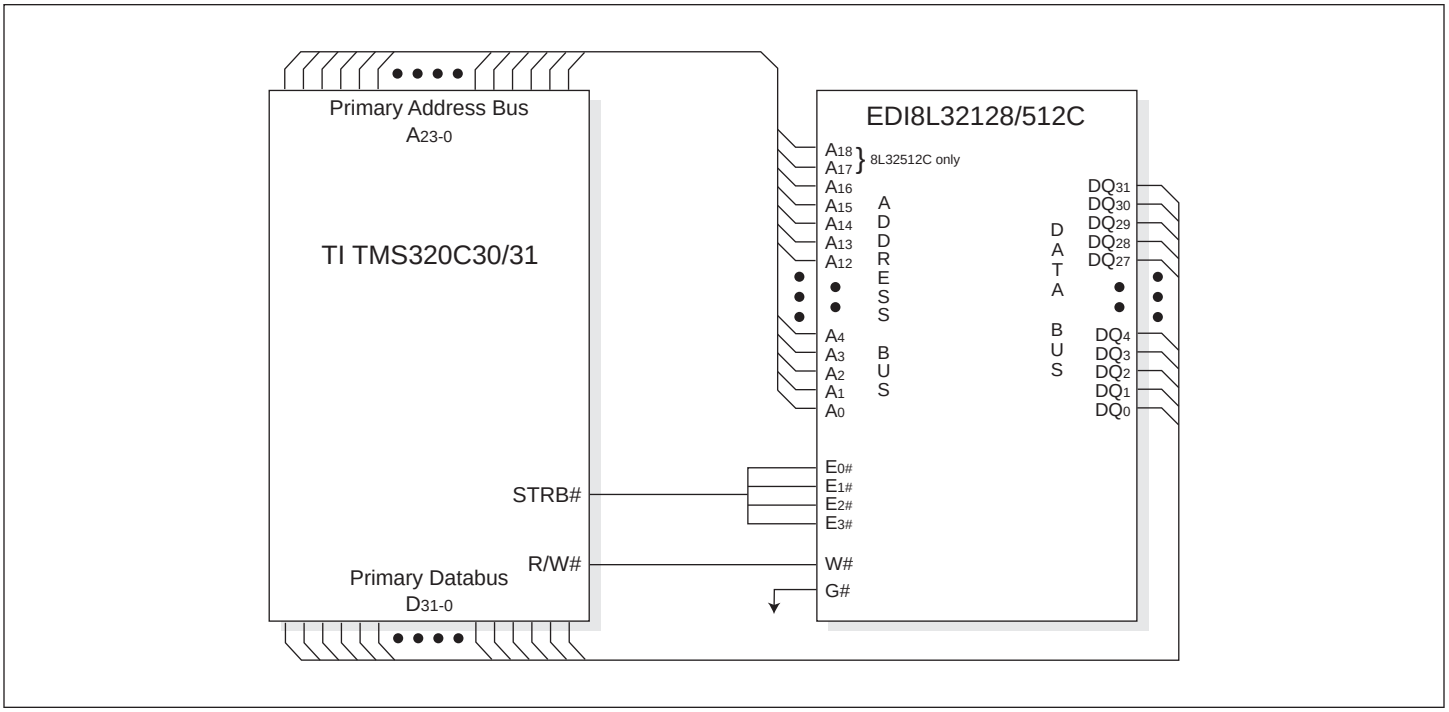


FIGURE 9 – INTERFACING THE TEXAS INSTRUMENT TMS320C32 WITH THE EDI8L32128C (128KX32) OR THE EDI8L32512C (512KX32)

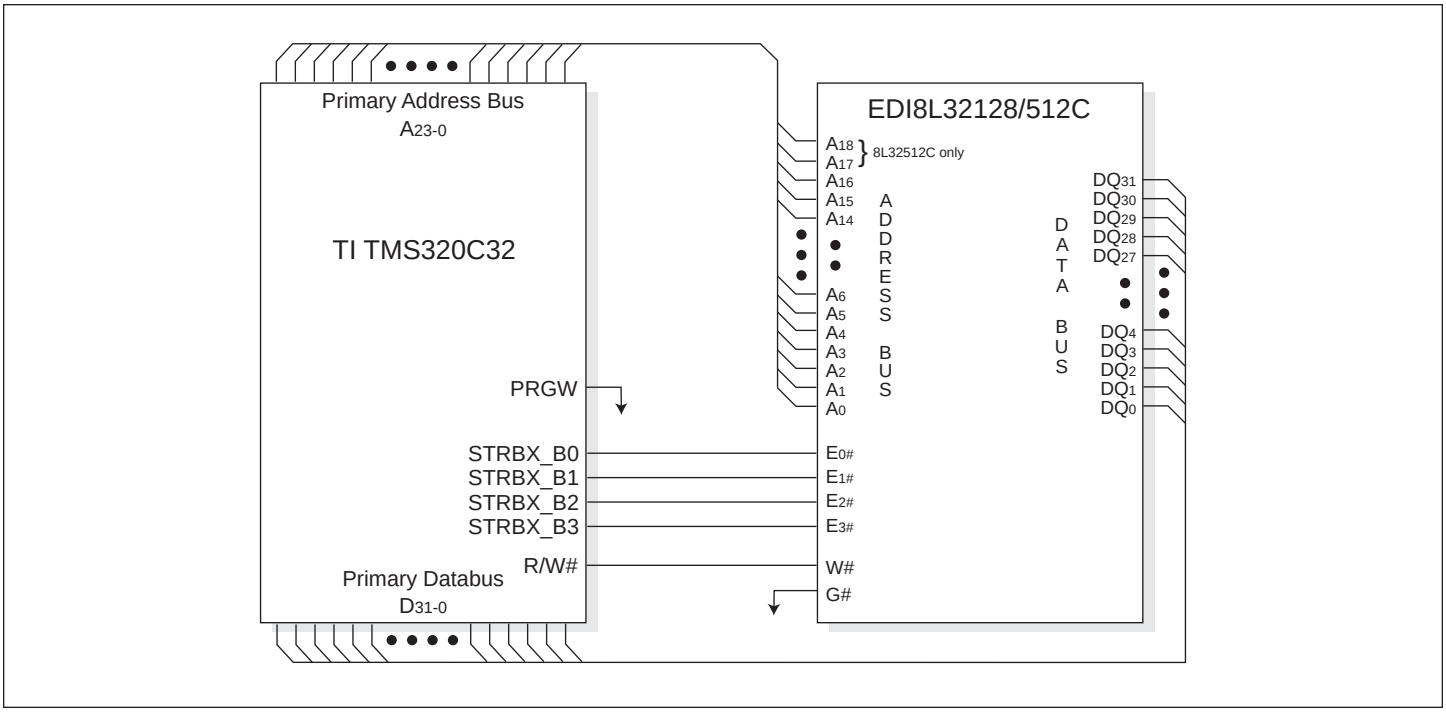


FIGURE 10 – INTERFACING THE TEXAS INSTRUMENT TMS320C4x WITH THE EDI8L32128C (128KX32) OR THE EDI8L32512C (512KX32)

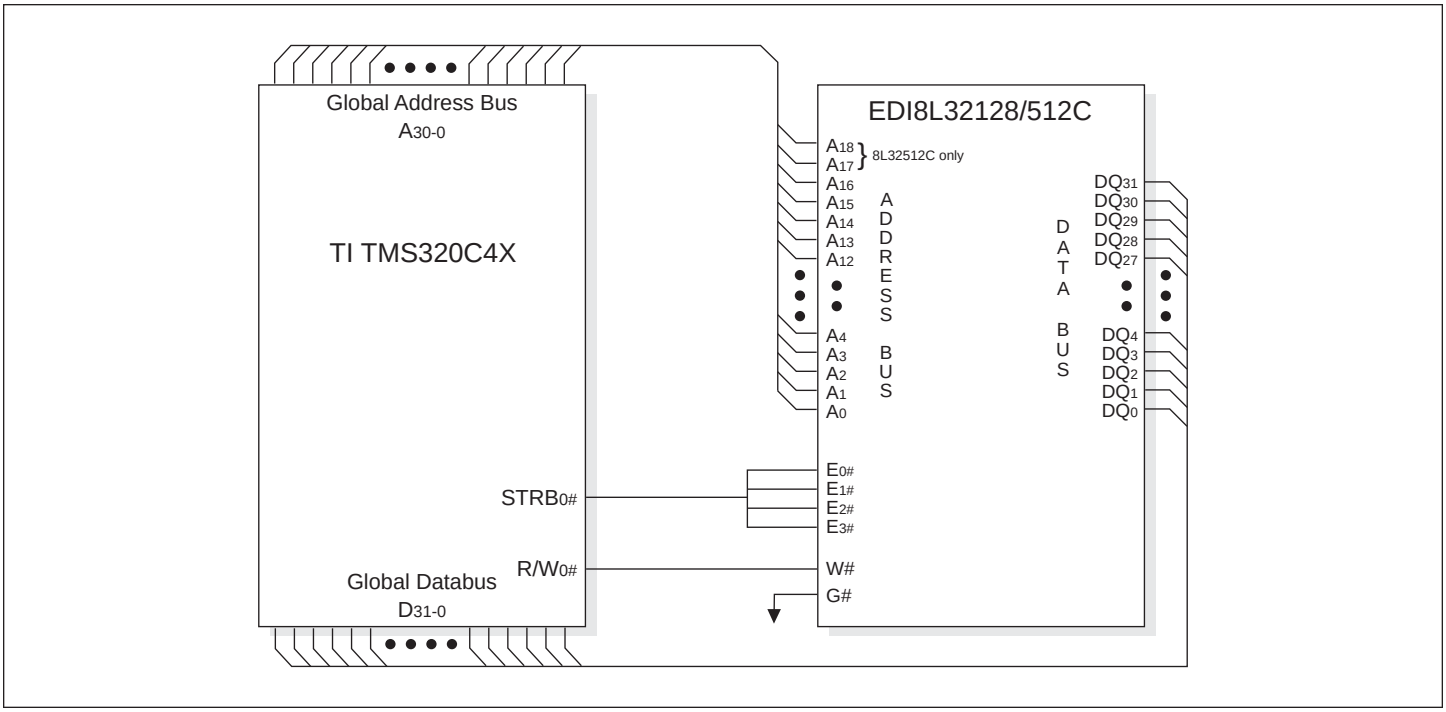


FIGURE 11 – INTERFACING THE ANALOG SHARC DSP WITH THE EDI8L32512C (512KX32)

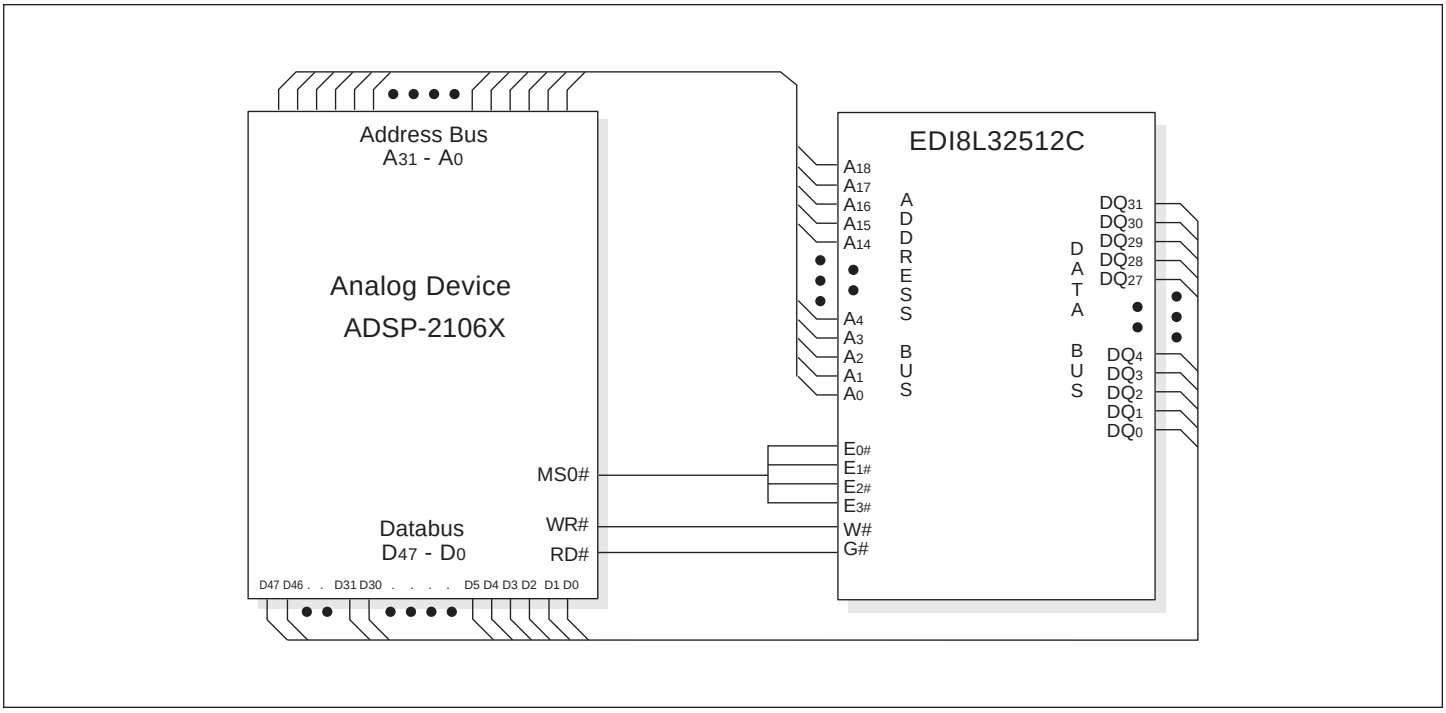


FIGURE 12 – INTERFACING THE ANALOG SHARC DSP WITHTHE EDI8L32512C (1MX48)

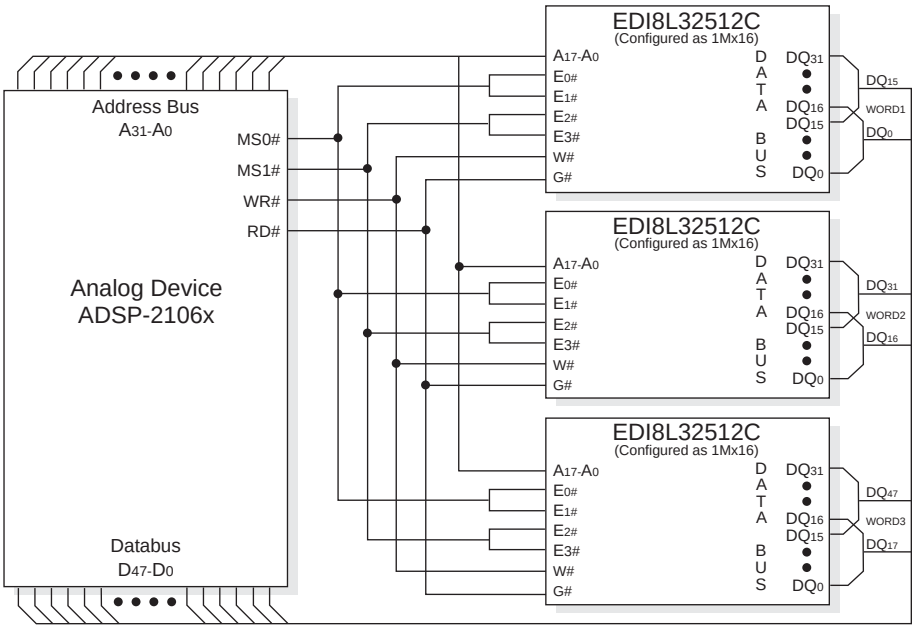
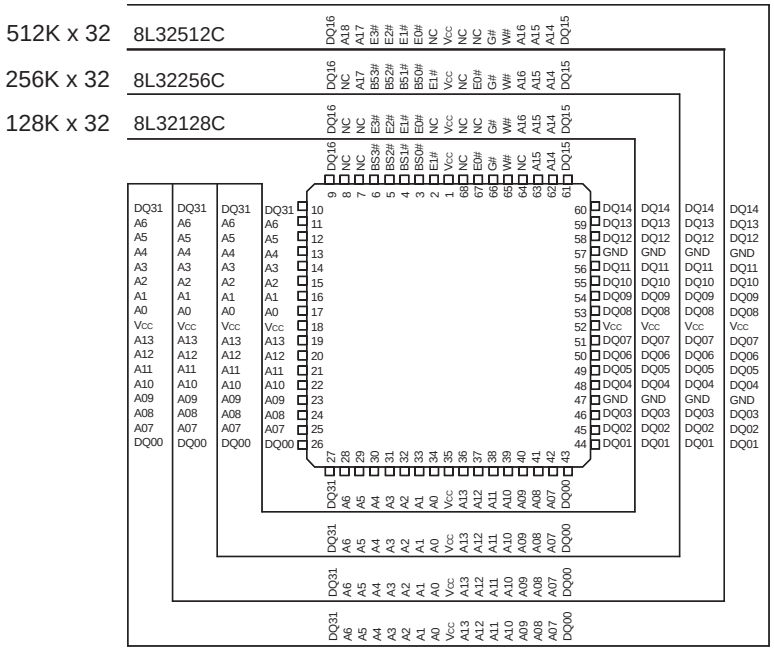


FIGURE 12 – EDI MCM-L-UPGRADE PATH



Document Title

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Revision History

Rev #	History	Release Date	Status
Rev 8	Changes (Pg. 1-9) 8.1 Change document layout from White Electronic Designs to Microsemi 8.2 Add document Revision History page	May 2011	Final