1XA M.2 Module Datasheet

- 802.11a/b/g/n/ac 2x2 MIMO, RSDB and BT/BLE 5.x
- PCIe interface, in M.2 form factor (22 x 30 mm)
- Chipset: Infineon/Cypress CYW54591

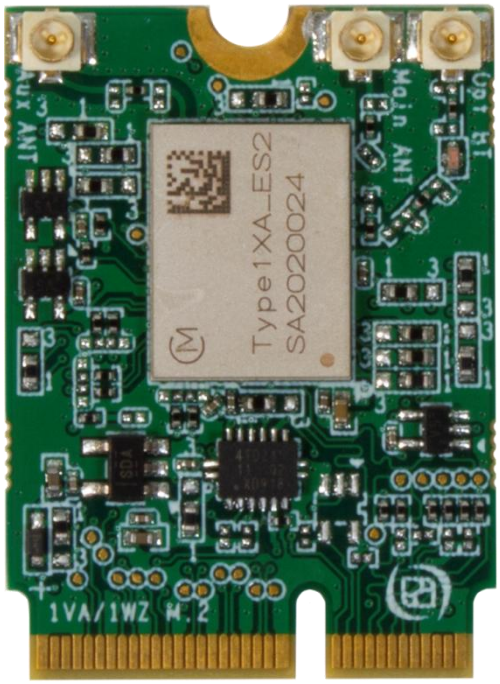

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Table of Contents

1 Document Revision History

Revision	*Date*	*Description*
PA1	2020-12-28	First version.

2 Introduction

This document is a datasheet that specifies and describes the *1XA M.2 module* mainly from a hardware point of view. Software related issues, like the Linux driver, are not addressed. There are separate documents for that.

2.1 Benefits of Using an M.2 Module to get Wi-Fi/BT Connectivity

There are several benefit to use an *M.2 module* to add connectivity to an embedded design:

- Drop-in, certified solution!
- Modular and flexible approach to evaluate different Wi-Fi/BT solutions - with different trade-offs around performance, cost, power consumption, longevity, etc.
- Access to maintained software drivers (Linux) with responsive support from Murata.
- Supported by Embedded Artists' Developer's Kits for i.MX 6/7/8 development, including advanced debugging support on carrier boards
- One component to buy, instead of 50+
- No RF expertise is required
- Developed in close collaboration with Murata and NXP

2.2 More M.2 Related Information

For more information about the M.2 standard and Embedded Artists' adaptation, see: M.2 Primer

For more general information about the M.2 standard, see: https://en.wikipedia.org/wiki/M.2

The official M.2 specification (PCI Express M.2 Specification) is available from: www.pcisig.com

2.3 ESD Precaution and Handling

Please note that the M.2 module come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace modules that have been damaged by ESD.

2.4 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS3, Conflict Minerals, REACH, etc.

3 Specification

This chapter lists some of the more important characteristics of the M.2 module, but it is not a full specification of performance and timing. The main component in the design is Murata's 1XA module (full part number: LBEE5XV1XA), which in turn is based around Infineon (former Cypress) CYW54591 chipset.

For a full specification, see on Murata's 1XA module (LBEE5XV1XA) see Murata's 1XA product page (https://wireless.murata.com/eng/type-1xa.html) and the 1XA datasheet (https://wireless.murata.com/datasheet?/RFM/data/type1xa.pdf).

Module / Chipset	
Murata module	LBEE5XV1XA
Chipset	Infineon (former Cypress) CYW54591

Wi-Fi	
Standards	802.11a/b/g/n/ac 5G 2x2 MIMO, RSDB (Real Simultaneous Dual Band)
Network	uAP and STA dual mode
Frequency	2.4GHz and 5 GHz band
Data rates	TBD
Host interface	PCIe

Bluetooth	
Standards	5.x BR/EDR/LE
Power Class	Class 1
Host interface	4-wire UART@3MBaud
Audio interface	PCM for audio

Powering			
Supply voltage to M.2 module	**Min**	**Typ**	**Max**
Note: Do not exceed minimum or maximum voltage. Module will be permanently damaged above this limit!	TBD minimum 3.3 RF specification	3.3V	3.6V **Note** that LBEE5XV1XA module specification has higher maximum voltage (6.0V), but other components on the M.2 module limits the maximum voltage.
Receive mode current (WLAN)	TBD mA typical max		
Transmit mode current (WLAN)	TBD mA typical max		

Environmental Specification		
Operational Temperature	-30 to +85 degrees Celsius	Functionally ok, but specification is

	derated at temperature extremes
Storage Temperature	-40 to +85 degrees Celsius
Relative Humidity (RH), operating and storage	10 - 90% non-condensing

3.1 Power Up Sequence

The supply voltage shall not rise (10 - 90%) faster than 40 microseconds and not slower than 100 milliseconds.

Signals WL_REG_ON and BT_REG_ON must be held low for at least 1 milliseconds after supply voltage has reached specification level before pulled high.

3.2 External Sleep Clock

The sleep clock signals can be applied to a powered and unpowered M.2 module.

Clock Specification	
Frequency	32.768 kHz
Frequency accuracy	±250 ppm (including tolerance, aging, temperature, etc)
Duty cycle	30 - 70%
Clock jitter	10 000 ppm max (during initial start-up)
Voltage level	3.3V logic, according to M.2 standard

3.3 Mechanical Dimensions

The M.2 module is of type: 2230-S3-E according to the M.2 nomenclature. This means width 22 mm, length 30mm, top side component height 1.5 mm and key-E connector. The table below lists the different dimensions and weight.

M.2 Module Dimension	Value (±0.15 mm)	Unit
Width	22	mm
Height	30	mm
PCB thickness	0.8	mm
Maximum component height on top side	1.5	mm
Maximum component height on bottom side	0	mm
Ground hole diameter	3.5	mm
Plating around ground hole, diameter	5.5	mm
Module weight	1.5 ±0.5 gram	gram

The picture below gives dimensions for the grounded center (half) hole and the u.fl. antenna connectors.

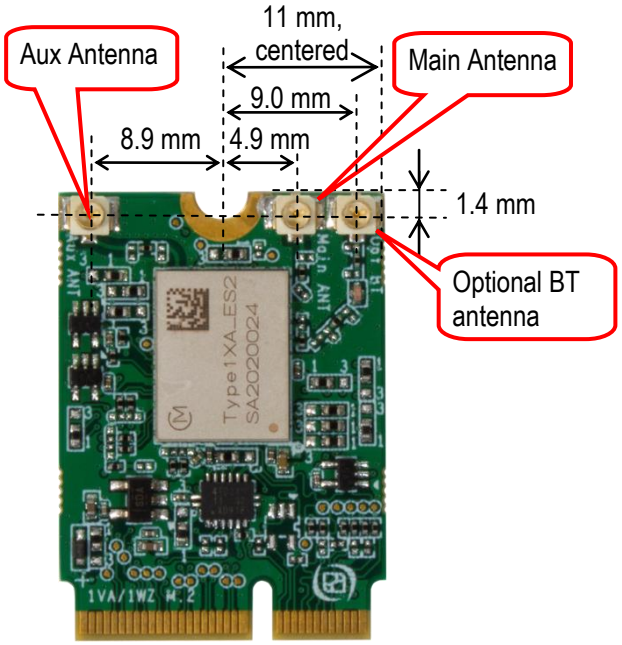

Figure 1 – M.2 Module Antenna Connector Measurements

3.4 M.2 Pinning

This section presents the pinning used for the M.2 module. It is essentially M.2 Key-E compliant with enhancements to support additional debug signals and 3.3V VDDIO override. The pin assignment for specific control and debug signals has been jointly defined by Embedded Artists, Murata, NXP and Infineon/Cypress.

The picture below illustrates the edge pin numbering. It starts on the right edge and alternates between top and bottom side. The removed pads in the keying notch counts (but as obviously non-existing).

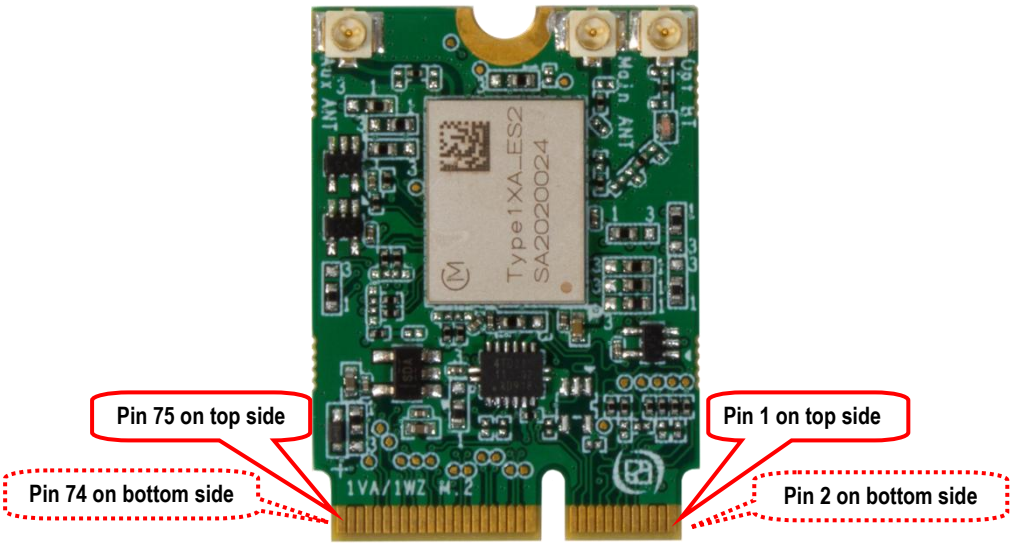

Figure 2 – M.2 Module Pin Numbering

The Wi-Fi interface uses the PCIe interface. The Bluetooth interface uses the UART interface for control and PCM interface for audio. The table below lists the pin usage for the 1XA M.2 modules. The column "When is signal needed" signals four different categories:

- Always: These signals shall always be connected.
- Wi-Fi: These signals shall always be connected then the Wi-Fi interface is used.
- Bluetooth: These signals shall always be connected then the Bluetooth interface is used.
- Optional: These signals are optional to connect.

Pin #	Side of pcb	M.2 Name	Voltage Level and Signal Direction	When is signal needed	Note
1	Top	GND	GND	Always	Connect to ground
2	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
3	Top	USB_D+			Not connected.
4	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
5	Top	USB_D-			Not connected.
6	Bottom	LED_1#			Not connected.
7	Top	GND	GND	Always	Connect to ground.
8	Bottom	PCM_CLK	1.8V I/O[1]	Bluetooth audio	For Bluetooth audio interface: BT_PCM_CLK
9	Top	SDIO CLK			Not connected.
10	Bottom	PCM_SYNC	1.8V I/O[1]	Bluetooth audio	For Bluetooth audio interface: BT_PCM_SYNC
11	Top	SDIO CMD			Not connected.
12	Bottom	PCM_OUT	1.8V output from M.2[1]	Bluetooth audio	For Bluetooth audio interface: BT_PCM_OUT
13	Top	SDIO DATA0			Not connected.
14	Bottom	PCM_IN	1.8V input to M.2[1]	Bluetooth audio	For Bluetooth audio interface: BT_PCM_IN
15	Top	SDIO DATA1			Not connected.
16	Bottom	LED_2#			Not connected.
17	Top	SDIO DATA2			Not connected.
18	Bottom	GND		Always	Connect to ground.
19	Top	SDIO DATA3			Not connected.
20	Bottom	UART WAKE#	3.3V OD output from M.2	Bluetooth	For Bluetooth UART interface: BT_HOST_WAKE_L Require an external 10K pull-up resistor to 3.3V.
21	Top	SDIO WAKE#			Not connected.
22	Bottom	UART TXD	1.8V output from M.2[1]	Bluetooth	For Bluetooth UART interface: BT_UART_TXD
23	Top	SDIO RESET#			Not connected.
24	Key, non existing				
25	Key, non existing				
26	Key, non existing				
27	Key, non existing				
28	Key, non existing				
29	Key, non existing				
30	Key, non existing				

31	Key, non existing				
32	Bottom	UART_RXD	1.8V input to M.2[1]	Bluetooth	For Bluetooth UART interface: BT_UART_RXD
33	Top	GND		Always	Connect to ground.
34	Bottom	UART_RTS	1.8V output from M.2[1]	Bluetooth	For Bluetooth UART interface: BT_UART_RTS
35	Top	PERp0	PCIe input to M.2	Wi-Fi PCIe	PCIe data input (receive, positive signal)
36	Bottom	UART_CTS	1.8V input to M.2[1]	Bluetooth	For Bluetooth UART interface: BT_UART_CTS
37	Top	PERn0	PCIe input to M.2	Wi-Fi PCIe	PCIe data input (receive, negative signal)
38	Bottom	VENDOR DEFINED	1.8V I/O[1]	Optional	GPIO_5 / JTAG_TDO
39	Top	GND		Always	Connect to ground.
40	Bottom	VENDOR DEFINED	1.8V I/O[1]	Optional	GPIO_4 / JTAG_TDI
41	Top	PETp0	PCIe output to M.2	Wi-Fi PCIe	PCIe data output (transmit, positive signal)
42	Bottom	VENDOR DEFINED	1.8V input to M.2[1]	Bluetooth	GPIO_12 / BT_DEV_WAKE_L
43	Top	PETn0	PCIe output to M.2	Wi-Fi PCIe	PCIe data output (transmit, negative signal)
44	Bottom	COEX3	1.8V I/O[1]	Optional	GPIO_6 / JTAG_TRST
45	Top	GND		Always	Connect to ground.
46	Bottom	COEX_TXD	1.8V I/O[1]	Optional	GPIO_2 / JTAG_TCK
47	Top	REFCLKp0	PCIe clock input to M.2	Wi-Fi PCIe	PCIe clock input (receive, positive signal)
48	Bottom	COEX_RXD	1.8V I/O[1]	Optional	GPIO_3 / JTAG_TMS
49	Top	REFCLKn0	PCIe clock input to M.2	Wi-Fi PCIe	PCIe clock input (receive, negative signal)
50	Bottom	SUSCLK	3.3V input to M.2	Always	External sleep clock input (32.768kHz)
51	Top	GND		Always	Connect to ground.
52	Bottom	PERST0#	3.3V input to M.2	Wi-Fi PCIe	PCIe PERST# signal, used to initialize the PCIe functions once power sources stabilize.
53	Top	CLKREQ0#	3.3V OD output from M.2	Wi-Fi PCIe	PCIe clock request (low level request reference clock) **Note**: Requires external 10Kohm pull-up
54	Bottom	W_DISABLE2#	3.3V input to M.2	Always	BT_REG_ON, High = BT part of module enabled/internally powered, Low = BT disabled/powered down
55	Top	PEWAKE0#	3.3V OD output from M.2	Wi-Fi PCIe	PCIe PERST# signal, used to implement host wakeup functionality **Note**: Requires external 10Kohm pull-up
56	Bottom	W_DISABLE1#	3.3V input to M.2	Always	WL_REG_ON, High = Wi-Fi part of module enabled/internally powered, Low = Wi-Fi disabled/powered down
57	Top	GND		Always	Connect to ground.
58	Bottom	I2C_SDA			Not connected.
59	Top	Reserved	1.8V I/O[1]	Optional	BT_GPIO_2
60	Bottom	I2C_CLK			Not connected.
61	Top	Reserved	1.8V I/O[1]	Optional	BT_GPIO_3
62	Bottom	ALERT#	1.8V I/O[1]	Optional	GPIO_11
63	Top	GND		Always	Connect to ground.
64	Bottom	RESERVED		Optional	Optional supply voltage input for control and data signal voltage level. Apply a stable, low-noise, 3.3V 100mA supply to set 3.3V voltage level on all control signals (that normally are 1.8V).
65	Top	Reserved	1.8V I/O[1]	Optional	BT_GPIO_4

66	Bottom	UIM_SWP			GPIO_10
67	Top	Reserved	1.8V I/O[1]	Optional	BT_GPIO_5
68	Bottom	UIM_POWER_SNK	1.8V I/O[1]	Optional	GPIO_9
69	Top	GND		Always	Connect to ground.
70	Bottom	UIM_POWER_SRC/GPIO_1	1.8V I/O[1]	Optional	GPIO_8
71	Top	Reserved		Optional	Not connected.
72	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
73	Top	Reserved			Not connected.
74	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
75	Top	GND		Always	Connect to ground.

[1] Note: If applying 3.3V to pin 64, the signaling voltage is changed to 3.3V

3.5 Test Points

There are some test points that can be of interest to probe for debugging purposes, as illustrated in the picture below.

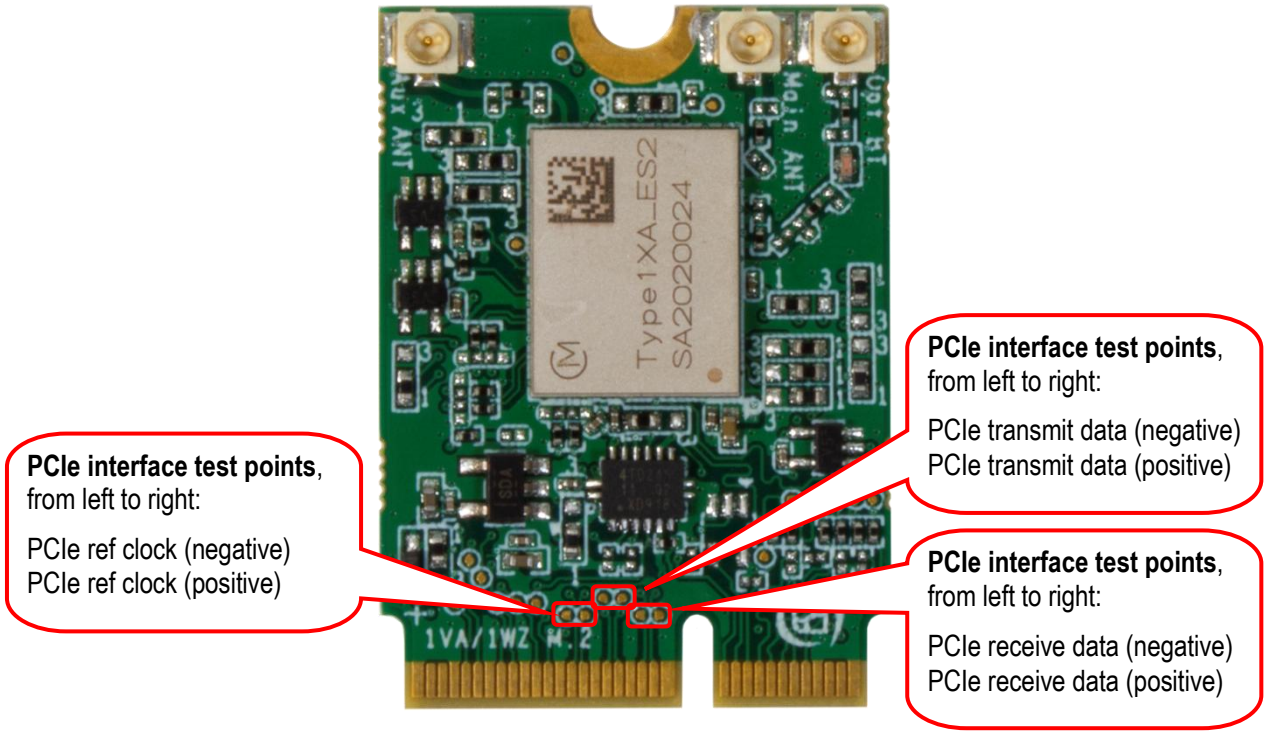

Figure 3 – 1XA M.2 Module Test Points and JTAG Control Resistor

3.6 VDDIO Override Feature

The M.2 standard specify 1.8V logic level on several of the data and control signals. It is possible to override the voltage level for the 1.8V signals via pin 64. Apply a 3.3V / 100 mA supply to pin 64 in order to get 3.3V voltage level on all data and control signals.

4 Antenna

The module does not have any on-board antenna because the module is too small to get spatial separation of the two antennas. Two external antennas must be connected (to support MIMO).

Molex 1461870100 is a balanced, dipole-type, high efficiency antenna used for the reference certification of the 1XA module. It is ground plane independent, dual band antenna that supports the 2400-2500MHz,5150-5850MHz, 5925-7125MHz frequency bands. The physical size if 40.95 x 9 x 0.7mm. The antenna cable come in 6 standard length options: 50/100/150/200/250/300mm (100mm is used for the reference certification) and the connector is MHF-I, which is a U.FL compatible connector.

Figure 4 – Reference Certified Antenna

5 Regulatory

The Murata 1XA module is being reference certified. More detailed information around this will be added in future versions of the document.

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