1MW M.2 Module Datasheet

- 802.11 a/b/g/n/ac and BT/BLE 5.0
- SDIO 3.0 interface, SDR100@200MHz
- 22 x 44 mm with integrated trace antenna

Get Up-and-Running Quickly and
Start Developing Your Application On Day 1!

Embedded Artists

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1 Document Revision History

Revision	*Date*	*Description*
PA1	2019-04-16	First version.
PA2	2019-08-29	Added some clarifications and corrected polarity of BT_DEV_WAKE (pin 42)
PA3	2019-10-04	Added information about BT_CLK errata

2 Introduction

This document is a datasheet that specifies and describes the *1MW M.2 module* mainly from a hardware point of view. Software related issues, like the Linux and WICED drivers, are not addressed. There are separate documents for that.

2.1 Benefits of Using an M.2 Module to get Wi-Fi/BT Connectivity

There are several benefit to use an *M.2 module* to add connectivity to an embedded design:

- Drop-in, certified solution!
- Modular and flexible approach to evaluate different Wi-Fi/BT solutions - with different trade-offs around performance, cost, power consumption, longevity, etc.
- Access to maintained software drivers (Linux and WICED) with responsive support from Murata.
- Supported by Embedded Artists' Developer's Kits for i.MX RT/6/7/8 development, including advanced debugging support on carrier boards
- One component to buy, instead of 50+
- No RF expertise is required
- Developed in close collaboration with Murata and Cypress

2.2 More M.2 Related Information

For more information about the M.2 standard and Embedded Artists' adaptation, see: M.2 Primer

For more general information about the M.2 standard, see: https://en.wikipedia.org/wiki/M.2

The official M.2 specification (PCI Express M.2 Specification) is available from: www.pcisig.com

2.3 ESD Precaution and Handling

Please note that the M.2 module come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace modules that have been damaged by ESD.

2.4 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS2, Conflict Minerals, REACH, etc.

3 Specification

This chapter lists some of the more important characteristics of the M.2 module, but it is not a full specification of performance and timing. The main component in the design is Murata's 1MW module (full part number: LBEE5HY1MW), which in turn is based around Cypress CYW43455 chipset.

For a full specification, see Murata's 1MW Module (LBEE5HY1MW) product page: https://wireless.murata.com/eng/type-1mw.html and the LBEE5HY1MW datasheet: https://wireless.murata.com/datasheet?/RFM/data/type1mw.pdf

Module / Chipset	
Murata module	LBEE5HY1MW
Chipset	Cypress CYW43455

Wi-Fi	
Standards	802.11a/b/g/n/ac
Network	AP and STA dual mode
Frequency	2.4GHz and 5 GHz band
Data rates	11, 54, 65, 150, 433 Mbps
Host interface	SDIO 3.0, SDR100@200MHz / DDR50@50MHz

Bluetooth	
Standards	5.0 BR/EDR/LE
Power Class	Class 1
Host interface	4-wire UART@3MBaud
Audio interface	PCM for audio

Powering			
Supply voltage to M.2 module	**Min**	**Typ**	**Max**
Note: Do not exceed minimum or maximum voltage. Module will be permanently damaged above this limit!	0.0V minimum 3.1V operating 3.2V RF specification	3.3V	3.6V **Note** that LBEE5HY1MW module specification is 4.2V, but other components on the M.2 module limits the maximum voltage
Receive mode current (WLAN)	130 mA typical max		
Transmit mode current (WLAN)	420 mA typical max		

Environmental Specification		
Operational Temperature	-20 to +75 degrees Celsius	Functionally ok, but specification is derated at temperature extremes

Storage Temperature	-40 to +85 degrees Celsius
Relative Humidity (RH), operating and storage	10 - 90% non-condensing

3.1 Power Up Sequence

The supply voltage shall not rise (10 - 90%) faster than 40 microseconds and not slower than 100 milliseconds.

Signals WL_REG_ON or BT_REG_ON must be held low for at least 700 microseconds after supply voltage has reached specification level before pulled high. 2 clock cycles of the 32.678kHz clock must also have passed before any of the signals is pulled high. These clock cycles will typically occur during the 700 microseconds but if the clock signal has a long delay during power-up, the 700 microsecond period can be extended.

3.2 External Sleep Clock

The sleep clock signals can be applied to a powered and unpowered M.2 module.

Clock Specification	
Frequency	32.768 kHz
Frequency accuracy	±200 ppm
Duty cycle	30 - 70%
Clock jitter	<10000 ppm
Voltage level	3.3V logic, according to M.2 standard

3.3 Mechanical Dimensions

The M.2 module is of type: 2230-S3-E according to the M.2 nomenclature. This means width 22 mm, length 30mm (without trace antenna), top side component height 1.5 mm and key-E connector. The table below lists the different dimensions and weight.

M.2 Module Dimension	Value (±0.15 mm)	Unit
Width	22	mm
Height, with pcb trace antenna Height, without pcb trace antenna	44 30	mm mm
PCB thickness	0.8	mm
Maximum component height on top side	1.5	mm
Maximum component height on bottom side	0	mm
Ground hole diameter	3.5	mm
Plating around ground hole, diameter	5.5	mm
Module weight	1.5 ±0.5 gram	gram

Embedded Artists has added a non-standard feature to the 2230 M.2 modules designed together with Murata and Cypress. The pictures below illustrates the how the standard module size has been extended by 14 mm in the length direction in order to include a pcb trace antenna.

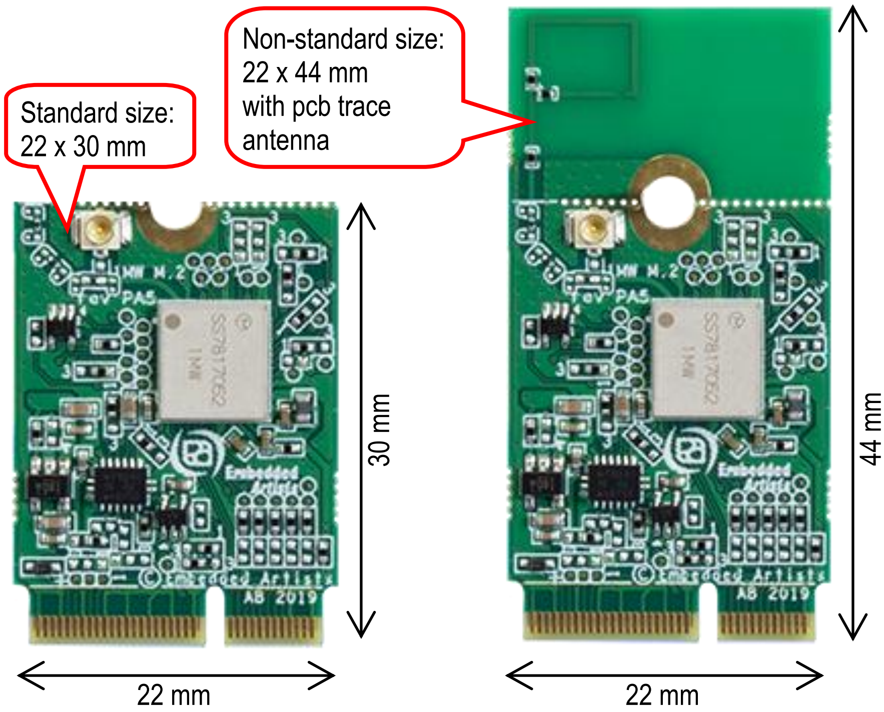


Figure 1 – M.2 Module with, and without, PCB Trace Antenna

The picture below gives dimensions for the grounded center (half) hole and the u.fl. antenna connector.

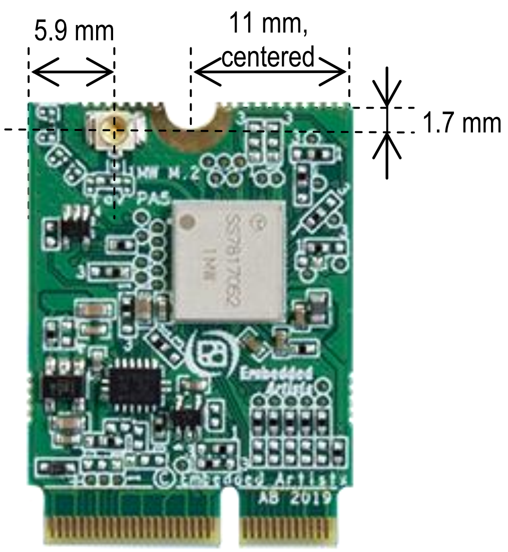


Figure 2 – M.2 Module With, and Without, Trace Antenna

3.4 M.2 Pinning

This section presents the pinning used for the M.2 module. It is essentially M.2 Key-E compliant with enhancements to support additional debug signals and 3.3V VDDIO override. The pin assignment for specific control and debug signals has been jointly defined by Embedded Artists, Murata and Cypress.

The picture below illustrates the edge pin numbering. It starts on the right edge and alternates between top and bottom side. The removed pads in the keying notch counts (but as obviously non-existing).

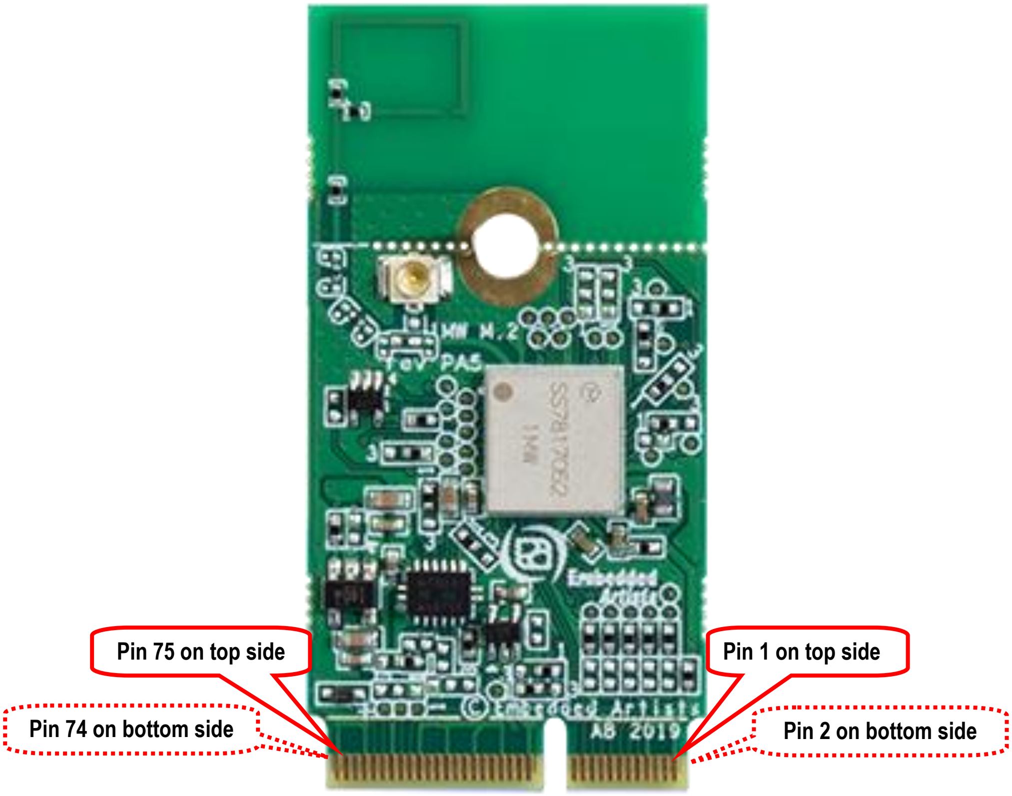


Figure 3 – M.2 Module Pin Numbering

The Wi-Fi interface uses the SDIO interface. The Bluetooth interface uses the UART interface for control and PCM interface for audio. The table below lists the pin usage for the 1MW M.2 modules. The column "When is signal needed" signals four different categories:

- Always: These signals shall always be connected.
- Wi-Fi: These signals shall always be connected then the Wi-Fi interface is used.
- Bluetooth: These signals shall always be connected then the Bluetooth interface is used.
- Optional: These signals are optional to connect.

Pin #	Side of pcb	M.2 Name	Voltage Level and Signal Direction	When is signal needed	Note
1	Top	GND	GND	Always	Connect to ground
2	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
3	Top	USB_D+			Not connected.
4	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
5	Top	USB_D-			Not connected.

6	Bottom	LED_1#			Not connected.
7	Top	GND	GND	Always	Connect to ground.
8	Bottom	PCM_CLK	1.8V I/O	Bluetooth audio	For Bluetooth audio interface: BT_PCM_CLK
9	Top	SDIO CLK	1.8V Input to M.2	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_CLK Note that maximum frequency is 200 MHz
10	Bottom	PCM_SYNC	1.8V I/O	Bluetooth audio	For Bluetooth audio interface: BT_PCM_SYNC
11	Top	SDIO CMD	1.8V I/O	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_CMD Note: 10-100K ohm pullup required
12	Bottom	PCM_OUT	1.8V output from M.2	Bluetooth audio	For Bluetooth audio interface: BT_PCM_OUT
13	Top	SDIO DATA0	1.8V I/O	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D0 Note: 10-100K ohm pullup required
14	Bottom	PCM_IN	1.8V input to M.2	Bluetooth audio	For Bluetooth audio interface: BT_PCM_IN
15	Top	SDIO DATA1	1.8V I/O	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D1 Note: 10-100K ohm pullup required
16	Bottom	LED_2#			Not connected.
17	Top	SDIO DATA2	1.8V I/O	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D2 Note: 10-100K ohm pullup required
18	Bottom	GND		Always	Connect to ground.
19	Top	SDIO DATA3	1.8V I/O	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D3 Note: 10-100K ohm pullup required
20	Bottom	UART WAKE#	3.3V OD output from M.2	Bluetooth	For Bluetooth UART interface: BT_HOST_WAKE_L Require an external 10K pullup resistor to 3.3V.
21	Top	SDIO WAKE#	1.8V OD output from M.2	Wi-Fi SDIO	For Wi-Fi SDIO interface WL_HOST_WAKE_L Require an external 10K pullup resistor to 1.8V.
22	Bottom	UART TXD	1.8V output from M.2	Bluetooth	For Bluetooth UART interface: BT_UART_TXD
23	Top	SDIO RESET#			Not connected. The Wi-Fi SDIO interface is controlled by pin 56, W_DISABLE1#, which is a 3.3V logic level signal.
24	Key, non existing				
25	Key, non existing				
26	Key, non existing				
27	Key, non existing				
28	Key, non existing				
29	Key, non existing				
30	Key, non existing				
31	Key, non existing				
32	Bottom	UART_RXD	1.8V input to M.2	Bluetooth	For Bluetooth UART interface: BT_UART_RXD
33	Top	GND		Always	Connect to ground.
34	Bottom	UART_RTS	1.8V output from M.2	Bluetooth	For Bluetooth UART interface: BT_UART_RTS
35	Top	PERp0			Not connected.
36	Bottom	UART_CTS	1.8V input to M.2	Bluetooth	For Bluetooth UART interface: BT_UART_CTS
37	Top	PERn0			Not connected.
38	Bottom	VENDOR	1.8V I/O	Optional	WL_GPIO_5

		DEFINED			
39	Top	GND		Always	Connect to ground.
40	Bottom	VENDOR DEFINED	1.8V I/O	Optional	WL_GPIO_4
41	Top	PETp0			Not connected.
42	Bottom	VENDOR DEFINED	1.8V input to M.2	Bluetooth	BT_DEV_WAKE
43	Top	PETn0			Not connected.
44	Bottom	COEX3	1.8V I/O	Optional	WL_GPIO_6
45	Top	GND		Always	Connect to ground.
46	Bottom	COEX_TXD	1.8V I/O	Optional	WL_GPIO_2
47	Top	REFCLKp0			Not connected.
48	Bottom	COEX_RXD	1.8V I/O	Optional	WL_GPIO_3
49	Top	REFCLKn0			Not connected.
50	Bottom	SUSCLK	3.3V input to M.2	Always	External sleep clock input (32.768kHz)
51	Top	GND		Always	Connect to ground.
52	Bottom	PERST0#			Not connected.
53	Top	CLKREQ0#			Not connected.
54	Bottom	W_DISABLE2#	3.3V input to M.2	Always	BT_REG_ON, High = BT enabled, Low = BT disabled
55	Top	PEWAKE0#			Not connected.
56	Bottom	W_DISABLE1#	3.3V input to M.2	Always	WL_REG_ON, High = Wi-Fi enabled, Low = Wi-Fi disabled
57	Top	GND		Always	Connect to ground.
58	Bottom	I2C_SDA			Not connected.
59	Top	Reserved	1.8V I/O	Optional	BT_GPIO_2
60	Bottom	I2C_CLK			Not connected.
61	Top	Reserved	1.8V I/O	Optional	BT_GPIO_3
62	Bottom	ALERT#			Not connected.
63	Top	GND		Always	Connect to ground.
64	Bottom	RESERVED		Optional	Optional supply voltage input for control and data signal voltage level. Apply a stable, low-noise, 3.3V 100mA supply to set 3.3V voltage level on all signals. **Note** that VDD-SDIO control resistor (10Kohm 0402) must be mounted for 3.3V SDIO voltage, see Figure 4 for details.
65	Top	Reserved	1.8V output from M.2	Optional	BT_GPIO4
66	Bottom	UIM_SWP	1.8V I/O	Wi-Fi SDIO	WL_GPIO_1, carrying signal WL_DEV_WAKE that is used for very low power Wi-Fi implementations. Signal can optionally connect to a 1.8V GPIO output on the host processor.
67	Top	Reserved	1.8V input to M.2	Optional	BT_GPIO5
68	Bottom	UIM_POWER_ SNK			Not connected.
69	Top	GND		Always	Connect to ground.
70	Bottom	UIM_POWER_ SRC/GPIO_1			Not connected.
71	Top	Reserved			Not connected.
72	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
73	Top	Reserved			Not connected.

74	Bottom	3.3 V	Always	Power supply input. Connect to stable, low-noise 3.3V supply.
75	Top	GND	Always	Connect to ground.

3.5 Test Points

There are some test points that can be of interest to probe for debugging purposes, as illustrated in the picture below.

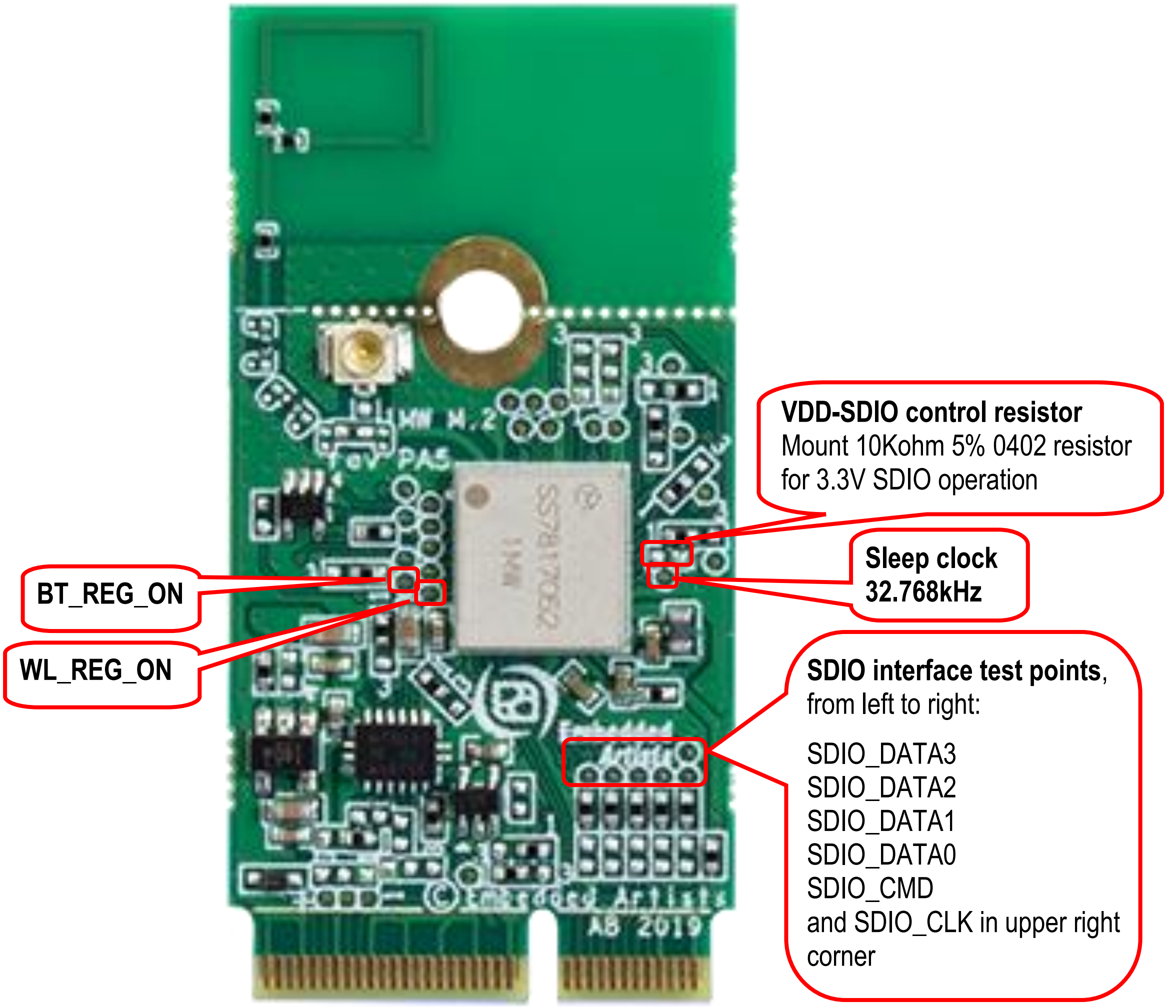


Figure 4 – 1MW M.2 Module Test Points and VDD-SDIO Control Resistor

3.6 VDDIO Override Feature

The M.2 standard specifies 1.8V logic level on several of the data and control signals. It is possible to override the voltage level for the 1.8V signals via pin 64. Apply a 3.3V / 100 mA supply to pin 64 in order to get 3.3V voltage level on all data and control signals.

Note that it is not enough to connect a 3.3V supply to pin 64. The VDD-SDIO control resistor must also be mounted (10Kohm, 5%, 0402 resistor), see Figure 4 for location of this resistor.

Note that using the 3.3V VIO option will limit SDIO clock to 50 MHz, thereby limiting throughput. Running at 1.8V VIO will support up to 200 MHz SDIO clock which is ultimately needed for maximum 802.11ac throughput.

4 Antenna

This chapter addresses the antenna side of the module. There is an on-board, reference certified pcb trace antenna. This can be used for testing/evaluation purposes, but also for the final product. Also, for testing and evaluation purposes, it is possible to disconnect the on-board antenna and instead use an u.fl. connector to connect an external antenna.

4.1 Mounting and Clearance

Ideally, arrange the M.2 module so that the antenna is located at a corner of the product. Keep plastic case (i.e., non-metallic) away from the antenna area with at least 5 mm clearance (in all directions). Also keep any metal elements (e.g., connectors, battery, etc.) away from the antenna area with at least 5 mm clearance (in all directions). Keep a clearance area under and above the antenna area of at least 7.5mm, both under and over the PCB.

Human hands or body parts should be kept away (in the normal use case) from the antenna area.

The ground hole in the middle shall be grounded. Use a metal stand-off according to M.2 standard (height suitable for selected M.2 connector) and use metal screw to create a proper ground connection.

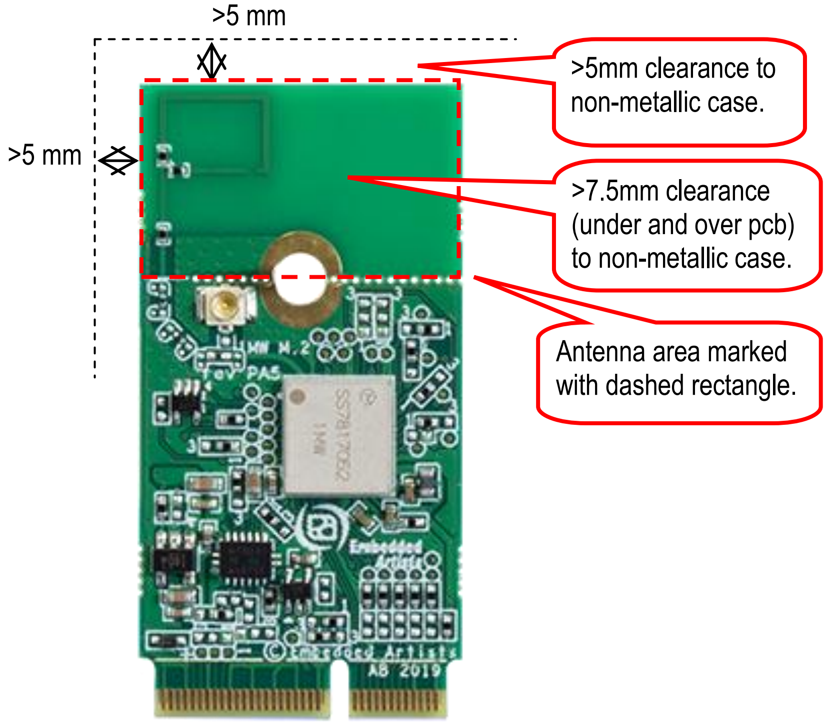


Figure 5 – M.2 Module Clearance Area

4.2 Overriding PCB Trace Antenna

The antenna connection from the 1MW module be redirected to the u.fl. connector by just moving one zero ohm 0402 resistor, see illustration below. The on-board trace antenna can be left as-is, or the antenna can be snapped-off.

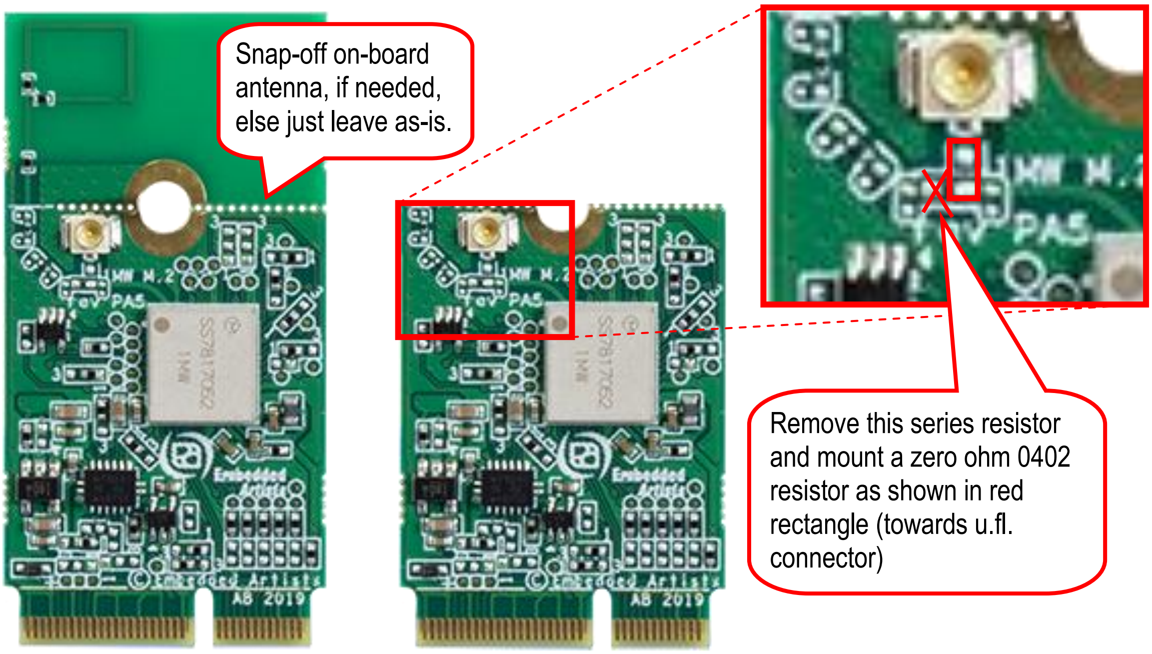


Figure 6 – Rework to Connect U.FL. Connector

4.3 On-board Trace Antenna Performance

The on-board pcb trace antenna type is monopole. The 1MW M.2 module has been measured both standalone and mounted on the iMX OEM Carrier Board (which is a typical carrier board design).

The table below lists total efficiency:

Measurement condition	Frequency MHz						Total Efficiency in dB		Total Efficiency in %	
	2400	2442	2484	5150	5500	5850	Average 2 GHz band	Average 5 GHz band	Average 2 GHz band	Average 5 GHz band
1MW M.2 module mounted on iMX OEM Carrier Board	-5.5	-5.3	-5.2	-6.3	-5.7	-6.5	-5.3	-6.1	29.2	24.3
1MW M.2 module standalone	-4.6	-4.6	-4.6	-5.4	-5.2	-5.2	-4.6	-5.3	34.6	29.7

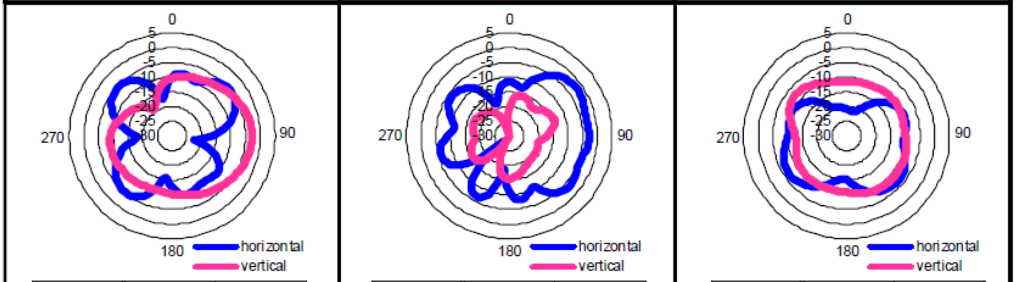
The table below lists peak gain:

Measurement condition	Frequency MHz						Max dBi	
	2400	2442	2484	5150	5500	5850	Max 2 GHz band	Max 5 GHz band
1MW M.2 module mounted on iMX OEM Carrier Board	-2.3	-2.0	-1.7	-2.7	-1.3	-1.2	-1.7	-1.2
1MW M.2 module standalone	-1.7	-1.5	-1.5	-3.0	-2.5	-2.8	-1.5	-2.5

4.3.1 1MW M.2 Module Mounted on iMX OEM Carrier Board

The 3D directivity measurements are presented below for the 2 GHz and 5GHz bands when the 1MW M.2 module is mounted on the iMX OEM Carrier Board.

@2442MHz



XY plane [dBi]

	HOR.	VER.
MAX	-4.8	-2.7
AVE	-8.9	-7.5

YZ plane [dBi]

	HOR.	VER.
MAX	-2.0	-13.8
AVE	-6.4	-17.6

ZX plane [dBi]

	HOR.	VER.
MAX	-6.6	-7.7
AVE	-10.4	-10.1

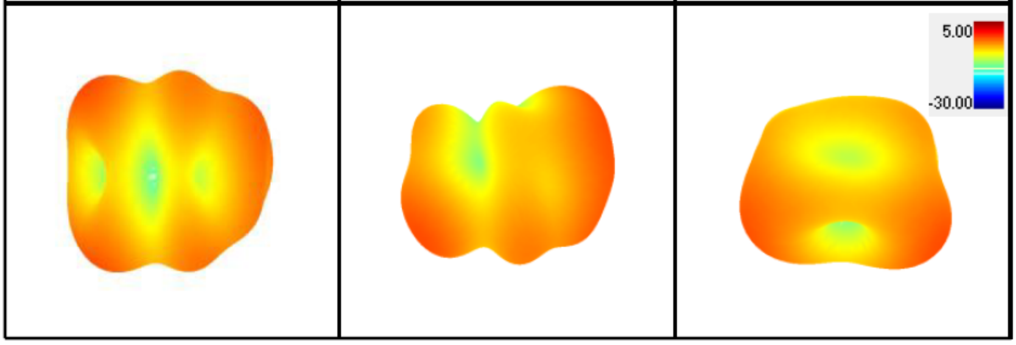
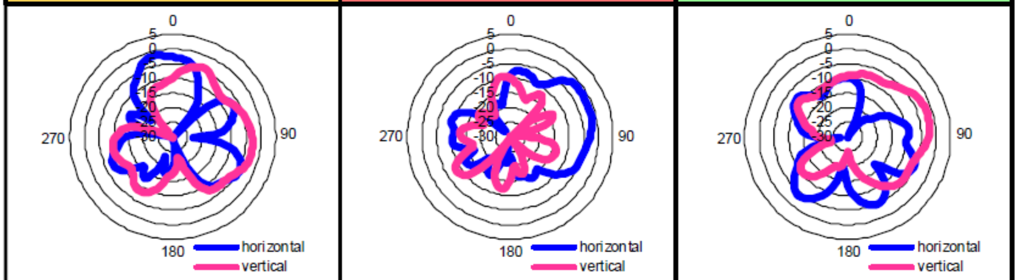


Figure 7 – 3D Directivity Measurements in 2 GHz Band

@5500MHz



XY plane [dBi]

	HOR.	VER.
MAX	-1.6	-2.8
AVE	-8.4	-8.1

YZ plane [dBi]

	HOR.	VER.
MAX	-1.3	-8.2
AVE	-7.8	-14.5

ZX plane [dBi]

	HOR.	VER.
MAX	-3.9	-1.8
AVE	-9.6	-8.0

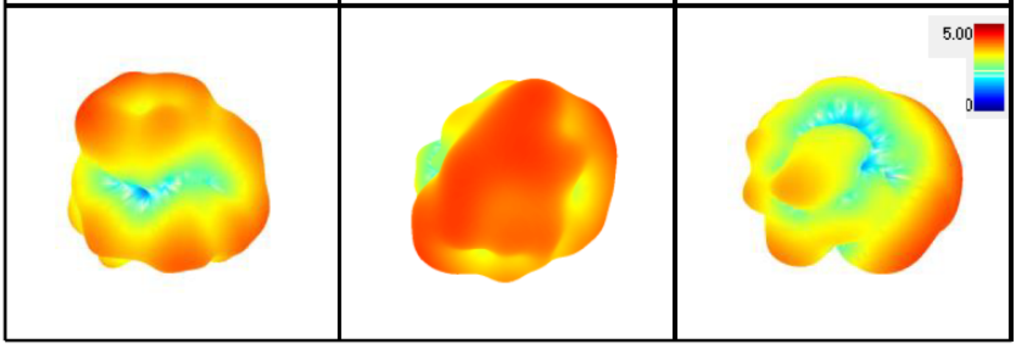


Figure 8 – 3D Directivity Measurements in 5 GHz Band

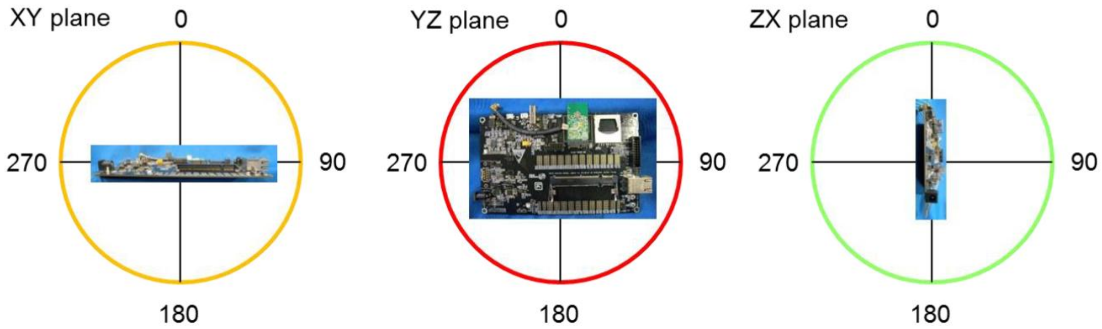


Figure 9 – 3D Directivity Measurements Plane Orientations

The pictures below illustrates the return loss, efficiency and directivity when the 1MW M.2 module is mounted on the iMX OEM Carrier Board.

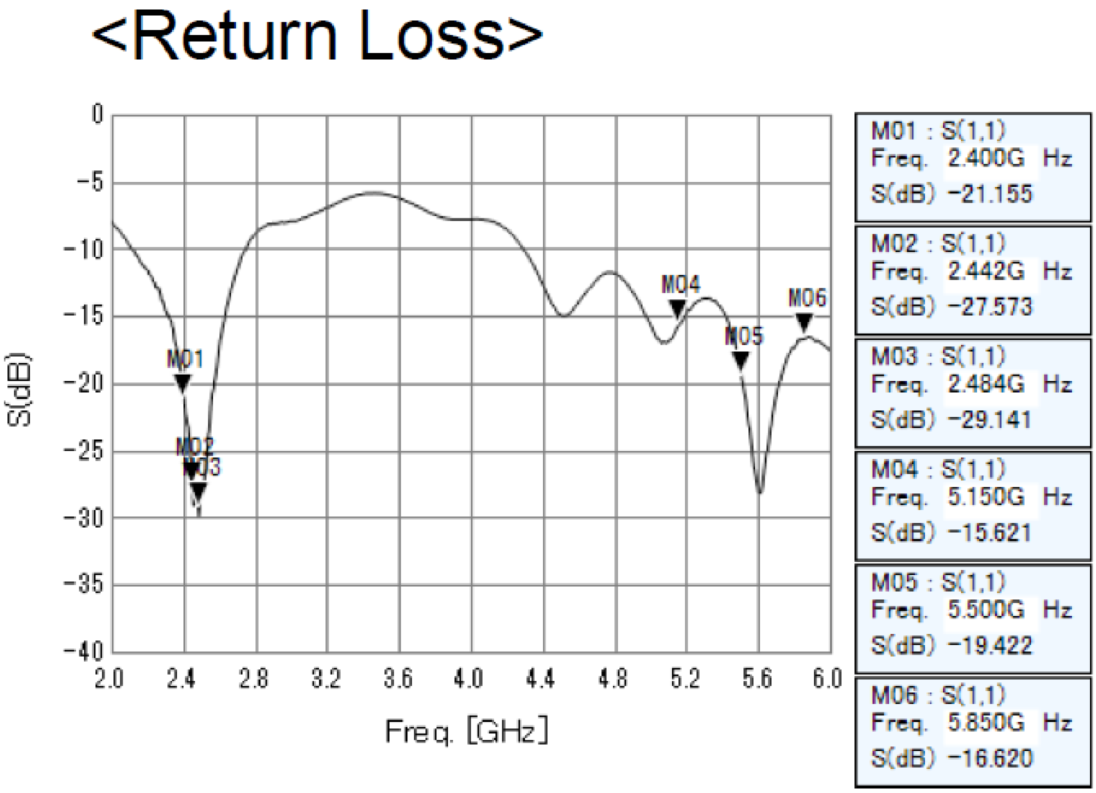


Figure 10 – Return Loss for 1MW M.2 Module Mounted on iMX OEM Carrier Board

<Efficiency>

[dBi] [dB]

LINEAR POLARIZATION		XY-plane hor.	XY-plane ver.	YZ-plane hor.	YZ-plane ver.	ZX-plane hor.	ZX-plane ver.	Total Efficiency
2400 MHz	MAX.	-5.2	-2.8	-2.3	-13.9	-7.6	-7.7	
	AVE.	-9.1	-7.5	-6.5	-17.5	-11.0	-10.0	-5.5
2442 MHz	**MAX.**	**-4.8**	**-2.7**	**-2.0**	**-13.8**	**-6.6**	**-7.7**	
	AVE.	**-8.9**	**-7.5**	**-6.4**	**-17.6**	**-10.4**	**-10.1**	**-5.3**
2484 MHz	MAX.	-4.7	-2.9	-1.7	-14.2	-6.0	-7.9	
	AVE.	-8.9	-7.6	-6.4	-18.0	-10.1	-10.3	-5.2

[dBi] [dB]

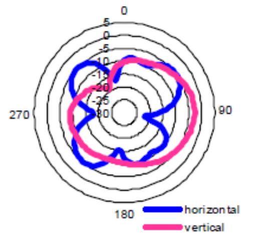
LINEAR POLARIZATION		XY-plane hor.	XY-plane ver.	YZ-plane hor.	YZ-plane ver.	ZX-plane hor.	ZX-plane ver.	Total Efficiency
5150 MHz	MAX.	-3.2	-3.6	-2.7	-7.4	-4.4	-2.7	
	AVE.	-9.3	-7.9	-8.9	-14.4	-9.8	-8.0	-6.3
5500 MHz	**MAX.**	**-1.6**	**-2.8**	**-1.3**	**-8.2**	**-3.9**	**-1.8**	
	AVE.	**-8.4**	**-8.1**	**-7.8**	**-14.5**	**-9.6**	**-8.0**	**-5.7**
5850 MHz	MAX.	-1.2	-5.0	-3.7	-8.6	-7.6	-2.2	
	AVE.	-8.6	-9.9	-9.8	-15.0	-12.5	-8.0	-6.5

Figure 11 – Efficiency for 1MW M.2 Module Mounted on iMX OEM Carrier Board

<Directivity>

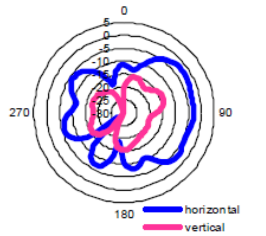
@2442MHz

XY plane [dBi]



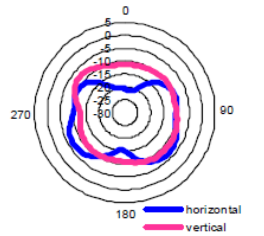
	HOR.	VER.
MAX	-4.8	-2.7
AVE	-8.9	-7.5

YZ plane [dBi]



	HOR.	VER.
MAX	-2.0	-13.8
AVE	-6.4	-17.6

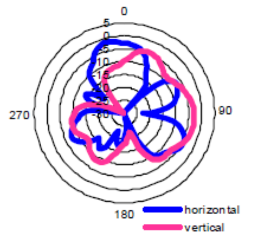
ZX plane [dBi]



	HOR.	VER.
MAX	-6.6	-7.7
AVE	-10.4	-10.1

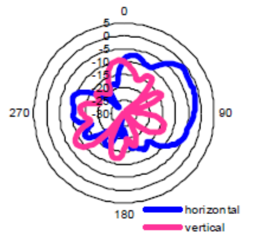
@5500MHz

XY plane [dBi]



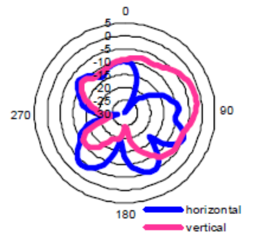
	HOR.	VER.
MAX	-1.6	-2.8
AVE	-8.4	-8.1

YZ plane [dBi]



	HOR.	VER.
MAX	-1.3	-8.2
AVE	-7.8	-14.5

ZX plane [dBi]



	HOR.	VER.
MAX	-3.9	-1.8
AVE	-9.6	-8.0

Figure 12 – Directivity for 1MW M.2 Module Mounted on iMX OEM Carrier Board

4.3.2 1MW M.2 Module Standalone

The pictures below illustrate the return loss, efficiency and directivity when the 1MW M.2 module is mounted on the iMX OEM Carrier Board.

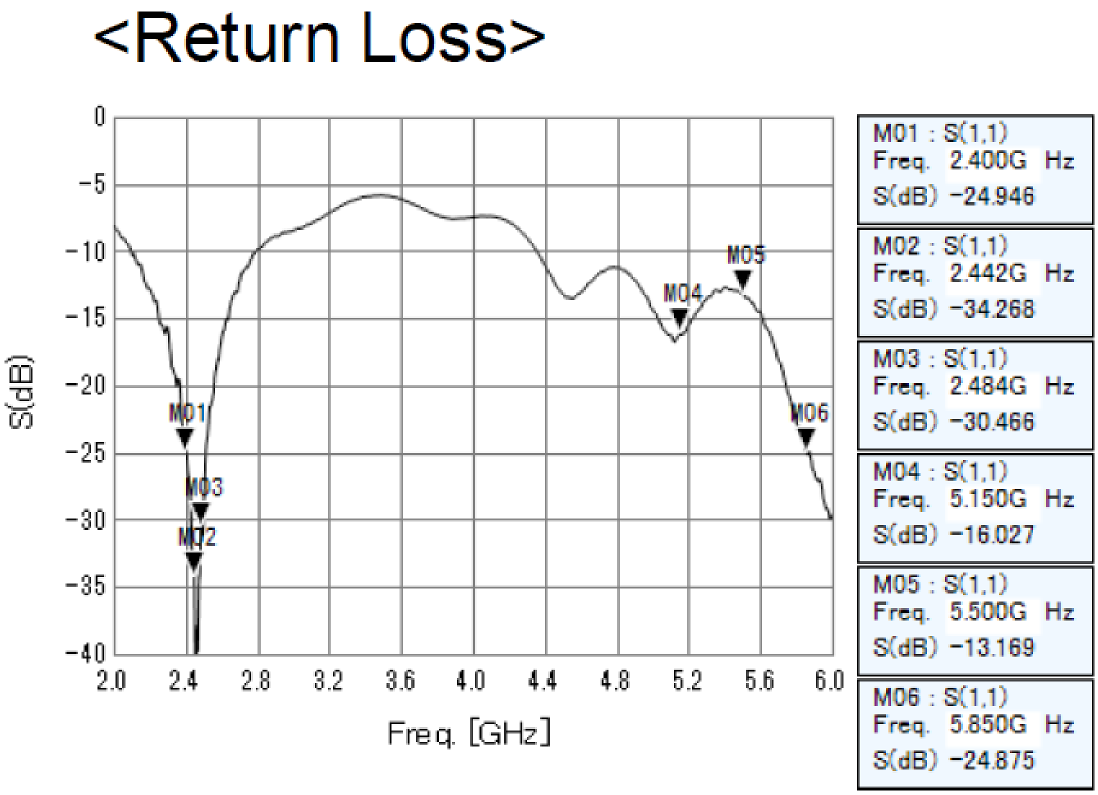


Figure 13 – Return Loss for 1MW M.2 Module Standalone

<Efficiency>

LINEAR POLARIZATION		XY-plane [dBi]		YZ-plane [dBi]		ZX-plane [dBi]		Total Efficiency [dB]
		hor.	ver.	hor.	ver.	hor.	ver.	
2400 MHz	MAX.	-14.9	-1.7	-2.1	-21.1	-2.7	-11.8	
	AVE.	-19.1	-2.9	-6.0	-27.8	-6.3	-13.4	-4.6
2442 MHz	**MAX.**	**-14.9**	**-1.5**	**-2.2**	**-22.2**	**-2.4**	**-11.9**	
	AVE.	**-18.7**	**-2.8**	**-6.1**	**-28.8**	**-6.1**	**-13.4**	**-4.6**
2484 MHz	MAX.	-14.9	-1.5	-2.5	-23.0	-2.4	-11.7	
	AVE.	-19.0	-2.8	-6.1	-29.3	-6.1	-13.4	-4.6

LINEAR POLARIZATION		XY-plane [dBi]		YZ-plane [dBi]		ZX-plane [dBi]		Total Efficiency [dB]
		hor.	ver.	hor.	ver.	hor.	ver.	
5150 MHz	MAX.	-3.5	-3.0	-3.1	-10.5	-5.2	-3.8	
	AVE.	-9.0	-8.0	-6.8	-15.9	-10.1	-6.5	-5.4
5500 MHz	**MAX.**	**-4.5**	**-2.7**	**-2.5**	**-17.5**	**-4.4**	**-3.4**	
	AVE.	**-9.2**	**-7.9**	**-6.4**	**-24.2**	**-9.7**	**-5.7**	**-5.2**
5850 MHz	MAX.	-4.6	-3.2	-2.8	-17.2	-4.3	-3.5	
	AVE.	-9.7	-8.1	-6.4	-23.7	-9.9	-5.7	-5.2

Figure 14 – Efficiency for 1MW M.2 Module Standalone

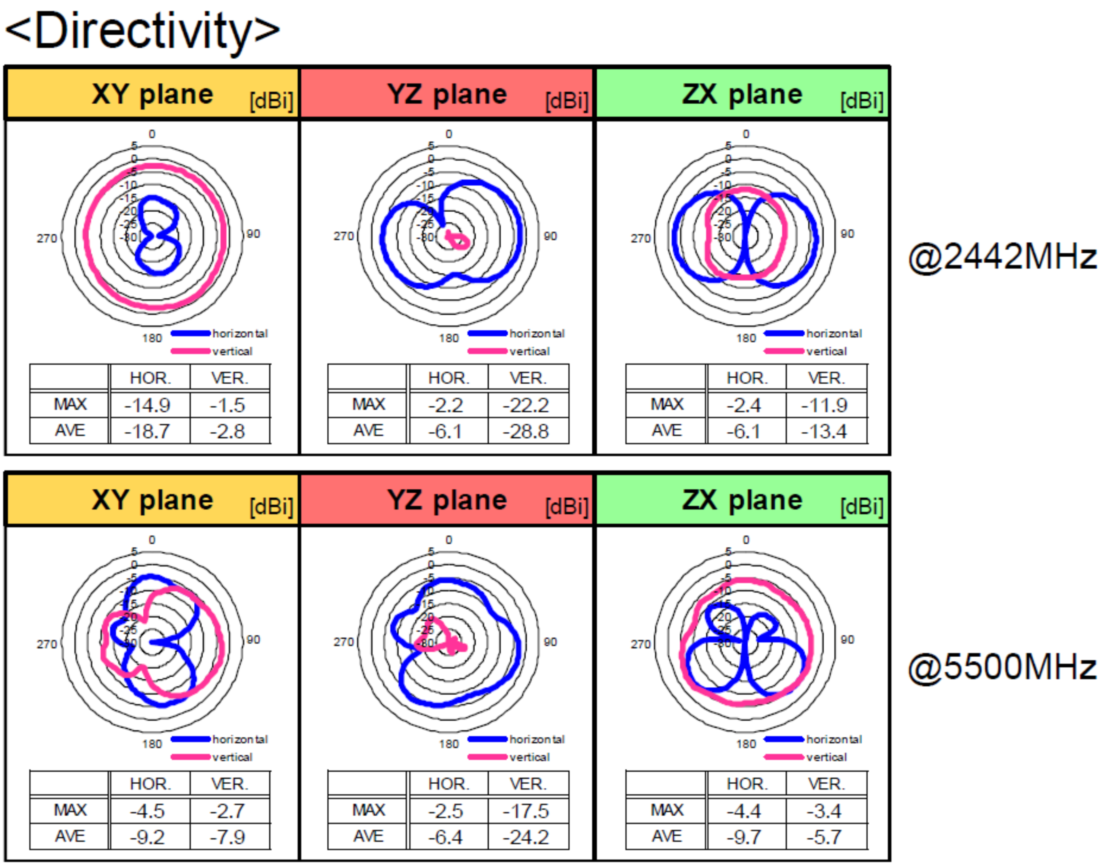


Figure 15 – Directivity for 1MW M.2 Module Standalone

5 Errata

5.1 Audio Interface - PCM CLK Not Connected Correctly

Signal PCM_CLK (on pin 8) is incorrectly routed to pin BT_I2S_CLK (pad 37 on the 1MW) instead of the correct pin BT_PCM_CLK (pad 35 on the 1MW).

The error exist on board revision PA5. The picture below illustrates where to find the board revision identifier. The picture also show how to correct the error - mount a 0402 size zero ohm resistor (or solder bump) in the lower position of SJ12.

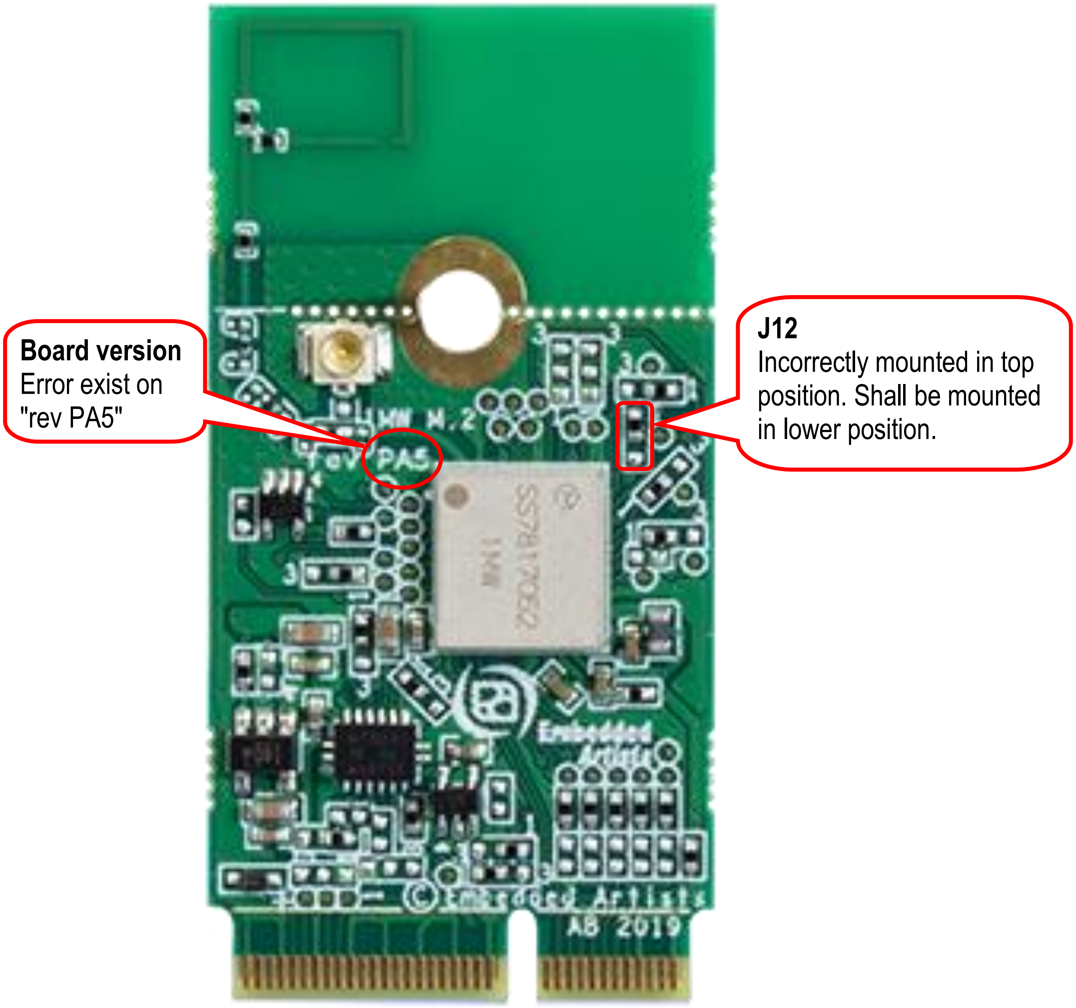


Figure 16 – 1MW M.2 Module J12 Location

6 Regulatory

<TBC>

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