DMOS FULL-BRIDGE MOTOR DRIVERS

Check for Samples: DRV8801-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With The Following Results:**
  - **Device Temperature Grade 1: –40ºC to 125ºC Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C4**
- **Low ON-Resistance [$r_{DS(on)}$] Outputs**
- **Overcurrent Protection**
- **Motor Lead Short-to-Supply Protection**
- **Short-to-Ground Protection**
- **Low-Power Mode**
- **Synchronous Rectification**
- **Diagnostic Output**
- **Internal Undervoltage Lockout (UVLO)**
- **Crossover-Current Protection**
- **16-Pin QFN With PowerPAD™ Package**

APPLICATIONS

- **Automotive Body Systems**
- **Door Locks**
- **HVAC Actuators**
- **Piezo Alarm**

DESCRIPTION

Designed to control dc motors by using pulse-width modulation (PWM), the DRV8801-Q1 is capable of peak output currents up to ±2.8 A and operating voltages up to 36 V.

The PHASE and ENABLE inputs provide dc motor speed and direction control by applying external pulse-width modulation (PWM) and control signals. Internal synchronous rectification control circuitry provides lower power dissipation during PWM operation.

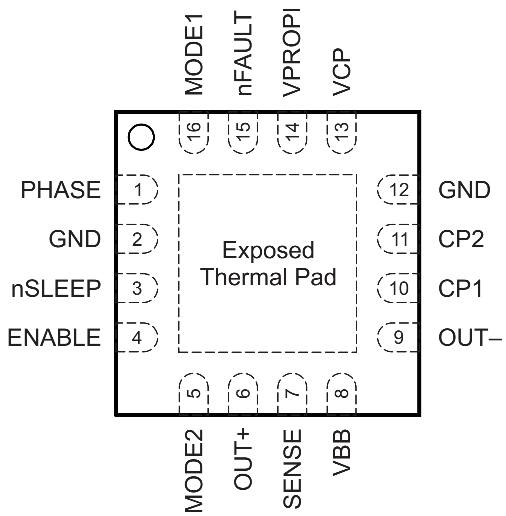
Internal circuit protection includes motor lead short-to-supply and short-to-ground, thermal shutdown with hysteresis, undervoltage monitoring of VBB and VCP, and crossover-current protection.

The DRV8801-Q1 is supplied in a thin-profile 16-pin QFN (RTY) PowerPAD™ package, providing enhanced thermal dissipation.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DRV8801-Q1
RTY PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
CP1	10	Charge-pump capacitor 1
CP2	11	Charge-pump capacitor 2
ENABLE	4	Enable logic input
GND	2, 12	Ground
MODE 1	16	Mode logic input
MODE 2	5	Mode 2 logic input
nFAULT	15	Fault open-drain output
nSLEEP	3	Sleep logic input
OUT+	6	DMOS full-bridge output positive
OUT–	9	DMOS full-bridge output negative
PHASE	1	Phase logic input for direction control
SENSE	7	Sense power return
VBB	8	Load supply voltage
VCP	13	Reservoir capacitor
VPROPI	14	Winding current proportional voltage output
Thermal pad		Exposed pad for thermal dissipation; connect to GND pins.

Figure 1. TYPICAL APPLICATION DIAGRAM

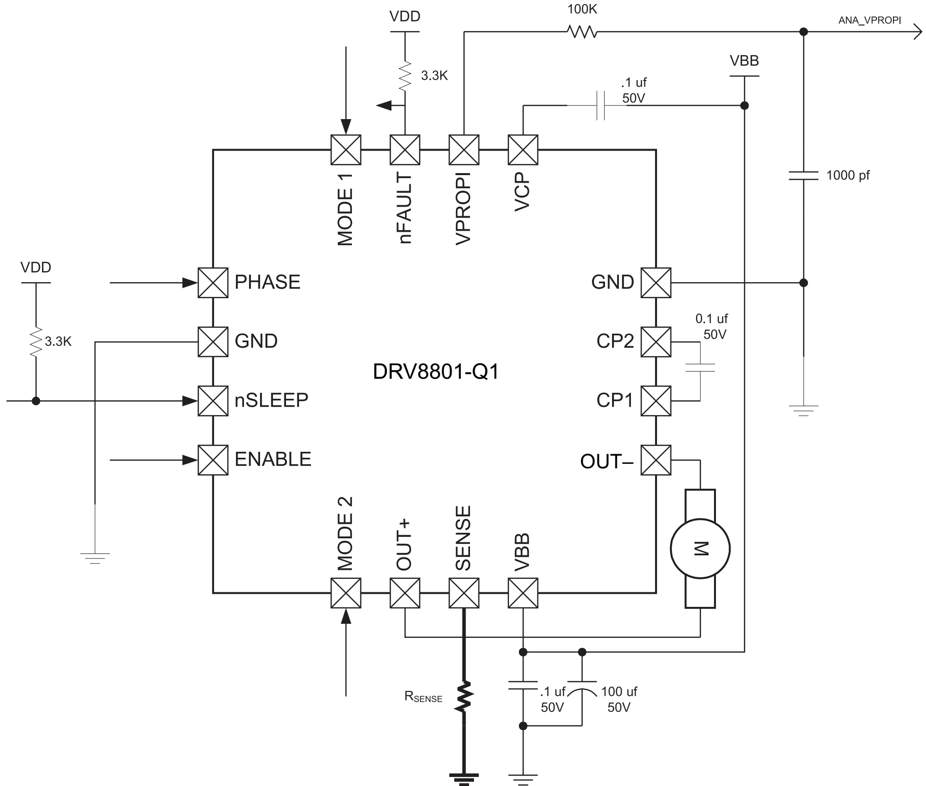
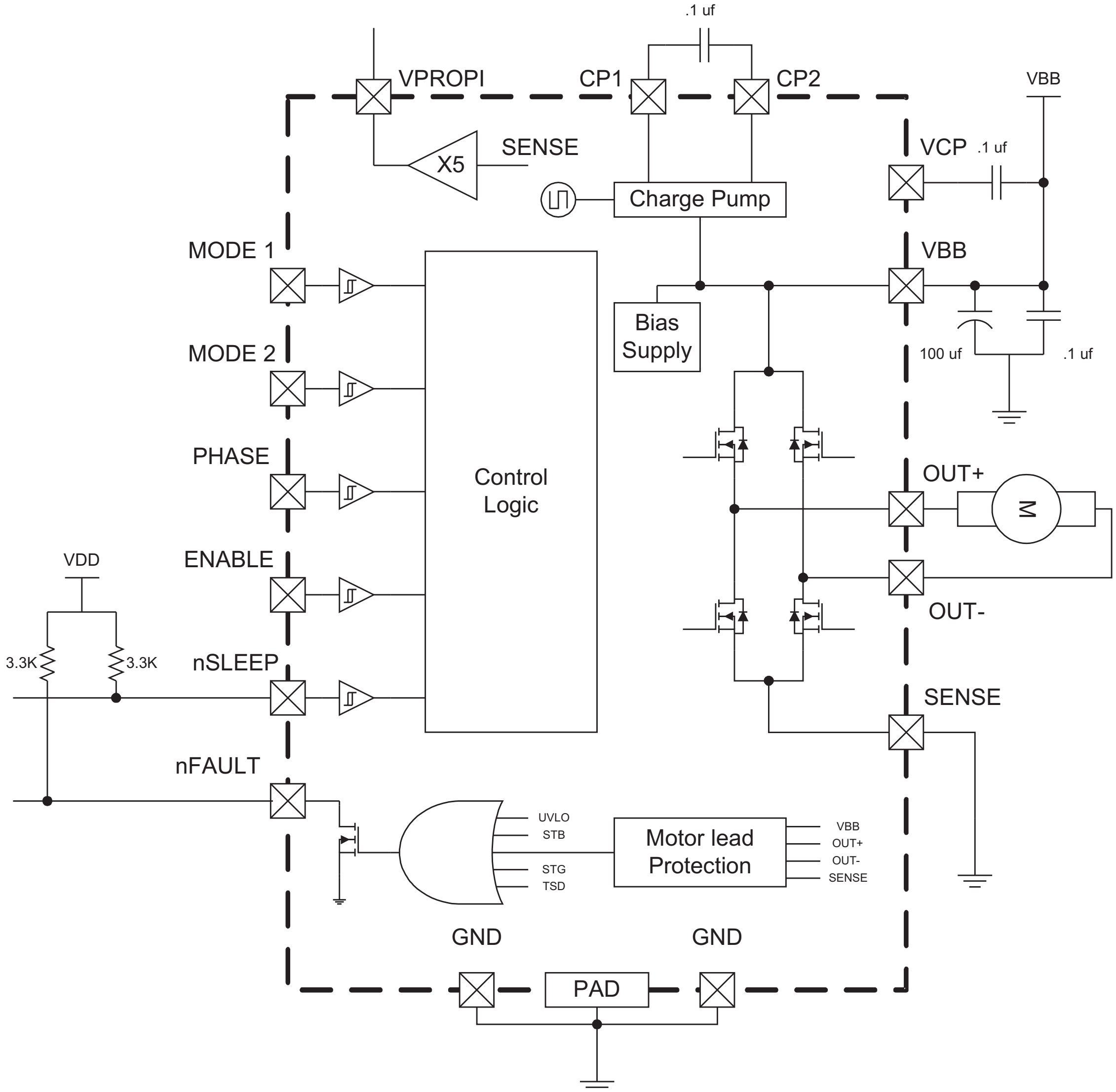


Figure 2. FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VBB	Load supply voltage(2)	–0.3	40	V
	Output current		2.8	A
V_{Sense}	Sense voltage		±500	mV
	VBB to OUTx		36	V
	OUTx to SENSE		36	V
VDD	Logic input voltage(2)	–0.3	7	V
ESD rating	Human-body model (HBM)		±2	kV
	Machine model (MM)		150	V
	Charged-device model (CDM)		750	
	Continuous total power dissipation	See Thermal Information Table		
T_A	Operating free-air temperature range	–40	125	°C
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature range	–40	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

Thermal Information

THERMAL METRIC(1)		DRV8801-Q1 RTY 16 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	38.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	36.7	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	16.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	16.2	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

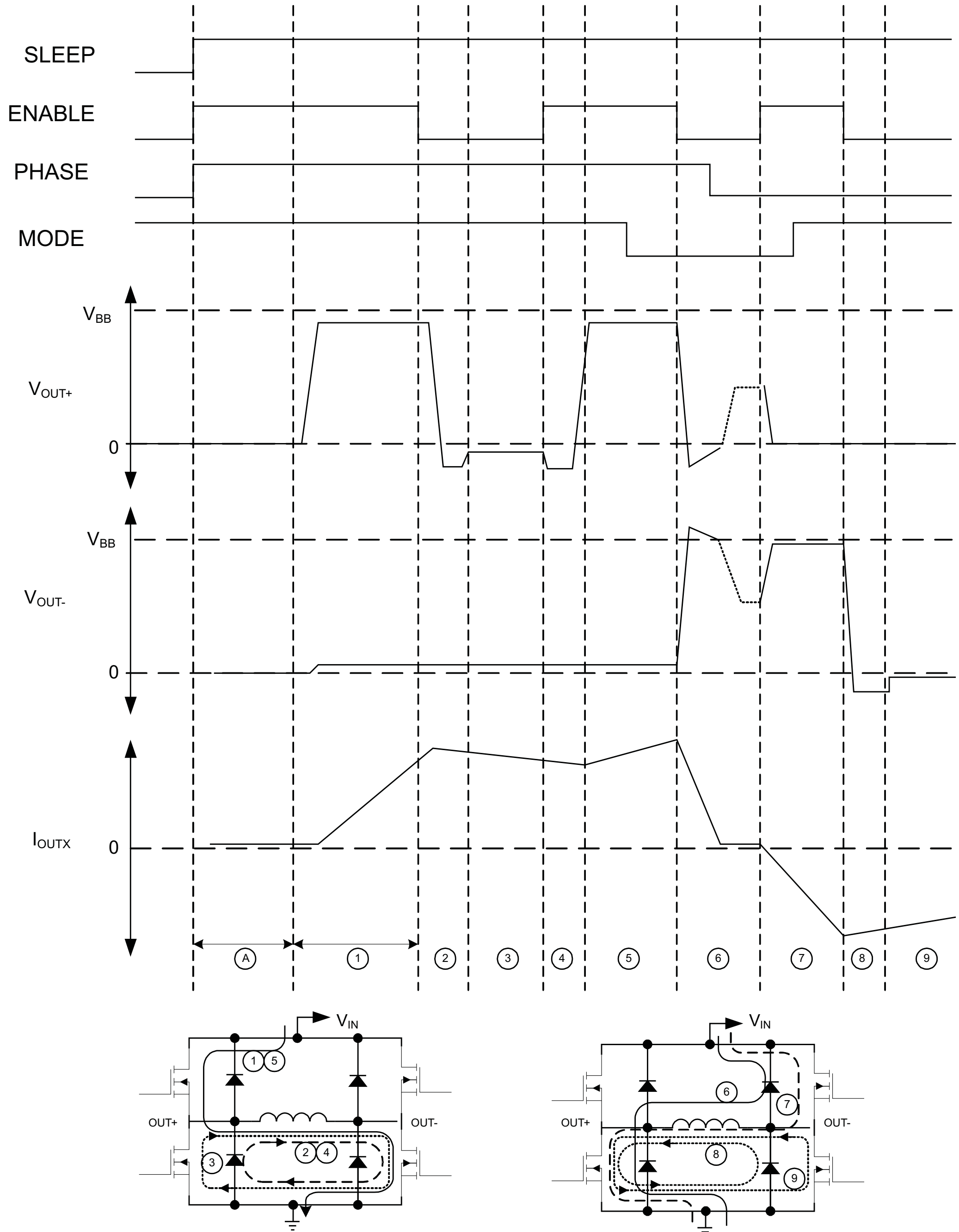
		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, VBB	8	32	38	V
T_A	Operating free-air temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IBB	Motor supply current	f_{PWM} < 50 kHz		6		mA
		Charge pump on, Outputs disabled		3.2		mA
		Sleep mode			10	μA
V_{IH}	PHASE, ENABLE, MODE input voltage		2			V
V_{IL}					0.8	V
V_{IH}	nSLEEP input voltage		2.7			V
V_{IL}					0.8	V
I_{IH}	PHASE, MODE input current	V_{IN} = 2 V		<1.0	20	μA
I_{IL}		V_{IN} = 0.8 V	–20	≤–2.0	20	μA
I_{IH}	ENABLE input current	V_{IN} = 2 V		40	100	μA
I_{IL}		V_{IN} = 0.8 V		16	40	μA
I_{IH}	nSLEEP input current	V_{IN} = 2.7 V		27	50	μA
I_{IL}		V_{IN} = 0.8 V		<1	10	μA
V_{OL}	nFAULT output voltage	I_{sink} = 1 mA			0.4	V
VBBNFR	VBB nFAULT release	8 V < VBB < 40 V		12	13.8	V
V_{IHys}	Input hysteresis, except nSLEEP		100	500	800	mV
$r_{DS(on)}$	Output ON resistance	Source driver, I_{OUT} = –2.8 A, T_J = 25°C		0.48		Ω
		Source driver, I_{OUT} = –2.8 A, T_J = 125°C		0.74	0.85	Ω
		Sink driver, I_{OUT} = 2.8 A, T_J = 25°C		0.35		Ω
		Sink driver, I_{OUT} = 2.8 A, T_J = 125°C		0.52	0.7	Ω
VTRP	RSENSE voltage trip	SENSE connected to ground through a 0.2-Ω resistance		500		mV
V_f	Body diode forward voltage	Source diode, I_f = –2.8 A			1.4	V
		Sink diode, I_f = 2.8 A			1.4	V
t_{pd}	Propagation delay time	PWM, change to source or sink ON		600		ns
		PWM, change to source or sink OFF		100		ns
t_{COD}	Crossover delay			500		ns
DAGain	Differential AMP gain	Sense = 0.1 V to 0.4 V		5		V/V
Protection Circuitry						
VUV	UVLO threshold	VBB increasing		6.5	7.5	V
IOCP	Overcurrent threshold		3			A
t_{DEG}	Overcurrent deglitch time			3		μs
t_{OCP}	Overcurrent retry time			1.2		ms
TJW	Thermal warning temperature	Temperature increasing (1)		160		°C
TJWHys	Thermal warning hysteresis	Recovery = TJW – TJWHys		15		°C
TJTSD	Thermal shutdown temperature	Temperature increasing (2)		175		°C
TJTSDHys	Thermal shutdown hysteresis	Recovery = TJTSD – TJTSDHys		15		°C

(1) Once the device reaches the thermal warning temperature of 160ºC, the device remains in thermal warning until the device cools to 145ºC. This is known as the thermal-warning hysteresis of the device.
(2) Once the device reaches the thermal shutdown temperature of 175ºC, the device remains in thermal shutdown until the device cools to 160ºC. This is known as the thermal-shutdown hysteresis of the device.



(A) Charge Pump and VREG power on delay (~200 us)

Figure 3. PWM Control Timing

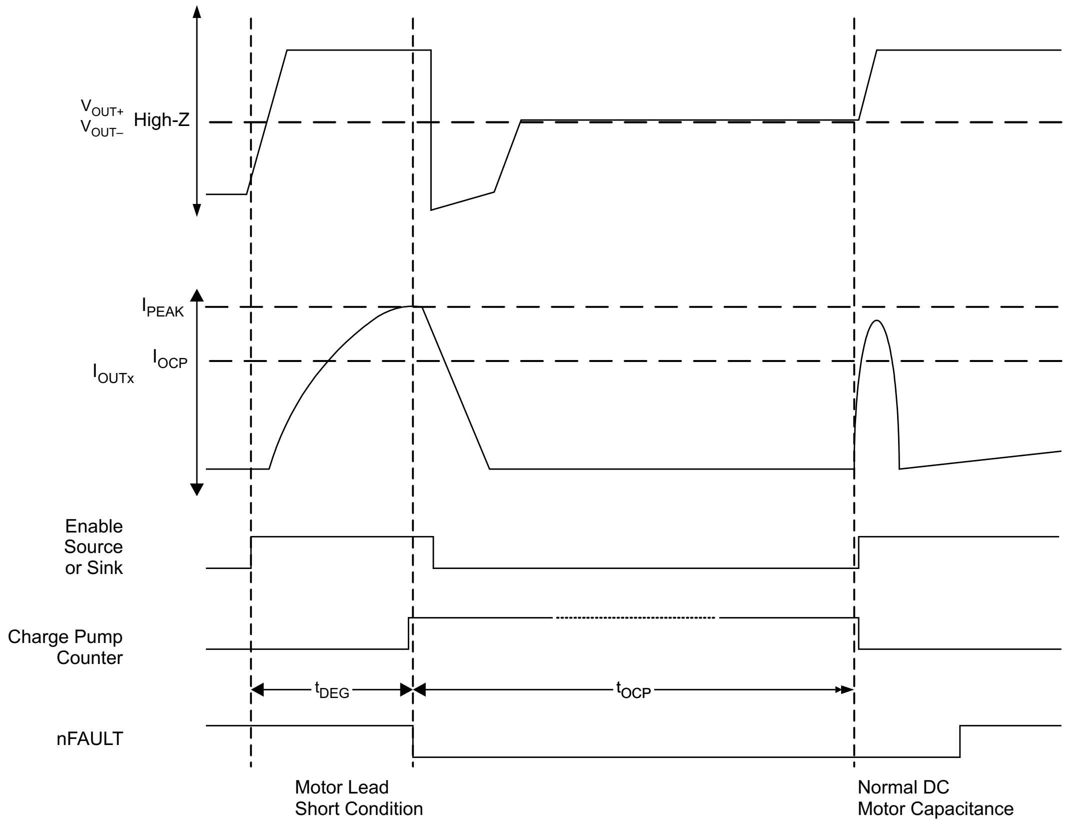


Figure 4. Overcurrent Control Timing

FUNCTIONAL DESCRIPTION

Device Operation

The DRV8801-Q1 is designed to drive one dc motor. The current through the output full-bridge switches and all N-channel DMOS are regulated with a fixed off-time PWM control circuit.

Logic Inputs

TI recommends using a high-value pullup resistor when logic inputs are pulled up to V_{DD}. This resistor limits the current to the input in case an overvoltage event occurs. Logic inputs are nSLEEP, MODE, PHASE, and ENABLE. Voltages higher than 7 V on any logic input can cause damage to the input structure.

VPROPI

This output offers an analog voltage proportional to the winding current. Voltage at this terminal is five times greater than the motor winding current (VPROPI = 5 × I). VPROPI is meaningful only if there is a resistor connected to the SENSE pin. If SENSE is connected to ground, VPROPI measures 0 V. During slow decay, VPROPI outputs 0 V. VPROPI can output a maximum of 2.5 V, because at 500 mV on SENSE, the H-bridge is disabled.

Charge Pump

The charge pump is used to generate a supply above VBB to drive the source-side DMOS gates. A 0.1-µF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1-µF ceramic monolithic capacitor, CStorage, should be connected between VCP and VBB to act as a reservoir to run the high-side DMOS devices. The VCP voltage level is internally monitored and, in the case of a fault condition, the outputs of the device are disabled.

Shutdown

As a measure to protect the device, faults caused by very high junction temperatures or low voltage on VCP disable the outputs of the device until the fault condition is removed. At power on, the UVLO circuit disables the drivers.

Low-Power Mode

Control input nSLEEP is used to minimize power consumption when the DRV8801-Q1 is not in use. This disables much of the internal circuitry, including the internal voltage rails and charge pump. nSLEEP is asserted low. A logic high on this input pin results in normal operation. When switching from low to high, the user should allow a 1-ms delay before applying PWM signals. This time is needed for the charge pump to stabilize.

- MODE 1

  Input MODE 1 is used to toggle between fast-decay mode and slow-decay mode. A logic high puts the device in slow-decay mode.

- MODE 2

  MODE 2 is used to select which set of drivers (high side versus low side) is used during the slow-decay recirculation. MODE 2 is meaningful only when MODE 1 is asserted high. A logic high on MODE 2 has current recirculation through the high-side drivers. A logic low has current recirculation through the low-side drivers.

Braking

The braking function is implemented by driving the device in slow-decay mode (MODE 1 pin is high) and deasserting the enable to low. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts out the motor-generated BEMF as long as the ENABLE chop mode is asserted. The maximum current can be approximated by VBEMF/RL. Care should be taken to ensure that the maximum ratings of the device are not exceeded in worst-case braking situations – high-speed and high-inertia loads.

Diagnostic Output

The nFAULT pin signals a problem with the chip via an open-drain output. A motor fault, undervoltage condition, or T_J > 160°C drives the pin low. This output is not valid when nSLEEP puts the device into minimum-power-dissipation mode (such as, nSLEEP is low). nFAULT stays asserted (nFAULT = L) until VBB reaches VBBNFR to give the charge pump headroom to reach its undervoltage threshold. nFAULT is a status-only signal and does not affect any device functionality. The H-bridge portion still operates normally down to VBB = 8 V with nFAULT asserted.

Thermal Shutdown (TSD)

Two die-temperature monitors are integrated on the chip. As die temperature increases toward the maximum, a thermal warning signal is triggered at 160°C. This fault drives nFAULT low, but does not disable the operation of the chip. If the die temperature increases further, to approximately 175°C, the full-bridge outputs are disabled until the internal temperature falls below a hysteresis of 15°C.

Control Logic Table(1)

PINS							OPERATION
PHASE	ENABLE	MODE 1	MODE 2	nSLEEP	OUT+	OUT–	
1	1	X	X	1	H	L	Forward
0	1	X	X	1	L	H	Reverse
X	0	1	0	1	L	L	Brake (slow decay)
X	0	1	1	1	H	H	Brake (slow decay)
1	0	0	X	1	L	H	Fast-decay synchronous rectification(2)
0	0	0	X	1	H	L	Fast-decay synchronous rectification(2)
X	X	X	X	0	Z	Z	Sleep mode

(1) X = don't care, Z = high impedance
(2) To prevent reversal of current during fast-decay synchronous rectification, outputs go to the high-impedance state as the current approaches 0 A.

Overcurrent Protection

The current flowing through the high-side and low-side drivers is monitored to ensure that the motor lead is not shorted to supply or ground. If a short is detected, the full-bridge outputs are turned off, flag nFAULT is driven low, and a 1.2-ms fault timer is started. After this 1.2-ms period, t_{OCP}, the device is then allowed to follow the input commands and another turnon is attempted (nFAULT becomes high again during this attempt). If there is still a fault condition, the cycle repeats. If after t_{OCP} expires it is determined the short condition is not present, normal operation resumes and nFAULT is deasserted.

APPLICATION INFORMATION

Power Dissipation

First-order approximation of power dissipation in the DRV8801-Q1 can be calculated by examining the power dissipation in the full-bridge during each of the operation modes. DRV8801-Q1 uses synchronous rectification. During the decay cycle, the body diode is shorted by the low-$r_{DS(on)}$ driver, which in turn reduces power dissipation in the full-bridge. In order to prevent shootthrough (high-side and low-side drivers on the same side are ON at the same time), DRV8801-Q1 implements a 500-ns typical crossover delay time. During this period, the body diode in the decay current path conducts the current until the DMOS driver turns on. High-current and high-ambient-temperature applications should take this into consideration. In addition, motor parameters and switching losses can add power dissipation that could affect critical applications.

Drive Current

This current path is through the high-side sourcing DMOS driver, motor winding, and low-side sinking DMOS driver. Power dissipation I^2R loses in one source and one sink DMOS driver, as shown in Equation 1.

$$P_D = I^2 (r_{DS(on)Source} + r_{DS(on)Sink}) \quad (1)$$

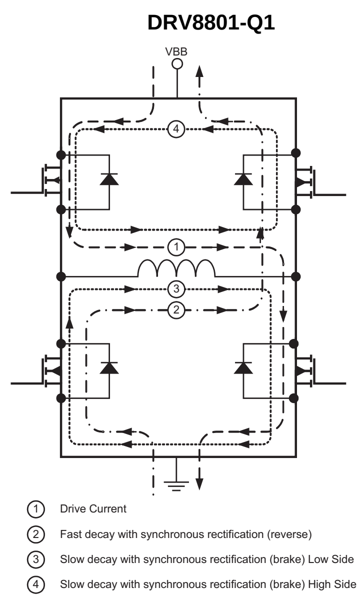


Figure 5. Current Path

Fast Decay With Synchronous Rectification

This decay mode is equivalent to a phase change where the opposite drivers are switched on. When in fast decay, the motor current is not allowed to go negative (direction change). Instead, as the current approaches zero, the drivers turn off. The power calculation is the same as the drive-current calculation (see Equation 1).

Slow-Decay SR (Brake Mode)

In slow-decay mode, both low-side sinking drivers turn on, allowing the current to circulate through the low side of the H-bridge (two sink drivers) and the load. Power dissipation I^2R loses in the two sink DMOS drivers:

$$P_D = I^2 (2 \times r_{DS(on)Sink}) \tag{2}$$

SENSE

A low-value resistor can be placed between the SENSE pin and ground for current-sensing purposes. To minimize ground-trace IR drops in sensing the output current level, the current-sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low-value sense resistors, the IR drops in the PCB can be significant, and should be taken into account.

NOTE

When selecting a value for the sense resistor, SENSE does not exceed the maximum voltage of ±500 mV. The H-bridge is disabled and enters recirculation while the motor winding current generates a SENSE voltage greater than or equal to 500 mV.

Ground

A ground power plane should be located as close to the DRV8801-Q1 as possible. The copper ground plane directly under the thermal pad makes a good location. This pad can then be connected to ground for this purpose.

Layout

The printed circuit board (PCB) should use a heavy ground plane. For optimum electrical and thermal performance, the DRV8801-Q1 must be soldered directly onto the board. On the underside of the DRV8801-Q1 is a thermal pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB. For more information on this technique, see document SLMA002.

The load supply pin, VBB, should be decoupled with an electrolytic capacitor (typically 100 μF) in parallel with a ceramic capacitor placed as close as possible to the device. The ceramic capacitors between VCP and VBB, connected to VREG, and between CP1 and CP2 should be as close to the pins of the device as possible, in order to minimize lead inductance.

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8801QRTYRQ1	ACTIVE	QFN	RTY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV 8801Q	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF DRV8801-Q1 :

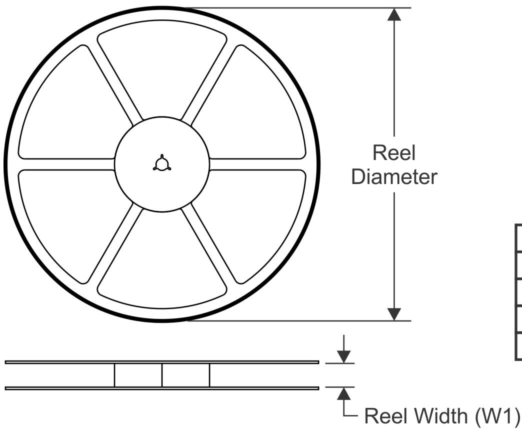
- Catalog: DRV8801

NOTE: Qualified Version Definitions:

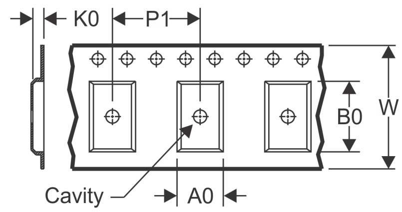
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

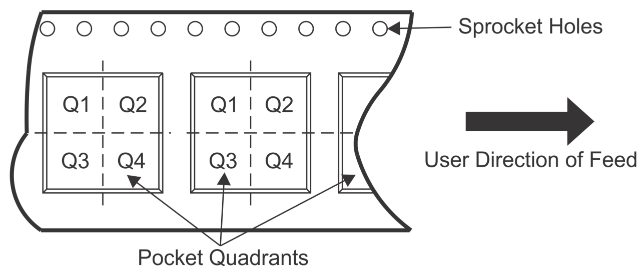


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

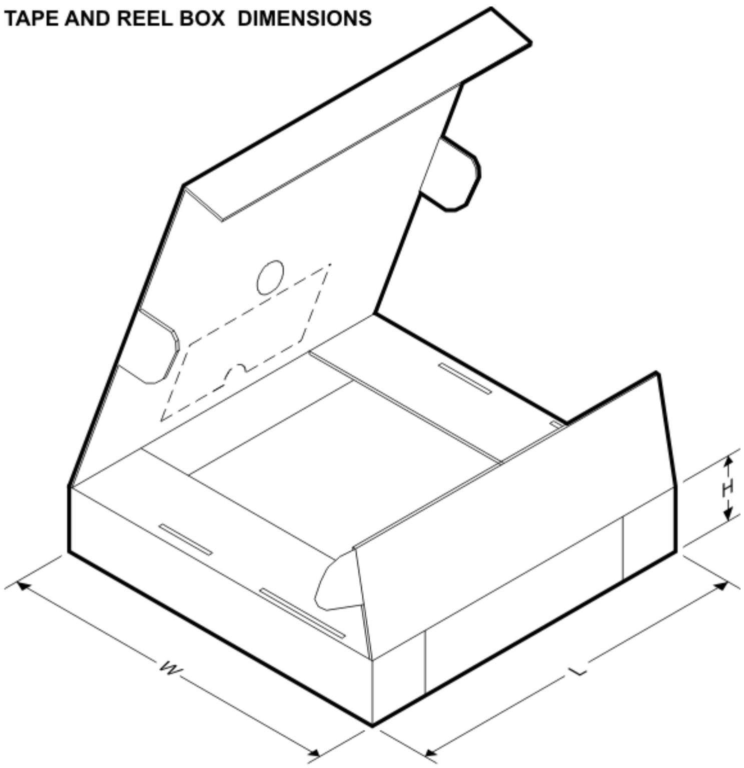
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8801QRTYRQ1	QFN	RTY	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

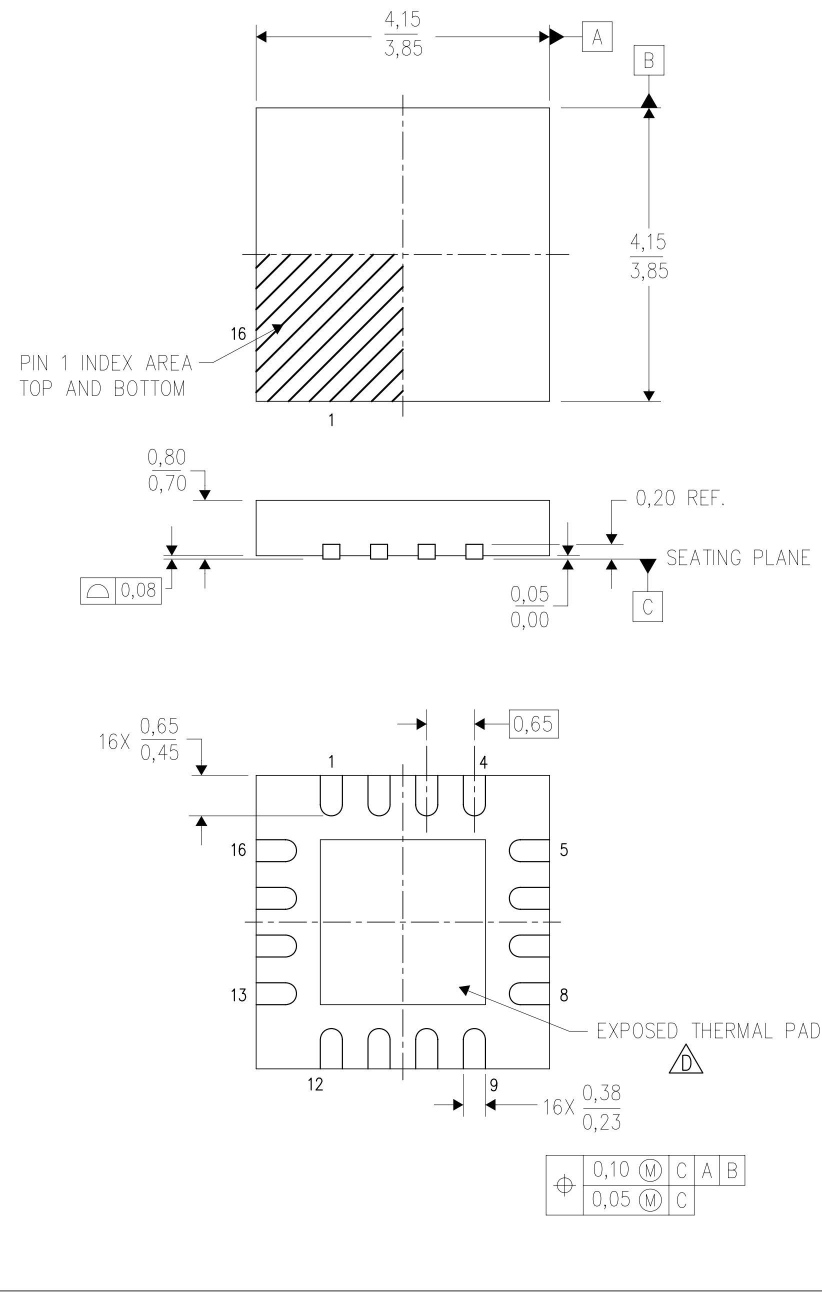
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8801QRTYRQ1	QFN	RTY	16	3000	367.0	367.0	35.0

RTY (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

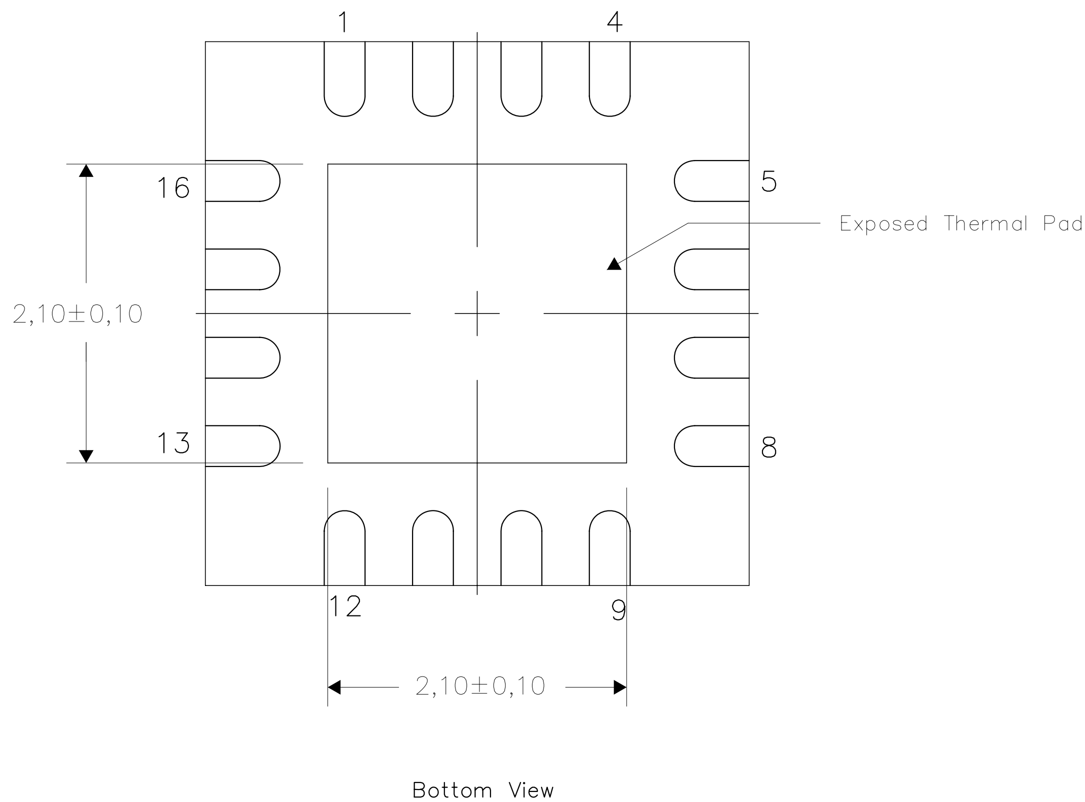
RTY (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

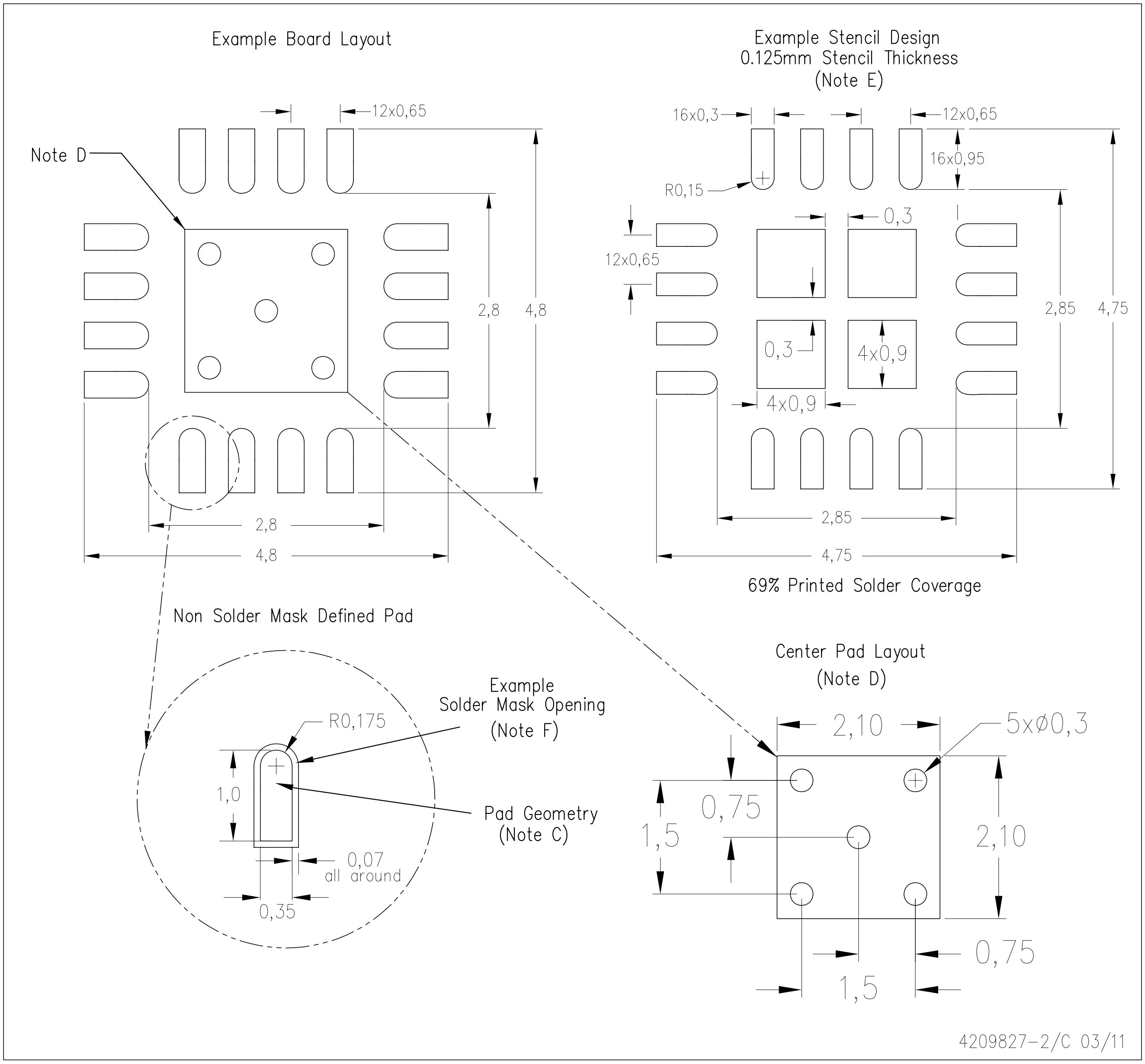


Exposed Thermal Pad Dimensions

4206277-2/E 03/11

NOTE: A. All linear dimensions are in millimeters

RTY (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

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