

DRV2604L 2 to 5.2 V Haptic Driver for LRA and ERM With Internal Memory and Smart-Loop Architecture

1 Features

- Flexible Haptic and Vibration Driver
 - LRA (Linear Resonance Actuator)
 - ERM (Eccentric Rotating Mass)
 - I²C-Controlled Digital Playback Engine
 - Waveform Sequencer and Trigger
 - Real-Time Playback Mode through I²C
 - Internal RAM for Customized Waveforms
 - I²C Dual-Mode Drive (Open and Closed Loop)
 - Smart-Loop Architecture⁽¹⁾
 - Automatic Overdrive and Braking
 - Automatic Resonance Tracking and Reporting (LRA Only)
 - Automatic Actuator Diagnostic
 - Automatic Level Calibration
 - Wide Support for Actuator Models
 - Immersion TouchSense[®] 3000 Compatible
 - Drive Compensation Over Battery Discharge
 - Wide Voltage Operation (2 V to 5.2 V)
 - Efficient Differential Switching Output Drive
 - PWM Input With 0% to 100% Duty-Cycle Control Range
 - Hardware Trigger Input
 - Fast Start-up Time
 - 1.8 V Compatible, V_{DD}-Tolerant Digital Interface
- ⁽¹⁾ Patent pending control algorithm

2 Applications

- Mobile Phones
- Tablets

3 Description

The DRV2604L device is a low-voltage haptic driver that provides a closed-loop actuator-control system for high-quality haptic feedback for ERM and LRA. This schema helps improve actuator performance in terms of acceleration consistency, start time, and brake time and is accessible through a shared I²C compatible bus or PWM input signal.

The DRV2604L device includes enough integrated RAM to allow the user to pre-load over 100 customized smart-loop architecture waveforms. These waveforms can be instantly played back through I²C or optionally triggered through a hardware trigger terminal.

Additionally, the real-time playback mode allows the host processor to bypass the memory playback engine and play waveforms directly from the host through I²C.

The smart-loop architecture inside the DRV2604L device allows simple auto-resonant drive for the LRA as well as feedback-optimized ERM drive allowing for automatic overdrive and braking. This architecture creates a simplified input waveform interface as well as reliable motor control and consistent motor performance. The DRV2604L device also features automatic transition to an open-loop system in the event that an LRA actuator is not generating a valid back-EMF voltage. When the LRA generates a valid back-EMF voltage, the DRV2604L device automatically synchronizes with the LRA. The DRV2604L also allows for open-loop driving through the use of internally-generated PWM.

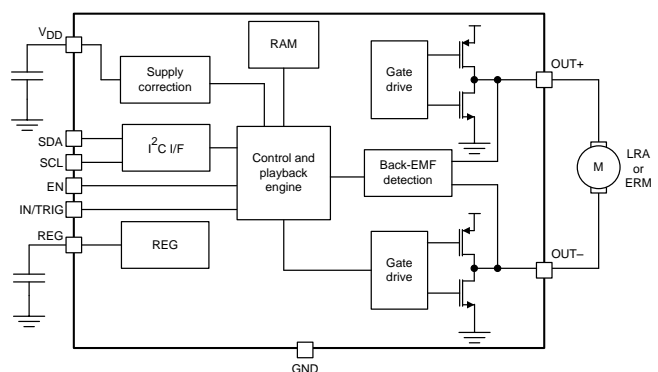
For the full data sheet, go to ti.com/product/DRV2604L and select the *Request Full Datasheet* link.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (MAX)
DRV2604L	DSBGA (9)	1.50 mm x 1.50 mm
DRV2604L	VSSOP (10)	3.00 mm x 3.00 mm

⁽¹⁾ For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2014) to Revision C Page

- Added VSSOP package option 3
 - Added IN/TRIG pin connection to GND required if not used..... 3
-

Changes from Revision A (May 2014) to Revision B Page

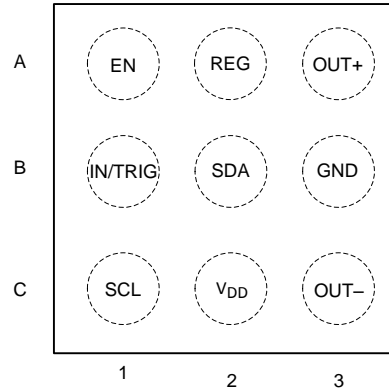
- Changed the view listed for the DSBGA package drawing from bottom to top..... 3
-

Changes from Original (May 2014) to Revision A Page

- Updated the description text, added the TouchSense feature to the *Features* list, and removed all applications except for mobile phones and tablets from the *Applications* list 1
 - Added *Pin Configuration and Functions* section 3
-

5 Pin Configuration and Functions

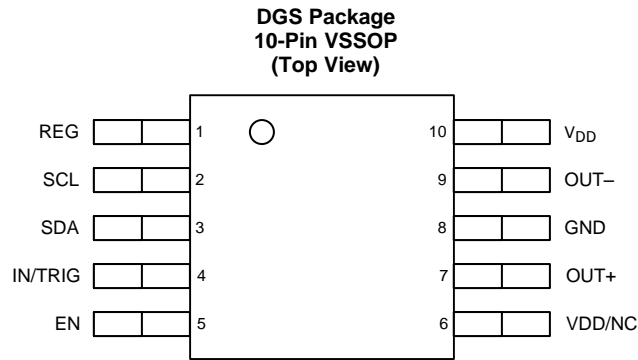
**YZF Package
9-Pin DSBGA With 0,5-mm Pitch
(Top View)**



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
A1	EN	I	Device enable
A2	REG	O	The REG pin is the 1.8-V regulator output. A 1- μ F capacitor is required.
A3	OUT+	O	Positive haptic driver differential output
B1	IN/TRIG	I	Multi-mode Input. I ² C selectable as PWM, analog, or trigger. If not used, this pin should be connected to GND
B2	SDA	I/O	I ² C data
B3	GND	P	Supply ground
C1	SCL	I	I ² C clock
C3	OUT-	O	Negative haptic-driver differential output
C2	V _{DD}	P	Supply input (2 to 5.2 V). A 1- μ F capacitor is required.

(1) I = input, O = output, I/O = input and output, P = power



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	REG	O	The REG pin is the 1.8-V regulator output. A 1- μ F capacitor required
2	SCL	I	I ² C clock
3	SDA	I/O	I ² C data
4	IN/TRIG	I	Multi-mode Input. I ² C selectable as PWM, analog, or trigger. If not used, this pin should be connected to GND
5	EN	I	Device enable
6	V _{DD} /NC	P	Optional supply input. This pin should be tied to V _{DD} or left floating.
7	OUT+	O	Positive haptic driver differential output
8	GND	P	Supply ground
9	OUT-	O	Negative haptic driver differential output
10	V _{DD}	P	Supply Input (2to 5.2 V). A 1- μ F capacitor is required.

(1) I = input, O = output, I/O = input and output, P = power

6 Device and Documentation Support

6.1 Trademarks

TouchSense is a registered trademark of Immersion Corporation. All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV2604LDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	04L	Samples
DRV2604LDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	04L	Samples
DRV2604LYZFR	ACTIVE	DSBGA	YZF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	2604L	Samples
DRV2604LYZFT	ACTIVE	DSBGA	YZF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	2604L	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2604LDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DRV2604LDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DRV2604LYZFR	DSBGA	YZF	9	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
DRV2604LYZFT	DSBGA	YZF	9	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

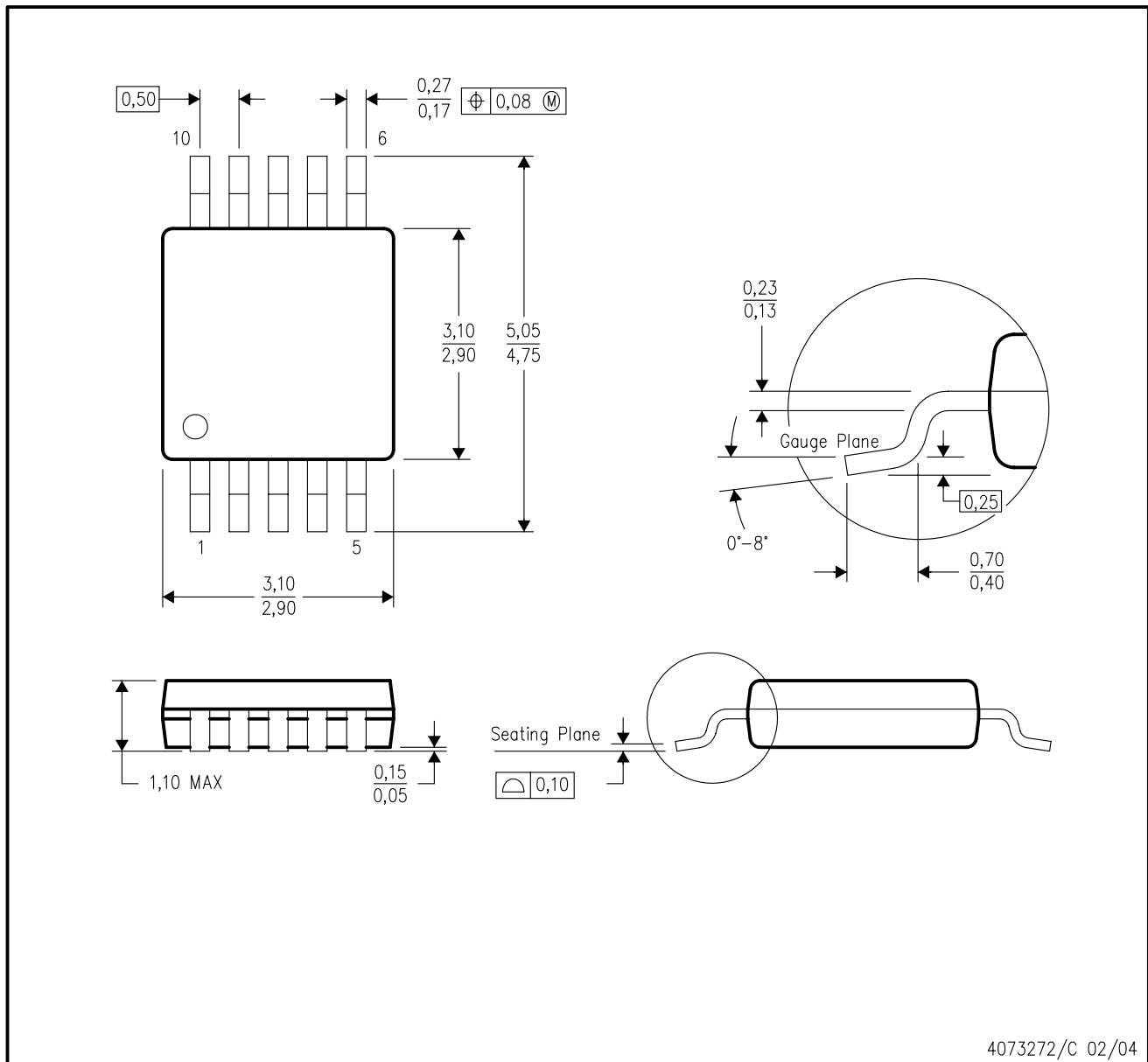
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2604LDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
DRV2604LDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
DRV2604LYZFR	DSBGA	YZF	9	3000	182.0	182.0	17.0
DRV2604LYZFT	DSBGA	YZF	9	250	182.0	182.0	17.0

DGS (S-PDSO-G10)

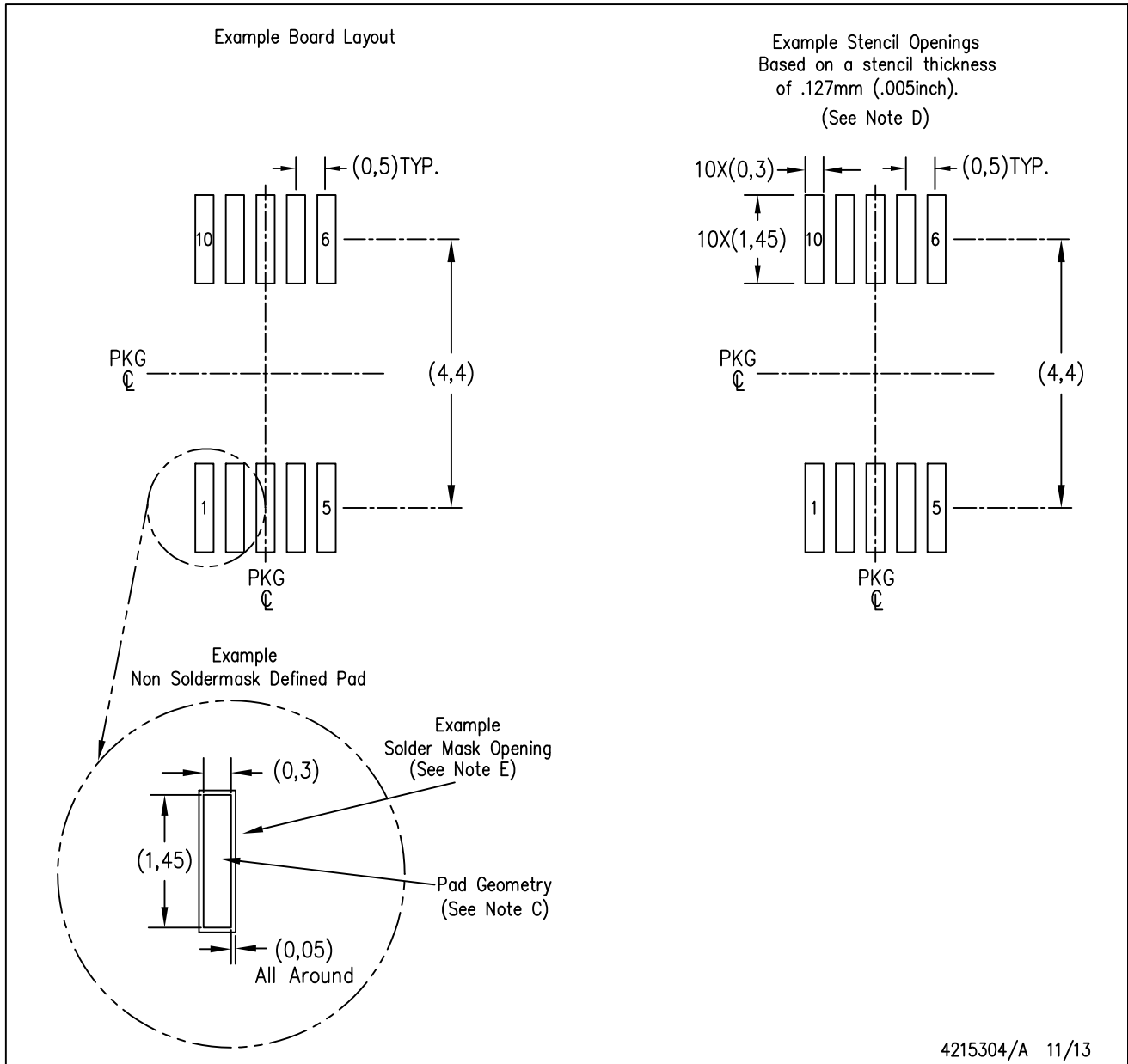
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

DGS (S-PDSO-G10)

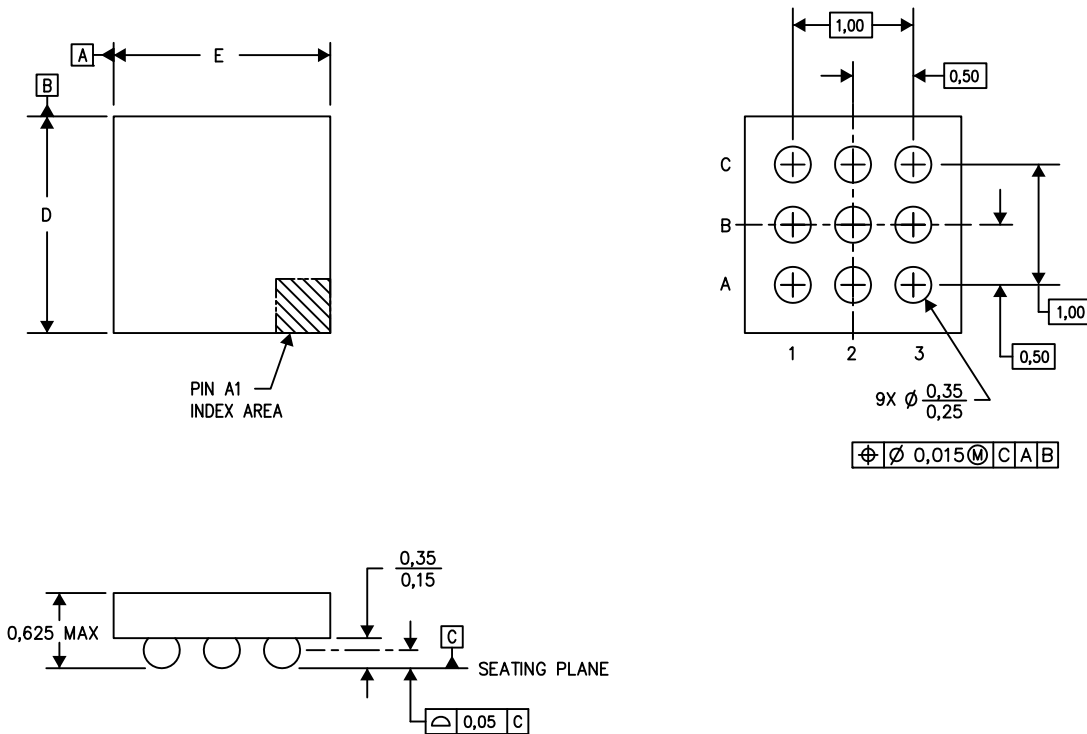
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZF (S-XBGA-N9)

DIE-SIZE BALL GRID ARRAY



D: Max = 1.47 mm, Min = 1.41 mm
 E: Max = 1.47 mm, Min = 1.41 mm

4205058-4/P 07/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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