Lead-free Green

DM1231-02SO

2-CHANNEL LOW CAPACITANCE ESD PROTECTION ARRAY

Product Summary

$V_{F\ (Typ)}$	$V_{P\ (Typ)}$	$C_{OUT\ (Typ)}$
0.8V	5V	1.5pF

Description

DM1231-02SO is a high-performance device suitable for protecting two high-speed channels. This product is assembled in SOT26 package. It has high ESD surge capability and low capacitance.

Applications

Typically Used for High Speed Ports such as:

- USB 2.0
- IEEE1394
- HDMI
- Laptop and Personal Computers
- Flat Panel Displays
- Video Graphics Displays
- SIM Ports

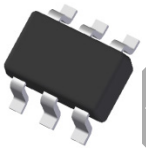
Features

- Contact discharge per IEC61000-4-2 standard: ±12 kV (OUT Pins), ±4 kV(IN Pins)
- Withstands over 1000 ESD Strikes
- 1.5pF Typical Capacitance from OUT to V_N
- Two channels of ESD Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

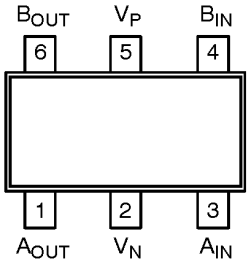
Mechanical Data

- Case: SOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020 (Lead Free Plating). Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.016 grams (Approximate)

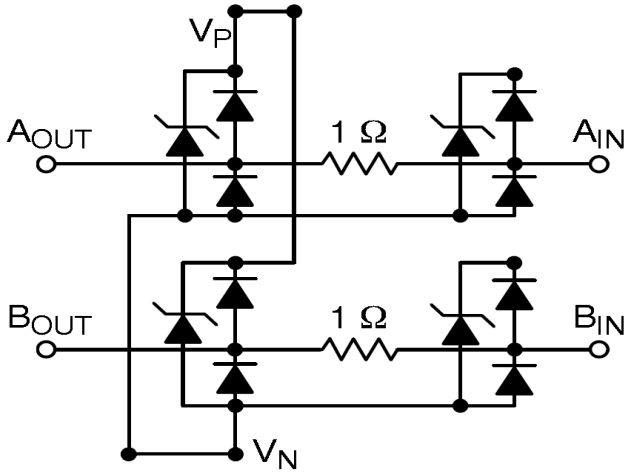
SOT26



Top View



PINOUT Diagrams



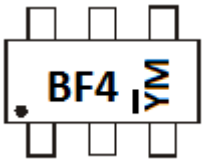
Device

Ordering Information (Note 4)

Product	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DM1231-02SO-7	Standard	BF4	7	8	3000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



BF4= Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: D = 2016)
M = Month (ex: 9 = September)
Note: "▬" represents internal code

Date Code Key

Year	2015	2016	2017	2018	2019	2020
Code	C	D	E	F	G	H

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Value	Unit
Operating Supply Voltage (V_P)	6	V
Diode Forward Current(A_{OUT}/B_{OUT} Side)	8	mA
Continuous Current through Signal Pins (IN to OUT) 1,000 hours	125	mA
ESD Protection – Contact Discharge (Note5)	±12	kV
	±4	kV

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 6)	P_D	300	mW
Thermal Resistance, Junction to Ambient Typical (Note 6)	$R_{\theta JA}$	417	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	ºC

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Operating Supply Voltage	V_P	—	5	5.5	V	—
Reverse Current (Note 7)	I_R	—	—	1	μA	V_P = 5V, V_P to V_N
Diode Forward Voltage	V_F	0.6	0.8	0.95	V	I_F = 8mA, Top Diode
Diode Forward Voltage	V_F	0.6	0.8	0.95	V	I_F = 8mA, Bottom Diode
Residual ESD Peak Current on RDUP(Resistance of Device Under Protection)	I_{RES}	—	2.3	—	A	IEC 61000-4-2 contact mode 8kV, RDUP = 5Ω
Channel Clamping Voltage (Note 8)	$V_{CL\_Positive}$	—	+9	—	V	I_{PP} =1A, tp = 8/20μs
	$V_{CL\_Negative}$	—	-1.4	—	V	Zap at OUT, Measure at IN
Dynamic Resistance	$R_{DYN\_Positive}$	—	0.4	—	Ω	I_{PP} =1A, tp = 8/20μs
	$R_{DYN\_Negative}$	—	0.3	—	Ω	Zap at OUT, Measure at IN
Channel Input Capacitance(Note 9)	C_{OUT}	—	1.5	—	pF	f = 1MHz, V_P = 5V, V_{OSC} = 2.5V, V_{OSC} = 30mV
Channel to Channel Capacitance Match	ΔC_{OUT}	—	0.02	—	pF	f = 1MHz, V_P = 5V, V_{OSC} = 2.5V, V_{OSC} = 30mV
Series Resistance	R_S	—	1	—	Ω	—
Channel to Channel Resistance Match	ΔR_S	—	±10	±30	mΩ	—

Notes:
5. Standard test condition is IEC61000-4-2 level 4 test circuit with each (AOUT/BOUT) pin subjected to ±12kV contact discharge for 1000 pulses. **Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run.**
6. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes, Inc. suggested pad layout, which can be found on our website at http://www.diodes.com/package-outlines.html.
7. Short duration pulse test used to minimize self-heating effect.
8. Clamping voltage value is based on an 8x20μs peak pulse current (I_{pp}) waveform.
9. Capacitance measured from V_{OUT} to V_N with V_{IN} floating.

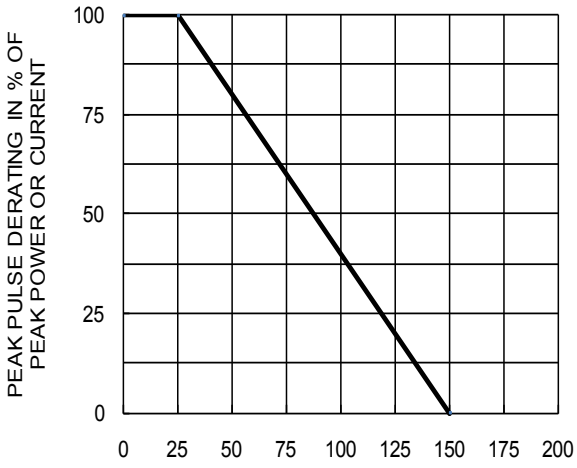


Figure1. Pulse Derating Curve

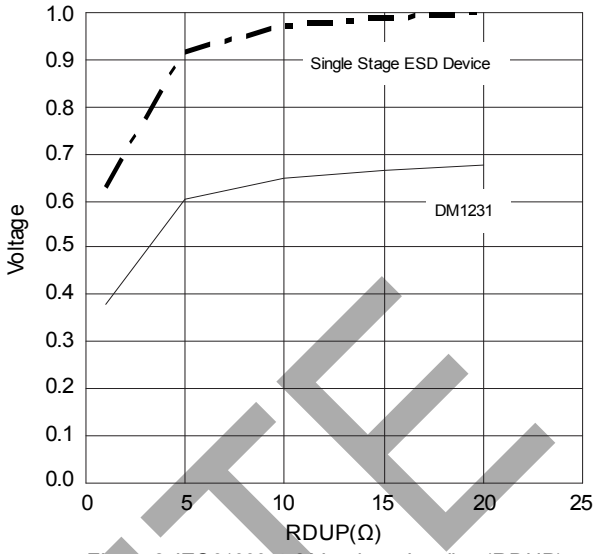


Figure 2. IEC61000-4-2 Vpeak vs. Loading (RDUP)

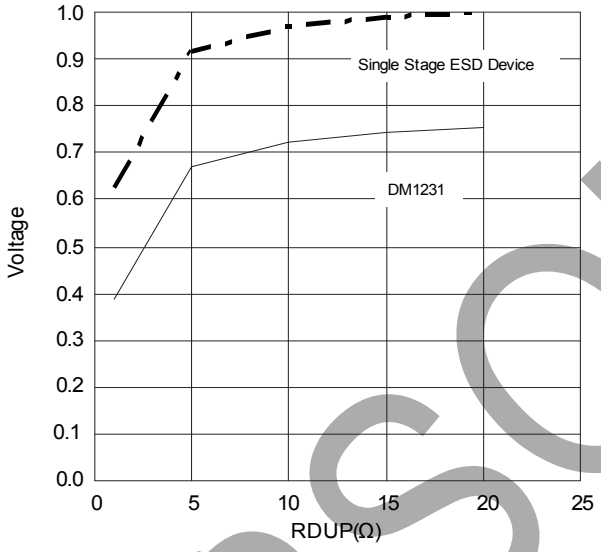


Figure 3. IEC61000-4-2 Vclamp vs. Loading (RUDP)

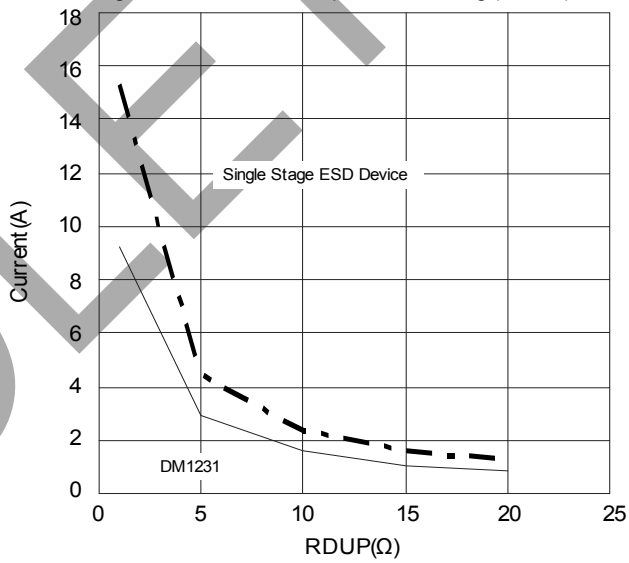


Figure 4. IEC61000-4-2
I_{RES} (Residual ESD Peak Current) vs. Loading (RDUP)

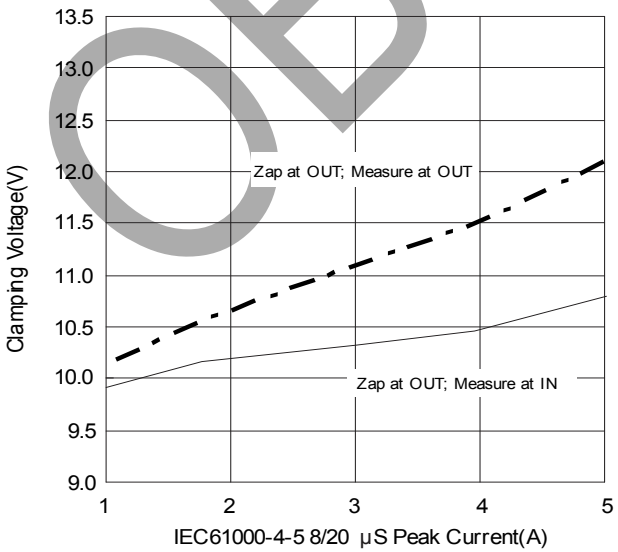


Figure 5. Clamping Voltage vs.Peak Current

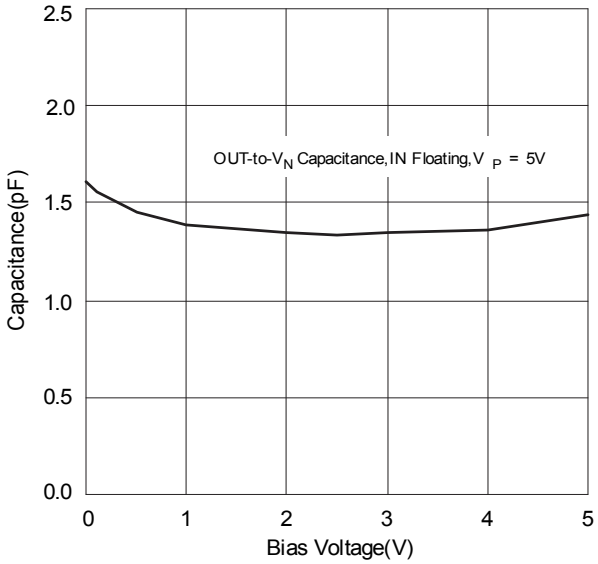


Figure 6. Capacitance vs. Bias Voltage

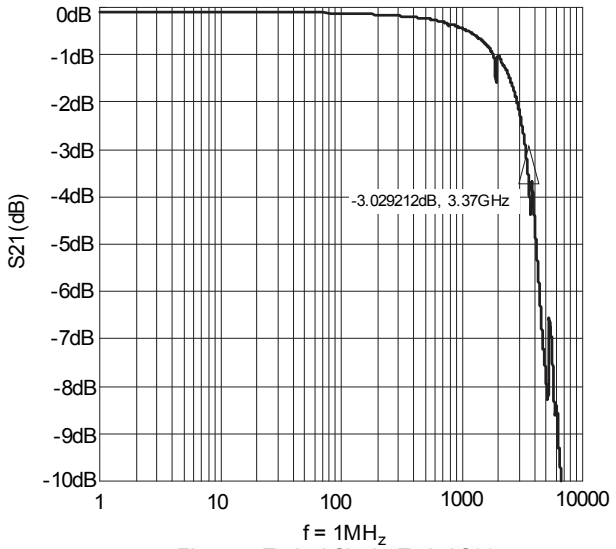
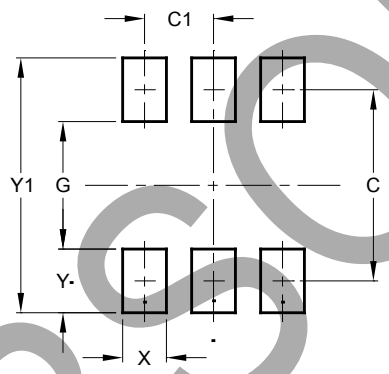


Figure 7, Typical Single-Ended S21 plot (1dB/div,1MHz to 10GHz)

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26 (SC74R)

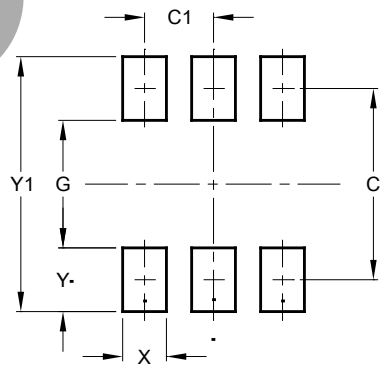


Dimensions	Value (in mm)
C	2.40
C1	0.95
G	1.60
X	0.55
Y	0.80
Y1	3.20

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26 (SC74R)



Dimensions	Value (in mm)
C	2.40
C1	0.95
G	1.60
X	0.55
Y	0.80
Y1	3.20

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