

DLPC910 Digital Controller for the DLP9000XFLS Digital Micromirror Device (DMD)

1 Features

- Required for Reliable Operation of the DLP9000XFLS DMD
- User-Selectable 400-MHz and 480-MHz Input Clock Rate
- Pixel Data Rate Greater than 61 Gigabits Per Second With Continuous Streaming Input Data
- Enables High-Speed Pattern Rates up to 15 kHz Binary Patterns per Second
- 8-Bit Gray Scale Pattern Rates up to 1.8 kHz With Modulated Illumination
- 64-Bit 2x LVDS Data Bus Interface
- Supports Random DMD Row Addressing and Load4 Loading
- Compatible With a Variety of User-Defined Application Processors or FPGAs
- Integrated I²C Interface for General Control and Status Queries

2 Applications

- Lithography
 - Direct Imaging
 - Flat Panel Display
 - Printed Circuit Board Manufacturing
- Industrial
 - 3D Printing
 - 3D Scanners for Machine Vision
 - Quality Control
- Displays
 - 3D Imaging
 - Augmented Reality and Information Overlay

3 Description

The DLPC910 device is required for reliable operation of the DLP9000XFLS DMD. This device enables one of the highest performing DLP[®] chipsets.

The DLPC910 provides a high-speed data and control interface for the DLP9000XFLS DMD enabling binary pattern rates of up to 15 kHz. These fast pattern rates set DLP technology apart from other spatial light modulators and offer customers a strategic advantage for equipment needing fast, accurate, and programmable light steering capability. The DLPC910 provides the required mirror clocking pulses and timing information to the DMD. The unique capability and value offered by the DLPC910 device makes it well suited to support a wide variety of lithography, industrial, and advanced display applications.

In DLP-based electronics solutions, image data is 100% digital from the DLPC910 input port to the projected image. The image stays in digital form and is never converted into an analog signal. The DLPC910 processes the digital input image and converts the data into a format needed by the DMD for proper display. The DMD then steers the light to the location determined by the pixel data loaded into the DMD.

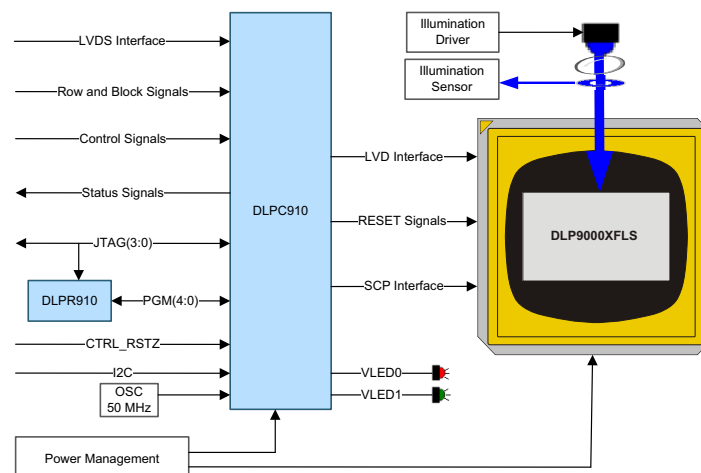
For complete electrical and mechanical specifications of the DLPC910, see the Virtex[®]-5 product specification at www.xilinx.com.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPC910	BGA (676)	27.00 mm x 27.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



4 Device and Documentation Support

4.1 Device Support

4.1.1 Device Nomenclature

Table 1. Part Number Description

TI PART NUMBER	DESCRIPTION
DLPC910ZYR	DLPC910 digital controller

4.1.2 Device Markings

Device markings are controlled by TI's supplier. TI packaging includes TI part number designation.

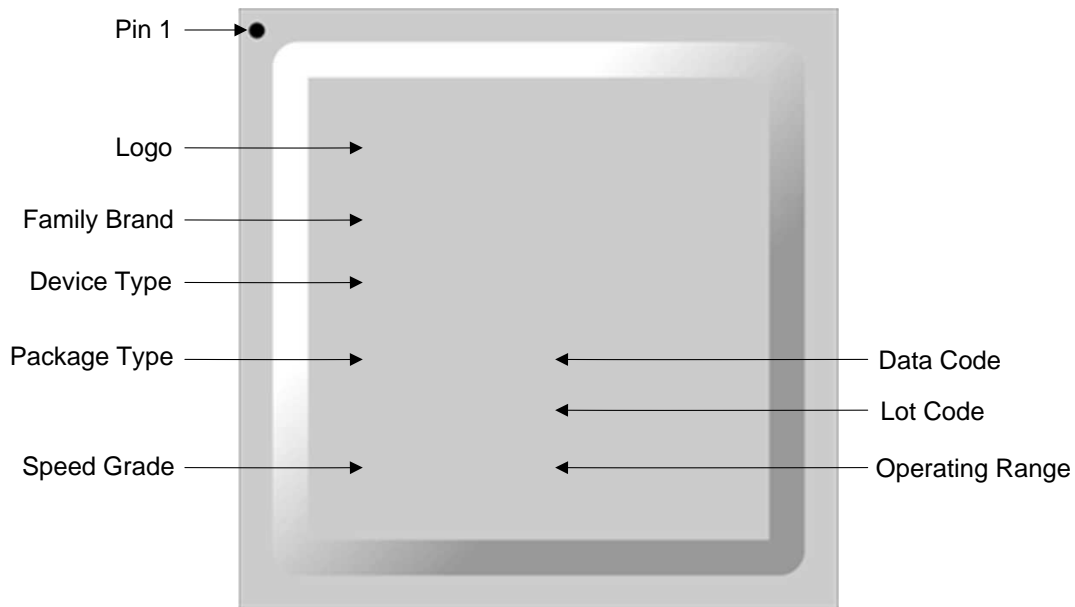


Figure 1. DLPC910 Device Markings

4.2 Documentation Support

4.2.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLPC910.

Table 2. Related Documentation

DOCUMENT	TI LITERATURE NUMBER
DLPR910YVA PROM data sheet	DLPS065
DLP9000XFLS DMD data sheet	DLPS036

4.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

4.4 Trademarks

E2E is a trademark of Texas Instruments.

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4.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

4.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC910ZYR	PREVIEW	FCBGA	ZYR	676	1	Pb-Free (RoHS)	Call TI	Level-4-250C-72 HRS			

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

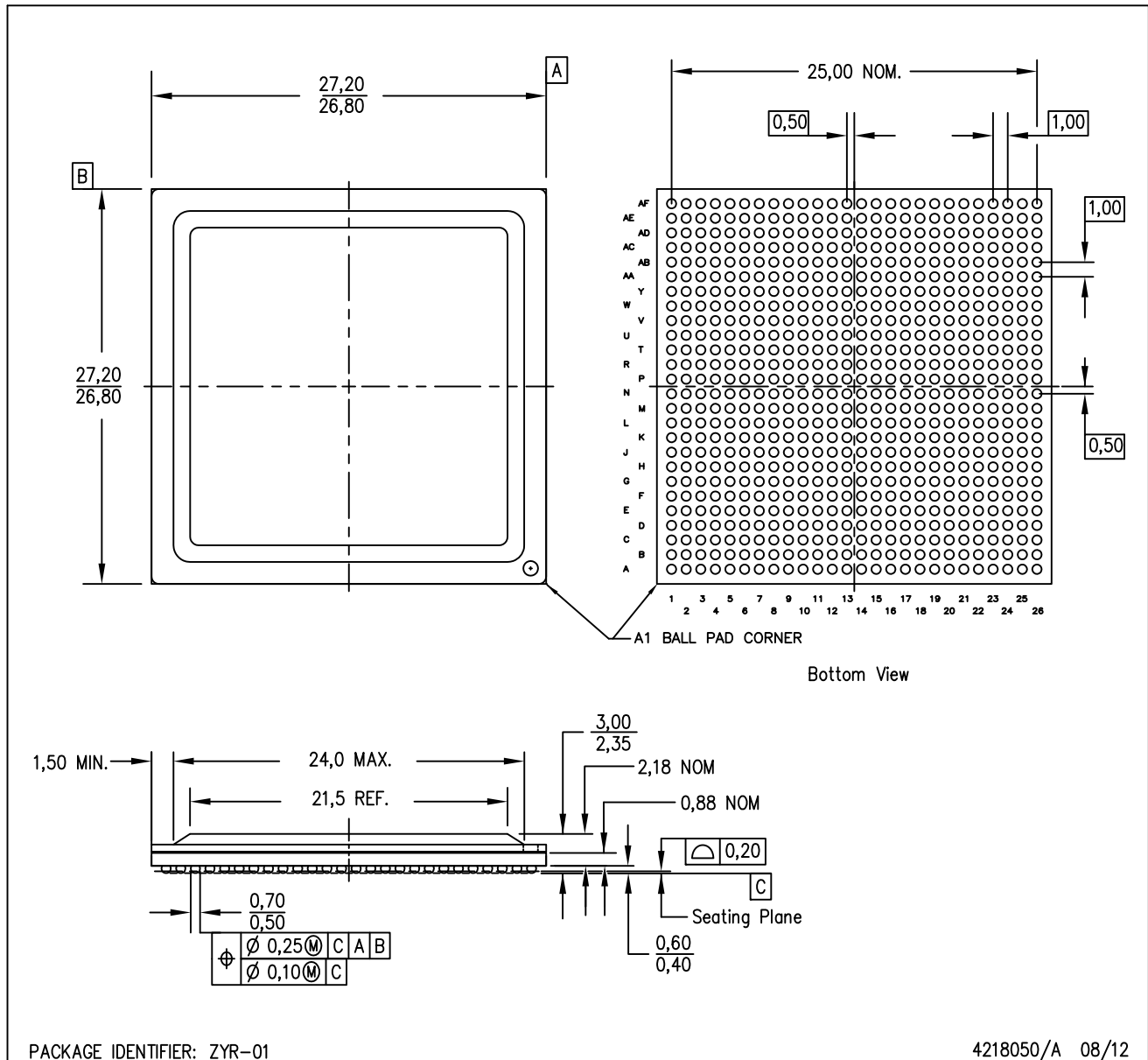
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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ZYR (S-PBGA-N676)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Flip chip application only.
 - D. Pb-free solder ball.

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