DLP® Discovery™ 4100 Digital Controller

Check for Samples: DLPC410

FEATURES

- **Operates the Following DLP Discovery 4100 Chipset Components**
  - **DMD: DLP7000 and DLP9500**
  - **DMD Micromirror Driver: DLPA200**
- **Enables Highest Speed DMD Pattern Rates**
  - **1-Bit Binary Pattern Rates up to 32-kHz (up to 48-kHz when used with DLPR4101)**
  - **8-Bit Monochrome Pattern Rates up to 1.9-kHz**
- **Allows Input Clock Rates Between 200 MHz and 400 MHz**
- **Provides up to a 64-Bit LVDS Data Bus Interface**
- **Supports Random DMD Row Addressing**
- **Compatible with a Variety of User Defined Processors or FPGAs**
- **676-Pin, 27 x 27 mm PBGA Package**

APPLICATIONS

- **Industrial:**
  - **Direct Imaging Lithography**
  - **Laser Marking and Repair Systems**
  - **Computer-to-Plate Printers**
  - **Rapid Prototyping Machines and 3D Printers**
  - **3D Scanners for Machine Vision and Quality Control**
- **Medical:**
  - **Phototherapy Devices**
  - **Ophthalmology**
  - **Vascular Imaging**
  - **Hyperspectral Imaging**
  - **3D Scanners for Limb and Skin Measurement**
  - **Confocal Microscopes**
- **Display:**
  - **3D Imaging Microscopes**
  - **Intelligent and Adaptive Lighting**
  - **Augmented Reality and Information Overlay**

DEVICE DESCRIPTION

The DLP Discovery 4100 Chipsets offer the highest speed pattern rates in the DLP Catalog portfolio with the option for random row addressing. The DLPC410 is a digital controller that supports both the 0.7 XGA chipset and 0.95 1080p chipset. DLPC410 provides:

- reliable operation of two digital micromirror device (DMD) options:
  - DLP7000
  - DLP9500
- reliable operation of the DMD Micromirror Driver(s): DLPA200
- a convenient, multi-functional interface between user electronics and the DMD

The DLPC410 provides a high-speed data and control interface for the DLP7000 DMD and DLP9500 DMD enabling binary pattern rates of up to 32 kHz and 23 kHz, respectively. These fast pattern rates set DLP technology apart from other spatial light modulators and offer customers a strategic advantage for equipment needing fast, accurate and programmable light steering capability. Moreover, the DLPC410 provides the DMD mirror clocking pulse and timing information to the TI DLPA200 DMD Micromirror Driver. The unique capability and value offered by DLPC410 makes it well suited to support a wide variety of industrial, medical, and advanced display applications.

In DLP based electronics solutions, image data is 100% digital from the DLPC410 input port to the image projected. The image stays in digital form and is never converted into an analog signal. The DLPC410 processes the digital input image and converts the data into a format needed by the image on the DMD. The DMD then steers the light using binary pulse-width modulation (PWM) for each pixel mirror.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

The DLPC410 is one of multiple components in the DLP Discovery 4100 Chipset (see Figure 1 and Figure 2). A dedicated chipset provides developers easier access to the DMD as well as high speed, independent micromirror control. See the list of required chipset components in Table 1:

Table 1. DLP Discovery 4100 Chipset Configurations

0.7 XGA Chipset				0.95 1080p Chipset		
Qty	TI Part	Description		Qty	TI Part	Description
1	DLP7000	0.7 XGA Type A DMD(digital micromirror device)		1	DLP9500	0.95 1080p Type A DMD(digital micromirror device)
1	DLPC410	DLP Discovery 4100 DMD Controller		1	DLPC410	DLP Discovery 4100 DMD Controller
1	DLPR410 DLPR4101	DLP Discovery 4100 Configuration PROM		1	DLPR410 DLPR4101	DLP Discovery 4100 Configuration PROM
1	DLPA200	DMD Micromirror Driver		2	DLPA200	DMD Micromirror Driver

Reliable function and operation of the DLPC410 requires that it be used in conjunction with the other components of the chipset in Table 1. For more information on the chipset components, see the DLP Discovery 4100 Chipset Data Sheet in Table 2).

RELATED DOCUMENTS

Table 2. Related Documentation

Document	TI Literature Number
DLP® Discovery™ 4100 Chipset Datasheet	DLPU008
DLP7000 0.7 XGA Type-A DMD data sheet	DLPS026
DLP9500 0.95 1080p Type-A DMD data sheet	DLPS025
DLPA200 DMD Micromirror Driver data sheet	DLPS015
DLPR410, DLPR4101 EEPROM data sheet	DLPS027

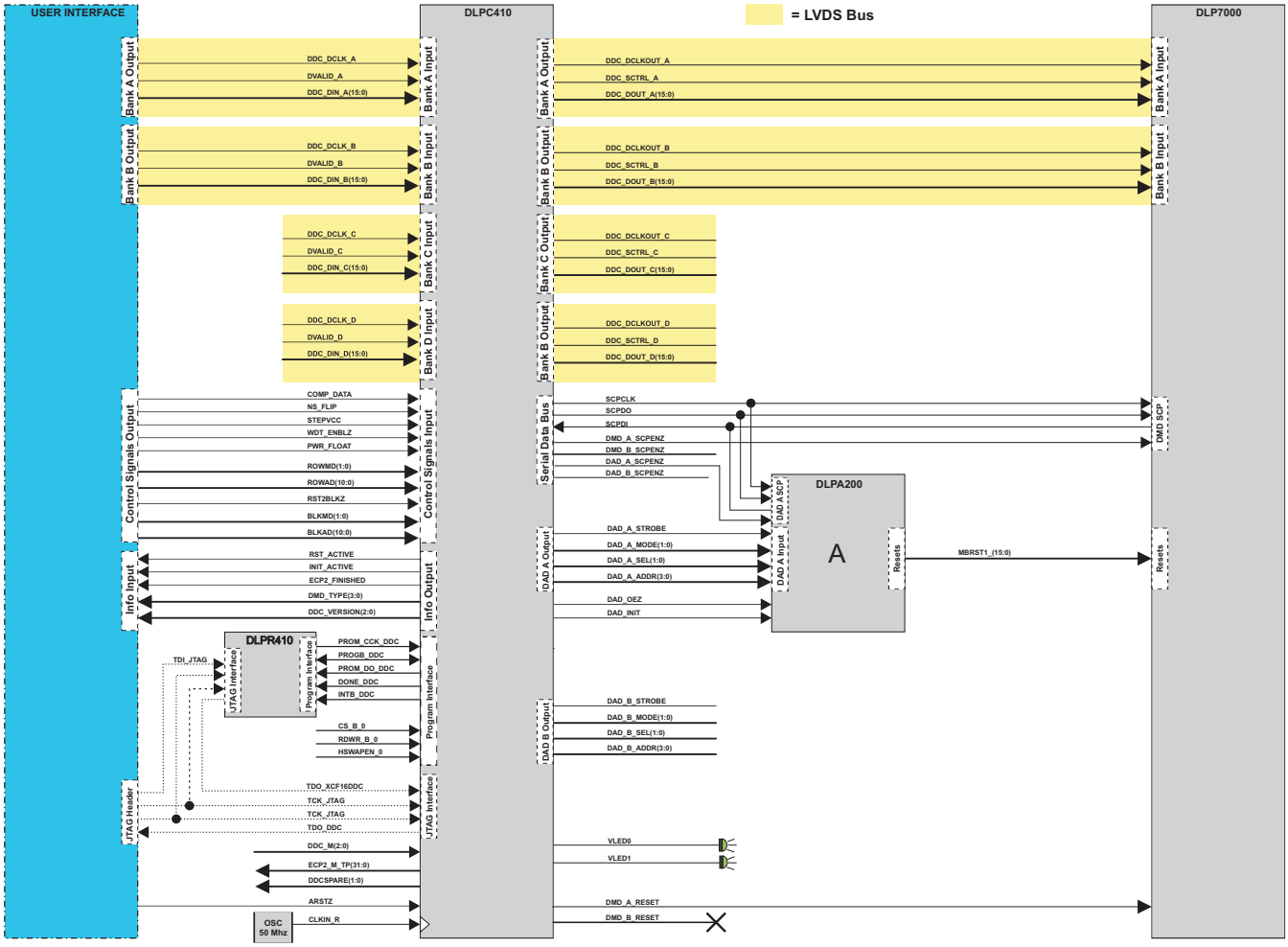


Figure 1. DLPC410 and DLP7000 Functional Block Diagram

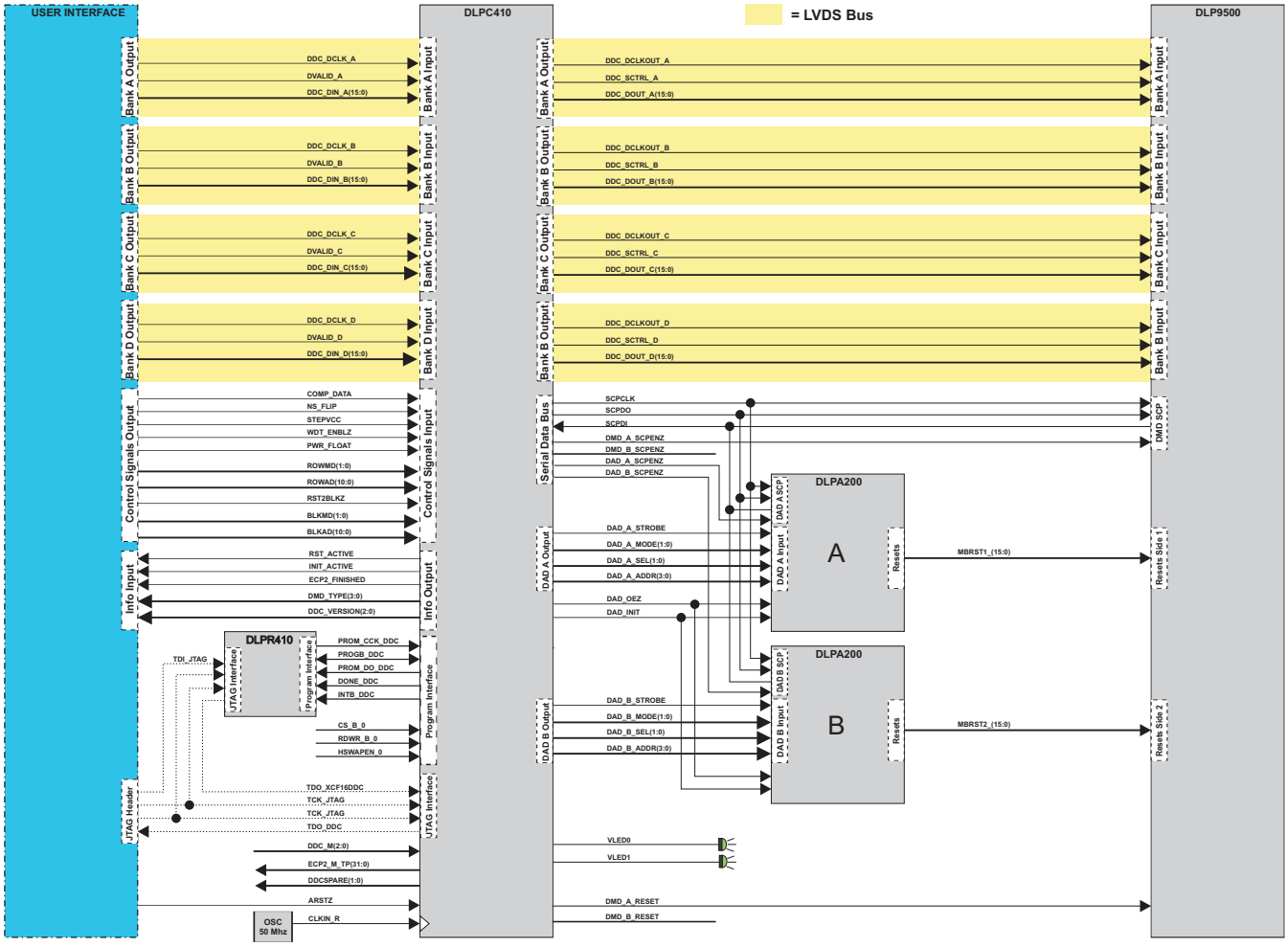


Figure 2. DLPC410 and DLP9500 Functional Block Diagram

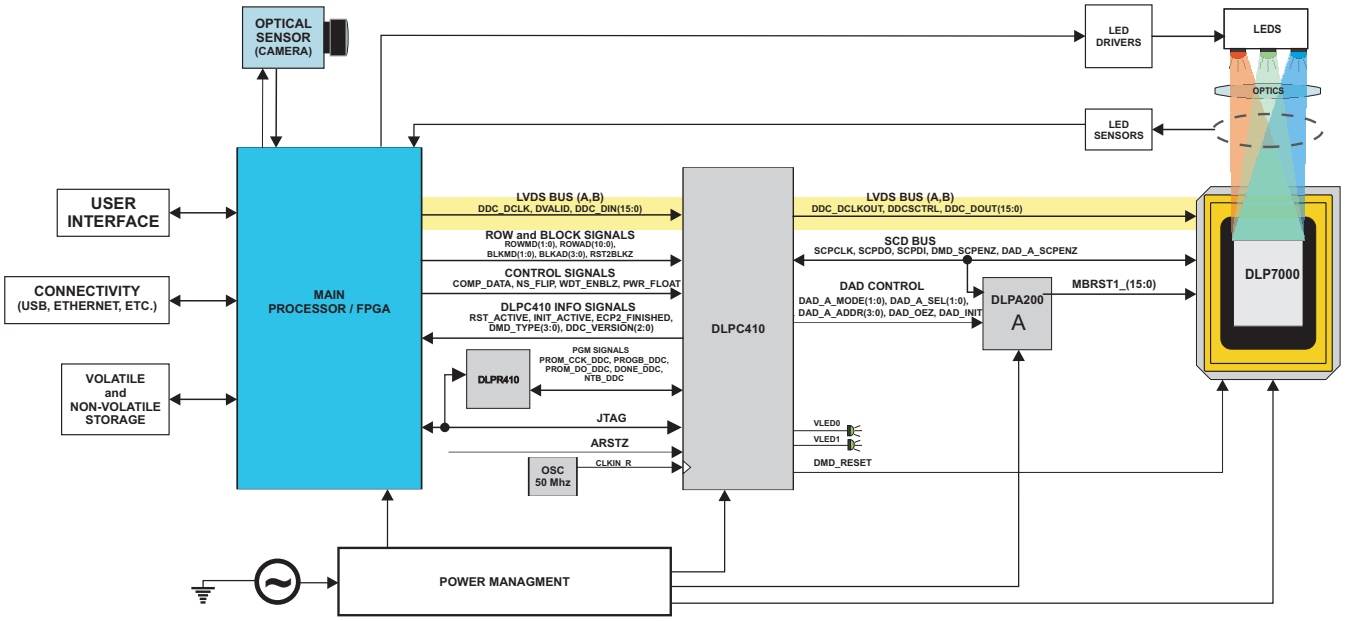


Figure 3. DLPC410 and DLP7000 Embedded Example Block Diagram

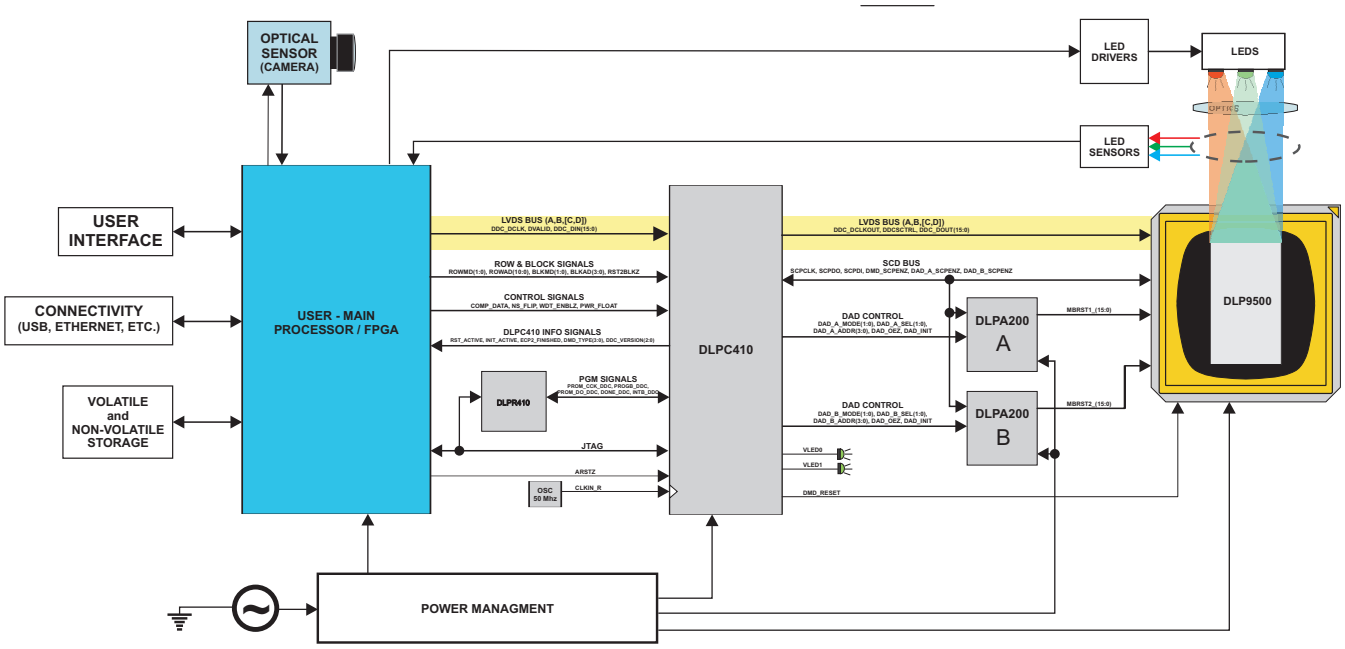


Figure 4. DLPC410 and DLP9500 Embedded Example Block Diagram

ORDERING INFORMATION

T_A	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 85°C	DLPC410ZYR	XC5VLX30-1FFG676C

DEVICE PART NUMBER NOMENCLATURE

Figure 5 provides a legend of reading the complete device name for any DLP device. The DLPC410ZYR is functionally equivalent to TI part number 2510440-001.

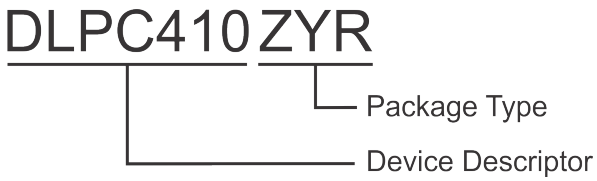


Figure 5. Device Nomenclature

DEVICE MARKING

Figure 6 is representative of the Xilinx XC5VLX30 FPGA configured for the DLPC410 device.

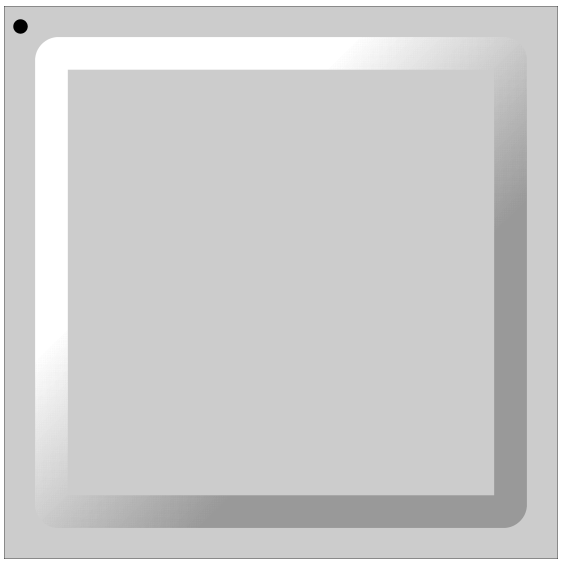


Figure 6. Diagram of the Xilinx XC5VLX30 FGPA

Figure 7 provides a legend for reading the Xilinx device marking for this DLP device.

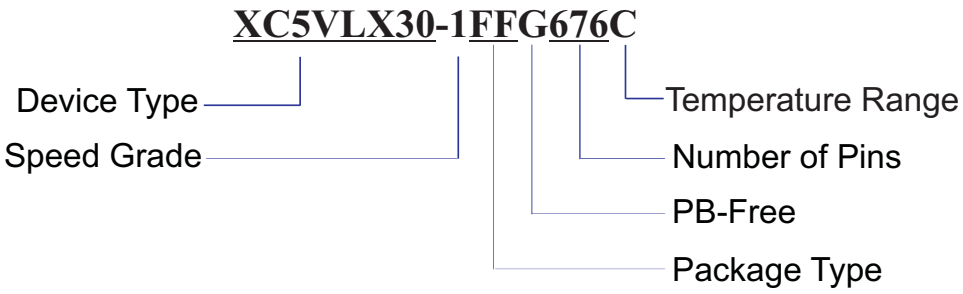


Figure 7. Legend

Signal Descriptions – I/O

A comprehensive description of pin functions is included in following sections.

Table 3. I/O Signal Descriptions

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
APPS_CNTL_DPN	F7	Not Used	NC	-	-	This pair connected with 100 Ω reisitor between pair.
APPS_CNTL_DPP	E7	Not Used	NC	-	-	
ARSTZ	AC13	DLPC410 Reset	LVCMOS25_S_12_I	Lo	-	
AVDD_0	M14	Voltage	NC	-	-	Ground (no name on schematic)
AVSS_0	M13	Voltage	NC	-	-	Ground (no name on schematic)
BLKAD_0	E12	Block Address bit 0	LVCMOS25_S_12_I	Hi = 1	DDC_DCLK_[A,B,C,D]	
BLKAD_1	D13	Block Address bit 1	LVCMOS25_S_12_I	Hi = 1	DDC_DCLK_[A,B,C,D]	
BLKAD_2	E13	Block Address bit 2	LVCMOS25_S_12_I	Hi = 1	DDC_DCLK_[A,B,C,D]	
BLKAD_3	F13	Block Address bit 3	LVCMOS25_S_12_I	Hi = 1	DDC_DCLK_[A,B,C,D]	
BLKMD_0	H13	Block Mode Bit 0	LVCMOS25_S_12_I	Hi = 1	DDC_DCLK_[A,B,C,D]	
BLKMD_1	H14	Block Mode Bit 1	LVCMOS25_S_12_I	Hi = 1	DDC_DCLK_[A,B,C,D]	
CLKIN_R	AD13	Reference Clock	LVCMOS25_S_12_I	-	Reference Clock	
COMP_DATA	G19	Compliment Data (0 <--> 1)	LVCMOS25_S_12_I	Hi	DDC_DCLK_[A,B,C,D]	
CS_B_0	N18	Xilinx Config	NC	Lo	-	1 KΩ pulldown to ground
D_OUT_BUSY_0	W11	Not Used	NC	-	-	No connection, but does not have an X at end
DAD_A_ADDR0	E1	DAD A Reset Block bit 0	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD A Address 0 pin
DAD_A_ADDR1	E2	DAD A Reset Block bit 1	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD A Address 1 pin
DAD_A_ADDR2	E3	DAD A Reset Block bit 2	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD A Address 2 pin
DAD_A_ADDR3	F3	DAD A Reset Block bit 3	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD A Address 3 pin
DAD_A_MODE0	C1	DAD A Mode bit 0	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD A Mode 0 pin
DAD_A_MODE1	D1	DAD A Mode bit 1	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD A Mode 1 pin
DAD_A_SCPENZ	AE3	DAD A SCP Communication Enable	LVCMOS25_F_12_O	Lo	-	Connected to DAD A SCPENZ poin
DAD_A_SEL0	AB12	DAD A Address bit 0	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD A SEL 0 pin
DAD_A_SEL1	AC12	DAD A Address bit 1	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD A SEL 1 pin
DAD_A_STROBE	AF3	DAD A Transition Strobe	LVCMOS25_F_12_O	Hi	-	Connected to DAD A STROBE pin
DAD_B_ADDR0	E26	DAD B Reset Block bit 0	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD B Address 1 pin
DAD_B_ADDR1	E25	DAD B Reset Block bit 1	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD B Address 2 pin
DAD_B_ADDR2	F25	DAD B Reset Block bit 2	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD B Address 3 pin
DAD_B_ADDR3	F24	DAD B Reset Block bit 3	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD B Address 0 pin
DAD_B_MODE0	D26	DAD B Mode bit 0	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD B Mode 0 pin
DAD_B_MODE1	D25	DAD B Mode bit 1	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD B Mode 1 pin
DAD_B_SCPENZ	AB19	DAD B SCP Communication Enable	LVCMOS25_F_12_O	Lo	-	Connected to DAD B SCPENZ poin
DAD_B_SEL0	R22	DAD B Address bit 0	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD B SEL 0 pin
DAD_B_SEL1	R23	DAD B Address bit 1	LVCMOS25_F_12_O	Hi = 1	-	Connected to DAD B SEL 1 pin
DAD_B_STROBE	AB20	DAD B Transition Strobe	LVCMOS25_F_12_O	Hi	-	Connected to DAD B STROBE pin
DAD_INIT	AF4	DAD A/B Init	LVCMOS25_F_12_O	Hi	-	Connected to DAD A and B RESETZ pin (shown as RESET with overline)
DAD_OEZ	AF5	DAD A/B Output Enable	LVCMOS25_F_12_O	Lo	-	Connected to DAD A and B OEZ pin (shown as OEZ with overline)
DDC_B11_VRN	L23	Reference Voltage	NC	-	-	51.1 Ω pullup to 2.5 V
DDC_B11_VRP	L22	Reference Voltage	NC	-	-	51.1 Ω pulldown to ground
DDC_B11_VRP	C22	Reference Voltage	NC	-	-	51.1 Ω pullup to 2.5 V
DDC_B12_VRN	M5	Reference Voltage	NC	-	-	51.1 Ω pulldown to ground
DDC_B12_VRP	M6	Reference Voltage	NC	-	-	51.1 Ω pullup to 2.5 V
DDC_B15_VRN	D23	Reference Voltage	NC	-	-	51.1 Ω pulldown to ground
DDC_B16_VRN	A4	Reference Voltage	NC	-	-	51.1 Ω pullup to 2.5 V
DDC_B16_VRP	A5	Reference Voltage	NC	-	-	51.1 Ω pulldown to ground
DDC_DCLK_A_DPN	B21	Bank A Input Clock (Neg)	LVDS_25	-	-	100 Ω across pair (not terminated in the DLPC410)
DDC_DCLK_A_DPP	C21	Bank A Input Clock (Pos)	LVDS_25_I	-	-	

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
DDC_DCLK_B_DPN	A7	Bank B Input Clock (Neg)	LVDS_25	-	-	100 Ω across pair (not terminated in the DLPC410)
DDC_DCLK_B_DPP	B7	Bank B Input Clock (Pos)	LVDS_25_I	-	-	
DDC_DCLK_C_DPN	K20	Bank C Input Clock (Neg)	LVDS_25	-	-	100 Ω across pair (not terminated in the DLPC410)
DDC_DCLK_C_DPP	K21	Bank C Input Clock (Pos)	LVDS_25_I	-	-	
DDC_DCLK_D_DPN	L5	Bank D Input Clock (Neg)	LVDS_25	-	-	100 Ω across pair (not terminated in the DLPC410)
DDC_DCLK_D_DPP	K5	Bank D Input Clock (Pos)	LVDS_25_I	-	-	
DDC_DCLKOUT_A_DPN	N1	Bank A Output Clock (Neg)	LVDS_25	-	-	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DCLKOUT_A_DPP	M1	Bank A Output Clock (Pos)	LVDS_25_O	-	-	
DDC_DCLKOUT_B_DPN	Y5	Bank B Output Clock (Neg)	LVDS_25	-	-	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DCLKOUT_B_DPP	Y6	Bank B Output Clock (Pos)	LVDS_25_O	-	-	
DDC_DCLKOUT_C_DPN	AA22	Bank C Output Clock (Neg)	LVDS_25	-	-	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DCLKOUT_C_DPP	AB22	Bank C Output Clock (Pos)	LVDS_25_O	-	-	
DDC_DCLKOUT_D_DPN	M26	Bank D Output Clock (Neg)	LVDS_25	-	-	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DCLKOUT_D_DPP	M25	Bank D Output Clock (Pos)	LVDS_25_O	-	-	
DDC_DIN_A0_DPN	A15	Data A bit 0 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A0_DPP	A14	Data A bit 0 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A1_DPN	B14	Data A bit 1 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A1_DPP	C14	Data A bit 1 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A2_DPN	B16	Data A bit 2 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A2_DPP	B15	Data A bit 2 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A3_DPN	C16	Data A bit 3 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A3_DPP	D16	Data A bit 3 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A4_DPN	A17	Data A bit 4 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A4_DPP	B17	Data A bit 4 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A5_DPN	C17	Data A bit 5 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A5_DPP	D18	Data A bit 5 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A6_DPN	A19	Data A bit 6 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A6_DPP	A18	Data A bit 6 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A7_DPN	C18	Data A bit 7 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A7_DPP	B19	Data A bit 7 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A8_DPN	D19	Data A bit 8 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A8_DPP	C19	Data A bit 8 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A9_DPN	B20	Data A bit 9 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A9_DPP	A20	Data A bit 9 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A10_DPN	A22	Data A bit 10 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A10_DPP	B22	Data A bit 10 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A11_DPN	A24	Data A bit 11 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A11_DPP	A23	Data A bit 11 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A12_DPN	C23	Data A bit 12 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A12_DPP	B24	Data A bit 12 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A13_DPN	C24	Data A bit 13 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A13_DPP	D24	Data A bit 13 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A14_DPN	A25	Data A bit 14 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A14_DPP	B25	Data A bit 14 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_A15_DPN	C26	Data A bit 15 Input (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_A15_DPP	B26	Data A bit 15 Input (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DDC_DIN_B0_DPN	A12	Data B bit 0 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B0_DPP	A13	Data B bit 0 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B1_DPN	B12	Data B bit 1 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B1_DPP	C13	Data B bit 1 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
DDC_DIN_B2_DPN	D10	Data B bit 2 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B2_DPP	D11	Data B bit 2 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B3_DPN	C12	Data B bit 3 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B3_DPP	C11	Data B bit 3 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B4_DPN	A10	Data B bit 4 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B4_DPP	B11	Data B bit 4 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B5_DPN	D9	Data B bit 5 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B5_DPP	C9	Data B bit 5 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B6_DPN	B10	Data B bit 6 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B6_DPP	B9	Data B bit 6 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B7_DPN	A8	Data B bit 7 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B7_DPP	A9	Data B bit 7 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B8_DPN	D6	Data B bit 8 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B8_DPP	D5	Data B bit 8 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B9_DPN	C7	Data B bit 9 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B9_DPP	C6	Data B bit 9 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B10_DPN	B6	Data B bit 10 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B10_DPP	B5	Data B bit 10 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B11_DPN	D4	Data B bit 11 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B11_DPP	D3	Data B bit 11 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B12_DPN	B4	Data B bit 12 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B12_DPP	C4	Data B bit 12 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B13_DPN	C3	Data B bit 13 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B13_DPP	C2	Data B bit 13 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B14_DPN	A3	Data B bit 14 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B14_DPP	A2	Data B bit 14 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_B15_DPN	B2	Data B bit 15 Input (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_B15_DPP	B1	Data B bit 15 Input (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DDC_DIN_C0_DPN	E20	Data C bit 0 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C0_DPP	E21	Data C bit 0 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C1_DPN	F20	Data C bit 1 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C1_DPP	G20	Data C bit 1 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C2_DPN	H19	Data C bit 2 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C2_DPP	J19	Data C bit 2 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C3_DPN	E23	Data C bit 3 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C3_DPP	E22	Data C bit 3 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C4_DPN	F23	Data C bit 4 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C4_DPP	F22	Data C bit 4 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C5_DPN	G22	Data C bit 5 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C5_DPP	G21	Data C bit 5 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C6_DPN	J20	Data C bit 6 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C6_DPP	J21	Data C bit 6 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C7_DPN	H22	Data C bit 7 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C7_DPP	H21	Data C bit 7 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C8_DPN	J23	Data C bit 8 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C8_DPP	H23	Data C bit 8 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C9_DPN	K22	Data C bit 9 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C9_DPP	K23	Data C bit 9 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C10_DPN	M19	Data C bit 10 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C10_DPP	M20	Data C bit 10 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C11_DPN	M21	Data C bit 11 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C11_DPP	M22	Data C bit 11 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C12_DPN	N19	Data C bit 12 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C12_DPP	P19	Data C bit 12 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
DDC_DIN_C13_DPN	N21	Data C bit 13 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C13_DPP	N22	Data C bit 13 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C14_DPN	P20	Data C bit 14 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C14_DPP	P21	Data C bit 14 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_C15_DPN	N23	Data C bit 15 Input (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_C15_DPP	P23	Data C bit 15 Input (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DDC_DIN_D0_DPN	T3	Data D bit 0 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D0_DPP	R3	Data D bit 0 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D1_DPN	R5	Data D bit 1 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D1_DPP	R6	Data D bit 1 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D2_DPN	R7	Data D bit 2 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D2_DPP	P6	Data D bit 2 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D3_DPN	N3	Data D bit 3 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D3_DPP	P3	Data D bit 3 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D4_DPN	P4	Data D bit 4 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D4_DPP	P5	Data D bit 4 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D5_DPN	N6	Data D bit 5 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D5_DPP	N7	Data D bit 5 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D6_DPN	N4	Data D bit 6 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D6_DPP	M4	Data D bit 6 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D7_DPN	M7	Data D bit 7 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D7_DPP	L7	Data D bit 7 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D8_DPN	K7	Data D bit 8 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D8_DPP	K6	Data D bit 8 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D9_DPN	J4	Data D bit 9 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D9_DPP	J5	Data D bit 9 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D10_DPN	H7	Data D bit 10 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D10_DPP	J6	Data D bit 10 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D11_DPN	G4	Data D bit 11 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D11_DPP	H4	Data D bit 11 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D12_DPN	G5	Data D bit 12 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D12_DPP	H6	Data D bit 12 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D13_DPN	G7	Data D bit 13 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D13_DPP	G6	Data D bit 13 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D14_DPN	F4	Data D bit 14 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D14_DPP	F5	Data D bit 14 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DIN_D15_DPN	E5	Data D bit 15 Input (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DDC_DIN_D15_DPP	E6	Data D bit 15 Input (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DDC_DOUT_A0_DPN	AE2	Data A bit 0 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A0_DPP	AF2	Data A bit 0 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A1_DPN	AD1	Data A bit 1 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A1_DPP	AE1	Data A bit 1 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A2_DPN	AC1	Data A bit 2 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A2_DPP	AC2	Data A bit 2 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A3_DPN	AB1	Data A bit 3 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A3_DPP	AB2	Data A bit 3 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A4_DPN	Y2	Data A bit 4 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A4_DPP	AA2	Data A bit 4 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A5_DPN	W1	Data A bit 5 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A5_DPP	Y1	Data A bit 5 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A6_DPN	V1	Data A bit 6 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A6_DPP	V2	Data A bit 6 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A7_DPN	U1	Data A bit 7 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A7_DPP	U2	Data A bit 7 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
DDC_DOUT_A8_DPN	R2	Data A bit 8 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A8_DPP	T2	Data A bit 8 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A9_DPN	N2	Data A bit 9 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A9_DPP	M2	Data A bit 9 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A10_DPN	K1	Data A bit 10 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A10_DPP	L2	Data A bit 10 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A11_DPN	K2	Data A bit 11 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A11_DPP	K3	Data A bit 11 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A12_DPN	J3	Data A bit 12 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A12_DPP	H3	Data A bit 12 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A13_DPN	H2	Data A bit 13 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A13_DPP	J1	Data A bit 13 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A14_DPN	H1	Data A bit 14 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A14_DPP	G1	Data A bit 14 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_A15_DPN	G2	Data A bit 15 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_A15_DPP	F2	Data A bit 15 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_DOUT_B0_DPN	AE5	Data B bit 0 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B0_DPP	AE6	Data B bit 0 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B1_DPN	AD3	Data B bit 1 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B1_DPP	AD4	Data B bit 1 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B2_DPN	AD5	Data B bit 2 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B2_DPP	AD6	Data B bit 2 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B3_DPN	AC3	Data B bit 3 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B3_DPP	AC4	Data B bit 3 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B4_DPN	AB5	Data B bit 4 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B4_DPP	AB6	Data B bit 4 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B5_DPN	AB7	Data B bit 5 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B5_DPP	AC6	Data B bit 5 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B6_DPN	AA5	Data B bit 6 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B6_DPP	AA4	Data B bit 6 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B7_DPN	AA7	Data B bit 7 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B7_DPP	Y7	Data B bit 7 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B8_DPN	Y3	Data B bit 8 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B8_DPP	W3	Data B bit 8 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B9_DPN	W4	Data B bit 9 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B9_DPP	V4	Data B bit 9 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B10_DPN	W6	Data B bit 10 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B10_DPP	W5	Data B bit 10 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B11_DPN	V7	Data B bit 11 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B11_DPP	V6	Data B bit 11 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B12_DPN	U4	Data B bit 12 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B12_DPP	V3	Data B bit 12 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
DDC_DOUT_B13_DPN	T4	Data B bit 13 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B13_DPP	T5	Data B bit 13 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B14_DPN	U6	Data B bit 14 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B14_DPP	U5	Data B bit 14 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_B15_DPN	U7	Data B bit 15 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_B15_DPP	T7	Data B bit 15 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_DOUT_C0_DPN	T22	Data C bit 0 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C0_DPP	T23	Data C bit 0 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C1_DPN	R20	Data C bit 1 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C1_DPP	R21	Data C bit 1 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C2_DPN	T19	Data C bit 2 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C2_DPP	T20	Data C bit 2 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C3_DPN	U21	Data C bit 3 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C3_DPP	U22	Data C bit 3 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C4_DPN	U20	Data C bit 4 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C4_DPP	U19	Data C bit 4 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C5_DPN	V23	Data C bit 5 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C5_DPP	V24	Data C bit 5 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C6_DPN	V22	Data C bit 6 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C6_DPP	V21	Data C bit 6 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C7_DPN	W19	Data C bit 7 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C7_DPP	V19	Data C bit 7 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C8_DPN	W23	Data C bit 8 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C8_DPP	W24	Data C bit 8 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C9_DPN	Y22	Data C bit 9 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C9_DPP	Y23	Data C bit 9 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C10_DPN	Y20	Data C bit 10 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C10_DPP	Y21	Data C bit 10 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C11_DPN	AA24	Data C bit 11 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C11_DPP	AA23	Data C bit 11 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C12_DPN	AA19	Data C bit 12 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C12_DPP	AA20	Data C bit 12 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C13_DPN	AC24	Data C bit 13 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C13_DPP	AB24	Data C bit 13 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C14_DPN	AC19	Data C bit 14 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C14_DPP	AD19	Data C bit 14 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_C15_DPN	AC22	Data C bit 15 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_C15_DPP	AC23	Data C bit 15 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_DOUT_D0_DPN	AB26	Data D bit 0 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D0_DPP	AC26	Data D bit 0 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D1_DPN	AA25	Data D bit 1 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D1_DPP	AB25	Data D bit 1 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D2_DPN	Y26	Data D bit 2 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D2_DPP	Y25	Data D bit 2 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
DDC_DOUT_D3_DPN	W26	Data D bit 3 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D3_DPP	W25	Data D bit 3 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D4_DPN	U26	Data D bit 4 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D4_DPP	V26	Data D bit 4 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D5_DPN	U25	Data D bit 5 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D5_DPP	U24	Data D bit 5 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D6_DPN	T25	Data D bit 6 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D6_DPP	T24	Data D bit 6 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D7_DPN	R26	Data D bit 7 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D7_DPP	R25	Data D bit 7 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D8_DPN	P24	Data D bit 8 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D8_DPP	P25	Data D bit 8 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D9_DPN	N24	Data D bit 9 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D9_DPP	M24	Data D bit 9 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D10_DPN	L25	Data D bit 10 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D10_DPP	L24	Data D bit 10 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D11_DPN	K26	Data D bit 11 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D11_DPP	K25	Data D bit 11 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D12_DPN	J26	Data D bit 12 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D12_DPP	J25	Data D bit 12 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D13_DPN	J24	Data D bit 13 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D13_DPP	H24	Data D bit 13 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D14_DPN	H26	Data D bit 14 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D14_DPP	G26	Data D bit 14 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_DOUT_D15_DPN	G25	Data D bit 15 Output (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_DOUT_D15_DPP	G24	Data D bit 15 Output (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_M0	W18	Xilinx Configuration	NC	Hi	-	4.7 KΩ pullup to 2.5V
DDC_M1	Y17	Xilinx Configuration	NC	Hi	-	4.7 KΩ pullup to 2.5V
DDC_M2	V18	Xilinx Configuration	NC	Hi	-	4.7 KΩ pullup to 2.5V
DDC_SCTRL_AN	R1	Bank A Serial Control Data (Neg)	LVDS_25	-	DDC_DCLKOUT_A	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_SCTRL_AP	P1	Bank A Serial Control Data (Pos)	LVDS_25_O	-	DDC_DCLKOUT_A	
DDC_SCTRL_BN	AA3	Bank B Serial Control Data (Neg)	LVDS_25	-	DDC_DCLKOUT_B	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_SCTRL_BP	AB4	Bank B Serial Control Data (Pos)	LVDS_25_O	-	DDC_DCLKOUT_B	
DDC_SCTRL_CN	W20	Bank C Serial Control Data (Neg)	LVDS_25	-	DDC_DCLKOUT_C	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_SCTRL_CP	W21	Bank C Serial Control Data (Pos)	LVDS_25_O	-	DDC_DCLKOUT_C	
DDC_SCTRL_DN	N26	Bank D Serial Control Data (Neg)	LVDS_25	-	DDC_DCLKOUT_D	Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω)
DDC_SCTRL_DP	P26	Bank D Serial Control Data (Pos)	LVDS_25_O	-	DDC_DCLKOUT_D	
DDC_VERSION_0	F18	DLPC410 Firmware Rev Number bit 0	LVCMOS25_F_12_O	Hi = 1	-	
DDC_VERSION_1	G17	DLPC410 Firmware Rev Number bit 1	LVCMOS25_F_12_O	Hi = 1	-	
DDC_VERSION_2	H18	DLPC410 Firmware Rev Number bit 2	LVCMOS25_F_12_O	Hi = 1	-	

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
DDC_SPARE_0	AB21	(Not Used with DLPR410 PROM, Used to enable "Load 4" with DLPR4101 PROM)	LVCMOS25_F_12_I/O	NC - with DLPR410, Active Lo with DLPR4101	-	When used with the DLPR410 PROM this output is unused and should not be connected. When used with the DLPR4101 Enhanced Functionality PROM this becomes a LVCMOS input with an internal pullup - active low.
DDC_SPARE_1	AC21	Not Used	LVCMOS25_F_12_O	-	-	
DMD_A_RESET	AD14	DMD Circuitrly Reset (not data reset)	LVCMOS25_F_12_O	Lo	-	Connected to 36 Ω resitor with 27 pF cap to ground (signal name DMD_A_RESET_FILT after resisitor - connects to DMD signal DMDRSTZ)
DMD_A_SCPENZ	AB14	DMD SCP Output Enable	LVCMOS25_F_12_O	Lo	-	Connected to 36 Ω resitor with 27 pF cap to ground (called DMD_A_SCPEN# on schematic - signal name DMD_A_SCPEN#_FILT after resisitor - connects to DMD signal DMDSELZ)
DMD_B_RESET	AA12	Not Used	LVCMOS25_S_12	(not used)	-	Connected to 36 Ω resitor with 27 pF cap to ground (signal name DMD_B_RESET_FILT after resisitor - NC after that point)
DMD_B_SCPENZ	AC14	Not Used	NC	Lo (not used)	-	Connected to 36 Ω resitor with 27 pF cap to ground (called DMD_B_SCPEN# on schematic - signal name DMD_B_SCPEN#_FILT after resisitor - NC after that point)
DMD_TYPE_0	AA17	DMD Attached Type bit 0	LVCMOS25_F_12_O	Hi = 1	-	
DMD_TYPE_1	AC16	DMD Attached Type bit 1	LVCMOS25_F_12_O	Hi = 1	-	
DMD_TYPE_2	AB17	DMD Attached Type bit 2	LVCMOS25_F_12_O	Hi = 1	-	
DMD_TYPE_3	AD15	DMD Attached Type bit 3	LVCMOS25_F_12_O	Hi = 1	-	
DONE_DDC	K10	DLPR410 Initialization Routine Complete	NC	Hi	-	4.7 KΩ pullup to 2.5V - connected to DLPR410 CEZ pin and LED D3 pin 3 (cathode) in series with 62 Ω resistor to 3.3 V
DVALID_A_DPN	D20	Bank A Valid Input Signal (Neg)	LVDS_25	-	DDC_DCLK_A	100 Ω across pair (not terminated in the DLPC410)
DVALID_A_DPP	D21	Bank A Valid Input Signal (Pos)	LVDS_25_I	-	DDC_DCLK_A	
DVALID_B_DPN	C8	Bank B Valid Input Signal (Neg)	LVDS_25	-	DDC_DCLK_B	100 Ω across pair (not terminated in the DLPC410)
DVALID_B_DPP	D8	Bank B Valid Input Signal (Pos)	LVDS_25_I	-	DDC_DCLK_B	
DVALID_C_DPN	L19	Bank C Valid Input Signal (Neg)	LVDS_25	-	DDC_DCLK_C	100 Ω across pair (not terminated in the DLPC410)
DVALID_C_DPP	L20	Bank C Valid Input Signal (Pos)	LVDS_25_I	-	DDC_DCLK_C	
DVALID_D_DPN	L3	Bank D Valid Input Signal (Neg)	LVDS_25	-	DDC_DCLK_D	100 Ω across pair (not terminated in the DLPC410)
DVALID_D_DPP	L4	Bank D Valid Input Signal (Pos)	LVDS_25_I	-	DDC_DCLK_D	
DXN_0	R13	-	NC	-	-	TP17
DXP_0	R14	-	NC	-	-	TP14
ECP2_FINISHED	Y18	DLPR410 Initialization Routine Complete	LVCMOS25_F_12_O	Hi	-	Connected to LED D3 pin 2 (anode) in series with 62 Ω resistor to 3.3 V
ECP2_M_TP0	AD11	Not Defined	NC	-	-	Mictor J8 Pin 2
ECP2_M_TP1	AD10	Not Defined	NC	-	-	Mictor J8 Pin 4
ECP2_M_TP2	AD8	Not Defined	NC	-	-	Mictor J8 Pin 6
ECP2_M_TP3	AC8	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 8
ECP2_M_TP4	AC7	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 10
ECP2_M_TP5	AC9	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 12
ECP2_M_TP6	AB9	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 14
ECP2_M_TP7	AA8	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 16
ECP2_M_TP8	AA9	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 18
ECP2_M_TP9	Y8	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 20
ECP2_M_TP10	AB10	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 22
ECP2_M_TP11	AA10	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 24
ECP2_M_TP12	Y10	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 26
ECP2_M_TP13	AC11	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 28
ECP2_M_TP14	Y12	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 30
ECP2_M_TP15	Y11	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 32
ECP2_M_TP16	AB11	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 34

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
ECP2_M_TP17	H8	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 36
ECP2_M_TP18	H9	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 38
ECP2_M_TP19	F12	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 37
ECP2_M_TP20	G11	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 35
ECP2_M_TP21	G12	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 33
ECP2_M_TP22	E11	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 31
ECP2_M_TP23	E10	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 29
ECP2_M_TP24	E8	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 27
ECP2_M_TP25	F10	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 25
ECP2_M_TP26	F9	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 23
ECP2_M_TP27	F8	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 21
ECP2_M_TP28	G10	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 19
ECP2_M_TP29	G9	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 17
ECP2_M_TP30	H11	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 15
ECP2_M_TP31	H12	Test Point	LVCMOS25_F_12_O	Test Point		Mictor J8 Pin 13

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
GND	A1, A6, A11, A16, A21, A26, AA1, AA11, AA21, AA26, AB8, AB18, AC5, AC15, AC25, AD2, AD12, AD22, AE4, AE9, AE14, AE19, AF1, AF6, AF11, AF16, AF21, AF26, B3, B8, B13, B18, C5, C15, C25, D2, D12, D22, E9, E19, F1, F6, F16, F26, G3, G13, G18, G23, H10, H20, J7, J9, J13, J15, J17, K4, K8, K12, K14, K16, K19, K24, L1, L9, L11, L13, L15, L17, L21, L26, M3, M8, M10, M12, M16, M18, N5, N9, N11, N15, N17, N25, P2, P7, P8, P10, P12, P16, P22, R9, R11, R15, R17, R19, T1, T6, T8, T10, T12, T14, T16, T26, U3, U9, U13, U15, U17, U18, U23, V8, V10, V14, V16, V20, W7, W9, W13, W15, W17, Y4, Y14, Y16, Y19, Y24, M13, M14	Ground	GND	-	-	
HSWAPEN	L18	Xilinx Configuration	NC	-	-	4.7 KΩ pullup to 2.5 V
INIT_ACTIVE	AA18	DLPC410 Initilization Routine Active	LVCMOS25_F_12_O	Hi	-	
INTB_DDC	J11	Xilinx Configuration	NC	Hi	-	4.7 KΩ pullup to 2.5 V connected to DLPR410 OE/RESETZ
NS_FLIP	F19	Top/Bottom image flip on DMD	LVCMOS25_S_12_I	Hi	-	
PROGB_DDC	J18	Xilinx Configuration	NC	Hi	-	4.7 KΩ pullup to 2.5 V connected to DLPR410 CFZ
PROM_CCK_DDC	J10	Configuration PROM Clock	LVCMOS25_S_12	-	PROM_CCK_DDC	Connected to center of voltage divider (100/100 Ω) and through R53 to DLPR410 CLKOUT

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
PROM_D0_DDC	K11	Configuration PROM Data Out	NC	-	PROM_CCK_DDC	Connected to DLPR410 Data 0 (D0)
PWR_FLOAT	AC17	DMD Power	LVCMOS25_S_12_I	Hi	-	Connected to output of U22 NOR Gate (inputs V5_PWR_FLOATZ and PWRGD)
RDWR_B	P18	Xilinx Configuration	NC	-	-	1 KΩ pulldown to ground
ROWAD_0	D14	DMD Row Address bit 0	LVCMOS25_S_12_I	Hi = 1	-	
ROWAD_1	D15	DMD Row Address bit 1	LVCMOS25_S_12_I	Hi = 1	-	
ROWAD_2	E15	DMD Row Address bit 2	LVCMOS25_S_12_I	Hi = 1	-	
ROWAD_3	F14	DMD Row Address bit 3	LVCMOS25_S_12_I	Hi = 1	-	
ROWAD_4	G14	DMD Row Address bit 4	LVCMOS25_S_12_I	Hi = 1	-	
ROWAD_5	E16	DMD Row Address bit 5	LVCMOS25_S_12_I	Hi = 1	-	
ROWAD_6	F15	DMD Row Address bit 6	LVCMOS25_S_12_I	Hi = 1	-	
ROWAD_7	G15	DMD Row Address bit 7	LVCMOS25_S_12_I	Hi = 1	-	
ROWAD_8	E17	DMD Row Address bit 8	LVCMOS25_S_12_I	Hi = 1	-	
ROWAD_9	F17	DMD Row Address bit 9	LVCMOS25_S_12_I	Hi = 1	-	
ROWAD_10	G16	DMD Row Address bit 10	LVCMOS25_S_12_I	Hi = 1	-	
ROWMD_0	H17	DMD Row Mode bit 0	LVCMOS25_S_12_I	Hi = 1	-	
ROWMD_1	H16	DMD Row Mode bit 1	LVCMOS25_S_12_I	Hi = 1	-	
RST_ACTIVE	AB16	DMD Reset in Progress	LVCMOS25_F_12_O	Hi = 1	-	
RST2BLKZ	E18	Dual Block Reset bit	LVCMOS25_S_12_I	Hi = 1	-	
RSVD_0	R18	Not Used	NC	-	-	Schematic to Ground
RSVD_0	T18	Not Used	NC	-	-	Schematic to Ground
SCPCLK	AB15	SCP Clock	LVCMOS25_F_12_O	-	SCPCLK	Connected to DAD A and B SCPCLK and to R105 36 Ω filter resistor with 27 pF cap after - called DMD_A_SCPCLK_FILT after - connects to DMD SCPCLK (also connects to R97 filter resistor with 27 pF cap after - called DMD_B_SCPCLK_FILT but NC after)
SCPDI	AA15	SCP Clock	LVCMOS25_S_12_I	-	SCPCLK	1 KΩ pullup to 2.5 V - connects to DAD Aand B SCPDO and to DMD SCPDO through flex A - on DMD board there is an LCR filter [2 x 100 pF caps, inductor and 34 Ω resistor] also connects to flex B but NC on other end.
SCPDO	AA14	SCP Clock	LVCMOS25_F_12_O	-	SCPCLK	1 KΩ pullup to 2.5 V - connects to DAD Aand B SCPDI and to R96 filter cap with 27 pF cap after - called DMD_A_FILTER - connect through flex A to DMD SCPDI - also connects to R71 36 Ω filter resistor with 27 pF cap to DMD_B_SCPDO_FILT but NC on other end.
STEPVCC	Y13	Not Used	LVCMOS25_S_12_I	Hi	SCPCLK	Tie to Ground - not used
TCK_JTAG	U11	JTAG Clock	NC	-	TCK_JTAG	Connects to DLPC410, DLPR410, and JTAG header TCK (if user has JTAG they must build their chain accordingly)
TDO_DDC	W10	JTAG Data Clock out of DLPC410	NC	-	TCK_JTAG	Connects to JTAG return TDO on JTAG header
TDO_XCF16DDC	V11	JTAG Data Clock out of DLPR410 to DLPC410	NC	-	TCK_JTAG	Connects to DLPR410 TDO (DLPC410 internal signal TDI_0)
TMS_JTAG	V12	JTAG	NC	Hi	TCK_JTAG	Connects to DLPC410, DLPR410, and JTAG header TMS
VBATT_0	K18	Not Used	NC	-	-	On Eval board this is connected to 4.7 KΩ pullup to 2.5 V
VCCAUX	J8, K17, L8, M17, N8, P17, R8, T17, U8, V17, W8, W16	Aux Power	POWER	-	-	VCC_2P5V

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
VCCINT	H15, J12, J14, J16, K9, K13, K15, L10, L12, L14, L16, M9, M11, M15, N10, N12, N16, P9, P11, P15, R10, R12, R16, T9, T11, T13, T15, U10, U12, U14, U16, V9, V13, V15, W14, Y15	Power	POWER	-	-	VCC_1P0V
VCCO_0	Y9, W12	Power	POWER	-	-	VCC_2P5V
VCCO_1	C10, F11	Power	POWER	-	-	
VCCO_2	AA16, AD17	Power	POWER	-	-	
VCCO_3	D17, E14	Power	POWER	-	-	
VCCO_4	AB13, AC10					
VCCO_11	F21, H25, J22	Power	POWER	-	-	
VCCO_12	H5, J2, L6	Power	POWER	-	-	
VCCO_13	M23, N20, R24	Power	POWER	-	-	
VCCO_14	R4, V5, W2	Power	POWER	-	-	
VCCO_15	B23,C20, E24	Power	POWER	-	-	
VCCO_16	D7, E4, G8	Power	POWER	-	-	
VCCO_17	T21, V25, W22	Power	POWER	-	-	
VCCO_18 VCCO_21	AA6, AB3, AD7	Power	POWER	-	-	
VLED0	AC18	Power Indicator LED Output	LVCMOS25_F_12_O	Hi = On	-	Connects to LED D9 in series with 22.1 Ω resistor to 2.5 V
VLED1	AD18	Heartbeat Indicator LED Output	LVCMOS25_F_12_O	Hi = On	-	Connects to LED D10 in series with 22.1 Ω resistor to 2.5 V
VN_0	P13	-	NC	-	-	Ground in Schematic
VP_0	N14	-	NC	-	-	Ground in Schematic
VREFN_0	N13	Reference Voltage	LVCMOS25_S_12	-	-	Ground in Schematic
VREFP_0	P14	Reference Voltage	LVCMOS25_S_12	-	-	Ground in Schematic
WDT_ENBLZ	AA13	DMD Reset Watchdog Timer Enable	LVCMOS25_S_12_I	Lo	-	

Table 3. I/O Signal Descriptions (continued)

PIN		DESCRIPTION	I/O Type	ACTIVE (Hi or Lo)	CLOCK SYSTEM	NOTES
NAME	NO.					
UNUSED	AB23, AC20, AD9, AD16, AD20, AD21, AD23, AD24, AD25, AD26, AE7, AE8, AE10, AE11, AE12, AE13, AE13, AE15, AE16, AE17, AE18, AE20, AE21, AE22, AE23, AE24, AE25, AE26, AF7, AF8, AF9, AF10, AF12, AF12, AF13, AF14, AF15, AF17, AF18, AF19, AF20, AF22, AF23, AF24, AF25	Unused Pins	NC	-	-	No Connection (listed as Xilinx NC0 - NC42)

ELECTRICAL AND ENVIRONMENTAL CHARACTERISTICS

The information contained in the following sections has been adapted from the Xilinx XC5VLX30 Datasheet. For any information beyond what is listed here, consult the Xilinx XC5VLX30 Datasheet. Where appropriate, DLPC410 specific values have been substituted in place of generic parameters.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		VALUES		UNITS
Electrical		**MIN**	**MAX**	
Supply voltage range(2)	V_{CCINT}	–0.50	1.05	V
	V_{CCO}	–0.50	3.45	V
	V_{CCAUX}	2.35	2.625	V
Input voltage range, V_I(3)	2.5 V	–0.75	V_{CCO} + 0.50	V
Output voltage range, V_O (4)	2.5 V	–0.30	V_{CCO} + 0.30	V
Environmental				
Operating free-air temperature range, T_A (5)		0	85	°C
Storage temperature range, T_{stg}		–65	150	°C
ESD	Human Body Model		2000	V
	Device Charge Model		400	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Applies to external input and bidirectional buffers.
(4) Applies to external output and bidirectional buffers.
(5) Maximum Ambient Temperature may be further limited by the device’s power dissipation (which is data and configuration dependent), air flow and resultant junction temperature.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CCINT}	1 V Supply voltage, core logic		0.95	1.00	1.05	V
V_{CCO}	2.5 V Supply voltage, I/O		1.14	2.50	3.45	V
V_{CCAUX}	2.5V Supply voltage, I/O		2.375	2.500	2.625	V
V_I	Input voltage	2.5V CMOS	0		V_{CCO}	V
		2.5V LVDS	0.3		2.2	V
V_O	Output voltage	2.5V CMOS	0		V_{CCO}	V
		2.5V LVDS	0.825		1.675	
T_J	Operating junction temperature(1)		0		125	°C
P_D	Continuous total power dissipation			2.7	2.8	W

(1) Thermal analysis and design should be carefully considered to ensure that the junction temperature is maintained within the above specifications.

I/O CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
V_{IH}	High-level Input voltage	2.5V CMOS	1.7			V
V_{IL}	Low-level Input voltage	2.5V CMOS			0.7	V
V_{OH}	High-level output voltage	2.5V Interface	V_{CCO}-.4			V
		2.5V LVDS		1.38		
V_{OL}	Low-level output voltage	2.5V Interface			0.4	V
		2.5V LVDS		1.03		
C_I	Input capacitance	2.5V Interface		8		pF
		2.5V LVDS		8		
I_{CCINT}	Supply voltage range, Core Supply			300		mA
I_{CCO}	Supply voltage range, I/O Supply			850		mA

TIMING REQUIREMENTS(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{cd}	Clock frequency, DCLKIN_n (2)		200		400	MHz
f_{cr}	Clock frequency, CLK_R			50		MHz
t_c	Cycle time, DCLKIN_n		2.5		5	ns
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	1.25		2.5	ns
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	1.25		2.5	ns
t_t	Transition time, $t_t = t_f / t_r$	20% to 80% reference points (signal)			.6	ns
t_{jp}	Period Jitter DCLKIN_n (3)			150		ps
t_{SK}	Skew, DIN_A(15-0) to DCLKIN_A		–150		150	ps
	Skew, DIN_B(15-0) to DCLKIN_B		–150		150	
	Skew, DIN_C(15-0) to DCLKIN_C		–150		150	
	Skew, DIN_D(15-0) to DCLKIN_D		–150		150	
	Skew, DVALID_n to DCLKIN_n↑		–150		150	
	Skew, BLK_MD BLK_AD to DCLKIN_n↑ (4)		–150		150	
	Skew, ROWMD or ROWAD to DCLKIN_n↑ (4)		–150		150	
	Skew, STEPVCC to DCLKIN↑ (4)		–150		150	

(1) It is recommended that the COMP_DATA, NS_FLIP and RST2BLKZ flags be set to one value and not adjusted during normal system operation.
(2) Preferred DCLKIN_n duty cycle = 50%
(3) This is the deviation in period from ideal period due solely to high frequency jitter.
(4) First edge of DIN*, ROW*, BLK* and STEPVCC should be synchronous to DVALID rising edge

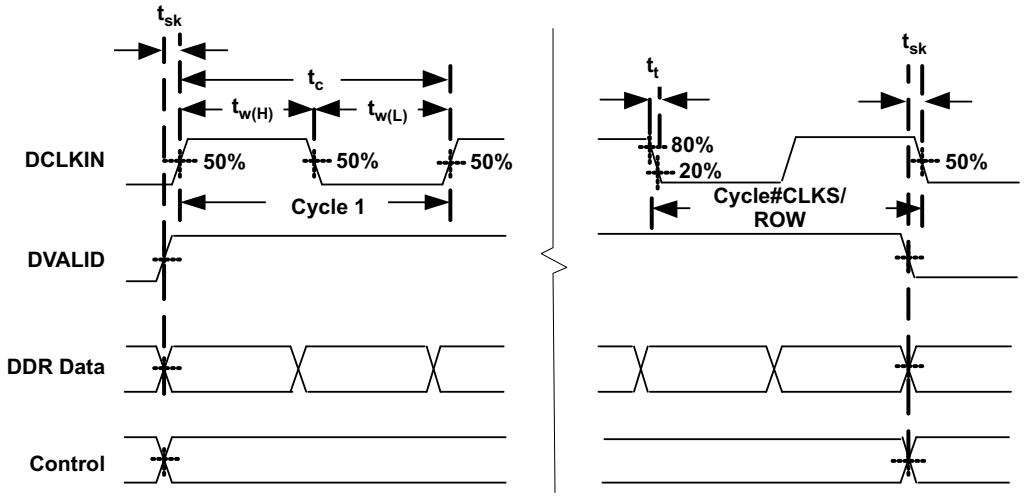


Figure 8. Input Interface Timing

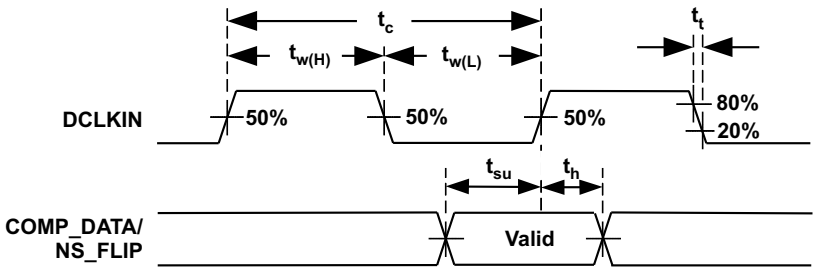


Figure 9. Control Timing

NOTE

Dynamic changes to NS_FLIP and COMP_DATA during normal operation is not recommended.

DLPC410 Control Interface

Clocks and Reset Inputs

ARSTZ

ARSTZ is an active low, asynchronous reset. This reset can be sourced from a voltage supervisor or from the customer interface. Be aware that the chipset will not operate correctly if all DLPC410 power supplies are not in range at the time this reset is released.

CLKIN_R

The reference clock, CLKIN_R, supplied from an oscillator must be 50MHz. This is required for precise timing used to perform the DMD Mirror Clocking Pulse (Reset). This clock should be valid prior to releasing ARSTZ.

DDC_DCLKIN_[A, B, C, D]

The data clock, DDC_DCLKIN, must operate continuously. All signals associated with the data clock should be synchronous to these signals. For example, DDC_DIN_* and DVALID should be synchronous to the rising edge of DDC_DCLKIN. This clock should be valid prior to releasing ARSTZ. DDC_DCLKIN is a DDR clock with data loaded on both rising and falling edges of DDC_DCLKIN. The jitter on this clock should be minimal.

Control Inputs

The DLPC410 supports two 2XLVDS DMD types as shown in Table 4.

Table 4. DMD Characteristics

TYPE	DMD_TYPE	COLS	ROWS	BLKS	ROWS and BLK	CLKS and ROW	#DIN
DLP9500 - 0.95 1080p Type A	000	1920	1080	15	72	16	64
DLP7000 - 0.7 XGA Type A	001	1024	768	16	48	16	32

Note 1 : The DLP9500 DMD is loaded as 15 blocks of 72 rows each. The first 64 bits of pixel data and last 64 bits of pixel data for all rows are not visible.

System Initialization Signals

The INIT_ACTIVE signal indicates that the DMD, Digital Micromirror Driver, and the Digital Controller are in an initialization state after power is applied. During this initialization period, the DLPC410 is calibrating the data interface, and initializing the DMD and DLPA200 by setting all internal registers to their correct states. When this signal goes low, the system has completed initialization. System initialization takes approximately 220 ms to complete. Data and command write cycles must not be asserted during the initialization. This signal is driven by a CLK_R register and should be considered an asynchronous signal. Standard synchronization techniques should be applied if monitoring this signal with a synchronous circuit clocked by a clock other than CLK_R. After initialization is complete, a delay of at least 64 clocks should be observed before the first DVALID is asserted (to ensure a clean start up process).

Note: The NS_FLIP, COMP_DATA, and RST2BLKZ signals should be kept low during initialization to ensure proper setup of the system.

DMD Operations

The DMD data is loaded one row at a time with two (DLP7000) or four (DLP9500) LVDS buses into the DMD SRAM pixels. The DLP9500 requires all four data buses (A,B,C,D) while the DLP7000 requires only two data buses (A,B). Each bus consists of a clock (DDC_DCLKOUT), a control signal (SCTRL) and 16 differential pairs of LVDS signals (DDC_DOUT[15:0]) that are output from the DLPC410 as listed in Table 3. Data, and control are clocked into the DMD on both the rising and falling edges of the DDR data clocks -- DDC_DCLKOUT_[A, B, C, D]. Data loading does not cause mirror switching until a Mirror Clocking Pulse (Reset) operation is completed.

The row load length in clocks can be determined by the equation (number of pixels per rows) / (data bus bit width x 2 edges per clock). There is a two in the denominator because the DMD data bus is dual data rate. This equation yields 15 clocks per row for 1920 x 1080 and a 64 bit bus or 16 clocks per row for 1024x768 and a 32 bit bus. However, with the DLP9500 there are 64 bits at the beginning and end of each row that are not displayed, yielding 16 clocks per row for both 1920x1080 and 1024x768 displays.

DLPC410 LVDS Input Data Bus Operations

Figure 10 shows an example of how the data should be formatted for a DLP9500 which takes 16 clocks to load a row. The clock should be synchronous and edge aligned with all data and control signals. Depending on the design, skewing the clock to data relationship may cause a problem.

No visible data is loaded for the first clock cycle for A and B data and for the last clock cycle for C and D data for each row load operation. This only applies to the DLP9500.

Figure 11 shows an example of the data formatting for the DLP7000.

The DVALID signal should be asserted synchronous to the data it is meant to frame. DVALID can be asserted as:

- Framing individual row loads with breaks between rows
- Framing block loads
- Framing the entire DMD load

If the DVALID frames blocks or the whole DMD, assure that block and row controls are adjusted at the proper locations in the data stream. See section Block Operations for further information.

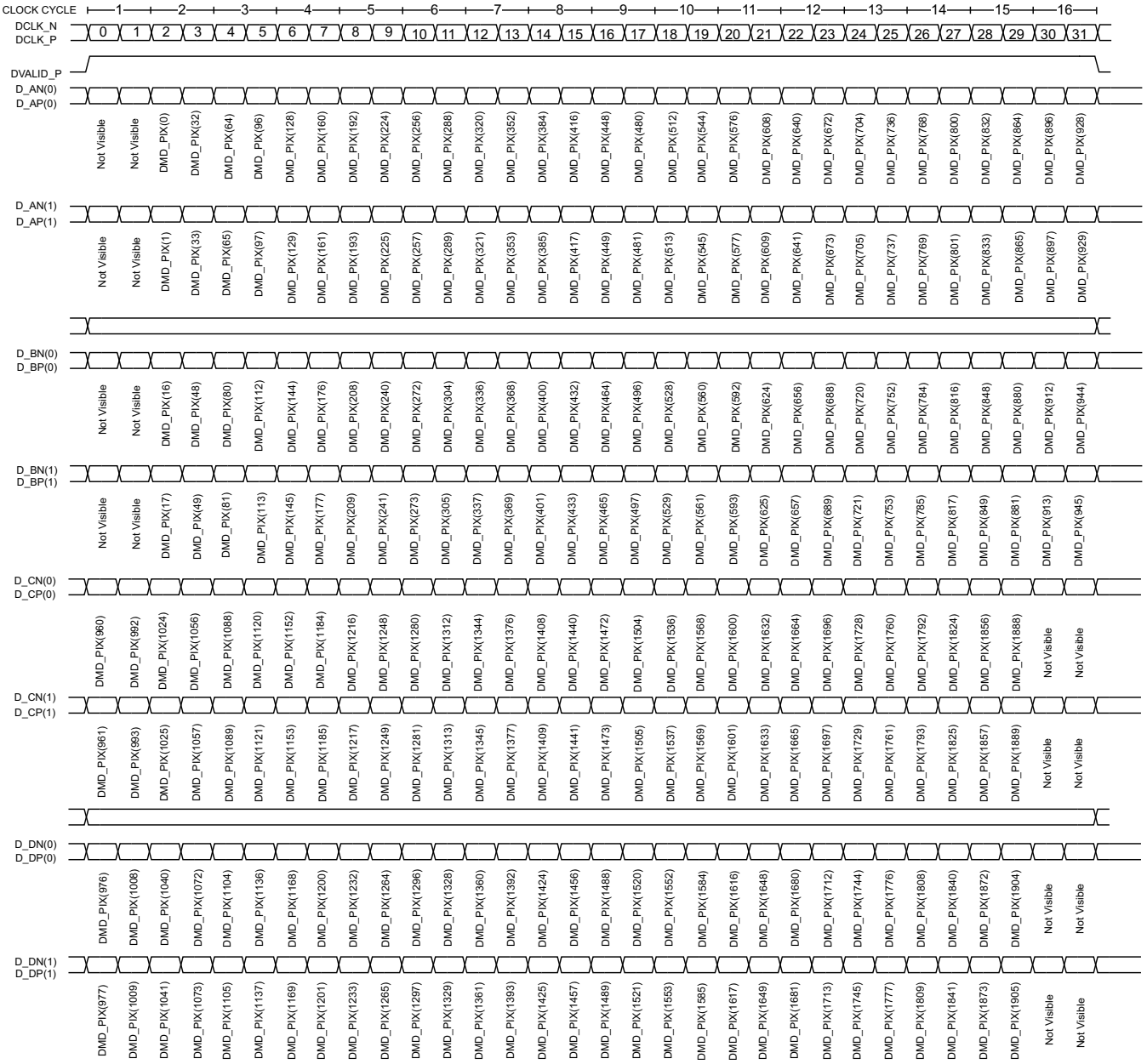


Figure 10. DLP9500 2XLVDS DMD Input Data Bus

Table 5. DLP9500 2XLVDS DMD Data Pixel Mapping

DCLK Edge	D_A(0)	D_A(1)	D_A(2)	D_A(3)	D_A(4)	D_A(5)	D_A(6)	D_A(7)	D_A(8)	D_A(9)	D_A(10)	D_A(11)	D_A(12)	D_A(13)	D_A(14)	D_A(15)
0	Not Visible															
1																
2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
3	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
5	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
6	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
7	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
8	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
9	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
10	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271
11	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
12	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335
13	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367
14	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399
15	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431
16	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463
17	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495
18	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527
19	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559
20	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591
21	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623
22	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655
23	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687
24	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719
25	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751
26	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783
27	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815
28	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847
29	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879
30	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911
31	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943

DCLK Edge	D_B(0)	D_B(1)	D_B(2)	D_B(3)	D_B(4)	D_B(5)	D_B(6)	D_B(7)	D_B(8)	D_B(9)	D_B(10)	D_B(11)	D_B(12)	D_B(13)	D_B(14)	D_B(15)
0	Not Visible															
1																
2	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
4	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
5	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
6	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
7	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
8	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
9	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
10	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
11	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
12	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
13	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
14	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
15	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447
16	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
17	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511
18	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
19	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
20	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607

DCLK Edge	D_B(0)	D_B(1)	D_B(2)	D_B(3)	D_B(4)	D_B(5)	D_B(6)	D_B(7)	D_B(8)	D_B(9)	D_B(10)	D_B(11)	D_B(12)	D_B(13)	D_B(14)	D_B(15)
21	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
22	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
23	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
24	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
25	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
26	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
27	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
28	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
29	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
30	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
31	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959

DCLK Edge	D_C(0)	D_C(1)	D_C(2)	D_C(3)	D_C(4)	D_C(5)	D_C(6)	D_C(7)	D_C(8)	D_C(9)	D_C(10)	D_C(11)	D_C(12)	D_C(13)	D_C(14)	D_C(15)
0	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975
1	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007
2	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
3	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
4	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
5	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
6	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
7	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
8	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
9	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
10	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
11	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
12	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
13	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
14	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
15	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
16	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
17	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
18	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
19	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
20	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
21	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
22	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
23	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
24	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
25	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
26	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
27	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
28	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
29	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
30	Not Visible															
31																

DCLK Edge	D_D(0)	D_D(1)	D_D(2)	D_D(3)	D_D(4)	D_D(5)	D_D(6)	D_D(7)	D_D(8)	D_D(9)	D_D(10)	D_D(11)	D_D(12)	D_D(13)	D_D(14)	D_D(15)
0	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
1	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023
2	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
3	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
4	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
5	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
6	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
7	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215

DCLK Edge	D_D(0)	D_D(1)	D_D(2)	D_D(3)	D_D(4)	D_D(5)	D_D(6)	D_D(7)	D_D(8)	D_D(9)	D_D(10)	D_D(11)	D_D(12)	D_D(13)	D_D(14)	D_D(15)
8	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
9	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
10	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
11	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
12	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
13	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
14	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
15	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
16	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
17	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535
18	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
19	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
20	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
21	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
22	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
23	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
24	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
25	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791
26	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
27	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
28	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
29	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
30	Not Visible															
31																

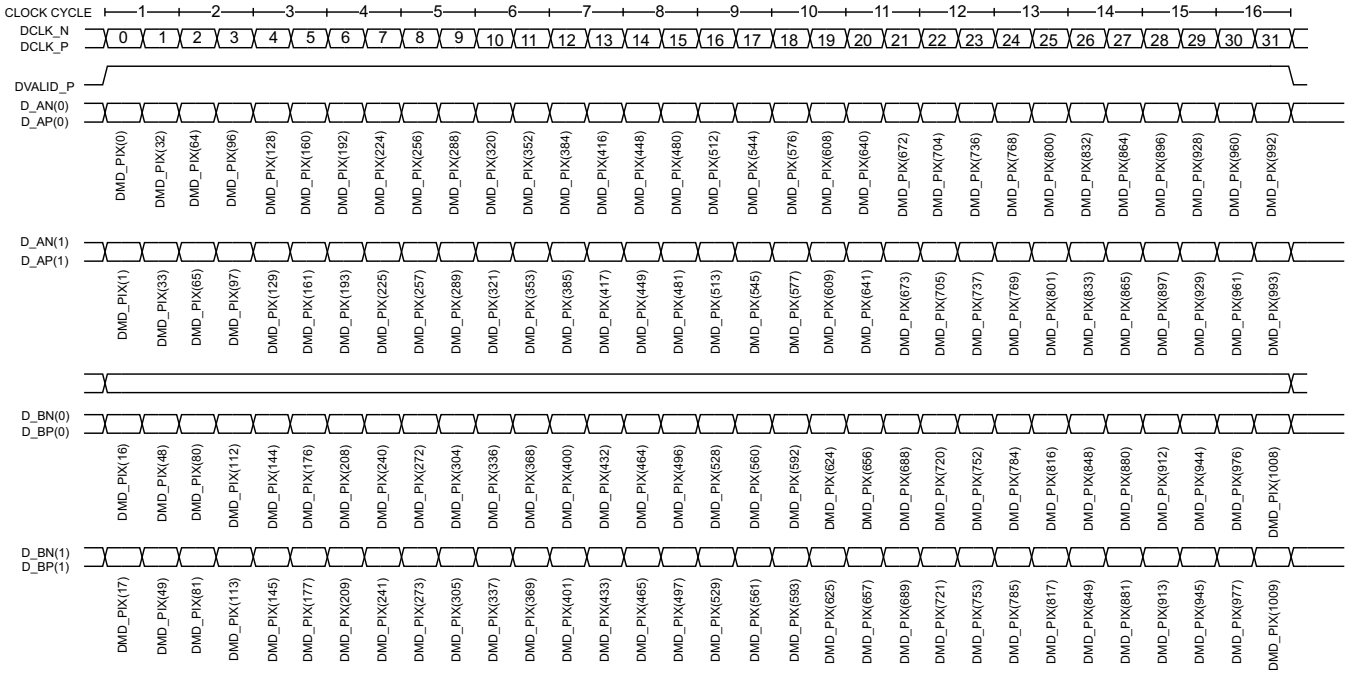


Figure 11. DLP7000 2XLVDS DMD Input Data Bus

Table 6. DLP7000 2XLVDS DMD Data Pixel Mapping

DCLK Edge	D_A(0)	D_A(1)	D_A(2)	D_A(3)	D_A(4)	D_A(5)	D_A(6)	D_A(7)	D_A(8)	D_A(9)	D_A(10)	D_A(11)	D_A(12)	D_A(13)	D_A(14)	D_A(15)
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
2	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
3	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
4	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
5	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
6	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
7	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
8	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271
9	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
10	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335
11	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367
12	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399
13	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431
14	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463
15	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495
16	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527
17	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559
18	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591
19	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623
20	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655
21	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687
22	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719
23	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751
24	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783
25	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815
26	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847
27	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879
28	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911
29	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943
30	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975
31	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007

DCLK Edge	D_B(0)	D_B(1)	D_B(2)	D_B(3)	D_B(4)	D_B(5)	D_B(6)	D_B(7)	D_B(8)	D_B(9)	D_B(10)	D_B(11)	D_B(12)	D_B(13)	D_B(14)	D_B(15)
0	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
1	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
2	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
3	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
4	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
5	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
6	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
7	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
8	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
9	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
10	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
11	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
12	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
13	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447
14	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
15	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511
16	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
17	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
18	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
19	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
20	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671

DCLK Edge	D_B(0)	D_B(1)	D_B(2)	D_B(3)	D_B(4)	D_B(5)	D_B(6)	D_B(7)	D_B(8)	D_B(9)	D_B(10)	D_B(11)	D_B(12)	D_B(13)	D_B(14)	D_B(15)
21	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
22	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
23	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
24	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
25	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
26	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
27	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
28	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
29	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959
30	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
31	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

Block Operations

The DMD mirrors and corresponding SRAM pixels are organized into BLKS and each block is broken into groups of ROWS per BLK as described in Table 4. Mirror blocks are addressed for either the Mirror Clocking Pulse (Reset) or Memory Clear functions by asserting block control signals at the start of each row data load. RST2BLKZ, BLK_MD and BLK_AD are used as shown in Table 7 to designate which mirror block(s) is to be issued a Mirror Clocking Pulse or Cleared. Refer to the individual DMD data sheets for block location information.

- The clear operation sets all of the SRAM pixels in the designated block to logic zero during the current row cycle.
- It is possible to issue a Mirror Clocking Pulse a block while loading a different block.
- It is not possible to Clear a block while writing to a different block.
- It is not necessary to Clear a block if it is going to be reloaded with new data (just like a normal memory cell).
- For the DLP9500 a Block Clear operation must be followed by two no-op row load cycles.
- Note that the DLP9500 has 15 blocks (block 00 – block 14) so block operations on block 15 have no function for this DMD.
- It is recommended that RST2BLKZ be set to one value and not adjusted during normal system operation. A change in RST2BLKZ is not immediately effective and will require more than one row load cycle to complete.

WARNING: 1080p DMD only

To clear one Mirror Clocking Pulse (Reset) Group in the DMD Block, one Clear command followed by two consecutive No Operation commands are required. Therefore, 15 total Block Clear commands and 30 total No Operation commands are required to clear the entire DMD array.

NOTE

RST2BLKZ needs to be kept low during initialization for proper setup of the system.

Table 7. Block Operations

RST2BLKZ	BLK_MD 1	BLK_MD 0	BLK_AD 3	BLK_AD2	BLK_AD 1	BLK_AD 0	Operation
X	0	0	X	X	X	X	None
X	0	1	0	0	0	0	Clear block 00
X	0	1	0	0	0	1	Clear block 01
X	0	1	0	0	1	0	Clear block 02
X	0	1	0	0	1	1	Clear block 03
X	0	1	0	1	0	0	Clear block 04
X	0	1	0	1	0	1	Clear block 05
X	0	1	0	1	1	0	Clear block 06
X	0	1	0	1	1	1	Clear block 07
X	0	1	1	0	0	0	Clear block 08
X	0	1	1	0	0	1	Clear block 09
X	0	1	1	0	1	0	Clear block 10
X	0	1	1	0	1	1	Clear block 11
X	0	1	1	1	0	0	Clear block 12
X	0	1	1	1	0	1	Clear block 13
X	0	1	1	1	1	0	Clear block 14
X	0	1	1	1	1	1	Clear block 15
X	1	0	0	0	0	0	Reset block 00
X	1	0	0	0	0	1	Reset block 01
X	1	0	0	0	1	0	Reset block 02
X	1	0	0	0	1	1	Reset block 03
X	1	0	0	1	0	0	Reset block 04
X	1	0	0	1	0	1	Reset block 05
X	1	0	0	1	1	0	Reset block 06
X	1	0	0	1	1	1	Reset block 07
X	1	0	1	0	0	0	Reset block 08

Table 7. Block Operations (continued)

RST2BLKZ	BLK_MD 1	BLK_MD 0	BLK_AD 3	BLK_AD2	BLK_AD 1	BLK_AD 0	Operation
X	1	0	1	0	0	1	Reset block 09
X	1	0	1	0	1	0	Reset block 10
X	1	0	1	0	1	1	Reset block 11
X	1	0	1	1	0	0	Reset block 12
X	1	0	1	1	0	1	Reset block 13
X	1	0	1	1	1	0	Reset block 14
X	1	0	1	1	1	1	Reset block 15
0	1	1	0	0	0	0	Reset blocks 00-01
0	1	1	0	0	0	1	Reset blocks 02-03
0	1	1	0	0	1	0	Reset blocks 04-05
0	1	1	0	0	1	1	Reset blocks 06-07
0	1	1	0	1	0	0	Reset blocks 08-09
0	1	1	0	1	0	1	Reset blocks 10-11
0	1	1	0	1	1	0	Reset blocks 12-13
0	1	1	0	1	1	1	Reset blocks 14-15
1	1	1	0	0	0	X	Reset blocks 00-03
1	1	1	0	0	1	X	Reset blocks 04-07
1	1	1	0	1	0	X	Reset blocks 08-11
1	1	1	0	1	1	X	Reset blocks 12-15
X	1	1	1	0	X	X	Reset blocks 00-15
X	1	1	1	1	X	X	Float blocks 00-15

Mirror Clocking Pulse (Reset) and Float Operations

A Mirror Clocking Pulse (Reset) sequence begins by asserting BLK_MD and BLK_AD as described in Table 7. Shortly after, RST_ACTIVE goes high for approximately 4.5 µs, indicating a Mirror Clocking Pulse operation is in progress. During this time, no additional Mirror Clocking Pulses may be initiated until RST_ACTIVE returns low. RST_ACTIVE does not return to low unless continuous no-op or data loading row cycles are issued. See the Figure 12 and Figure 13 for typical Mirror Clocking Pulse sequences in which consecutive DMD blocks are loaded then sent Mirror Clocking Pulses. Mirror Clocking Pulse time is identical for single, dual, quad or global operations.

Note that it may take longer to complete a Mirror Clocking Pulse on a block than it does to load, depending on the clock rate and the DMD type, so the scenario in Figure 12 does not show the situation when the Mirror Clocking Pulse time exceeds the block load time. The block load time may be calculated as:

Block Load Time = Clock Period × number CLKS per ROW × number ROWS per BLK

Table 8. DMD Block Load Time at 400MHz DMD Clock

DMD	Minimum Block Load Time
DLP7000	1.92 µsec
DLP9500	2.88 µsec

For any case which involves sending a Mirror Clocking Pulse or Clearing blocks without data loading, the customer interface must send no-op row cycles. This can be accomplished by asserting DVALID, while holding ROWMD at “00” and BLKMD at “00” for number of CLKS per ROW (Table 8) clock cycles, as in Figure 14. For example, the sequence shown in Figure 13 does not show the required no-op row during the Delay cycle where the Mirror Clocking Pulse of Block 0 occurs. At least one row cycle must be completed to initiate the Mirror Clocking Pulse. The same procedure applies to the Global Mirror Clocking Pulse case as shown in Figure 15. Following the loading of all rows in the device, a no-op row cycle must be completed to initiate the Mirror Clocking Pulse. If the global Mirror Clocking Pulse is asserted prior to loading all rows of the device, rows which were not updated will show old data. Additional Mirror Clocking Pulse operations may not be initiated until RST_ACTIVE is low. Block clear operations for DLP9500 must be followed by two consecutive no-op row cycle commands.

To obtain full utilization of the DLP9500 bandwidth (at 400MHz data rate), load two blocks and then issue a Mirror Clocking Pulse to the two blocks at a time by setting RST2BLKZ to “0” and BLK_MD to “11” and the appropriate address in BLK_AD. This method is indicated in Figure 16. To obtain full utilization of the DLP7000 bandwidth (at 400 MHz data rate), load and issue a Mirror Clocking Pulse to four blocks at a time by setting RST2BLKZ to “1” and BLK_MD to “11” and the appropriate address in BLK_AD.

IMPORTANT:

While RST_ACTIVE is high, and for 8 µs after, the data for the block(s) being issued a Mirror Clocking Pulse should not be changed to allow for the settling required for the mirrors to become stable.

It is possible to load other blocks while the block previously issued a Mirror Clocking Pulse is settling. Figure 17 shows a single block load, Mirror Clocking Pulse and reload sequence with the light gray areas indicating mirror settling time.

It is best to issue a float command to avoid leaving a static image on the DMD for extended periods of time. A mirror float sequence begins by asserting the proper BLK_MD and BLK_AD as described in Table 7. During the following row cycle, the DMD releases the tension under each mirror so that all mirrors are in a relatively flat position. The float operation takes approximately 3 µs to complete, during which time RST_ACTIVE is asserted.

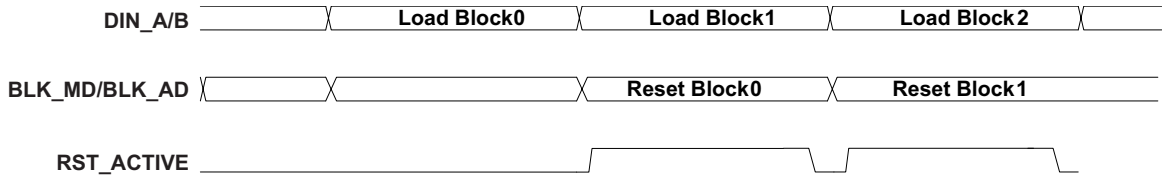


Figure 12. Typical Phased Mirror Clocking Pulse Sequence

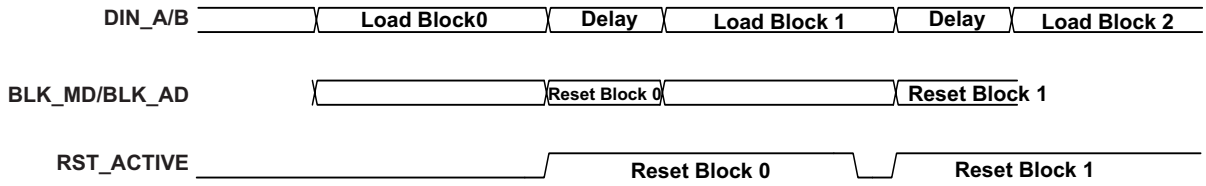


Figure 13. Alternate Phased Mirror Clocking Pulse Sequence

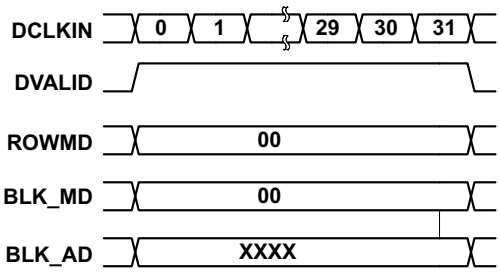


Figure 14. DMD No-op Row Cycle

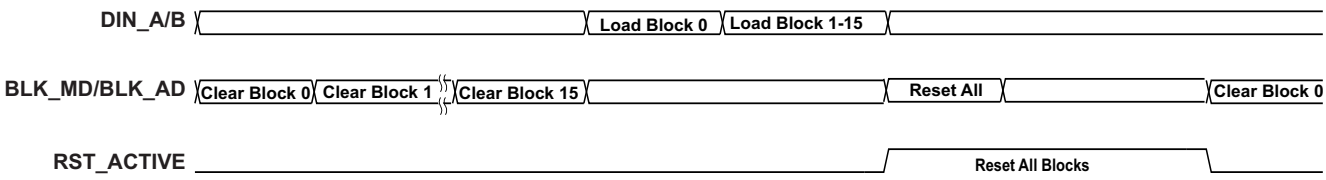


Figure 15. Full Device Load and Global Mirror Clocking Pulse

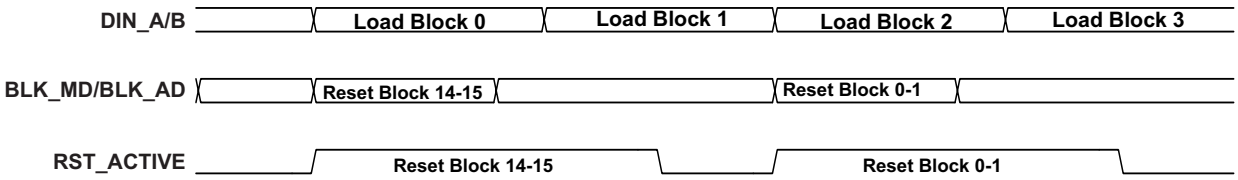


Figure 16. Phased Mirror Clocking Pulse Sequence with Dual Block Mirror Clocking Pulses without Memory Clear

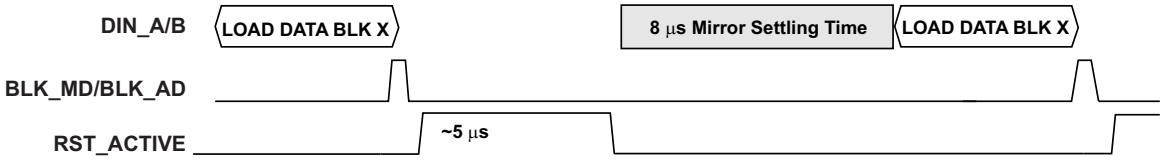


Figure 17. Block Load and Reload

NOTE

After a Mirror Clocking Pulse or Clear command is given, RST_ACTIVE may not be asserted until up to 60ns (depending on the clock frequency) after the command. During this time, no other command should be given.

Power Down Operation

For correct operation of the DMD, the following power down procedure must be executed. Prior to power removal, assert PWR_FLOAT and allow approximately 300 µs for the procedure to complete. This procedure will assure the mirrors are in a flat state, similar to the float operation. Following this procedure, the power can be safely removed.

To restart after assertion of PWR_FLOAT the DLPC410 must be reset (ARSTZ low then high) or power must be cycled.

Global Mirror Clocking Pulse (Reset) Consideration

A Global Mirror Clocking Pulse (BLK_MD = “11” and BLK_AD = “10XX”), takes the same amount of time as the single, dual, and quad block Mirror Clocking Pulses. In addition to requiring a no-op row cycle to initiate a global Mirror Clocking Pulse, a row cycle (either no-op or data loading) is also required to complete the operation. If the customer interface is monitoring RST_ACTIVE to determine when to send a subsequent row cycle, it never sees RST_ACTIVE transition low. One method of operation would be to continue sending no-op row cycles until RST_ACTIVE goes low then continue loading data with real row cycles. Another method of operation is to delay greater than 4.5µs, then start loading new data to DMD.

RST_ACTIVE

After a Mirror Clocking Pulse (Reset) or Float operation is requested, RST_ACTIVE is asserted to indicate that the operation is in progress. Mirror Clocking Pulse and Float Operations has more details about the use of this signal. RST_ACTIVE is synchronized to a version of DCLKIN. As such, circuits in the application FPGA should consider this signal asynchronous and use standard synchronization techniques to assure reliable registering of this signal.

Interface Training Pattern

The DLPC410 detects the phase differences between the ½ speed clock (used in the device driving the LVDS data) and the internally generated ½ speed data clocks and automatically corrects their alignment. This is done by supplying a simple repeating pattern on all of the data inputs while the “INIT_ACTIVE” output of the DLPC410 is high/active. The details of the training pattern are described below.

This is a simple block diagram of the training pattern insertion logic.

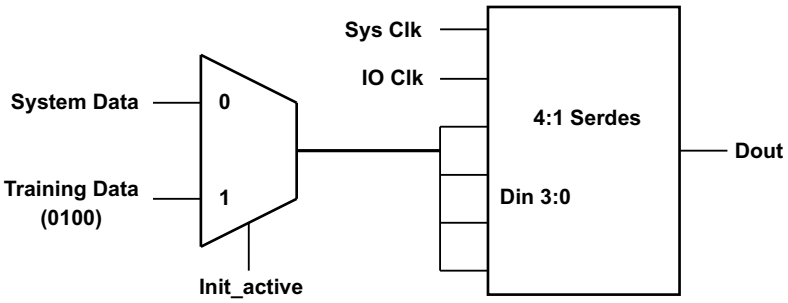


Figure 18. Block Diagram of Training Pattern Logic

The expected training pattern is “0100”. In Figure 19 the data input to the 4:1 SERDES cells is captured on the rising edge of the ½ speed system clock. The output latency shown is based on the documentation for the Xilinx SERDES cells. Individual implementation may vary depending on the type of cells, technology, and design technique used.

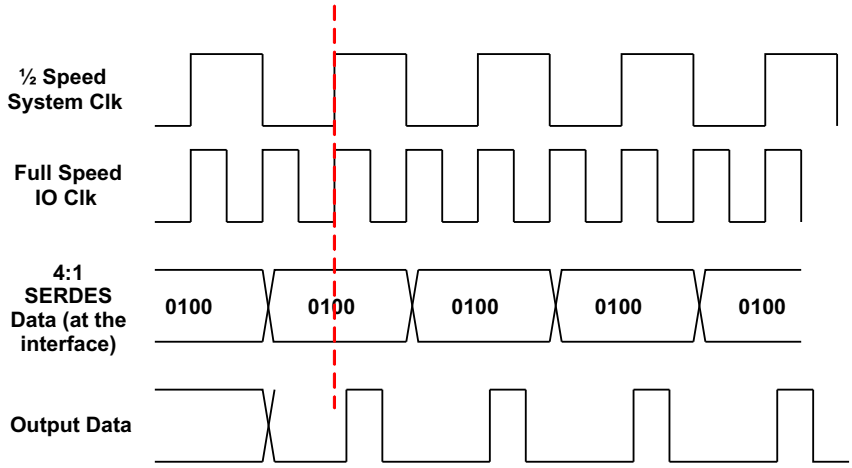


Figure 19. Training Pattern Alignment

NOTE

In Xilinx FPGAs (due to the construction of the ISERDES and OSERDES cells) a pattern of “0010” needs to be applied to the output/transmitting SERDES cells data pins (D1 = 0, D2 = 0, D3 = 1, D4 = 0) in order to receive a result of “0100” (Q1 = 0, Q2 = 1, Q3 = 0, Q4 = 0) at the input/receiving SERDES cell.

The patterns should be applied on all of the data and DVALID pins. In this respect, the interface is treated as a 17 bit interface with DVALID being the 17th data bit. The receiving logic in the DLPC410 will shift the data until the correct pattern is seen at the inputs. The SERDES cells align the incoming data with the ½ speed system clock (derived from the full speed data clock). This allows DLPC410 to correctly align the DVALID signal and the incoming data and will contribute to a more robust interface. It is important that the training pattern is applied to the DVALID and data inputs of the DLPC410 before reset to the device is de-asserted, as training commences immediately on the de-assertion of reset. The INIT_ACTIVE signal is asserted while the device is held in reset in order to help facilitate this behavior.

LED0

The LED0 signal is typically connected to an LED to show that the DLPC410 is operating normally. The signal is 1 Hz with 50% duty cycle, otherwise known as the heartbeat.

LED1

The LED1 signal is typically connected to an LED indicator to show the status of system initialization and the status of the clock circuits. The LED1 signal is asserted only when system initialization is complete and clock circuits are initialized. Logically, these signals are ANDed together to show an indication of the health of the system. If the Phase Locked Loop (PLL) connected to the data clock and the DMD clock are functioning correctly after system initialization, the LED will be illuminated.

Data and Command Write Cycle

Once initialization is complete (INIT_ACTIVE = 0) the user is free to send data and control information to the DLPC410. When the user asserts the DVALID signal for the LVDS input buses, the DLPC410 begins sampling the LVDS data inputs and synchronously sending this information to the DMD along with row address control information. The row cycle period is exactly CLKS and ROW (Table 4) clocks long and begins with DVALID as shown in Figure 10. DLP9500 2XLVDS DMD Input Data Bus. If DVALID is removed, the DLPC410 stops loading data and commands until DVALID goes active again.

Figure 20 shows an example of data written to the DLPC410 for a single row using the DLP7000. Data is written to the DMD 32 bits (16 A bits + 16 B bits) on each clock edge. An entire line must be written for data to be latched into memory and it requires number of CLKS per ROW (Table 4) DDR clock cycles to write a single row of number COLS (Table 4) bits. For the DLP9500 64 data bits (16 A bits + 16 B bits + 16 C bits + 16 D bits) are written on each clock edge. C data and D data bits are not used for the DLP7000.

The DMD incorporates single row write operations using a row address counter that is randomly addressable. As shown in Table 9 and Table 10, ROWMD(1:0) determines the single row write count mode and ROWAD(10:0) determines the single row write address. ROWMD and ROWAD must be asserted and de-asserted synchronously with DVALID and must be valid synchronous to the beginning of the data as shown in Figure 20.

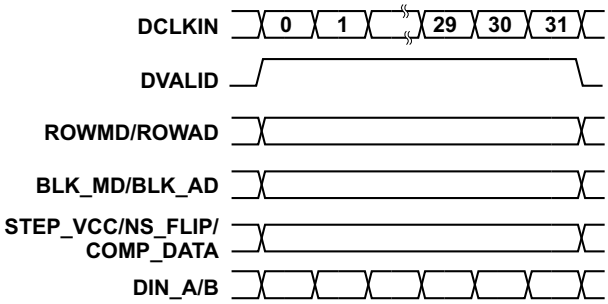


Figure 20. Single Row Write Operation

Row address orientation depends on the North or South Flip Flag (NS_FLIP) input to the DLPC410. See the individual DMD data sheets for orientation of rows, columns, and Mirror Clocking Pulse blocks. The row address counter does not automatically wrap-around when using the increment row address pointer instruction. After the final row is addressed, the row address pointer must be cleared to 0.

Table 9. Row Write Modes - N/S Flip Flag = 0

ROWMD		ROWAD											Action
1	0	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	None
0	1	0	0	0	0	0	0	0	0	0	0	0	Increment row address pointer and write the concurrent data into that row
1	0	R	R	R	R	R	R	R	R	R	R	R	Set row address pointer to R and write the concurrent data into that row.
1	1	0	0	0	0	0	0	0	0	0	0	0	Clear row address pointer to 0 and write concurrent data into first row (that is, row ‘0’)

Table 10. Row Write Modes - N/S Flip Flag = 1

ROWMD		ROWAD											Action
1	0	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	None
0	1	0	0	0	0	0	0	0	0	0	0	0	Decrement the row address pointer and write the concurrent data into that row
1	0	R	R	R	R	R	R	R	R	R	R	R	Set the row address pointer to R and write the concurrent data into that row.
1	1	0	0	0	0	0	0	0	0	0	0	0	Set row address pointer to row = last row and write concurrent data into last row (that is, the last row = 767 for the 0.7 XGA)

Watchdog Timer

The DLPC410 contains a watchdog timer that initiates a global DMD Mirror Clocking Pulse in the event that any DMD reset block has not been Mirror Clocking Pulse by the user within 10 seconds. This auto-Mirror Clocking Pulse function can be disabled by taking WDT_ENABLEZ high.

Miscellaneous DMD Controls

It is recommended that the Complement and Flip flags be set to one value and not adjusted during normal system operation. These controls are asserted through a different mechanism than the data and row controls, hence their effect is asynchronous and cannot be expected to take effect immediately upon assertion.

Complement Data

By setting the COMP_DATA flag high, the user is able to command the DMD to internally complement its data inputs prior to loading the data into the mirror array. At least 0.6 ms is needed for the signal to be loaded. This signal should not be used to invert data on a row basis. When used with the “Clear” command, the mirrors are still set to zero regardless of the COMP_DATA bit. The COMP_DATA signal should be kept low during initialization to ensure proper setup of the system.

North/South Flip

NS_FLIP allows the user to specify the loading direction of rows in the DMD when used with ROWMD = “01”. This control has no effect if ROWMD = “10”.

Table 9 and Table 10 describe the effect of N/S flip. If NS_FLIP is set, this does not reverse the direction of Mirror Clocking Pulse groups. For example, the normal case is to Mirror Clocking Pulse blocks 0 – 15 in order. When NS_FLIP is set, the order of block Mirror Clocking Pulses must be reversed to 15 – 0.

The NS_FLIP signal should be kept low during initialization to ensure proper setup of the system.

Step DMD SRAM Memory Voltage

When the STEP_VCC signal goes high, the DMD internal SRAM voltage is stepped from its normal VCC value (nominally 3.3 V) to the higher VCC2 value (nominally 7.5 V and 8.5 V). The SRAM voltage is stepped back down when this flag goes back low.

This input signal is provided for experimental use and should not be used for normal operation. Contact Texas Instruments for more information.

The step signal should only be asserted when data is not being loaded into the DMD. Therefore, it is necessary to assert a no-op row cycle when stepping up or stepping down the memory voltage.

The watchdog function may override the memory voltage setting if the watchdog times out. The watchdog performs a global Mirror Clocking Pulse, which steps the memory voltage down at the end of the cycle. If this operation is undesirable, disable the watchdog before issuing the STEP_VCC signal.

DMD_A_RESET

DMD_A_RESET is an active low reset to the DMD. This signal is de-asserted as appropriate at the end of system initialization.

DLPA200 Control Signals

Coordinating the operation of the DLPA200 with the DMD is one of the primary functions of the DLPC410. During system initialization, the DLPC410 releases the reset pin (DAD_INIT) and communicates with the DLPA200 via a serial bus to configure the device. Once this is complete, the high voltage output pins are enabled to prepare for command execution. As the DLPC410 is commanded to load data and perform Mirror Clocking Pulses, the DAD_ADDR address, DAD_MODE mode, DAD_SEL select and DAD_STROBE strobe signals are asserted as appropriate to cause the Mirror Clocking Pulse.

DDC_VERSION(3:0)

These four pins identify the version of the DLPC410 determined by the contents of DLPR410, DLPR4101. If a problem is encountered, provide the version number with detailed information of the problem. See the DLPR410, DLPR4101 datasheet (DLPS027) for the version number reported on these pins.

DMD_TYPE(3:0)

Four Output pins from the DLPC410 identify the DMD type detected by the DLPC410 (shown in Table 4). DMD_TYPE will return “1111” if the DMD is not attached or not recognized.

ecm2m_tp_ (31:0)

Reserved signals for test signal output. Do not drive these signals.

"Load 4" Enhanced Functionality (with DLPR4101 PROM only)

The DLPR4101 PROM provides enhanced functionality; improved global binary pattern rates for applications that can trade vertical addressable resolution for higher pattern rates. Examples of these types of applications are shutter/chopper applications and vertical structured light patterns. “Load 4” causes the attached DMD to load 4 rows for every row of data sent, reducing the pattern load time to ¼. It does not reduce the “Mirror Clocking Pulse” and “Settling Time” timings.

Enabling "Load 4"

“Load 4” is enabled by pulling the DLPC410 signal “DDC_SPARE_0” low. It is recommended that for systems using the DLPR4101 PROM Enhanced Functionality that this pin be re-named to a more descriptive name in customer designs (i.e. “LOAD4_ENABLE_Z” or similar)..

Loading Data with "Load 4"

“Load 4” causes the attached DMD to load four rows for every one row of data loaded. “Automatic Increment” mode and “Row Address” mode can still be used as before, however the largest addressable row will be the Vertical Resolution (VRes) of the attached DMD divided by four. For example the XGA will have 1024/4 = 256 addressable rows (that is, 0 . . . 255). The addressable vertical resolution is reduced by four, although the physical resolution is unchanged.

“Automatic Increment” address mode will automatically increment the Row Address input by one (or decrement by one for N/S flip). The Row Address input will be re-mapped as shown in the next section.

Row Mapping with "Load 4"

The rows addresses are re-mapped in a specific way. The following table shows how the rows will be re-mapped:

Table 11. "Load 4" Row Address Mapping

Row Address Input	Physical Rows loaded on DMD
0	0, 1, 2, 3
1	4, 5, 6, 7
2	8, 9, 10, 11
3	12, 13, 14, 15

Table 11. "Load 4" Row Address Mapping (continued)

Row Address Input	Physical Rows loaded on DMD
. . .	. . .
N	4N, 4N+1, 4N+2, 4N+3
. . .	. . .
(VRes/4) -1	VRes-4, VRes-3, VRes-2, VRes-1

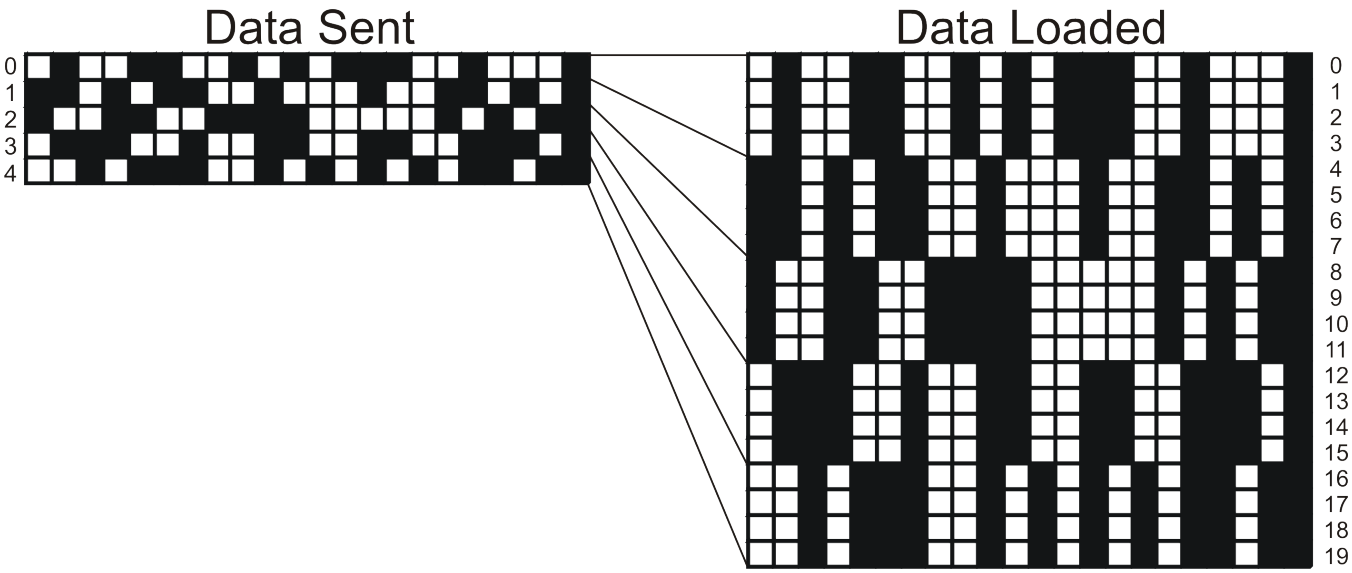


Figure 21. Load 4 Row Address Mapping

Using Block Clear with "Load 4"

While “Load 4” is enabled, Block Clear requests will be ignored. To load using “Load 4” followed by Block Clear request(s), simply de-assert “Load 4” at the beginning of the “Mirror Clocking Pulse” request(s) preceding the Block Clear request(s). Re-assert “Load 4” at the beginning of the “Mirror Clocking Pulse” request(s) preceding the next desired “Load 4” operation. This will ensure that the DLPC410 Controller has sufficient time to disable or enable “Load 4” before data is loaded or Block Clear(s) are requested.

Timing Requirements for "Load 4"

“Load 4” functionality is primarily intended to be used with Global Mirror Clocking Pulses. However, It is possible to use a subset of the DMD array including individual Mirror Clocking Pulse Blocks. The driving software/hardware MUST ensure that the average “Mirror Clocking Pulse” (MCP) rate does not exceed 50k MCPs/sec and that the “Mirror Settling Time” is not violated for any Block.

Average rate means averaged over 2-3 Load/Clear cycles. For example if a pattern is loaded and displayed with a Mirror Clocking Pulse followed by a Block Clear and a Mirror Clocking Pulse the “on” display time is very short. However, If the next pattern is loaded and displayed immediately, the average MCP rate may be exceeded, depending on the DMD and the number of Blocks in use. Therefore idle time must be added in the Load or Block Clear cycle to ensure an average MCP rate of 50 MCPs/sec or lower. Typically the smallest pattern display time is desired so that the time is added during the Load cycle rather than the Block Clear cycle so that the “off” time is extended, not the pattern display time.

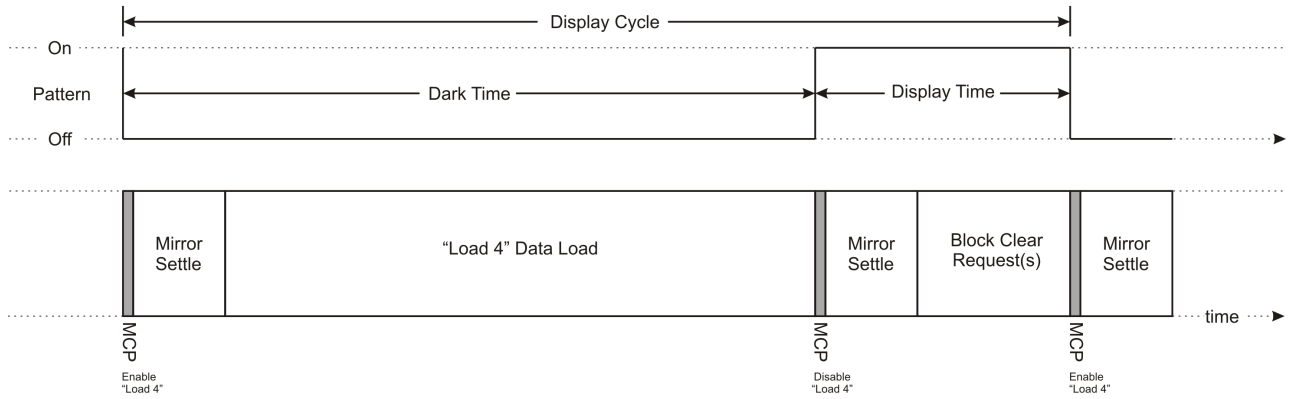


Figure 22. Load 4 with Block Clear - Timing

Global Pattern Rate increase under "Load 4"

Table 12 shows the improvements in binary pattern rate for the DMD's supported by the DLPC410 when using the "Load 4" enhanced functionality of the DLPR4101 PROM:

Table 12. DMD Block Load Time at 400MHz DMD Clock

DMD	Global Frame Rate (with DLPR410)	Global Frame Rate (with DLPR4101 - Enhanced)
DLP7000	23 k binary patterns/sec	48 k binary patterns/sec
DLP9500	18 k binary patterns/sec	42 k binary patterns/sec

REVISION HISTORY

Changes from Original (August 2012) to Revision A **Page**

- Changed the device From: Product Preview to Production 1

Changes from Revision A (September 2012) to Revision B **Page**

- Changed Feature From: 1-Bit Binary Pattern Rates up to 32-kHz To: 1-Bit Binary Pattern Rates up to 32-kHz (up to 48-kHz when used with DLPR4101) 1
- Added DLPR4101 to DLPR410 throughout document 2
- Added Section "Load 4" Enhanced Functionality (with DLPR4101 PROM only) 37

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC410ZYR	ACTIVE	FCBGA	ZYR	676	3	Pb-Free (RoHS)	Call TI	Level-4-250C-72 HRS			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

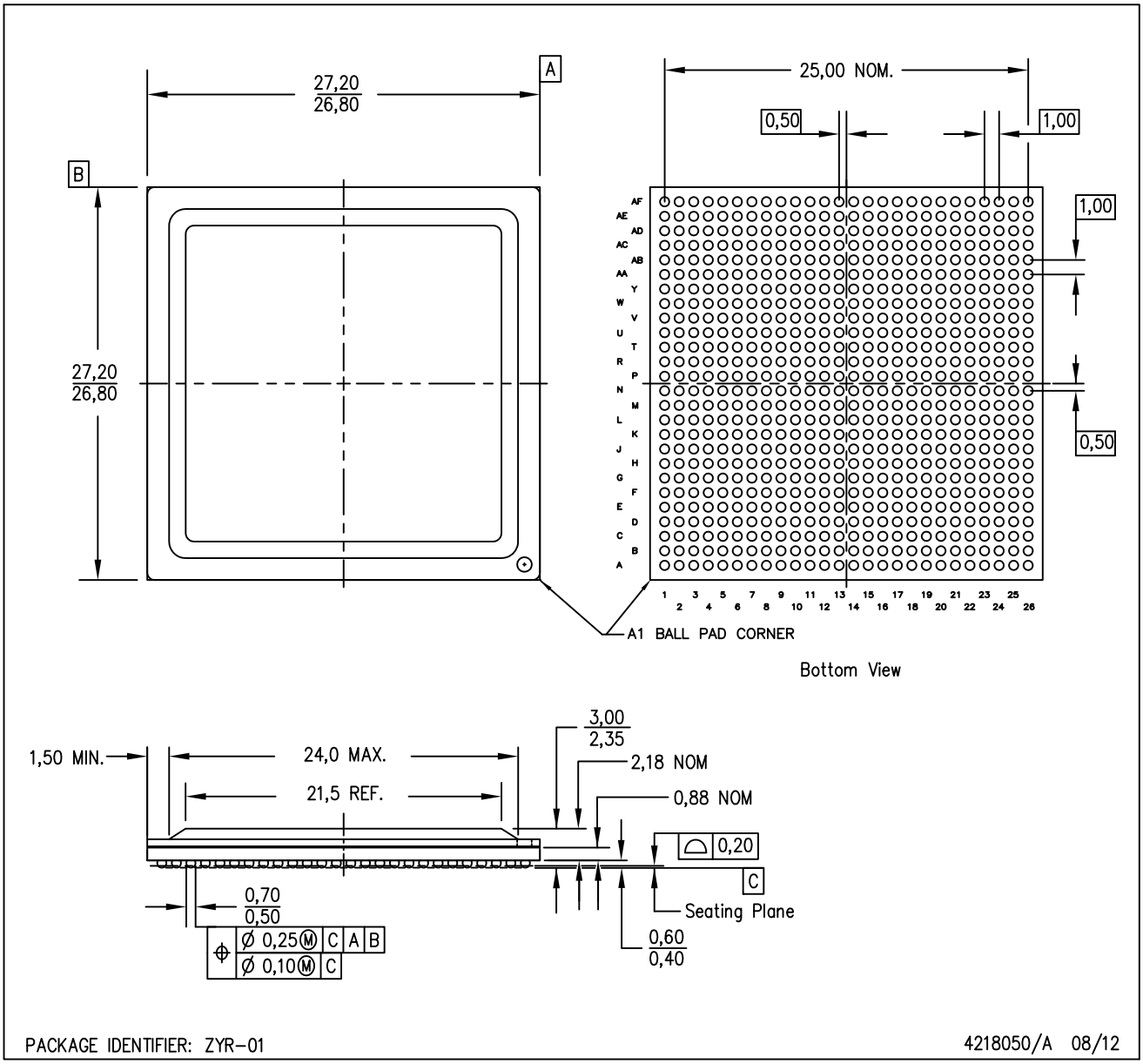
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

ZYR (S–PBGA–N676) PLASTIC BALL GRID ARRAY



PACKAGE IDENTIFIER: ZYR–01 4218050/A 08/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free solder ball.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265