

DLP9500UV DLP® 0.95 UV 1080p 2x LVDS Type A DMD

1 Features

- 0.95-Inch Diagonal Micromirror Array
 - 1920 × 1080 Array of Aluminum, Micrometer-Sized Mirrors (1080p Resolution)
 - 10.8- μ m Micromirror Pitch
 - $\pm 12^\circ$ Micromirror Tilt Angle (Relative to Flat State)
 - Designed for Corner Illumination
- Designed for Use With UV Light (363 to 420 nm):
 - Window Transmission 98% (Single Pass, Through Two Window Surfaces) (Nominal)
 - Micromirror Reflectivity 88% (Nominal)
 - Array Diffraction Efficiency 85% (Nominal)
 - Array Fill Factor 92% (Nominal)
- Four 16-Bit, Low-Voltage Differential Signaling (LVDS), Double Data Rate (DDR) Input Data Buses
- Up to 400-MHz Input Data Clock Rate
- 42.2-mm × 42.2-mm × 7-mm Package Footprint
- Hermetic Package

2 Applications

- Industrial:
 - Direct Imaging Lithography
 - Laser Marking and Repair Systems
 - Computer to Plate Printers
 - Rapid Prototype Machines
 - 3D Printers
- Medical:
 - Ophthalmology
 - Photo Therapy
 - Hyper-Spectral Imaging

3 Description

The 0.95 1080p UV DLP® Chipset is a new chipset addition to the DLP Discovery 4100 platform, which enables high resolution and high performance spatial light modulation beyond the visible spectrum into the UVA spectrum (363 nm to 420 nm). The DLP9500UV digital micromirror device (DMD) is designed with a special window that optimizes UV transmission.

The DLP9500UV is the 0.95 1080p DMD, with a hermetic package, that is sold with the following dedicated chipset (see):

- Dedicated DLPC410 controller for high speed pattern rates of >23000 Hz (1-bit binary) and >1700 Hz (8-bit gray)
- One unit DLPR410 (DLP Discovery 4100 Configuration PROM)
- Two units DLPA200 (DMD micromirror drivers)

Reliable function and operation of the DLP9500UV requires that it be used in conjunction with the other components of the chipset. A dedicated chipset provides developers easier access to the DMD as well as high speed, independent micromirror control.

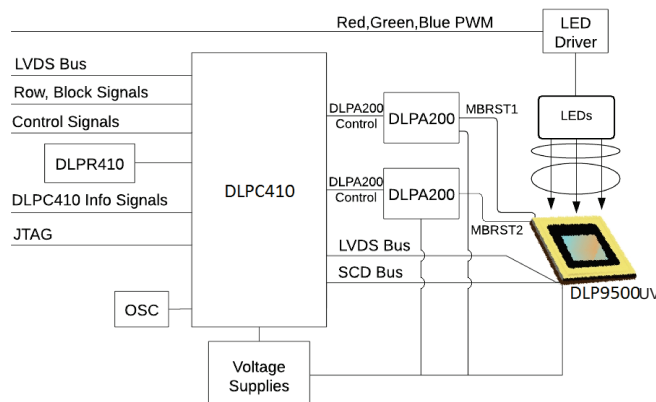
DLP9500UV is a digitally controlled micro-electromechanical system (MEMS) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP9500UV can be used to modulate the amplitude, direction, and/or phase of incoming light.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP9500UV	LCCC (355)	42.16 mm × 42.16 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



4 Revision History

Changes from Original (November 2014) to Revision A	Page
• Updated device status to product preview for release	1
• Updated front page graphic	1
• Added Community Resources	4

PRODUCT PREVIEW

5 Description (continued)

Electrically, the DLP9500UV consists of a two-dimensional array of 1-bit CMOS memory cells, organized in a grid of 1920 memory cell columns by 1080 memory cell rows. The CMOS memory array is addressed on a row-by-row basis, over four 16-bit LVDS DDR buses. Addressing is handled by a serial control bus. The specific CMOS memory access protocol is handled by the DLPC410 digital controller.

6 Device and Documentation Support

6.1 Device Support

6.1.1 Device Nomenclature

Figure 1 provides a legend of reading the complete device name for any DLP device.

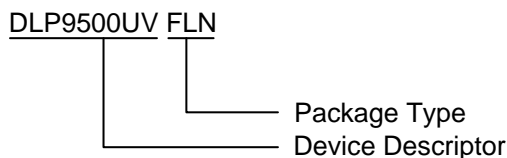


Figure 1. Device Nomenclature

6.1.2 Device Marking

Figure 2 shows the device marking fields.

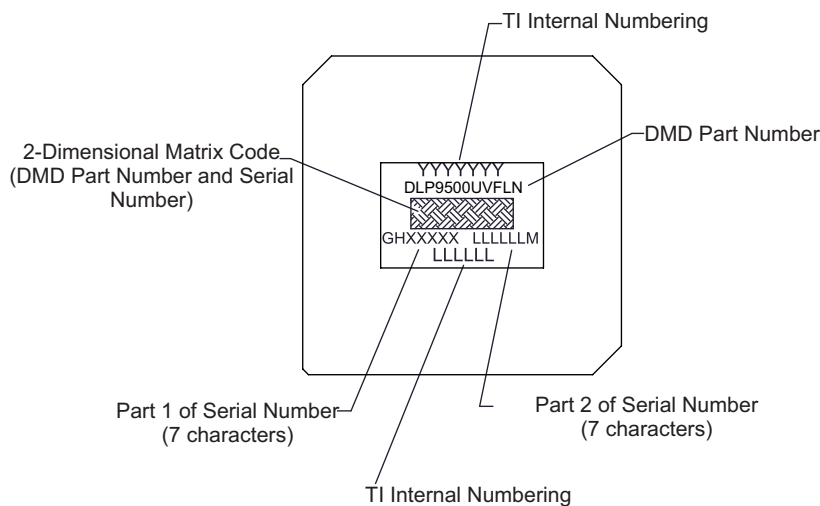


Figure 2. DLP9500UV Device Marking

6.2 Documentation Support

6.2.1 Related Documentation

The following documents contain additional information related to the use of the DLP9500UV device.

- [DLP Discovery 4100](#) chipset data sheet
- [DLPC410](#) digital controller data sheet
- [DLPA200](#) DMD micromirror driver data sheet
- [DLPR410](#) EEPROM data sheet

6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.4 Trademarks

E2E is a trademark of Texas Instruments.

DLP is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

6.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP9500UVFLN	PREVIEW	LCCC	FLN	355	5	Green (RoHS & no Sb/Br)	W NIAU	N / A for Pkg Type			
DLPA200PPF	ACTIVE	HTQFP	PPF	80	5	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR			Samples
DLPC410ZYR	ACTIVE	FCBGA	ZYR	676	3	Pb-Free (RoHS)	Call TI	Level-4-250C-72 HRS			Samples
DLPR410YVA	ACTIVE	DSBGA	YVA	48	3	Pb-Free (RoHS)	Call TI	Level-3-260C-168 HR			Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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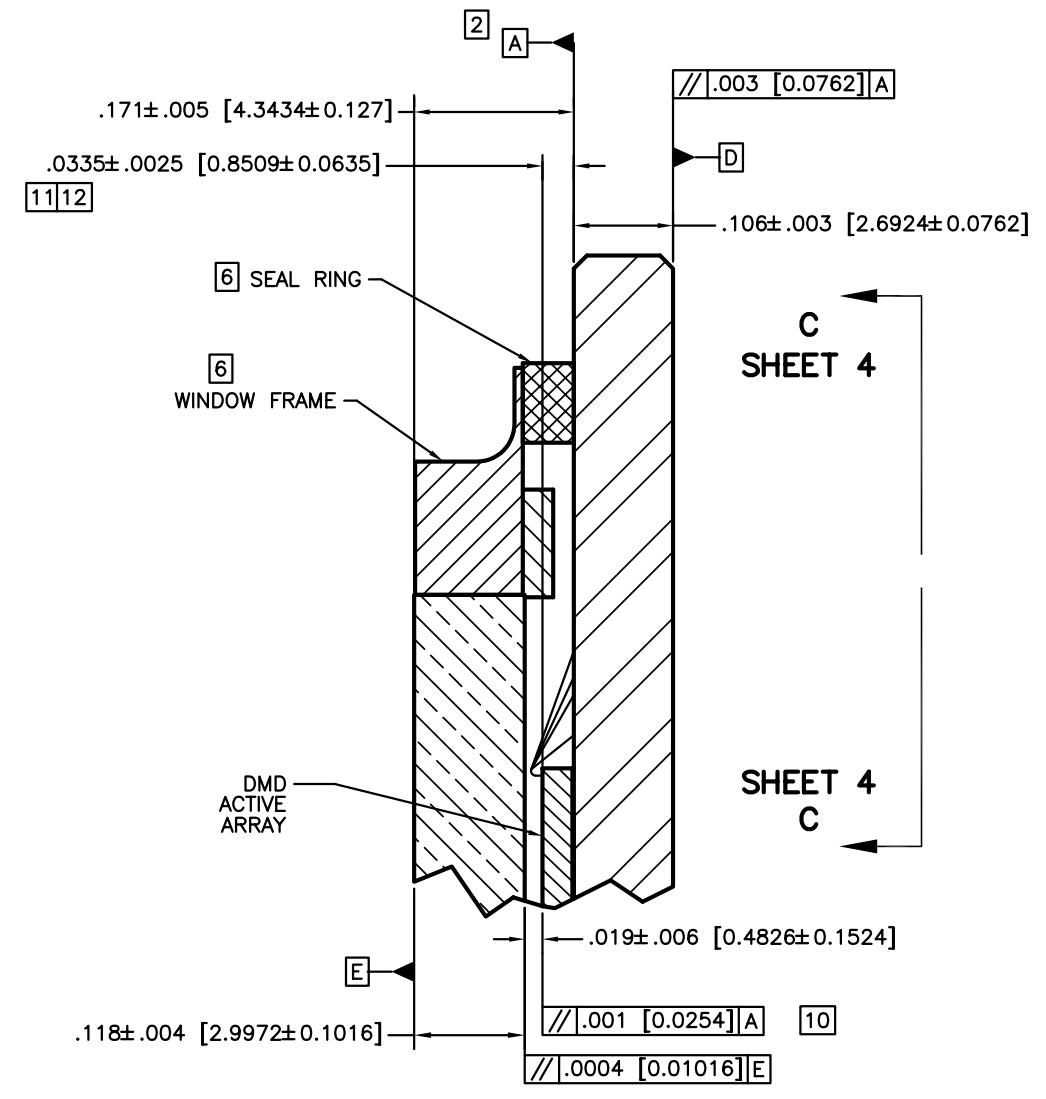
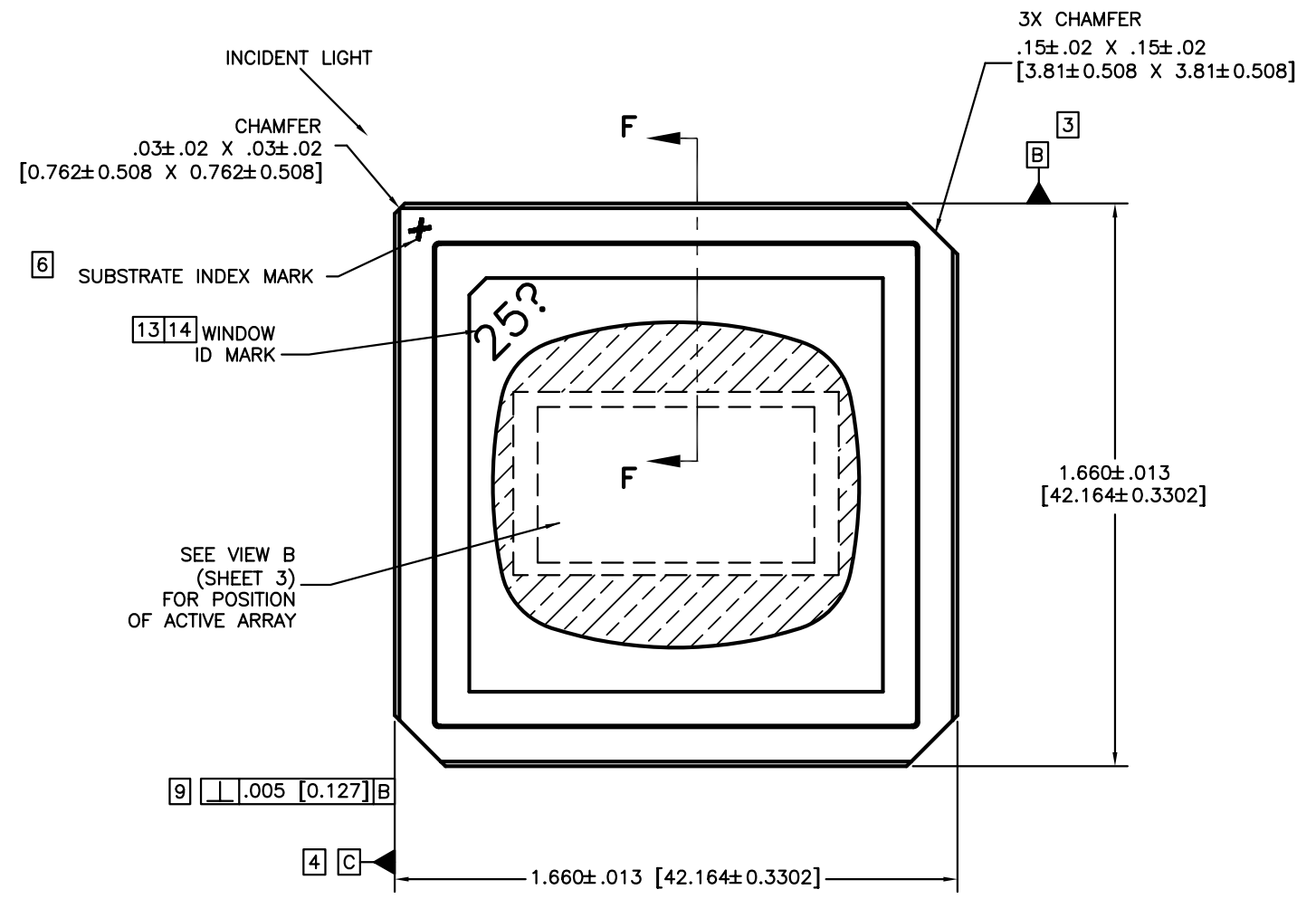
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

NOTES: UNLESS OTHERWISE SPECIFIED:

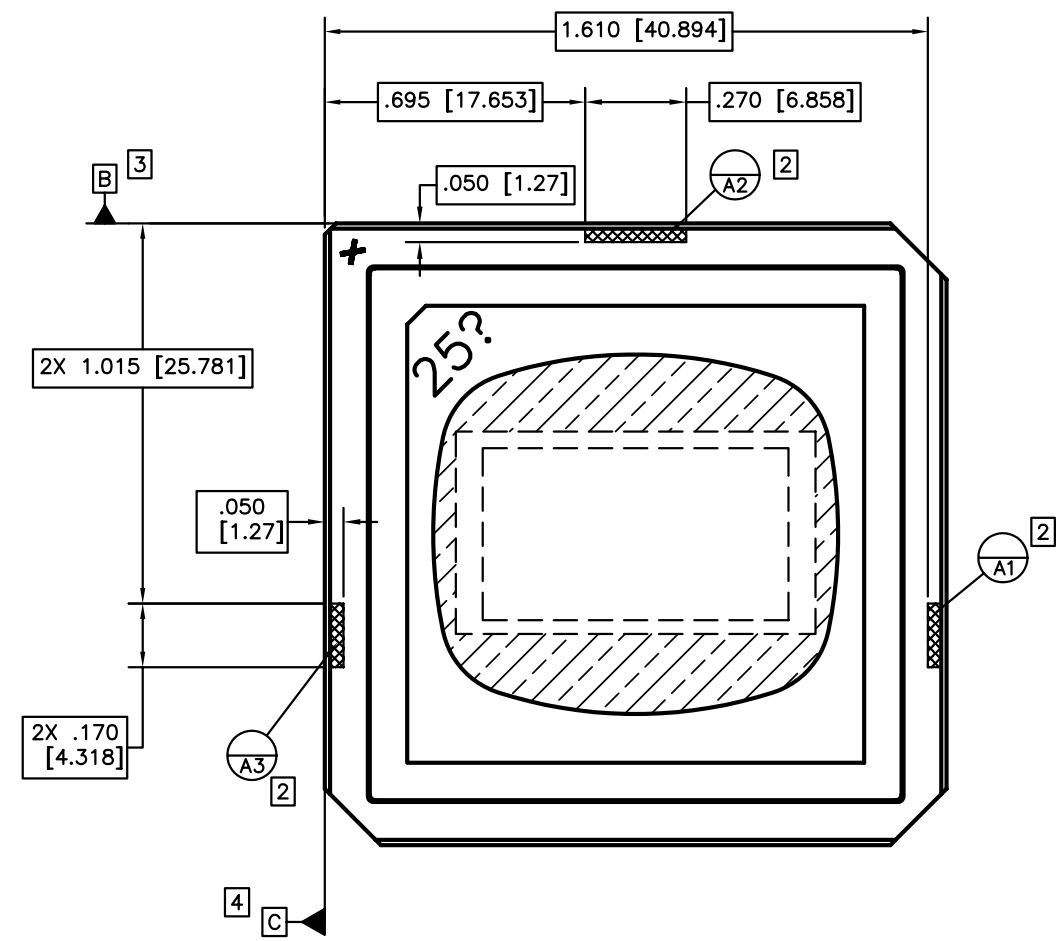
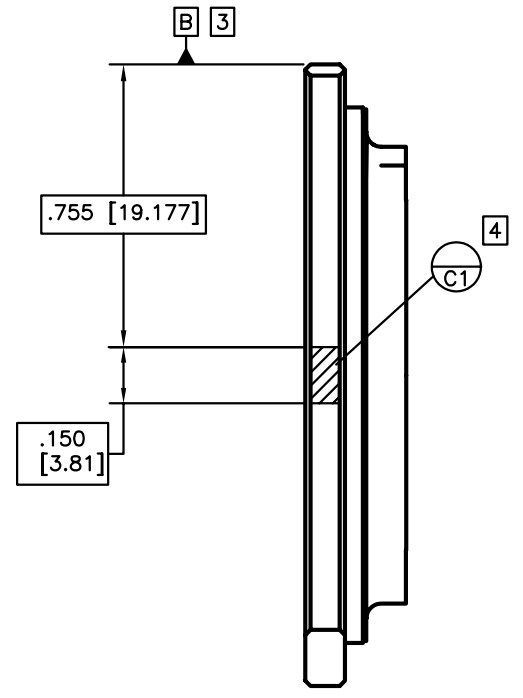
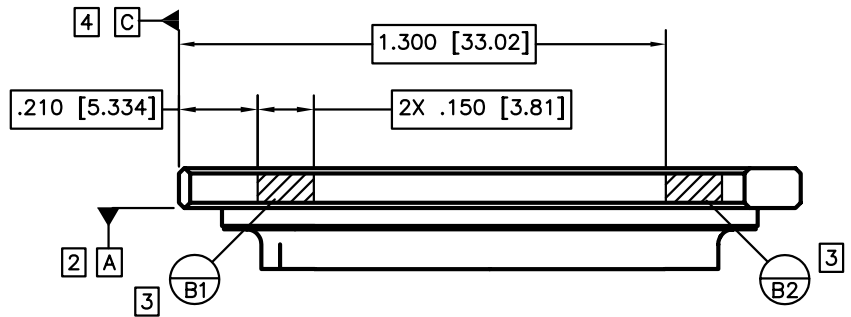
- 1 INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994.
- 2 DATUM A (SYSTEM INTERFACE PLANE) ESTABLISHED BY THREE DATUM AREAS SHOWN IN VIEW A (SHEET 2).
- 3 DATUM B ESTABLISHED BY TWO DATUM AREAS SHOWN IN VIEW A (SHEET 2).
- 4 DATUM C ESTABLISHED BY DATUM AREA SHOWN IN VIEW A (SHEET 2).
- 5 LOCALIZED BACKSIDE SURFACE FLATNESS APPLIES TO ENTIRE SURFACE.
- 6 SUBSTRATE INDEX MARK, BACK INDEX PAD, SYMBOLIZATION PAD, SEAL RING, AND WINDOW FRAME TO BE ELECTRICALLY CONNECTED TO VSS PLANE IN SUBSTRATE.
- 7 THE DIMENSIONS OF THE SYMBOLIZATION PAD REPRESENT THE APPROXIMATE SIZE AND LOCATION OF THE RECOMMENDED THERMAL INTERFACE AREA.
- 8 ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND IS THE MAXIMUM VALUE ALLOWED.
- 9 SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE.
- 10 DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
- 11 DIE HEIGHT TOLERANCE APPLIES TO CENTER OF DMD ACTIVE ARRAY ONLY.
- 12 DMD ACTIVE ARRAY ROTATION AND LOCATION DIMENSIONS ARE RELATED TO DATUM A (PRIMARY), DATUM B (SECONDARY), AND DATUM C (TERTIARY).
- 13 WINDOW SHALL BE ORIENTED SUCH THAT I.D. MARK ALIGNS WITH SUBSTRATE INDEX MARK AS SHOWN.
- 14 ? IS A WILD CARD CHARACTER AND CAN BE ANY LETTER.

D
C
B
A

D
C
B
A



-1	ITEM	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
QTY	NO			
PARTS LIST				
			DWN M. AVERY	DATE 2/28/05
			ENGR M. AVERY	2/28/05
			QA	
			APVD	
			SIZE D	DRAWING NO 2506491
			SCALE 4/1	REV A
				SHEET 1 OF 4



VIEW A (SHEET 1 NOTES)
DATUM A, B AND C DETAILS

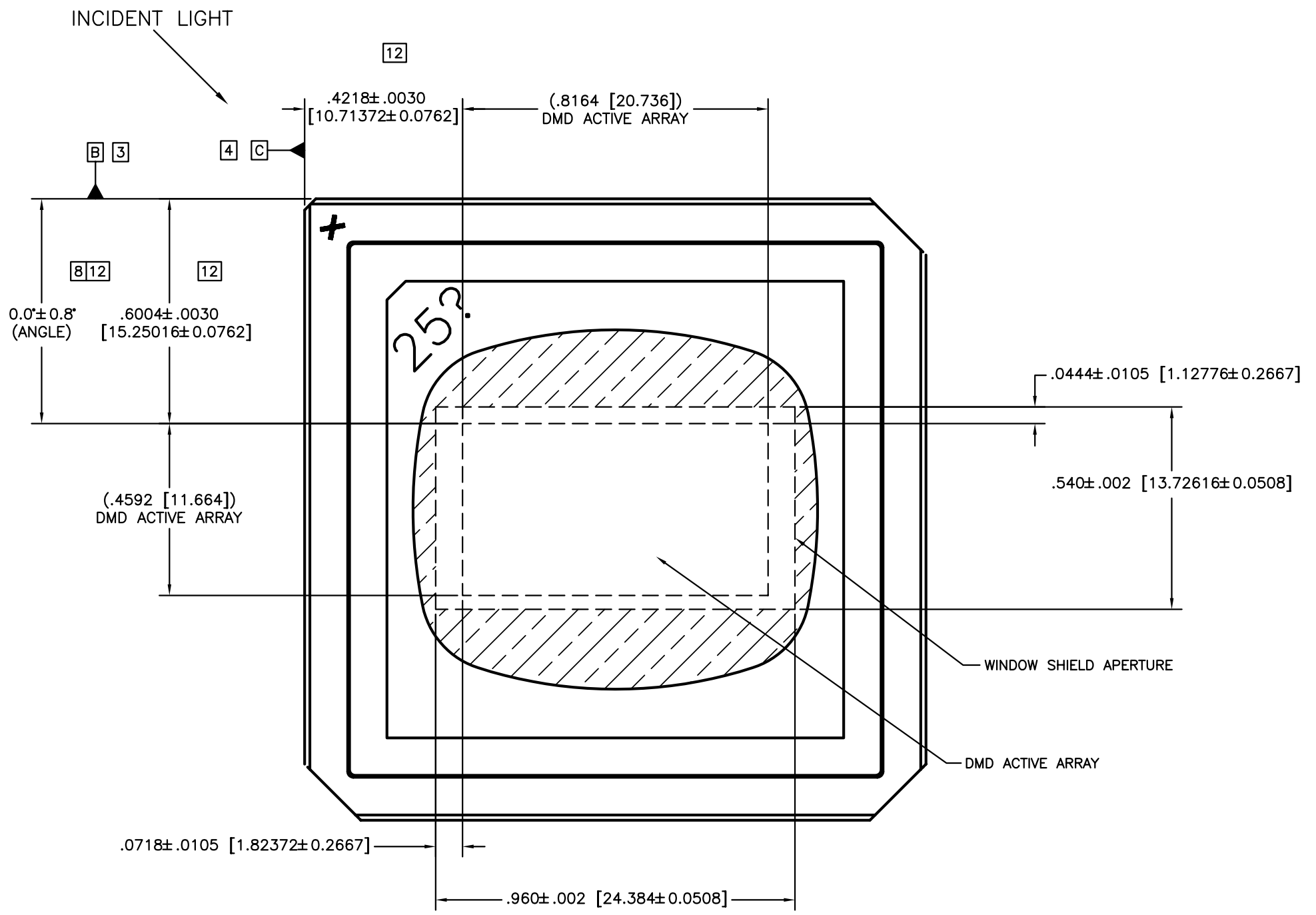
8 7 6 5 4 3 1

D D

C C

B B

A A



VIEW B (SHEET 1)
POSITION OF ACTIVE ARRAY
SCALE 6/1

8 7 6 5 4 3 2 1

D

C

B

A

D

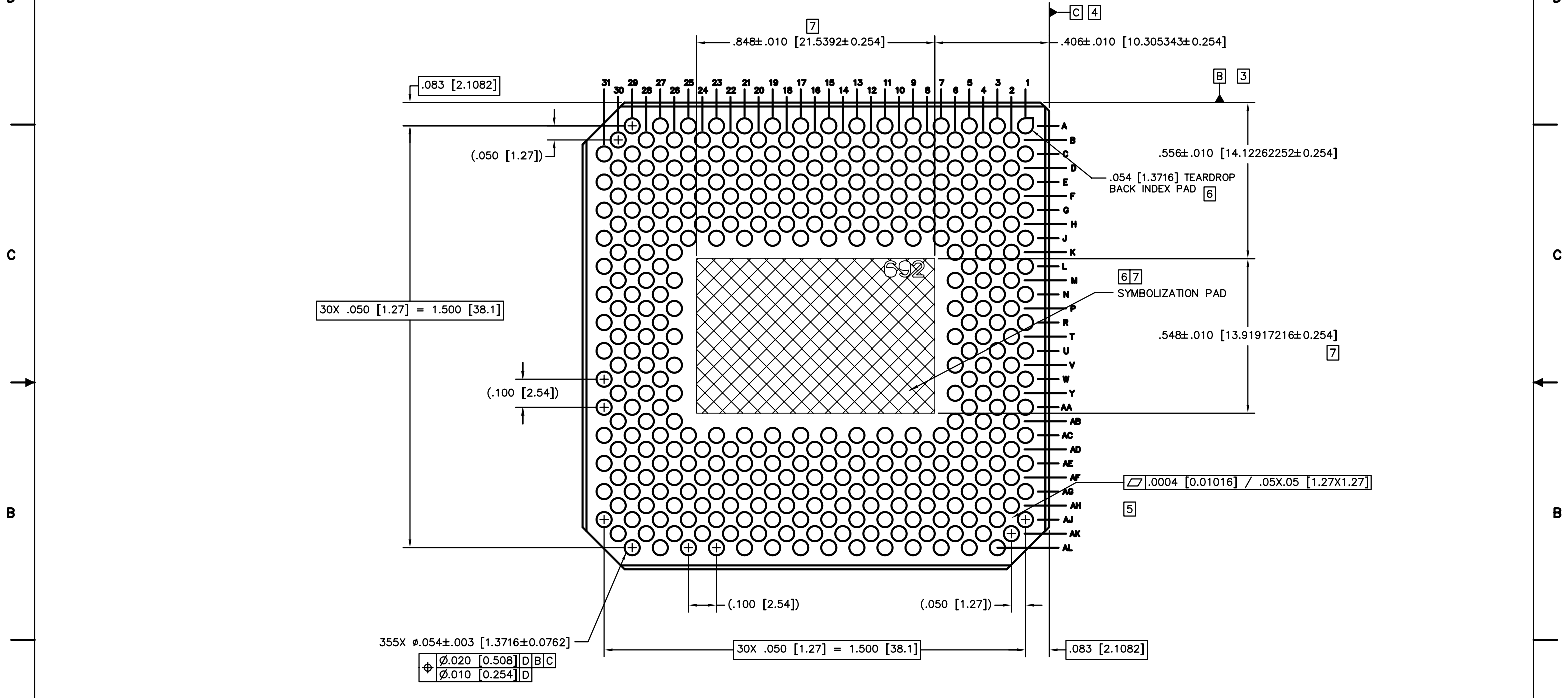
C

B

A

8 7 6 5 4 3 1

8 7 6 5 4 3 2 1



30X .050 [1.27] = 1.500 [38.1]

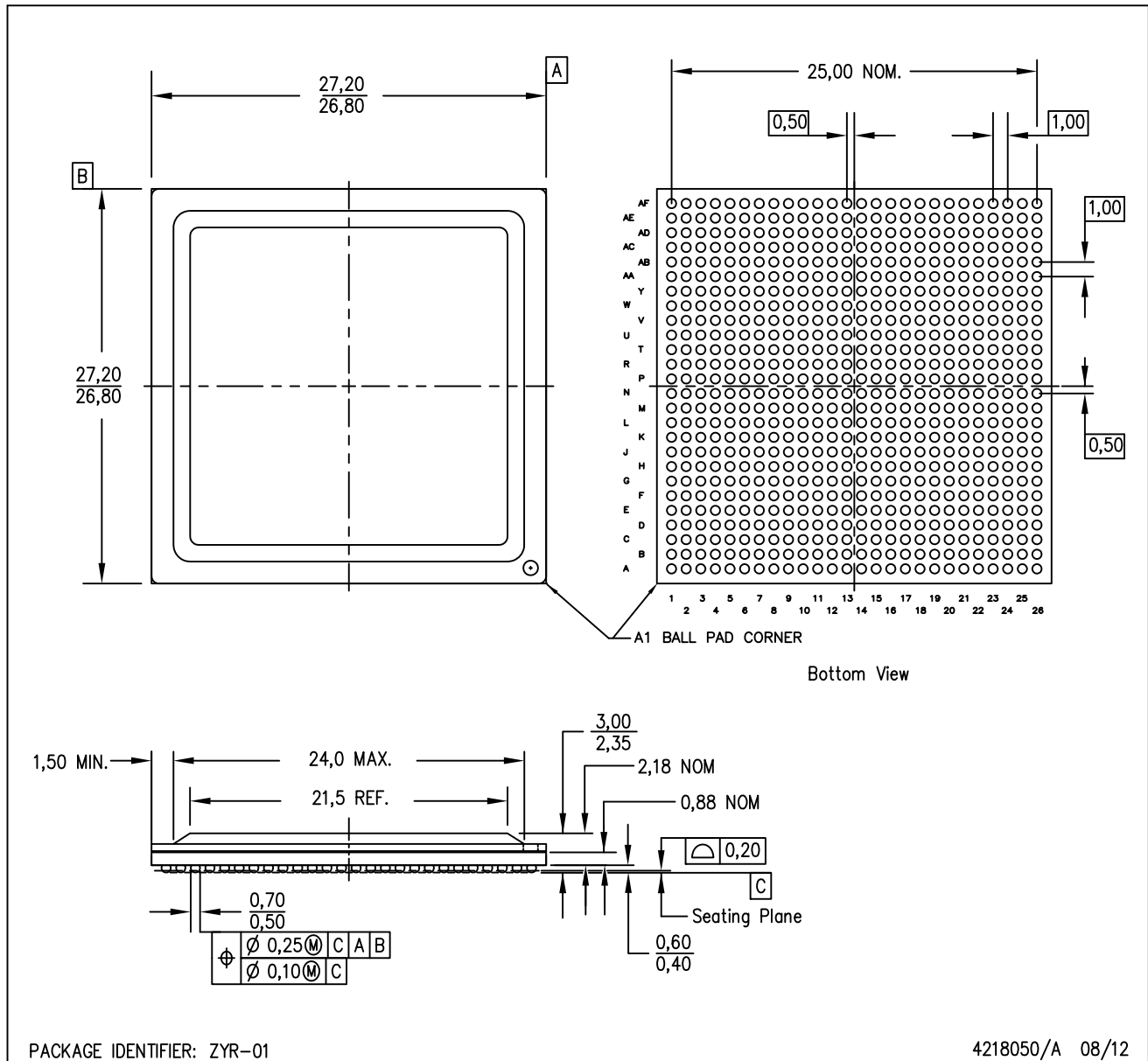
355X $\phi .054 \pm .003$ [1.3716 \pm 0.0762]

ϕ	$\phi .020$	[0.508]	D	B	C
	$\phi .010$	[0.254]	D		

VIEW C-C (SHEET 1)
BACK PADS
SCALE 6/1

ZYR (S-PBGA-N676)

PLASTIC BALL GRID ARRAY

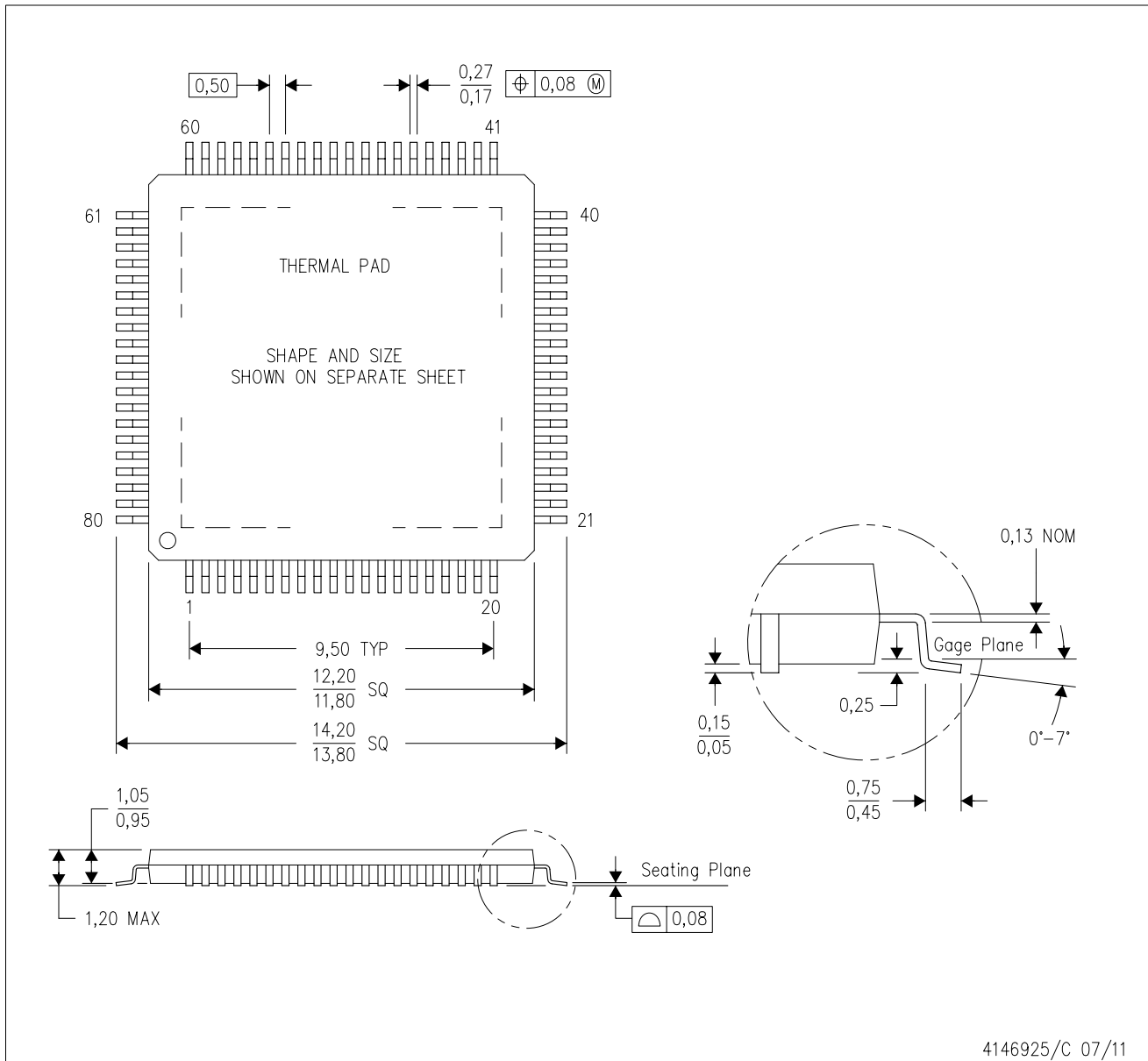


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Flip chip application only.
 - D. Pb-free solder ball.

MECHANICAL DATA

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



4146925/C 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

PFP (S-PQFP-G80)

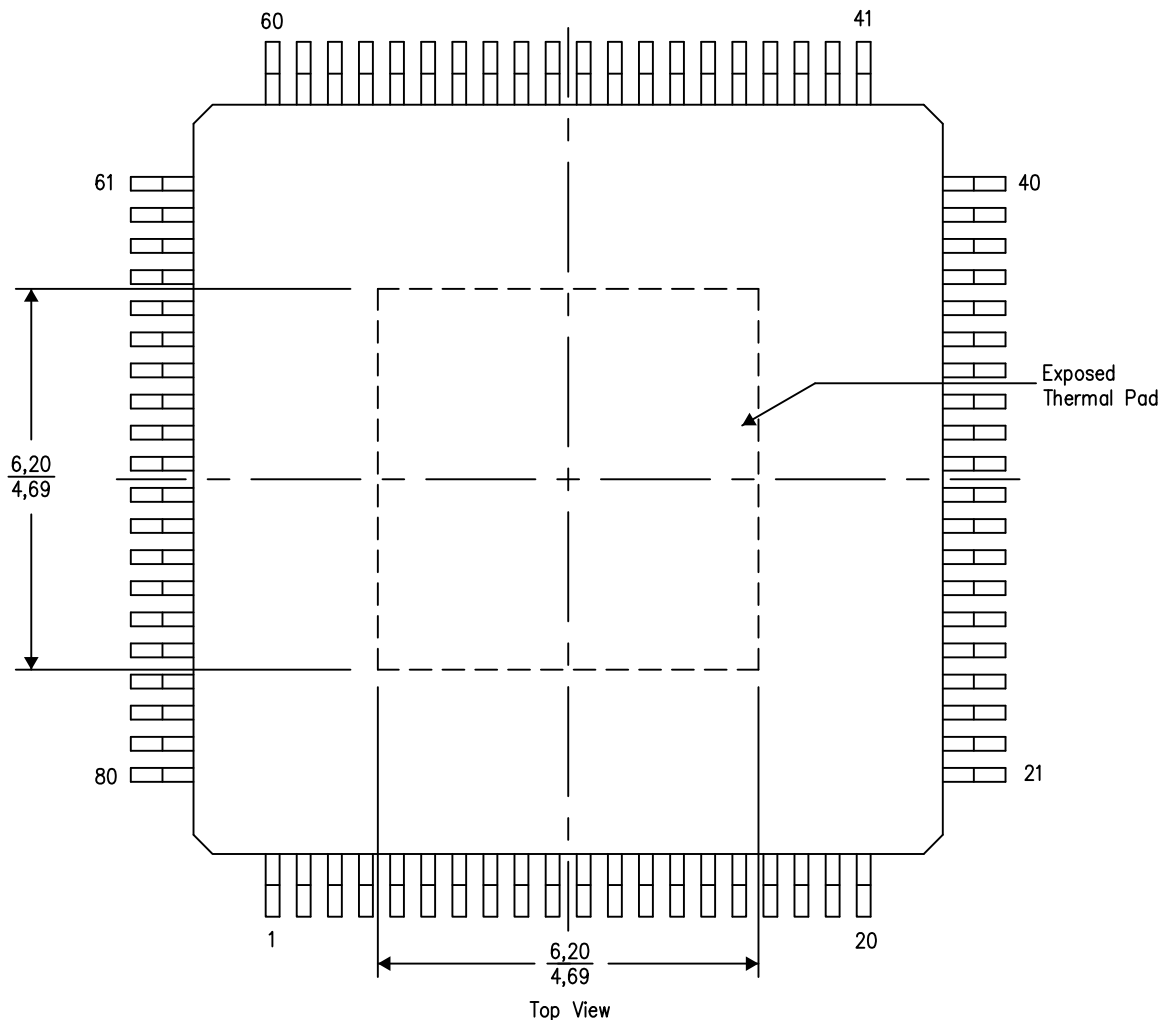
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



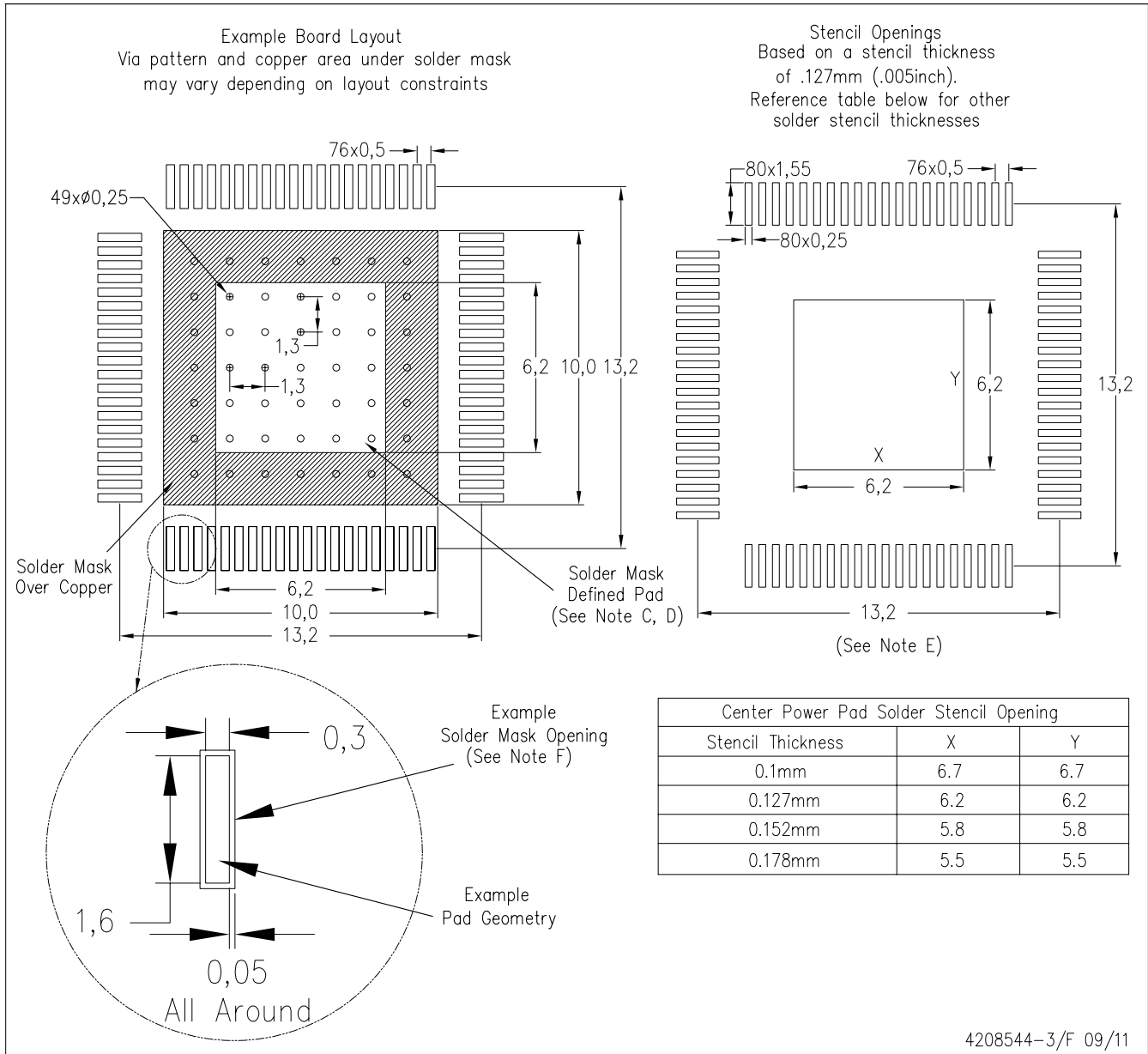
4206327-3/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK

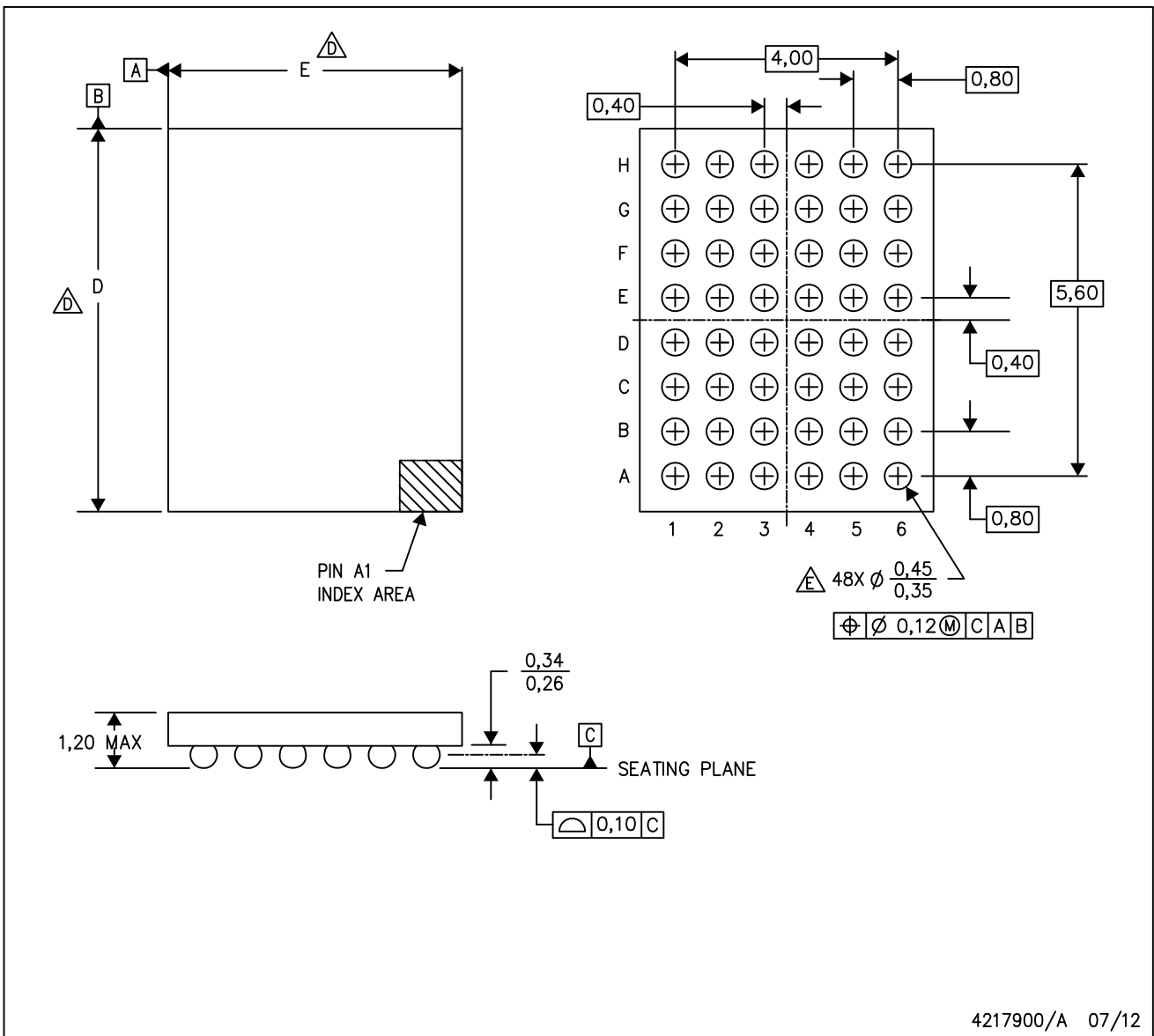


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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YVA (R-XBGA-N48)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - \triangle The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
6 x 8 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls.

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