1 pC Charge Injection, 100 pA Leakage, +5 V / +3 V, Dual SPST Analog Switches

DESCRIPTION

The DG9232E, DG9233E, and DG9234E are monolithic CMOS switches designed for precision signal switching. The 17 Ω low voltage parts feature low charge injection, leakage, parasitic capacitance, and fast switching.

The DG9232E, DG9233E, and DG9234E can switch both analog and digital signals. Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

The DG9232E, DG9233E, and DG9234E contain two independent single pole single throw (SPST) switches. Switch-1 and switch-2 are normally closed for the DG9232E and normally open for the DG9233E. For the DG9234E, switch-1 is normally open and switch-2 is normally closed with a break-before-make switching timing.

The DG9232E, DG9233E, and DG9234E offer 1 nW typical power consumption and 8 kV ESD/HBM, 1 kV ESD/CDM tolerance. They are the ideal switches for use in low voltage instruments and healthcare devices, fitting the circuits of low voltage ADC and DAC, sample and hold, analog front end gain control, and signal path control. The DG9232E, DG9233E, and DG9234E are available in 8-lead MSOP and SOIC packages.

BENEFITS

- Low charge injection and leakage
- Low parasitic capacitance
- Fast switching speed
- High ESD tolerance

FEATURES

Pb-free Available

RoHS* Available

- 1 pC charge injection
- Guaranteed 100 pA maximum switch on leakage at 25 °C
- 3.8 pF switch off and 7.8 pF switch on capacitances
- +2.7 V to +5 V single supply operation
- Low on-resistance - $R_{DS(on)}$: 17 Ω / typ. at 5 V
- t_{ON}: 32 ns, t_{OFF}: 10 ns switching time
- Typical power consumption: 1 nW
- Over voltage tolerant TTL / CMOS compatible
- ESD (HBM): 8000 V, ESD (CDM): 1000 V
- Latch-up current: > 300 mA (JESD78)
- Available in MSOP-8 and SOIC-8
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

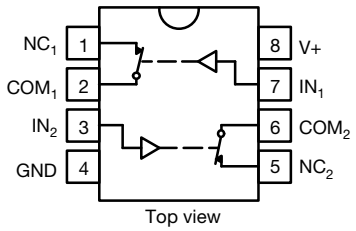
Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

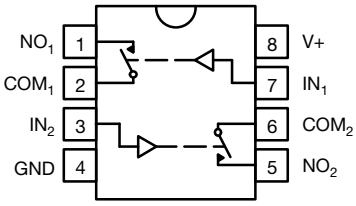
APPLICATIONS

- Automatic test equipment
- Process control and automation
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Sample-and-hold systems
- Relay replacements
- Battery powered systems

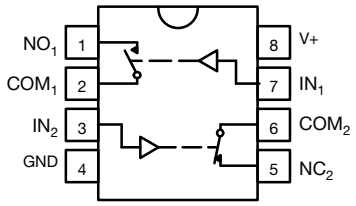
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top view



Top view



Top view

TRUTH TABLE - DG9232E

LOGIC	SWITCH
0	On
1	Off

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

TRUTH TABLE - DG9233E

LOGIC	SWITCH
0	Off
1	On

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

TRUTH TABLE - DG9234E

LOGIC	SWITCH-1	SWITCH-2
0	Off	On
1	On	Off

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION

TEMPERATURE RANGE	CONFIGURATION	PACKAGE	PART NUMBER	MINIMUM ORDER / PACKAGE QUANTITY
-40 °C to +85 °C lead (Pb)-free	DG9232E	8-pin MSOP	DG9232EDQ-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9232EDY-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9232EDY-GE3	Tube 500 units
	DG9233E	8-pin MSOP	DG9233EDQ-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9233EDY-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9233EDY-GE3	Tube 500 units
	DG9234E	8-pin MSOP	DG9234EDQ-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9234EDY-T1-GE3	Tape and reel 2500 units
		8-pin SOIC	DG9234EDY-GE3	Tube 500 units

ABSOLUTE MAXIMUM RATINGS

PARAMETER		LIMIT	UNIT
Reference V+ to GND		-0.3 to +6	V
IN, COM, NC, NO [a]		-0.3 to (V+ + 0.3)	
Continuous current (any terminal)		± 20	mA
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 40	
ESD (HBM) (MIL-STD-883, method 3015)		> 8000	V
ESD (CDM) (ANSI / ESDA / JEDEC® JS-002)		> 1000	V
Latch up current, per JESD78		300	mA
Storage temperature	D suffix	-65 to +125	°C
Power dissipation (packages) [b]	8-pin narrow body SOIC [c]	400	mW

Notes

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.5 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS OTHERWISE UNLESS SPECIFIED** V+ = 3 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V [e]	**TEMP.** [a]	**D SUFFIX** -40 °C to +85 °C			**UNIT**
				MIN. [c]	**TYP.** [b]	**MAX.** [c]	
Analog Switch							
Analog signal range [d]	V_{ANALOG}		Full	0	-	3	V
Drain-source on-resistance	$R_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V, V+ = 2.7 V, I_{COM} = 5 mA	Room	-	35	50	Ω
			Full	-	35	65	
$R_{DS(on)}$ match [d]	$\Delta R_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V	Room	-	0.4	2	
$R_{DS(on)}$ flatness [d]	$R_{DS(on)}$ flatness	V_{NO} or V_{NC} = 1 V and 2 V	Room	-	4	8	
NO or NC off leakage current [g]	$I_{NO/NC(off)}$	V_{NO} or V_{NC} = 1 V/2 V, V_{COM} = 2 V/1 V	Room	-100	5	100	pA
			Full	-5000	5	5000	
COM off leakage current [g]	$I_{COM(off)}$	V_{COM} = 1 V/2 V, V_{NO} or V_{NC} = 2 V/1 V	Room	-100	5	100	
			Full	-5000	5	5000	
Channel-on leakage current [g]	$I_{COM(on)}$	V_{COM} = V_{NO} or V_{NC} = 1 V/2 V	Room	-200	5	200	
			Full	-10 000	5	10 000	
Digital Control							
Input current	I_{INL} or I_{INH}		Full	-	0.001	-	µA
Dynamic Characteristics							
Turn-on time	t_{ON}	V_{NO} or V_{NC} = 1.5 V	Room	-	43	120	ns
			Full	-	-	200	
Turn-off time	t_{OFF}		Room	-	16	50	
			Full	-	-	120	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	-	-0.28	-	pC
Off-isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-80	-	dB
Crosstalk	X_{TALK}		Room	-	-108	-	
NC and NO capacitance	$C_{S(off)}$	f = 1 MHz	Room	-	4	-	pF
Channel-on capacitance	$C_{COM(on)}$		Room	-	8	-	
COM-off capacitance	$C_{COM(off)}$		Room	-	4	-	
Power Supply							
Positive supply range	V+			2.7	-	5.5	V
Power supply current	I+	V+ = 3.3 V, V_{IN} = 0 V or 3.3 V		0.0003	-	1	µA

Notes

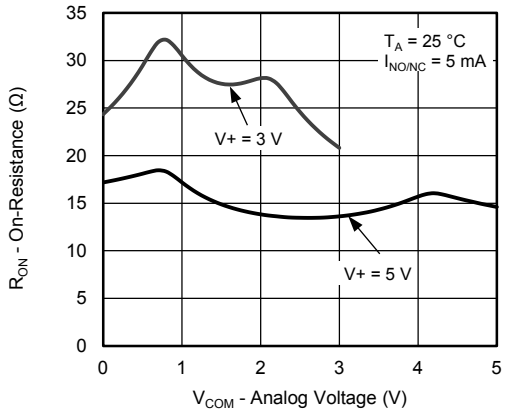
a. Room = 25 °C, full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min. and max. values.
g. Guaranteed by 5 V leakage tests, not production tested.

SPECIFICATIONS (V+ = 5 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS OTHERWISE UNLESS SPECIFIED** V+ = 5 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V [e]	**TEMP.** [a]	**D SUFFIX** -40 °C to +85°C			**UNIT**
				MIN. [c]	**TYP.** [b]	**MAX.** [c]	
Analog Switch							
Analog signal range [d]	V_{ANALOG}		Full	0	-	5	V
Drain-source on-resistance	$R_{DS(on)}$	V_{NO} or V_{NC} = 3.5 V, V+ = 4.5 V, I_{COM} = 5 mA	Room	-	17	25	Ω
			Full	-	17	35	
$R_{DS(on)}$ match [d]	$\Delta R_{DS(on)}$	V_{NO} or V_{NC} = 3.5 V	Room	-	0.4	2	
$R_{DS(on)}$ flatness [d]	$R_{DS(on)}$ flatness	V_{NO} or V_{NC} = 1 V, 2 V, and 3 V	Room	-	3.5	6	
NO or NC off leakage current [g]	$I_{NO/NC(off)}$	V_{NO} or V_{NC} = 1 V/4 V, V_{COM} = 4 V/1 V	Room	-100	10	100	pA
			Full	-5000	10	5000	
COM off leakage current	$I_{COM(off)}$	V_{COM} = 1 V/4 V, V_{NO} or V_{NC} = 4 V/1 V	Room	-100	10	100	
			Full	-5000	10	5000	
Channel-on leakage current	$I_{COM(on)}$	V_{COM} = V_{NO} or V_{NC} = 1 V/4 V	Room	-200	-	200	
			Full	-10 000	-	10 000	
Digital Control							
Input current	I_{INL} or I_{INH}		Full	-	0.001	-	µA
Dynamic Characteristics							
Turn-on time	t_{ON}	V_{NO} or V_{NC} = 3 V	Room	-	32	75	ns
			Full	-	-	150	
Turn-off time	t_{OFF}		Room	-	10	50	
			Full	-	-	100	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	-	-0.78	-	pC
Off-isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-80	-	dB
Crosstalk	X_{TALK}		Room	-	-108	-	
NC and NO capacitance	$C_{(off)}$	f = 1 MHz	Room	-	3.8	-	pF
Channel-on capacitance	$C_{D(on)}$		Room	-	7.8	-	
COM-off capacitance	$C_{D(off)}$		Room	-	3.8	-	
Power Supply							
Positive supply range	V+			2.7	-	5.5	V
Power supply current	I+	V+ = 5.5 V, V_{IN} = 0 V or 5.5 V		-	-	1	µA

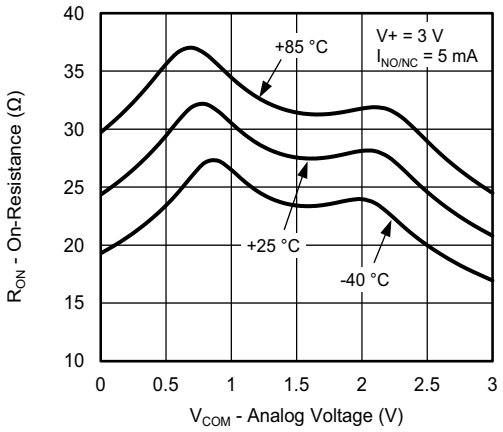
Notes

a. Room = 25 °C, full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min. and max. values.

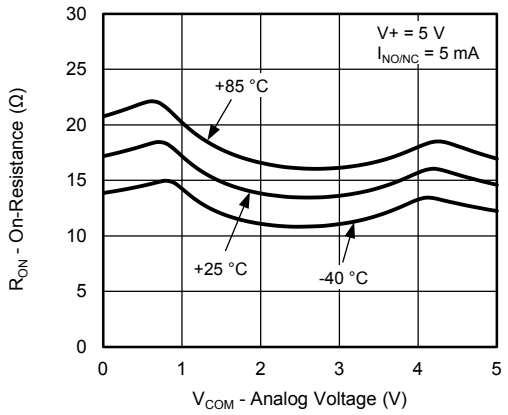
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



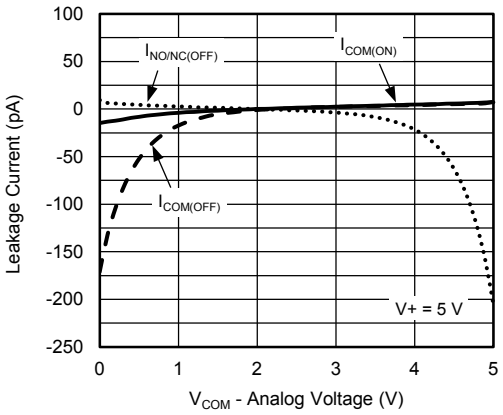
On-Resistance vs. Analog Voltage



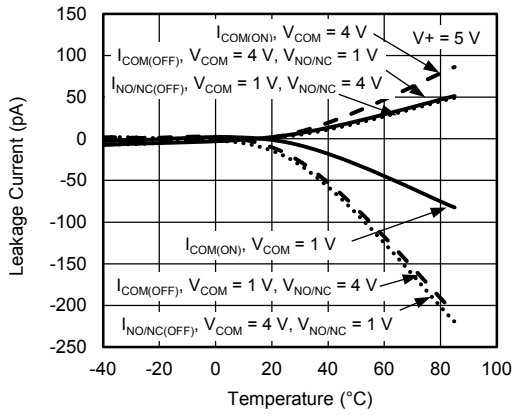
On-Resistance vs. Analog Voltage



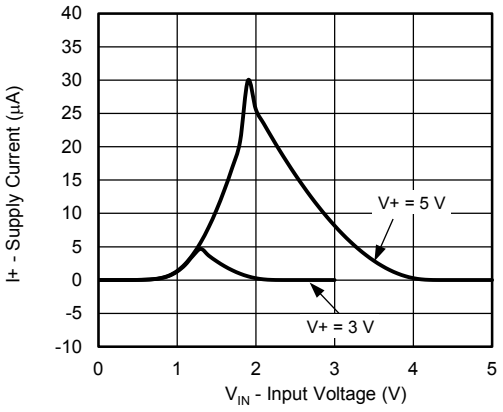
On-Resistance vs. Analog Voltage



Leakage Current vs. Analog Voltage

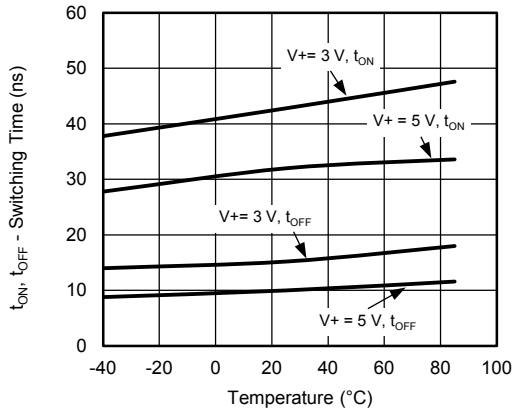


Leakage Current vs. Temperature

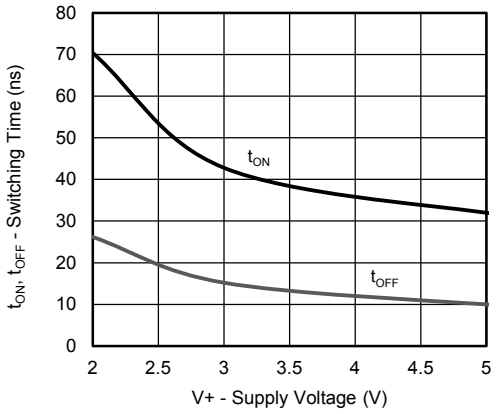


Supply Current vs. Input Voltage

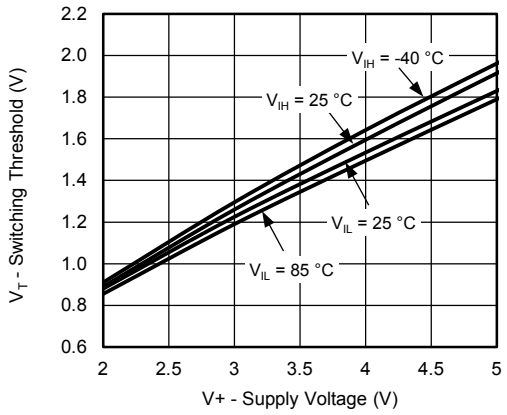
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



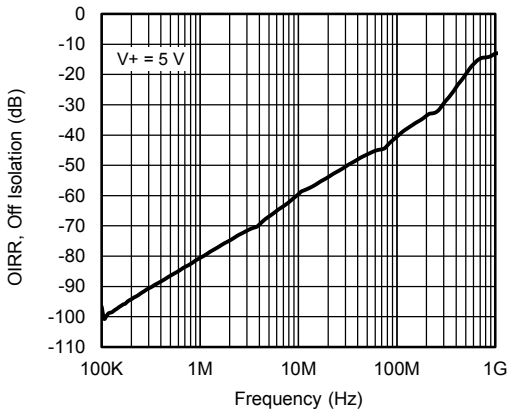
Switching Time vs. Temperature



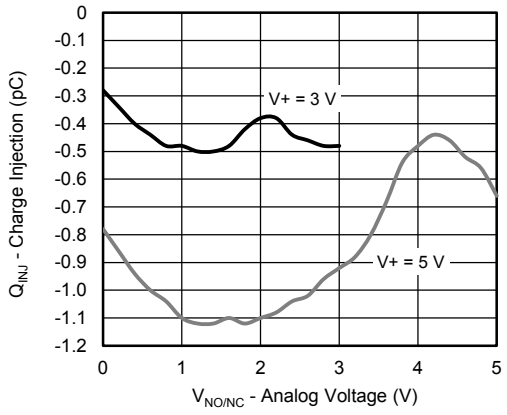
Switching Time vs. Supply Voltage



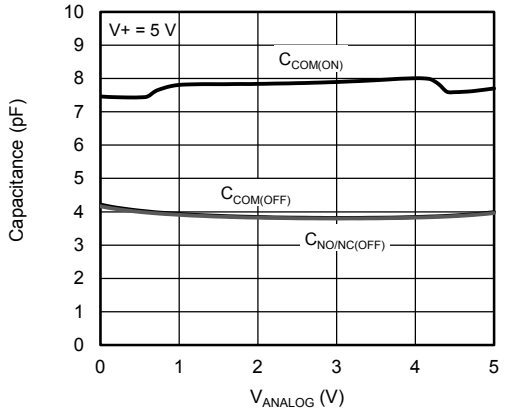
Switching Threshold vs. Supply Voltage



OIRR, Off Isolation vs. Frequency

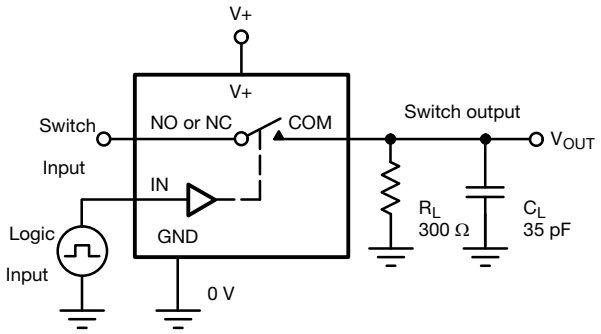


Charge Injection vs. Analog Voltage



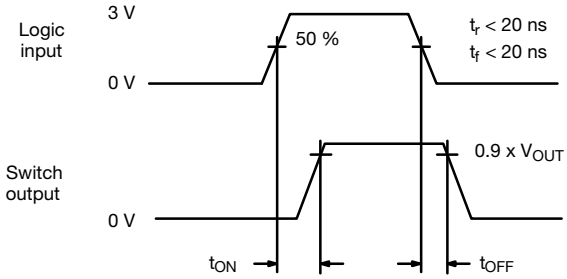
Capacitance

TEST CIRCUITS



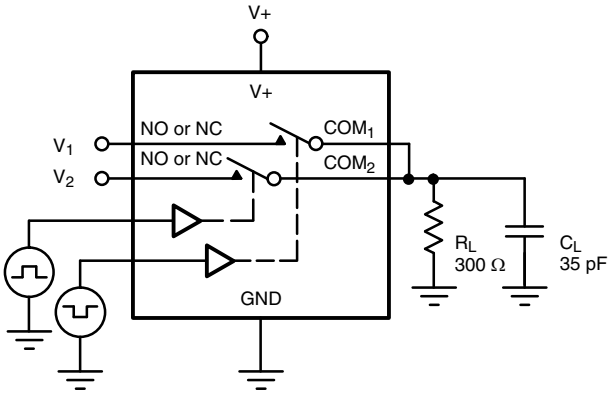
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time



C_L (includes fixture and stray capacitance)

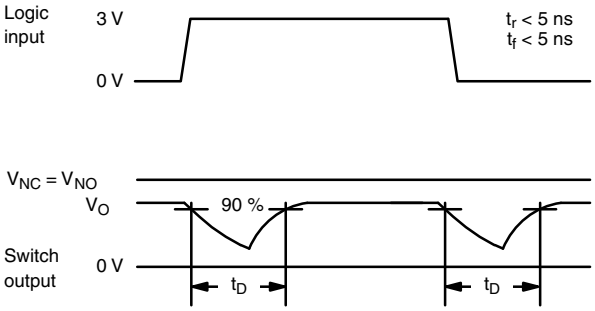
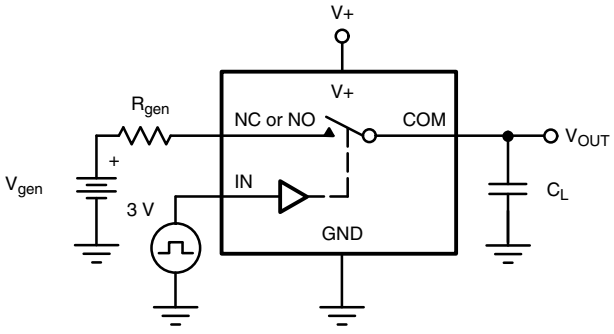
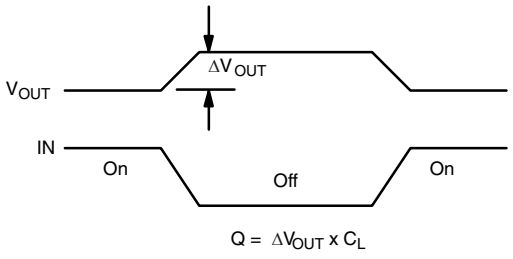


Fig. 2 - Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection

TEST CIRCUITS

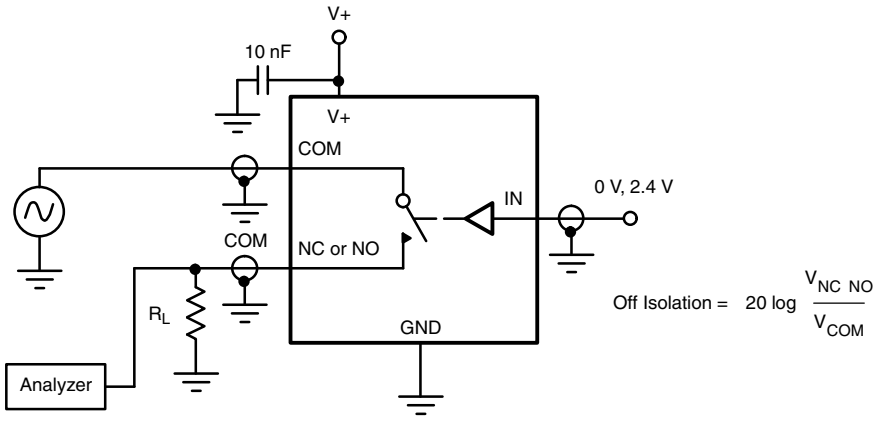


Fig. 4 - Off-Isolation

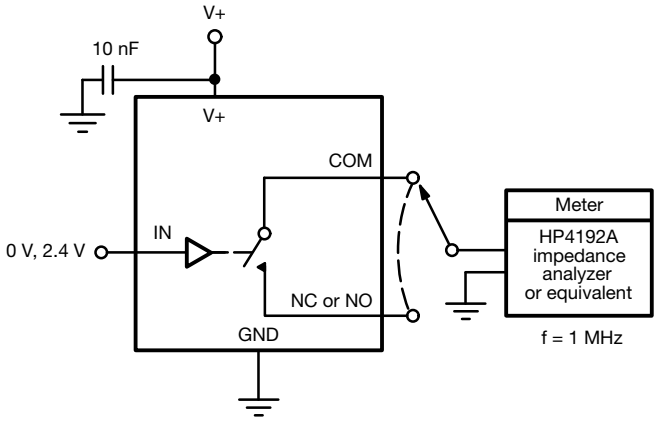
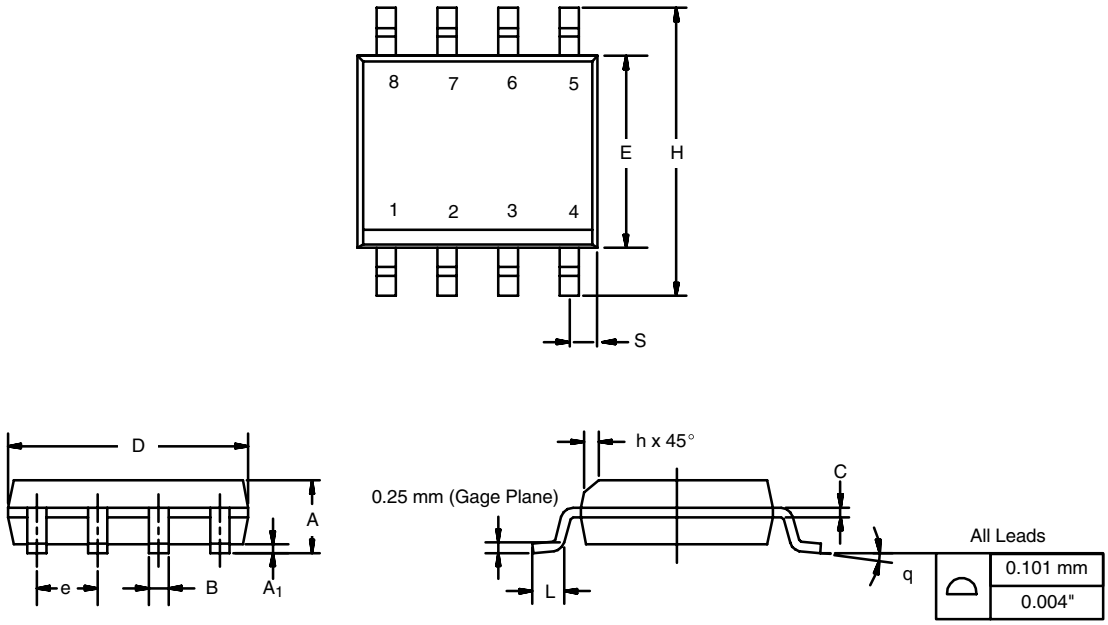


Fig. 5 - Channel Off/On Capacitance

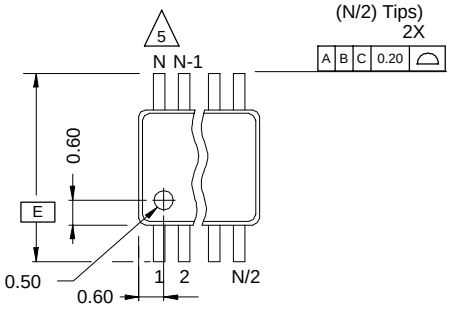
SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



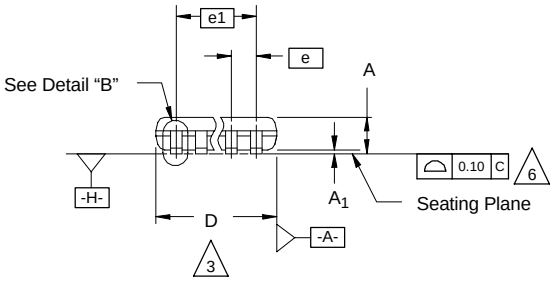
DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

MSOP: 8-LEADS

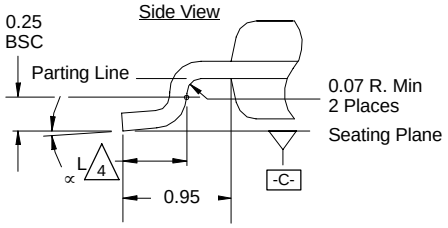
JEDEC Part Number: MO-187, (Variation AA and BA)



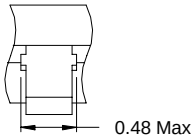
Top View



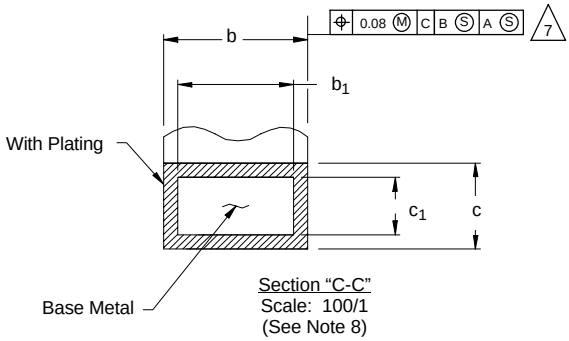
Side View



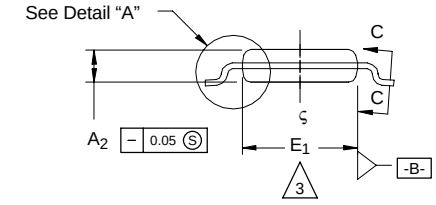
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

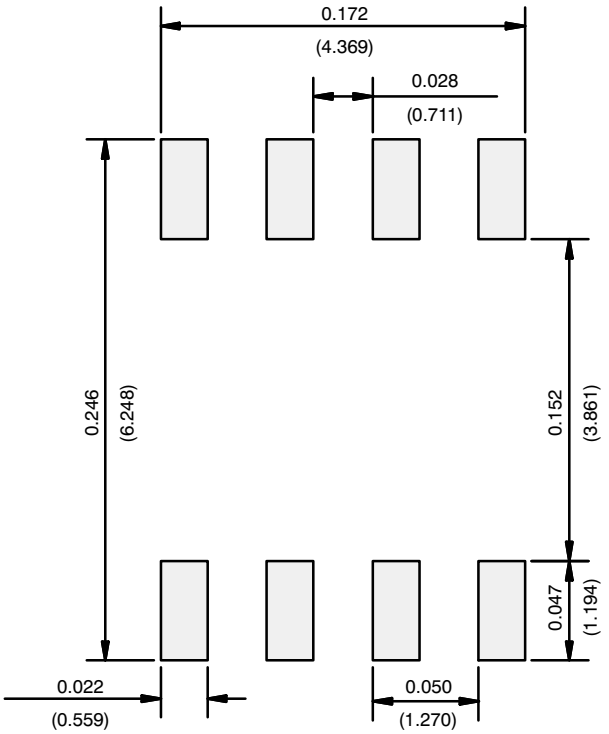
1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 8L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.25	-	0.38	8
b_1	0.25	0.30	0.33	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.65 BSC			
e_1	1.95 BSC			
L	0.40	0.55	0.70	4
N	8			5
∝	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
DWG: 5867

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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