



Precision Monolithic Quad SPST CMOS Analog Switches

DESCRIPTION

The DG411 series of monolithic quad analog switches was designed to provide high speed, low error switching of precision analog signals. Combining low power ($0.35 \mu\text{W}$) with high speed (t_{on} : 110 ns), the DG411 family is ideally suited for portable and battery powered industrial and military applications.

To achieve high-voltage ratings and superior switching performance, the DG411 series was built on Vishay Siliconix's high voltage silicon gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages up to the supply levels when off.

The DG411, DG412 respond to opposite control logic as shown in the Truth Table. The DG413 has two normally open and two normally closed switches.

BENEFITS

- Widest dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing

FEATURES

- 44 V supply max. rating
- $\pm 15 \text{ V}$ analog signal range
- On-resistance - $R_{\text{DS(on)}}$: 25Ω
- Fast switching - t_{on} : 110 ns
- Ultra low power - P_D : $0.35 \mu\text{W}$
- TTL, CMOS compatible
- Single supply capability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

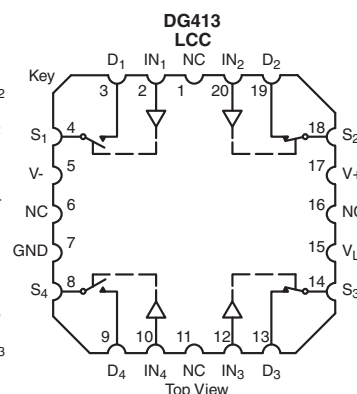
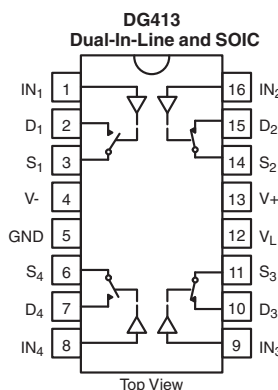
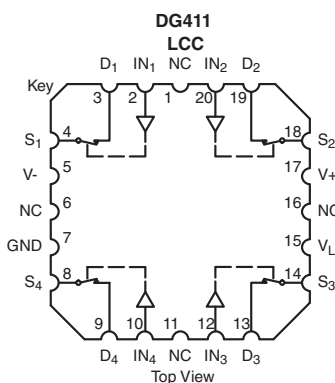
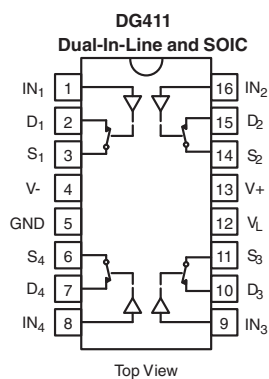


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Precision automatic test equipment
- Precision data acquisition
- Communication systems
- Battery powered systems
- Computer peripherals

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
LOGIC	DG411	DG412
0	On	Off
1	Off	On

Note

- Logic "0" $\leq 0.8 \text{ V}$
Logic "1" $\geq 2.4 \text{ V}$

TRUTH TABLE		
LOGIC	SW ₁ , SW ₄	SW ₂ , SW ₃
0	Off	On
1	On	Off

Note

- Logic "0" $\leq 0.8 \text{ V}$
Logic "1" $\geq 2.4 \text{ V}$



ORDERING INFORMATION		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	16-pin plastic DIP	DG411DJ DG411DJ-E3
		DG412DJ DG412DJ-E3
		DG413DJ DG413DJ-E3
	16-pin narrow SOIC	DG411DY DG411DY-E3 DG411DY-T1 DG411DY-T1-E3
		DG412DY DG412DY-E3 DG412DY-T1 DG412DY-T1-E3
		DG413DY DG413DY-E3 DG413DY-T1 DG413DY-T1-E3
	16-pin TSSOP	DG411DQ-E3 DG411DQ-T1-E3
		DG412DQ-E3 DG412DQ-T1-E3
		DG413DQ-E3 DG413DQ-T1-E3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ °C}$, unless otherwise noted)			
PARAMETER		LIMIT	UNIT
V_+ to V_-		44	V
GND to V_- GND to V_+		25	
V_L		(GND - 0.3) to (V_+) + 0.3	
Digital inputs ^a , V_S , V_D		(V_-) -2 to (V_+) + 2 or 30 mA, whichever occurs first	
Continuous current (any terminal)		30	mA
Peak current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage temperature	(AK, AZ suffix)	-65 to +150	°C
	(DJ, DY suffix)	-65 to +125	
Power dissipation (package) ^b	16-pin plastic DIP ^c	470	mW
	16-pin narrow SOIC ^d	600	
	16-pin CerDIP ^e	900	
	LCC-20 ^e	900	

Notes

- a. Signals on S_X , D_X , or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
- b. All leads welded or soldered to PC board
- c. Derate 6 mW/°C above 25 °C
- d. Derate 7.6 mW/°C above 75 °C
- e. Derate 12 mW/°C above 75 °C



SPECIFICATIONS ^a									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V ⁺ = 15 V, V ⁻ = -15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f	TEMP. ^b	TYP. ^c	A SUFFIX -55 °C TO +125 °C		D SUFFIX -40 °C TO +85 °C		UNIT
					MIN. ^d	MAX. ^d	MIN. ^d	MAX. ^d	
Analog Switch									
Analog signal range ^e	V _{ANALOG}		Full	-	- 15	15	- 15	15	V
Drain-source on-resistance	R _{DS(on)}	V ⁺ = 13.5 V, V ⁻ = -13.5 V, I _S = - 10 mA, V _D = ± 8.5 V	Room	25	-	35	-	35	Ω
			Full	-	-	45	-	45	
Switch off leakage current	I _{S(off)}	V ⁺ = 16.5, V ⁻ = -16.5 V, V _D = ± 15.5 V, V _S = ± 15.5 V	Room	± 0.1	-0.25	0.25	-0.25	0.25	nA
			Full	-	-20	20	-5	5	
	I _{D(off)}		Room	± 0.1	-0.25	0.25	-0.25	0.25	
			Full	-	-20	20	-5	5	
Channel on leakage current	I _{D(on)}	V ⁺ = 16.5 V, V ⁻ = -16.5 V, V _S = V _D = ± 15.5 V	Room	± 0.1	-0.4	0.4	-0.4	0.4	
			Full	-	-40	40	-10	10	
Digital Control									
Input current, V _{IN} low	I _{IL}	V _{IN} under test = 0.8 V	Full	0.005	-0.5	0.5	-0.5	0.5	μA
Input current, V _{IN} high	I _{IH}	V _{IN} under test = 2.4 V	Full	0.005	-0.5	0.5	-0.5	0.5	
Dynamic Characteristics									
Turn-on time	t _{on}	R _L = 300 Ω, C _L = 35 pF, V _S = ± 10 V, see Fig. 2	Room	110	-	175	-	175	ns
			Full	-	-	240	-	220	
Turn-off time	t _{off}		Room	100	-	145	-	145	
			Full	-	-	160	-	160	
Break-before-make time delay	t _D	DG413 only, V _S = 10 V, R _L = 300 Ω, C _L = 35 pF	Room	25	-	-	-	-	
Charge injection	Q	V _g = 0 V, R _g = 0 Ω, C _L = 10 nF	Room	5	-	-	-	-	pC
Off isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room	68	-	-	-	-	dB
Channel-to-channel crosstalk ^e	X _{TALK}		Room	85	-	-	-	-	
Source off capacitance ^e	C _{S(off)}	f = 1 MHz	Room	9	-	-	-	-	pF
Drain off capacitance ^e	C _{D(off)}		Room	9	-	-	-	-	
Channel on capacitance ^e	C _{D(on)}		Room	35	-	-	-	-	
Power Supplies									
Positive supply current	I ⁺	V ⁺ = 16.5 V, V ⁻ = -16.5 V, V _{IN} = 0 V or 5 V	Room	0.0001	-	1	-	1	μA
			Full	-	-	5	-	5	
Negative supply current	I ⁻		Room	-0.0001	-1	-	-1	-	
			Full	-	-5	-	-5	-	
Logic supply current	I _L		Room	0.0001	-	1	-	1	
			Full	-	-	5	-	5	
Ground current	I _{GND}		Room	-0.0001	-1	-	-1	-	
			Full	-	-5	-	-5	-	

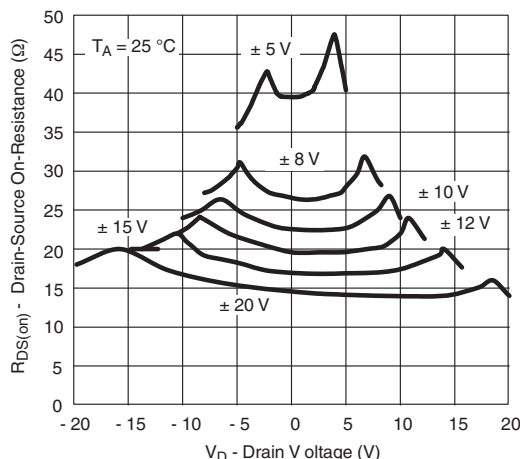
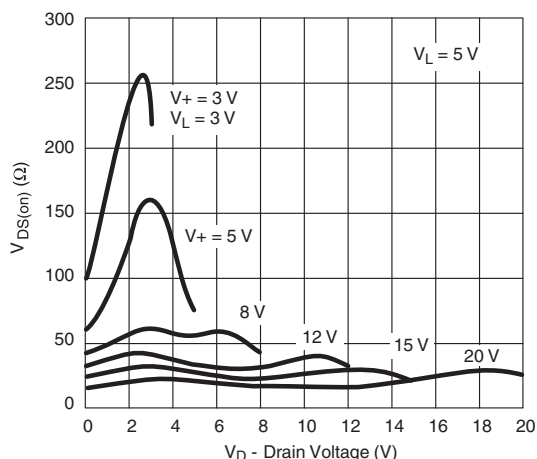
**SPECIFICATIONS ^a** (unipolar supplies)

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V + = 12 V, V - = 0 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f	TEMP. ^b	TYP. ^c	A SUFFIX -55 °C TO +125 °C		D SUFFIX -40 °C TO +85 °C		UNIT
					MIN. ^d	MAX. ^d	MIN. ^d	MAX. ^d	
Analog Switch									
Analog signal range ^e	V _{ANALOG}		Full	-	-	12	-	12	V
Drain-source on-resistance	R _{DS(on)}	V + = 10.8 V, I _S = -10 mA, V _D = 3 V, 8 V	Room	40	-	80	-	80	Ω
			Full	-	-	100	-	100	
Dynamic Characteristics									
Turn-on time	t _{on}	R _L = 300 Ω, C _L = 35 pF, V _S = 8 V, see Fig. 2	Room	175	-	250	-	250	ns
			Hot	-	-	400	-	315	
Turn-off time	t _{off}		Room	95	-	125	-	125	
			Hot	-	-	140	-	140	
Break-before-make time delay	t _D	DG413 only, V _S = 8 V, R _L = 300 Ω, C _L = 35 pF	Room	25	-	-	-	-	
Charge injection	Q	V _g = 6 V, R _g = 0 Ω, C _L = 10 nF	Room	25	-	-	-	-	pC
Power Supplies									
Positive supply current	I ₊	V + = 13.5 V, V _{IN} = 0 V or 5 V	Room	0.0001	-	1	-	1	μA
			Hot	-	-	5	-	5	
Negative supply current	I ₋		Room	-0.0001	-1	-	-1	-	
			Hot	-	-5	-	-5	-	
Logic supply current	I _L		Room	0.0001	-	1	-	1	
			Hot	-	-	5	-	5	
Ground current	I _{GND}		Room	-0.0001	-1	-	-1	-	
			Hot	-	-5	-	-5	-	

Notes

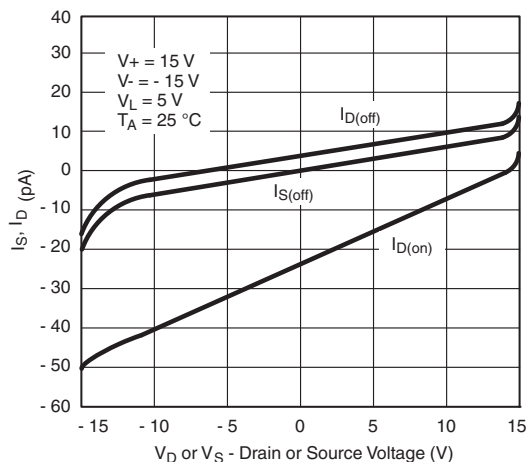
- a. Refer to process option flowchart
b. Room = 25 °C, full = as determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

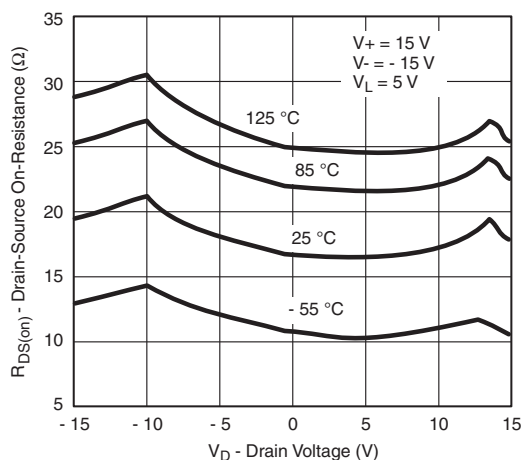
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)On-Resistance vs. V_D and Power Supply VoltageOn-Resistance vs. V_D and Unipolar Supply Voltage



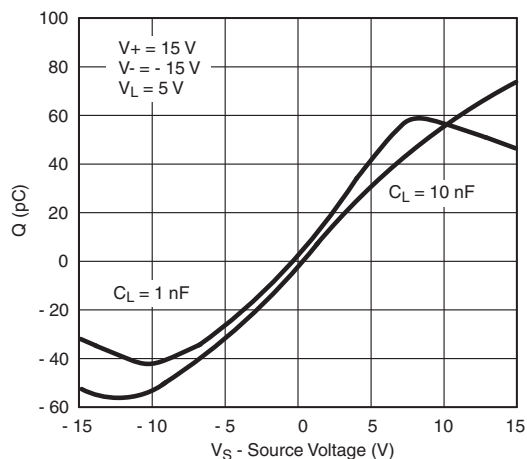
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



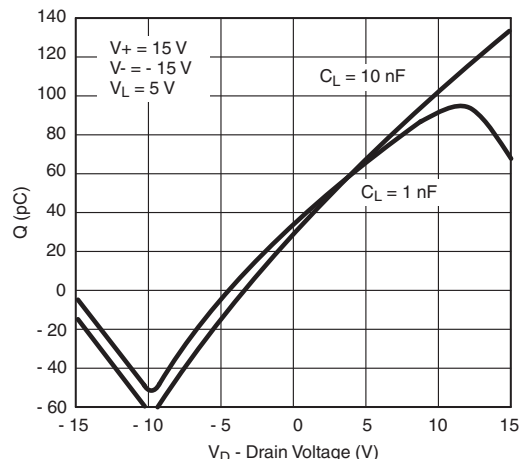
Leakage Current vs. Analog Voltage



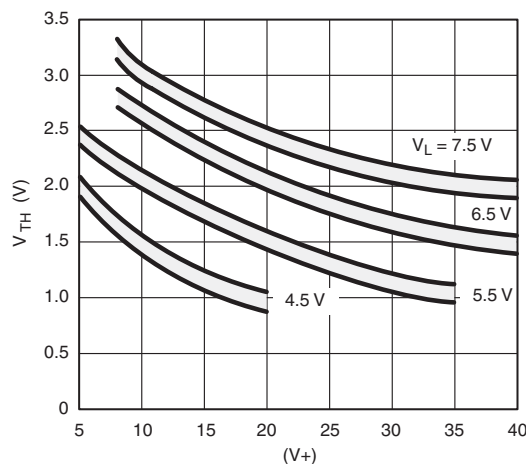
I_D, I_S Leakages vs. Temperature



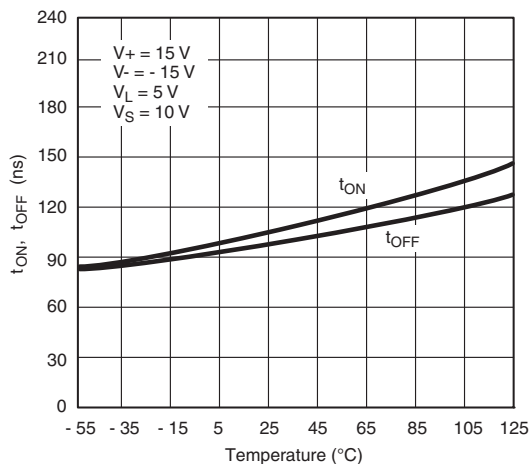
Charge Injection vs. Analog Voltage



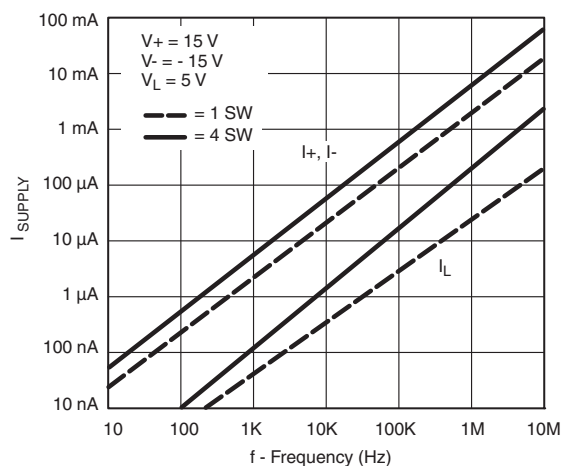
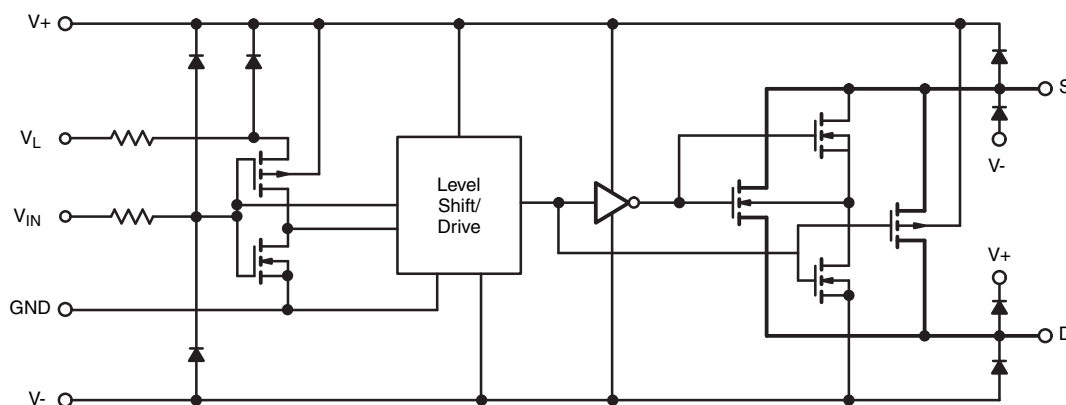
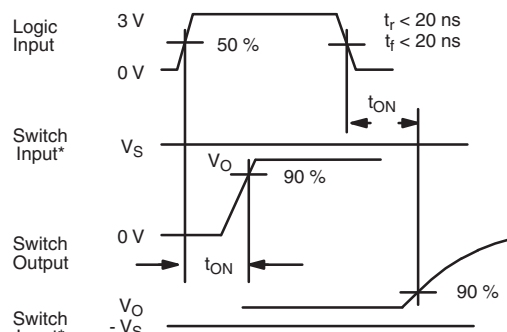
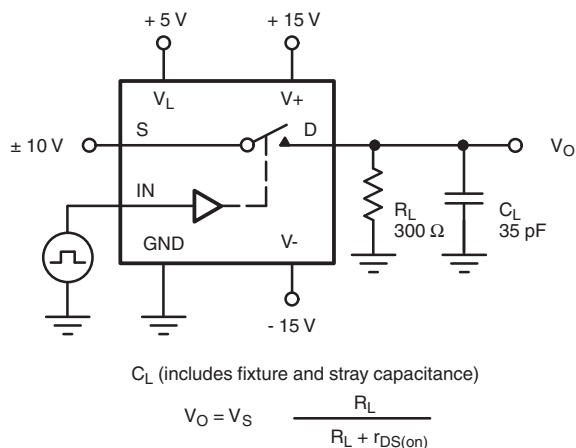
Charge Injection vs. Analog Voltage



Input Switching Threshold vs. Supply Voltage



Switching Time vs. Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Supply Current vs. Input Switching Frequency
SCHEMATIC DIAGRAM (typical channel)

Fig. 1
TEST CIRCUITS


* $V_S = 10\text{ V}$ for t_{ON} , $V_S = -10\text{ V}$ for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Fig. 2 - Switching Time

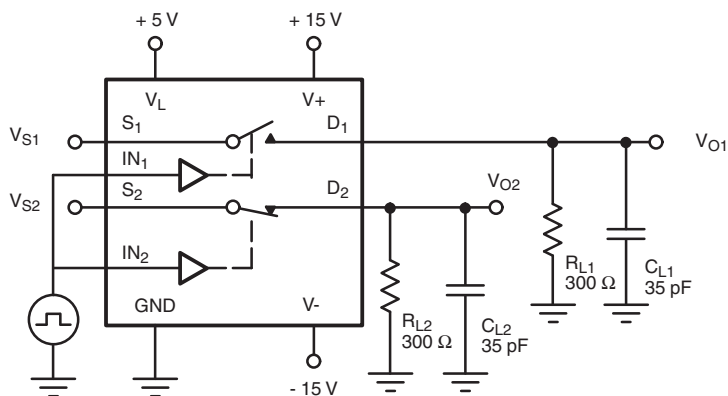
TEST CIRCUITS

 C_L (includes fixture and stray capacitance)

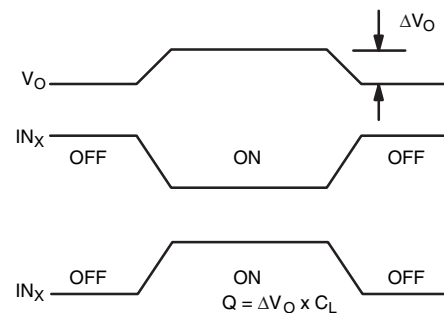
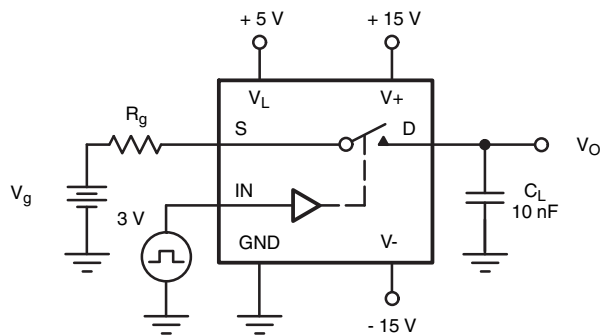
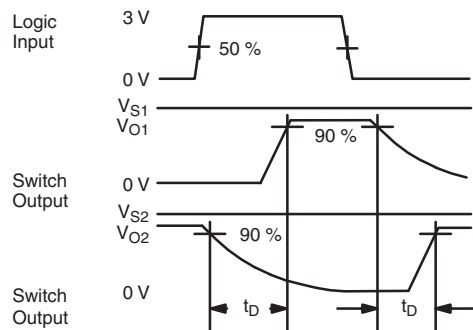
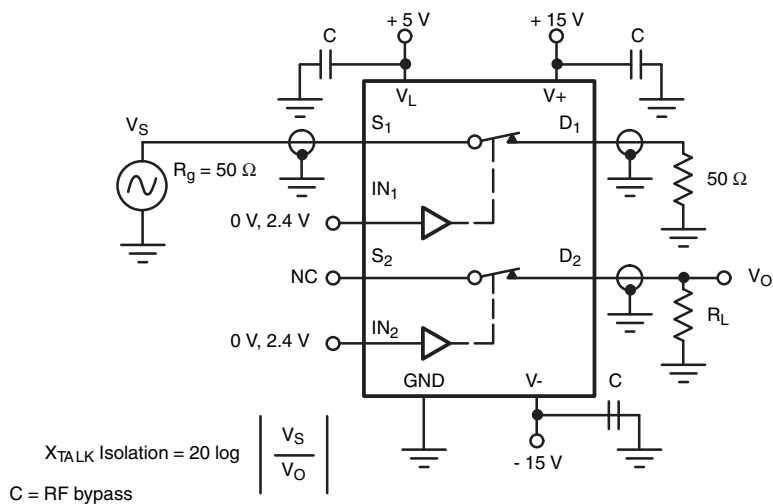
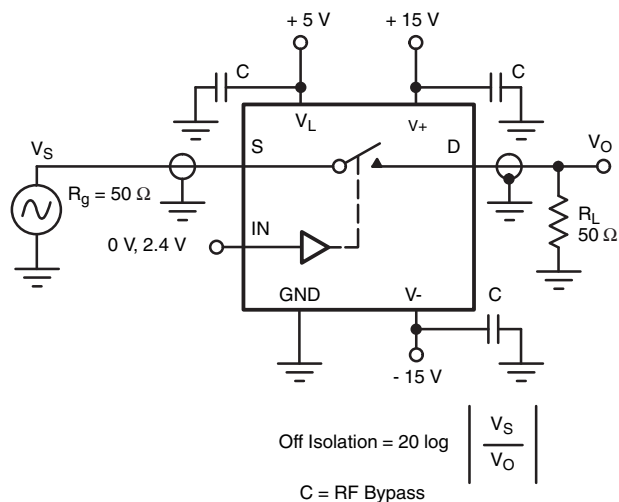
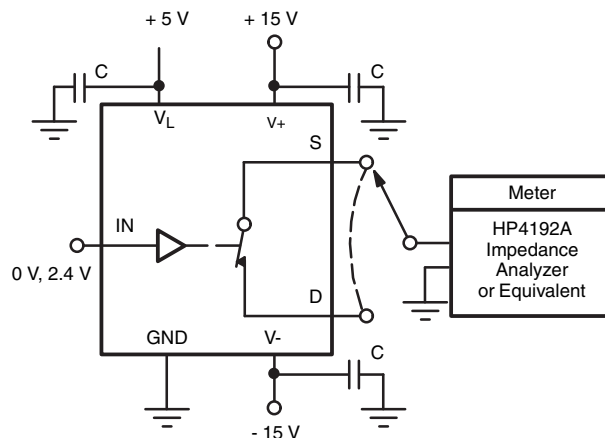
Fig. 3 - Break-Before-Make (DG413)

 IN_X dependent on switch configuration Input polarity determined by sense of switch.

Fig. 4 - Charge Injection

Fig. 5 - Crosstalk


Fig. 6 - Off Isolation

Fig. 7 - Source/Drain Capacitances

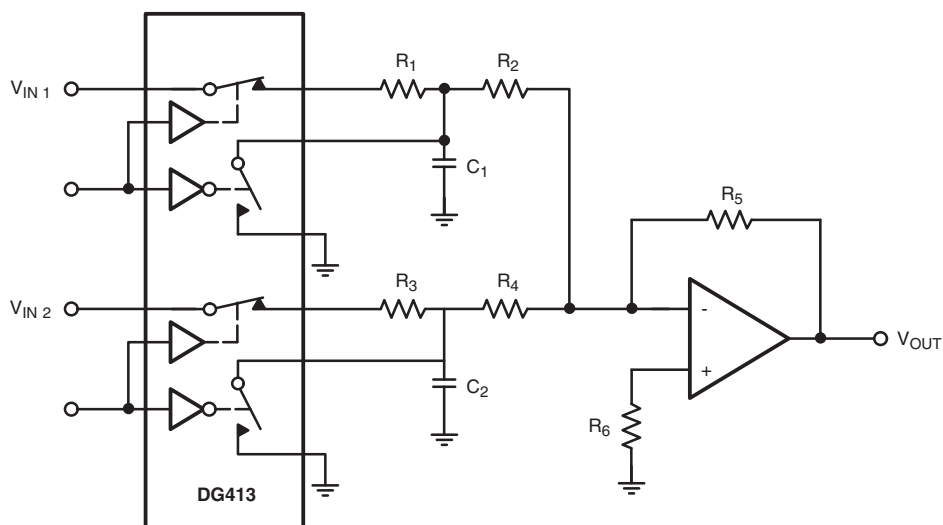
APPLICATIONS

Single Supply Operation

The DG411, DG412, DG413 can be operated with unipolar supplies from 5 V to 44 V. These devices are characterized and tested for unipolar supply operation at 12 V to facilitate the majority of applications. In single supply operation, V_+ is tied to V_L and V_- is tied to 0 V. See Input Switching Threshold vs. Supply Voltage curve for V_L versus input threshold requirements.

Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Fig. 8, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.


Fig. 8 - Summing Amplifier



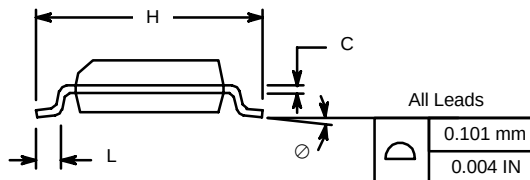
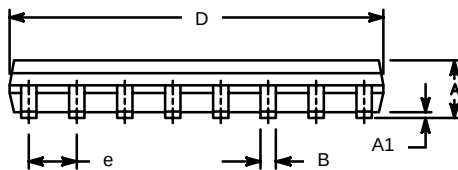
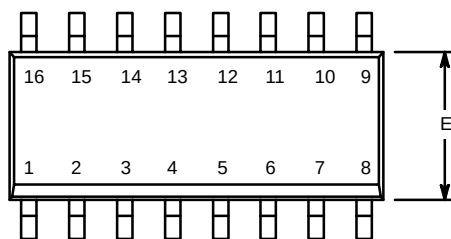
PRODUCT SUMMARY									
Part number	DG411	DG411	DG411	DG412	DG412	DG412	DG413	DG413	DG413
Status code	2	2	2	2	2	2	2	2	2
Configuration	SPST x 4, NC	SPST x 4, NC	SPST x 4, NC	SPST x 4, NO	SPST x 4, NO	SPST x 4, NO	SPST x 4, comp	SPST x 4, comp	SPST x 4, comp
Single supply min. (V)	5	5	5	5	5	5	5	5	5
Single supply max. (V)	44	44	44	44	44	44	44	44	44
Dual supply min. (V)	5	5	5	5	5	5	5	5	5
Dual supply max. (V)	22	22	22	22	22	22	22	22	22
On-resistance (Ω)	25	25	25	25	25	25	25	25	25
Charge injection (pC)	5	5	5	5	5	5	5	5	5
Source on capacitance (pF)	35	35	35	35	35	35	35	35	35
Source off capacitance (pF)	9	9	9	9	9	9	9	9	9
Leakage switch on typ. (nA)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Leakage switch off max. (nA)	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
-3 dB bandwidth (MHz)	-	-	-	-	-	-	-	-	-
Package	TSSOP-16	SO-16 (narrow) AS	Plastic DIP-16	SO-16 (narrow) AS	TSSOP-16	Plastic DIP-16	TSSOP-16	SO-16 (narrow) AS	Plastic DIP-16
Functional circuit / applications	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare
Interface	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel
Single supply operation	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Dual supply operation	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Turn on time max. (ns)	175	175	175	175	175	175	175	175	175
Crosstalk and off isolation	-85	-85	-85	-85	-85	-85	-85	-85	-85

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70050.



SOIC (NARROW): 16-LEAD

JEDEC Part Number: MS-012

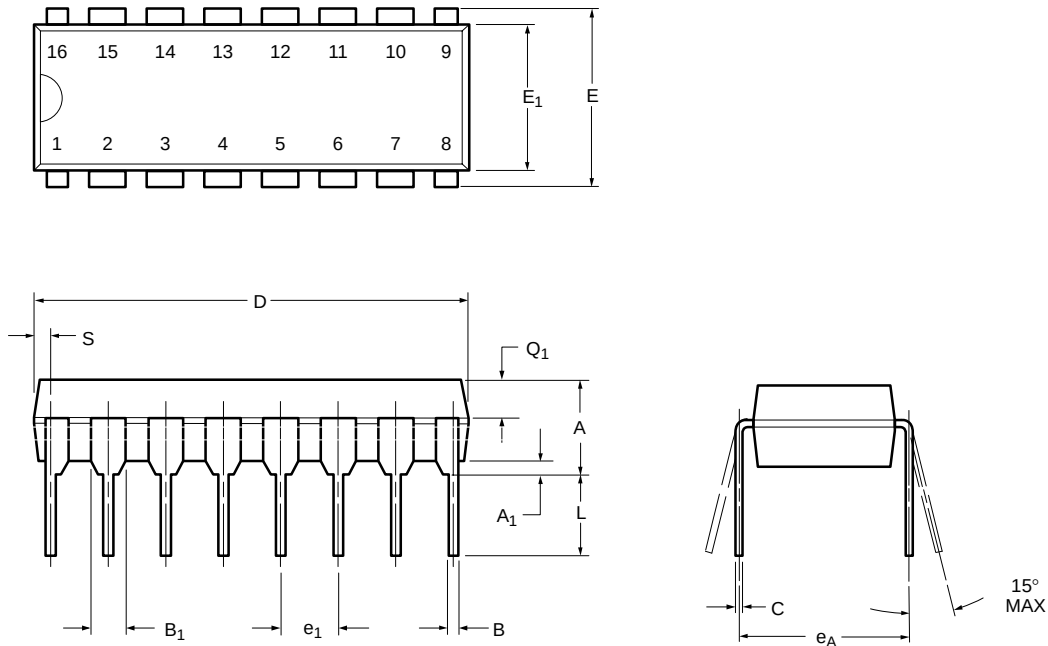


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
Ø	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

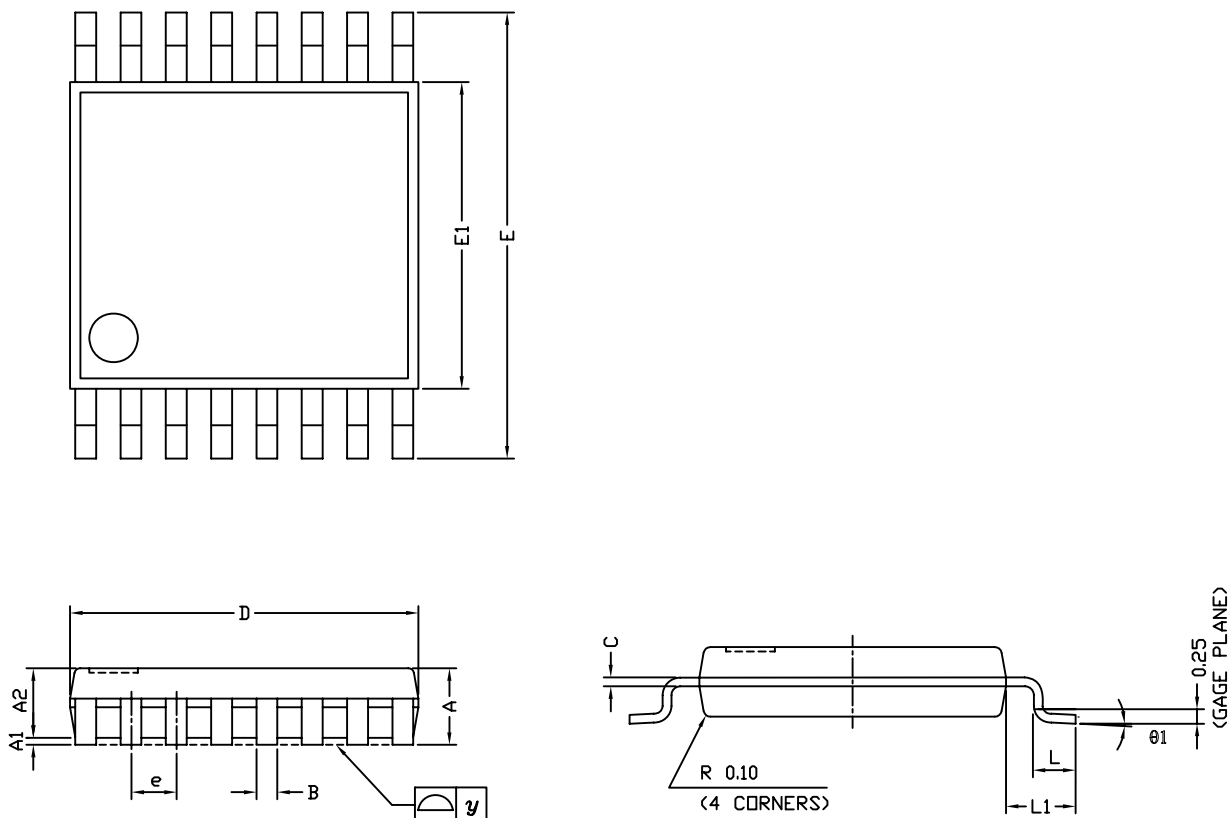


PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E₁	5.59	7.11	0.220	0.280
e₁	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q₁	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				

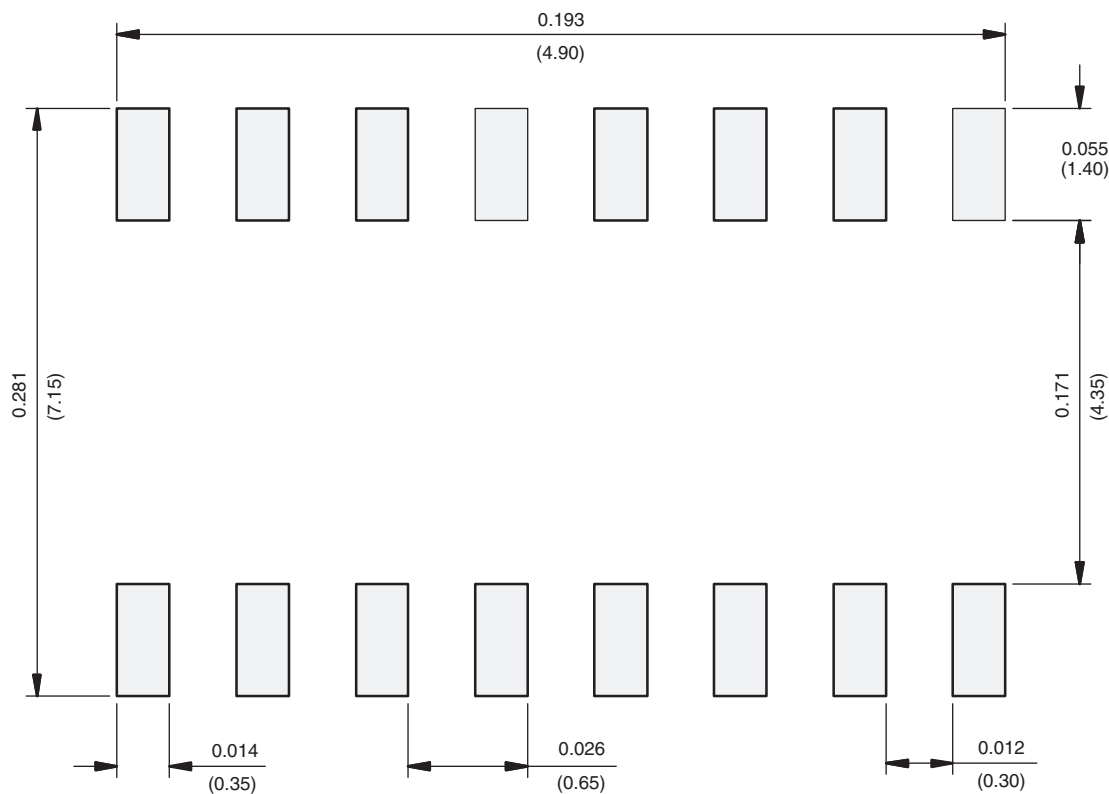
TSSOP: 16-LEAD



Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06			
DWG: 5624			

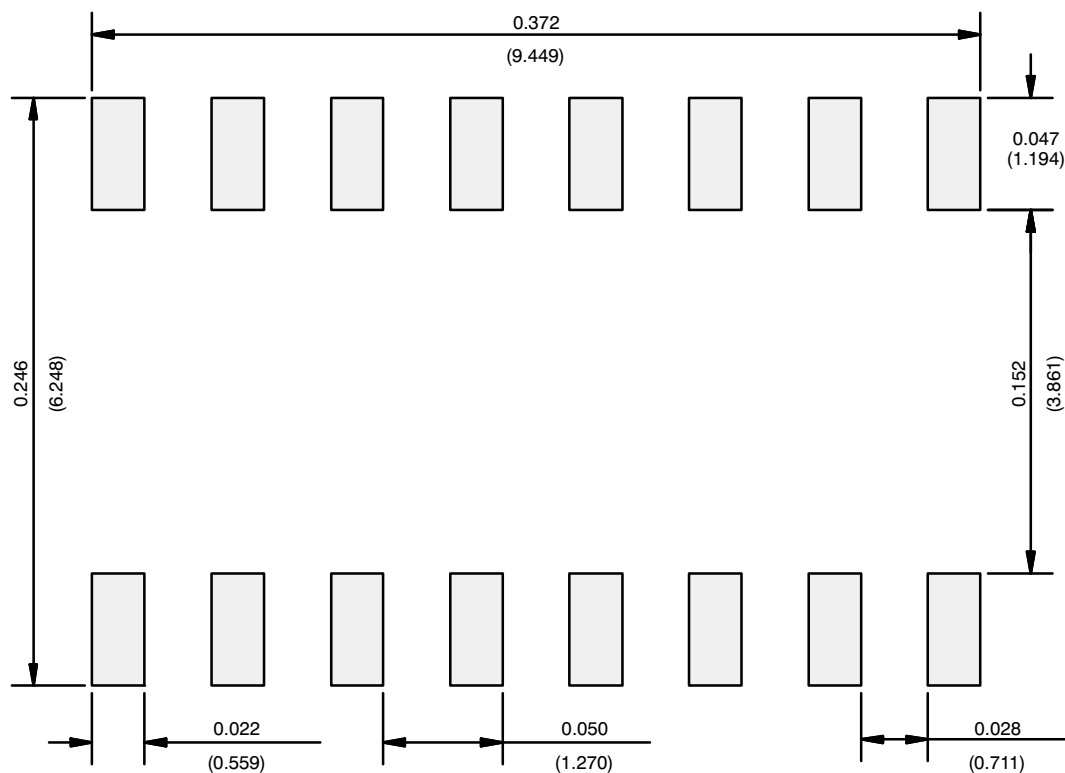


RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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