

DAC813

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- $\pm 1/2$ LSB NONLINEARITY OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- LOW POWER: 270mW typ
- DIGITAL INTERFACE DOUBLE BUFFERED: 12 AND 8 + 4 BITS
- SPECIFIED AT ± 12 V AND ± 15 V POWER SUPPLIES
- RESET FUNCTION TO BIPOLAR ZERO
- 0.3" WIDE DIP AND SO PACKAGES

DESCRIPTION

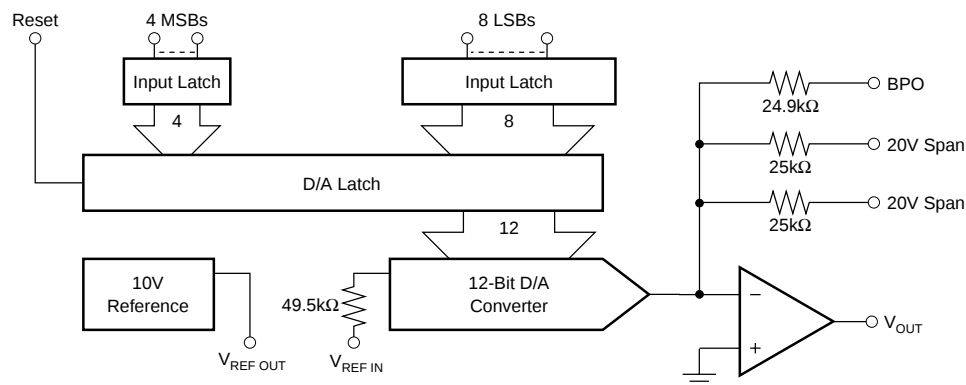
The DAC813 is a complete monolithic 12-bit digital-to-analog converter with a flexible digital interface. It includes a precision +10V reference, interface control logic, double-buffered latch and a 12-bit D/A

converter with voltage output operational amplifier. Fast current switches and laser-trimmed thin-film resistors provide a highly accurate, fast D/A converter.

Digital interfacing is facilitated by a double buffered latch. The input latch consists of one 8-bit byte and one 4-bit nibble to allow interfacing to 8-bit (right justified format) or 16-bit data buses. Input gating logic is designed so that the last nibble or byte to be loaded can be loaded simultaneously with the transfer of data to the D/A latch saving computer instructions.

A reset control allows the DAC813 D/A latch to asynchronously reset the D/A output to bipolar zero, a feature useful for power-up reset, recalibration, or for system re-initialization upon system failure.

The DAC813 is specified to $\pm 1/2$ LSB maximum linearity error (J, A grades) and $\pm 1/4$ LSB (K grade). It is packaged in 28-pin 0.3" wide plastic DIP and 28-lead plastic SOIC



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At $T_A = +25^{\circ}\text{C}$, $\pm V_{CC} = \pm 12\text{V}$ or $\pm 15\text{V}$ and load on $V_{OUT} = 5\text{k}\Omega \parallel 500\text{pF}$ to common, unless otherwise noted.

PARAMETER	CONDITIONS	DAC813JP, JU, AU			DAC813KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Resolution				12				Bits
Codes ⁽¹⁾			USB, BOB			*	*	
Digital Inputs Over Temperature Range ⁽²⁾								
V_{IH} ⁽³⁾		+2		+5.5	*		*	VDC
V_{IL}		0		+0.8	*		*	VDC
DATA Bits, $\overline{\text{WR}}$, $\overline{\text{Reset}}$, $\overline{\text{LDAC}}$, $\overline{\text{LMSB}}$, $\overline{\text{LLSB}}$				± 10			*	μA
I_{IH}	$V_{IN} = +2.7\text{V}$			± 10			*	μA
I_{IL}	$V_{IN} = +0.4\text{V}$							
ACCURACY								
Linearity Error			$\pm 1/4$	$\pm 1/2$		$\pm 1/8$	$\pm 1/4$	LSB
Differential Linearity Error			$\pm 1/2$	$\pm 3/4$		$\pm 1/4$	$\pm 1/2$	LSB
Gain Error ⁽⁴⁾			± 0.05	± 0.2		*	*	%
Unipolar Offset Error ⁽⁵⁾			± 0.01	± 0.02		*	*	% of FSR ⁽⁷⁾
Bipolar Zero Error ⁽⁶⁾			± 0.02	± 0.2		*	*	% of FSR
Monotonicity			Guaranteed			*	*	
Power Supply Sensitivity: $+V_{CC}$	20V Range		5	10		*	*	ppm of FSR/%
$-V_{CC}$			1	10		*	*	ppm of FSR/%
DRIFT								
Gain	Over Specification		± 5	± 30		*	± 15	ppm/ $^{\circ}\text{C}$
Unipolar Offset	Temperature Range		± 1	± 3		*	± 3	ppm of FSR/ $^{\circ}\text{C}$
Bipolar Zero			± 3	± 10		*	± 5	ppm of FSR/ $^{\circ}\text{C}$
Linearity Error Over Temperature Range			$\pm 1/2$	$\pm 3/4$		$\pm 1/4$	$\pm 1/2$	LSB
Monotonicity Over Temperature Range			Guaranteed			*		
SETTLING TIME⁽⁸⁾ (To Within $\pm 0.01\%$ of FSR of Final Value; $5\text{k}\Omega \parallel 500\text{pF}$ load)								
For Full Scale Range Change	20V Range		4.5	6		*	*	μs
	10V Range		3.3	5		*	*	μs
For 1LSB Change at Major Carry ⁽⁹⁾			2			*		μs
Slew Rate			10			*		V/ μs
ANALOG OUTPUT								
Voltage Range: Unipolar	$\pm V_{CC} > \pm 11.4\text{V}$		0 to +10			*		V
Bipolar	$\pm V_{CC} > \pm 11.4\text{V}$		± 5 , ± 10			*		V
Output Current		± 5			*			mA
Output Impedance	At DC		0.2			*		Ω
Short Circuit to Common Duration			Indefinite			*		
REFERENCE VOLTAGE								
Voltage		+9.95	+10	+10.05	*	*	*	V
Source Current Available for External Loads		5			*			mA
Impedance			2			*		Ω
Temperature Coefficient			± 5	± 25		*	*	ppm/ $^{\circ}\text{C}$
Short Circuit to Common Duration			Indefinite			*		
POWER SUPPLY REQUIREMENTS								
Voltage: $+V_{CC}$		+11.4	+15	+16.5	*	*	*	VDC
$-V_{CC}$		-11.4	-15	-16.5	*	*	*	VDC
Current: $+V_{CC} + V_L$	No Load		13	15		*	*	mA
$-V_{CC}$	No Load		-5	-7		*	*	mA
Potential at DCOM with Respect to ACOM ⁽¹⁰⁾		-3		+3	*	*	*	V
Power Dissipation			270	330		*	*	mW
TEMPERATURE RANGE								
Specification: J, K		0		+70	*		*	$^{\circ}\text{C}$
A		-40		+85	*		*	$^{\circ}\text{C}$
Operating: J, K		-40		+85	*		*	$^{\circ}\text{C}$
A		-55		+125	*		*	$^{\circ}\text{C}$
Storage: J, K		-60		+100	*		*	$^{\circ}\text{C}$
A		-65		+150	*		*	$^{\circ}\text{C}$

* Same as specification for DAC813AU, JP, JU.

NOTES: (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) TTL and 5V CMOS compatible. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY in the OPERATION section. (4) Specified with 500Ω Pin 6 to 7. Adjustable to zero with external trim potentiometer. (5) Error at input code 000_{HEX} for unipolar mode, FSR = 10V. (6) Error at input code 800_{HEX} for bipolar range. Specified with 100Ω Pin 6 to 4 and with 500Ω pin 6 to 7. See page 9 for zero adjustment procedure. (7) FSR means Full Scale Range and is 20V for the $\pm 10\text{V}$ range. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, 7FF_{HEX} to 800_{HEX} and 800_{HEX} to 7FF_{HEX}. (10) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	+V _L	Positive supply pin for logic circuits. Connect to +V _{CC} .
2, 3	20V Range	Connect Pin 2 or Pin 3 to Pin 9 (V _{OUT}) for a 20V FSR. Connect both to Pin 9 for a 10V FSR.
4	BPO	Bipolar offset. Connect to Pin 6 (V _{REF OUT}) through 100Ω resistor or 200Ω potentiometer for bipolar operation.
5	ACOM	Analog common, ±V _{CC} supply return.
6	V _{REF OUT}	+10V reference output referred to ACOM.
7	V _{REF IN}	Connected to V _{REF OUT} through a 1kΩ gain adjustment potentiometer or a 500Ω resistor.
8	+V _{CC}	Analog supply input, nominally +12V to +15V referred to ACOM.
9	V _{OUT}	D/A converter voltage output.
10	-V _{CC}	Analog supply input, nominally -12V or -15V referred to ACOM.
11	WR	Master enable for LDAC, LLSB, and LMSB. Must be low for data transfer to any latch.
12	LDAC	Load DAC. Must be low with WR for data transfer to the D/A latch and simultaneous update of the D/A converter.
13	Reset	When low, resets the D/A latch such that a Bipolar Zero output is produced. This control overrides all other data input operations.
14	LMSB	Enable for 4-bit input latch of D ₈ -D ₁₁ data inputs. NOTE: This logic path is slower than the WR path.
15	LLSB	Enable for 8-bit input latch of D ₀ -D ₇ data inputs. NOTE: This logic path is slower than the WR path.
16	DCOM	Digital common.
17	D0	Data Bit 1, LSB.
18	D1	Data Bit 2.
19	D2	Data Bit 3.
20	D3	Data Bit 4.
21	D4	Data Bit 5.
22	D5	Data Bit 6.
23	D6	Data Bit 7.
24	D7	Data Bit 8.
25	D8	Data Bit 9.
26	D9	Data Bit 10.
27	D10	Data Bit 11.
28	D11	Data Bit 12, MSB, positive true.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

+V _{CC} to ACOM	0 to +18V
-V _{CC} to ACOM	0 to -18V
+V _{CC} to -V _{CC}	0 to +36V
DCOM with respect to ACOM	±4V
Digital Inputs (Pins 11–15, 17–28) to DCOM	-0.5V to +V _{CC}
External Voltage Applied to BPO Span Resistor	±V _{CC}
V _{REF OUT}	Indefinite Short to ACOM
V _{OUT}	Indefinite Short to ACOM
Power Dissipation	750mW
Lead Temperature (soldering, 10s)	+300°C
Max Junction Temperature	+165°C
Thermal Resistance, θ _{J-A} : Plastic DIP and SOIC	130°C/W
Ceramic DIP	85°C/W

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C (LSB)	GAIN DRIFT (ppm/°C)
DAC813JP	28-Pin Plastic DIP	246	0°C to +70°C	±1/2	±30
DAC813JU	28-Lead Plastic SOIC	217	0°C to +70°C	±1/2	±30
DAC813KP	28-Pin Plastic DIP	246	0°C to +70°C	±1/4	±15
DAC813KU	28-Lead Plastic SOIC	217	0°C to +70°C	±1/4	±15
DAC813AU	28-Lead Plastic SOIC	217	-40°C to +85°C	±1/2	±30

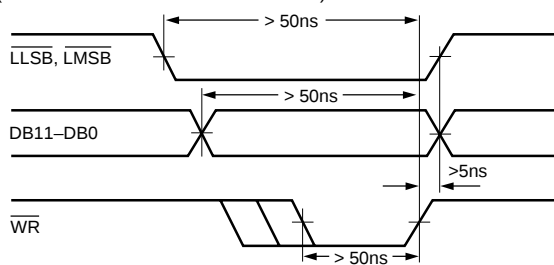
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

MINIMUM TIMING DIAGRAMS

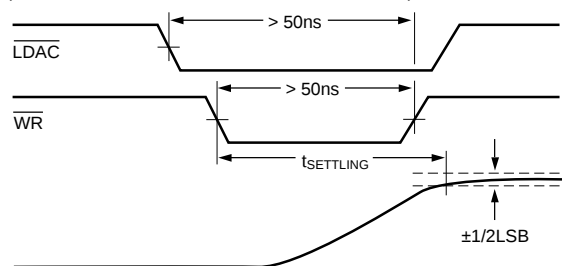
WRITE CYCLE #1

(Load first rank from Data Bus: $\overline{\text{LDAC}} = 1$)



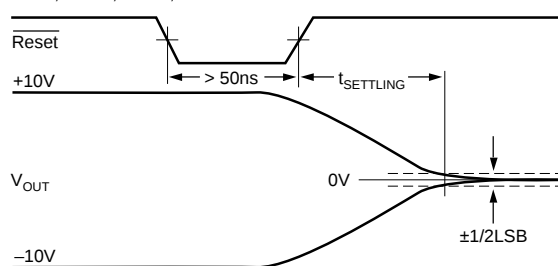
WRITE CYCLE #2

(Load second rank from first rank: $\overline{\text{LLSB}}$, $\overline{\text{LMSB}} = 1$)



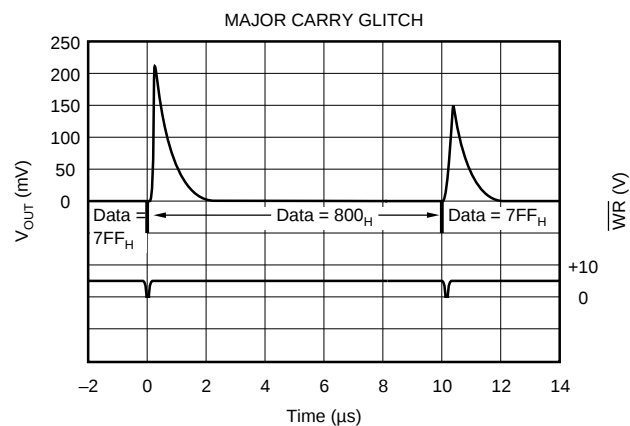
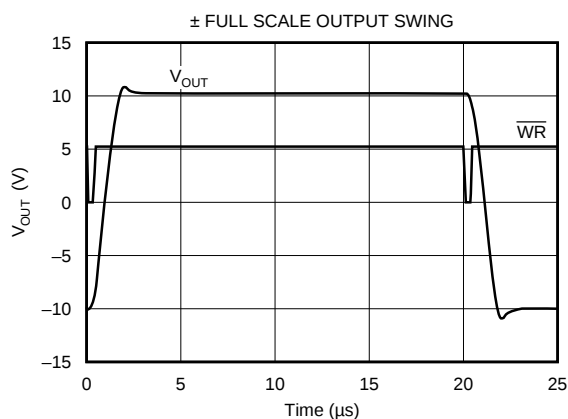
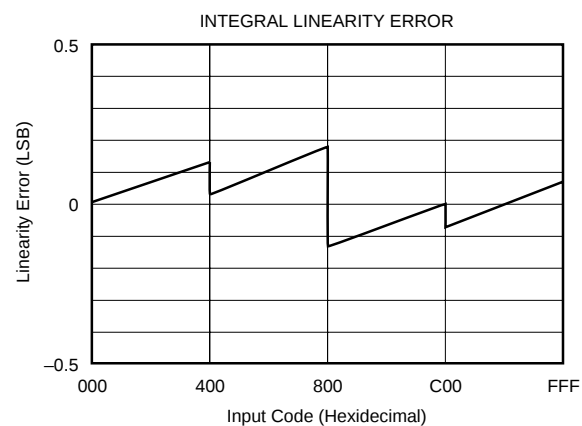
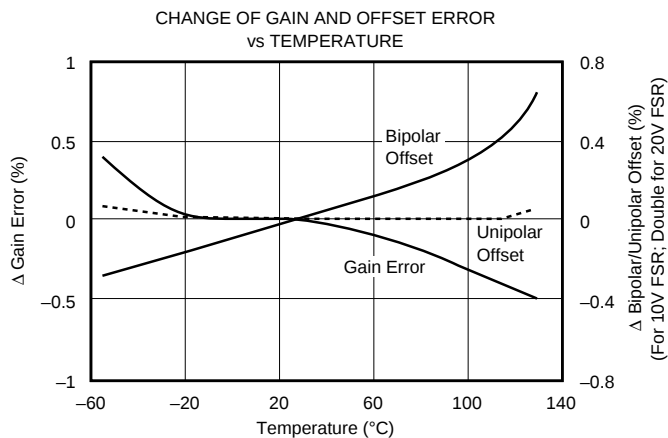
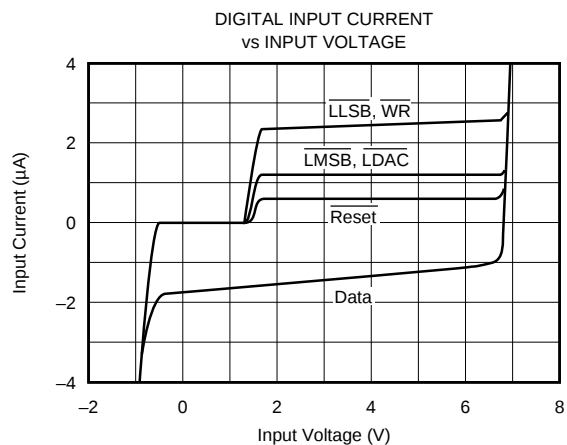
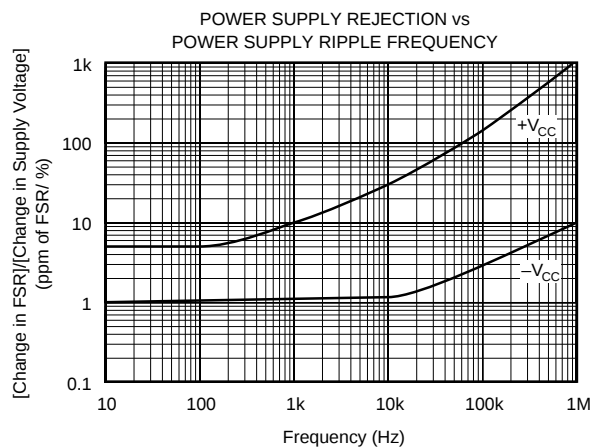
RESET COMMAND (Bipolar Mode)

$\overline{\text{LLSB}}$, $\overline{\text{LMSB}}$, $\overline{\text{LDAC}}$, $\overline{\text{WR}}$ = Don't Care



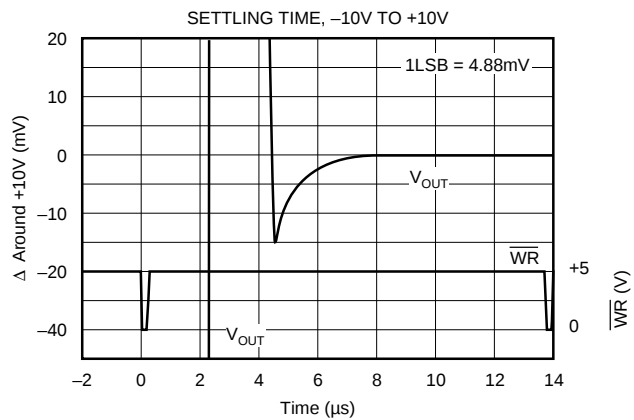
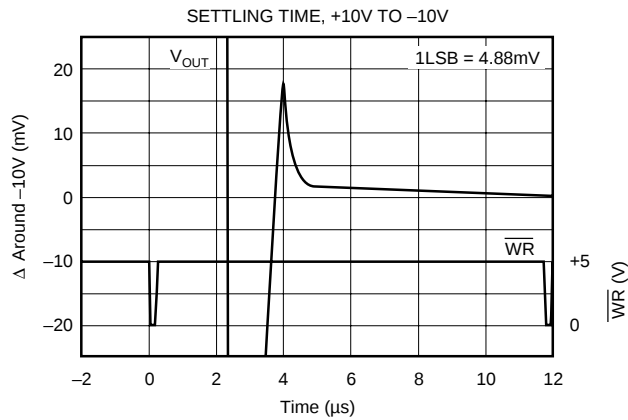
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, unless otherwise noted.



DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC813 accepts positive-true binary input codes. DAC813 may be connected by the user for any one of the following codes: USB (Unipolar Straight Binary), BOB (Bipolar Offset Binary) or, using an external inverter on the MSB line, BTC (Binary Two's Complement). See Table I.

DIGITAL INPUT	ANALOG OUTPUT		
	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
MSB to LSB			
FFF _{HEX}	+ Full Scale	+ Full Scale	Zero - 1LSB
800 _{HEX}	+ 1/2 Full Scale	Zero	- Full Scale
7FF _{HEX}	+ 1/2 Full Scale - 1LSB	Zero - 1LSB	+ Full Scale
000 _{HEX}	Zero	- Full Scale	Zero

* Invert MSB of BOB code with external inverter to obtain BTC code.

TABLE I. Digital Input Codes.

LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1s" and all "0s"). The DAC813 linearity error is specified at $\pm 1/4\text{LSB}$ (max) at $+25^\circ\text{C}$ K grades, and $\pm 1/2\text{LSB}$ (max) for J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of $1/2\text{LSB}$ means that the output step size can range from $1/2\text{LSB}$ to $3/2\text{LSB}$ when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC813 are monotonic over their specification temperature range.

DRIFT

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/ $^\circ\text{C}$).

Unipolar Offset Drift is measured with a data input of 000_{HEX}. The D/A is configured for unipolar output. Unipolar Offset Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/ $^\circ\text{C}$).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/ $^\circ\text{C}$).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to $\pm 0.012\%$ of Full Scale Range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (7FF_{HEX} to 800_{HEX} and 800_{HEX} to 7FF_{HEX}), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC813 contains an on-chip +10V reference. This voltage (pin 6) has a tolerance of $\pm 50\text{mV}$. $V_{\text{REF OUT}}$ must be connected to $V_{\text{REF IN}}$ through a gain adjust resistor with a nominal value of 500Ω . The connection can be made through an optional $1\text{k}\Omega$ trim resistor to provide adjustment to zero.



DAC813

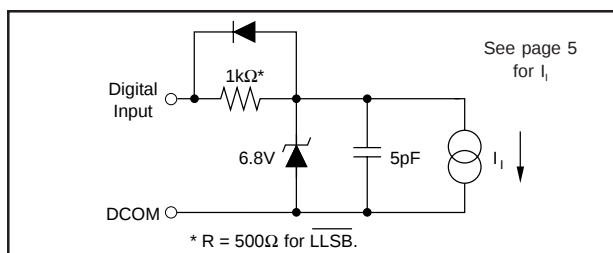


FIGURE 2. Equivalent Input Circuit for Digital Inputs.

the speed of the interface will be slower. A digital output driving a DATA input line of the DAC813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

RESET FUNCTION

When asserted low ($<0.8V$), $\overline{RESET}$ (Pin 13) forces the D/A latch to 800_{HEX} regardless of any other input logic condition. If the analog output is connected for bipolar operation (either $\pm 10V$ or $\pm 5V$), the output will be reset to Bipolar Zero (0V). If the analog output is connected for unipolar operation (0 to +10V), the output will be reset to half-scale (+5V).

If $\overline{RESET}$ is not used, it should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available Reset can be connected to $+V_{CC}$ through a 100kΩ to 1MΩ resistor to limit the input current.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB),

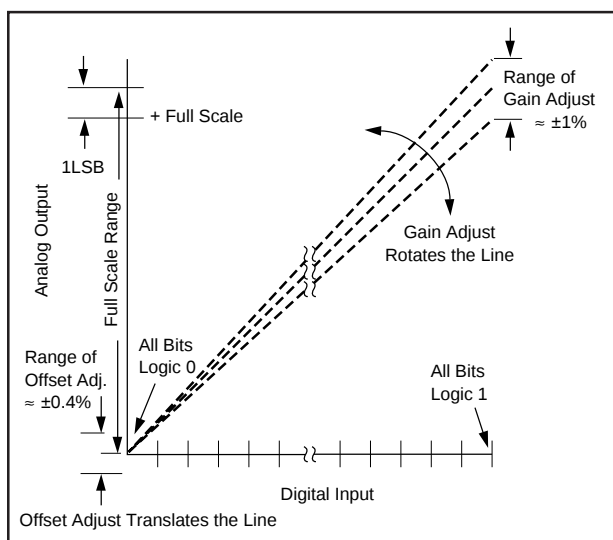


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. Example: If the full scale range is connected for 20V, the maximum negative output voltage is $-10V$. See Table III for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

DIGITAL INPUT MSB to LSB	ANALOG OUTPUT		
	0 to +10V	$\pm 5V$	$\pm 10V$
FFF _{HEX}	+9.9976V	+4.9976V	+9.9951V
800 _{HEX}	+5.0000V	0.0000V	0.0000V
7FF _{HEX}	+4.9976V	-0.0024V	-0.0049V
000 _{HEX}	0.0000V	-5.0000V	-10.0000V
1LSB	2.44mV	2.44mV	4.88mV

TABLE III. Digital Input/Analog Output.

INSTALLATION

POWER SUPPLY CONNECTIONS

Note that the lid of the ceramic packaged DAC813 is connected to $-V_{CC}$. Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Optimum settling performance occurs using a 1 to 10μF tantalum capacitor at $-V_{CC}$ and at least a 0.01μF ceramic capacitor at $+V_{CC}$. Applications with less critical settling time may be able to use 0.01μF at $-V_{CC}$ as well. The 0.01μF capacitors should be located close to the DAC813.

Pin 1 supplies internal logic and **must** be connected to $+V_{CC}$.

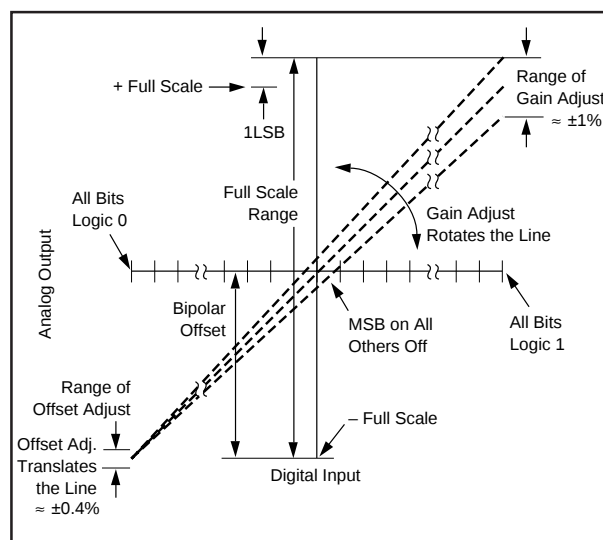


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

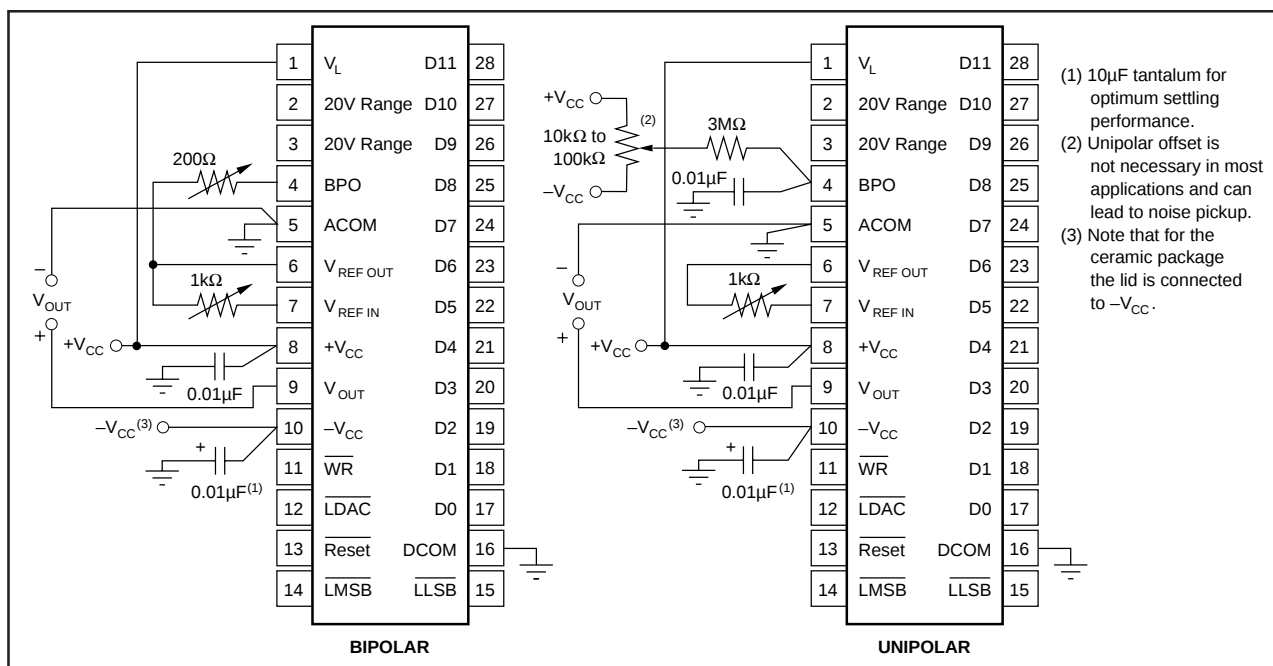


FIGURE 5. Power Supply, Gain, and Offset Connections.

DAC813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both Analog Common (ACOM, Pin 5) and Digital Common (DCOM, Pin 16) be connected directly to a ground plane under the package. If a ground plane is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and V_{REF OUT} is the ACOM pin, it is also important to connect the load directly to the ACOM pin. Refer to Figure 5.

The change in current in the Analog Common pin (ACOM, Pin 5) due to an input data word change from 000_{HEX} to FFF_{HEX} is only 800μA.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC813 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. Refer to Figure 6.

The internal feedback resistors (25kΩ) and the bipolar offset resistor (24.9kΩ) are trimmed to an absolute tolerance of less than ±2%. Therefore, one can change the range by adding a series resistor in various feedback circuit configurations. For example, a 600Ω resistor in series with the 20V range terminal can be used to obtain a 20.48V (±10.24V) range (5mV LSB). A 7.98kΩ resistor in series with the 10V range connection (20V ranges in parallel) gives a 16.384V (±8.192V) bipolar range (4mV LSB). Gain drift will be affected by the mismatch of the temperature coefficient of the external resistor with the internal D/A resistors.

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC813 interface logic allows easy interface to microcomputer bus structures. The control signal is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{\text{LMSB}}$, $\overline{\text{LLSB}}$, and $\overline{\text{LDAC}}$ determine which of the latches are selected. It is permissible to enable two or more latches simultaneously, as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC813s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are used, the base address decoder can be simplified or eliminated altogether.

8-BIT INTERFACE

The control logic of DAC813 permits interfacing to right-justified data formats, illustrated in Figure 7. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figure 8 illustrates an addressing scheme for right-justified data. The base address is decoded from the high-order address bits. A0 and A1 address the appropriate latches. Note that adjacent addresses are used. X10_{HEX} loads the 8 LSBs and X01_{HEX} loads the 4 MSBs and simultaneously transfers input latch data to the D/A latch. Addresses X00_{HEX} and X11_{HEX} are not used.

INTERFACING MULTIPLE DAC813s IN 8-BIT SYSTEMS

Many applications, such as automatic test systems, require that the outputs of several D/A converters be updated simultaneously. The interface shown in Figure 9 uses a 74LSB138 decoder to decode a set of eight adjacent addresses to load the input latches of four DAC813s. The example uses a right-justified data format.

A ninth address using A3 causes all DAC813s to be updated simultaneously. If a certain DAC813 is always loaded last (for instance, D/A #4), A3 is not needed, saving 8 address

spaces for other uses. Incorporate A3 into the base address decoder, remove the inverter, connect the common $\overline{\text{LDAC}}$ line to $\overline{\text{LLSB}}$ of D/A #4, and connect D1 of the 74LS138 to +5V.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines, $\overline{\text{LMSB}}$ and $\overline{\text{LLSB}}$, are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC813, is selected by the address decoder and strobed by $\overline{\text{WR}}$.

Be sure and read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.

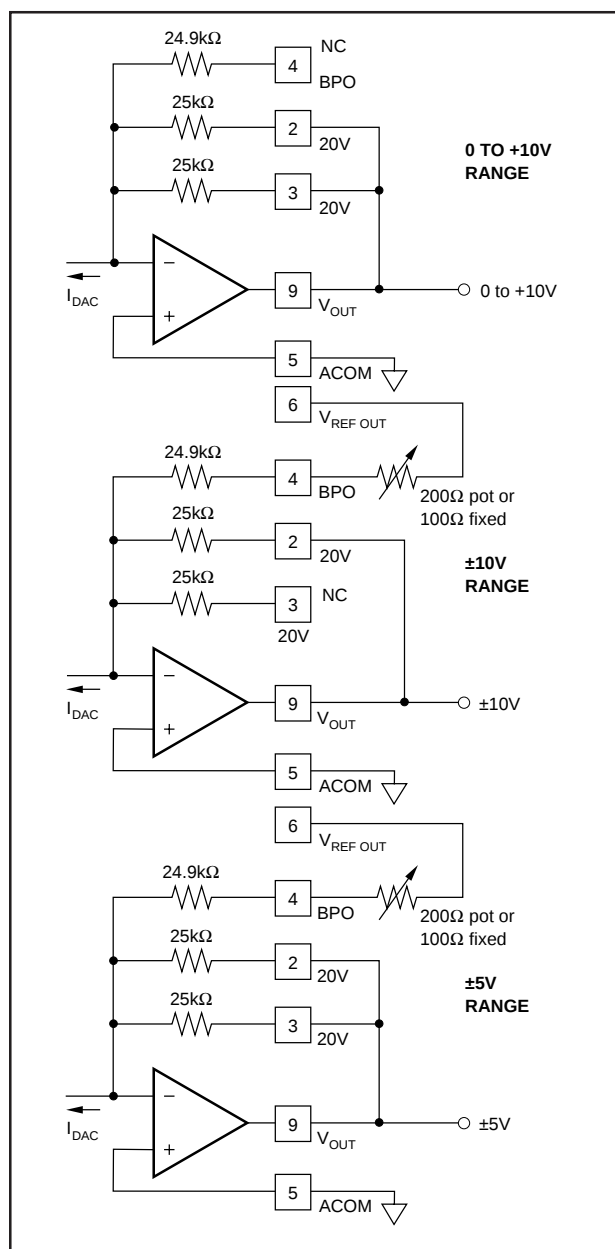


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

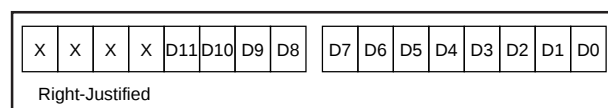


FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

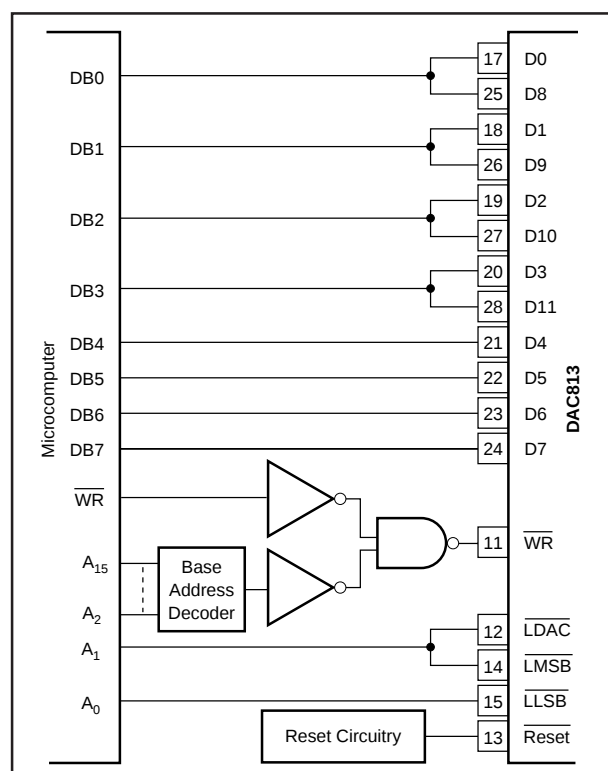
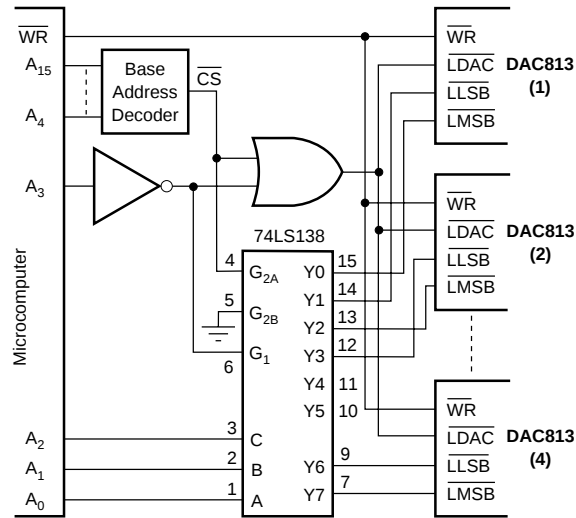


FIGURE 8. Right-Justified Data Bus Interface.



ADDRESS BUS				OPERATION
A3	A2	A1	A0	
0	0	0	0	Load 8 LSB – D/A #1
0	0	0	1	Load 4 MSB – D/A #1
0	0	1	0	Load 8 LSB – D/A #2
0	0	1	1	Load 4 MSB – D/A #2
0	1	0	0	Load 8 LSB – D/A #3
0	1	0	1	Load 4 MSB – D/A #3
0	1	1	0	Load 8 LSB – D/A #4
0	1	1	1	Load 4 MSB – D/A #4
1	X	X	X	Load D/A Latch—All D/A

FIGURE 9. Interfacing Multiple DAC813s to an 8-Bit Bus.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC813AU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC813AU	Samples
DAC813AU/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC813AU	Samples
DAC813AU/1KG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC813AU	Samples
DAC813AUG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC813AU	Samples
DAC813JP	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	DAC813JP	
DAC813JPG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	DAC813JP	
DAC813JU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC813JU	Samples
DAC813JU/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC813JU	Samples
DAC813JUG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC813JU	Samples
DAC813KP	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	DAC813KP	
DAC813KPG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	DAC813KP	
DAC813KU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC813KU	Samples
DAC813KUG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC813KU	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC813AU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
DAC813JU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC813AU/1K	SOIC	DW	28	1000	367.0	367.0	55.0
DAC813JU/1K	SOIC	DW	28	1000	367.0	367.0	55.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com