Single 14-/12-/10-Bit 500 MSPS Digital-to-Analog Converters

Check for Samples: DAC3151, DAC3161, DAC3171

FEATURES

- **Single Channel**
- **Resolution**
  - **DAC3151: 10-Bit**
  - **DAC3161: 12-Bit**
  - **DAC3171: 14-Bit**
- **Maximum Sample Rate: 500 MSPS**
- **Pin-Compatible Family**
- **Input Interface:**
  - **Parallel LVDS Inputs**
  - **Single or Dual DDR Data Clock**
  - **Internal FIFO**
- **Chip to Chip Synchronization**
- **Power Dissipation: 375mW**
- **Spectral Performance at 20 MHz IF**
  - **SNR: 76 dBFS for DAC3171; 72dBFS for DAC3161; 62 dBFS for DAC3151**
  - **SFDR: 78 dBc for DAC3171; 77dBc for DAC3161; 76 dBc for DAC3151**
- **Current Sourcing DACs**
- **Compliance Range: -0.5V to 1V**
- **Package: 64 Pin QFN (9x9mm)**

APPLICATIONS

- **Wireless Infrastructure**
  - **PA Bias, Envelope Tracking, TX**
- **Radar**
- **Software-Defined Radio**
- **Signal/Waveform Generators**
- **Cable Head-End Equipment**

DESCRIPTION

The DAC3151/DAC3161/DAC3171 is a family of single channel 500MSPS digital-to-analog converters with resolutions of 10-/12-/14-bits. The family uses a 10-/12-/14-bit wide LVDS digital bus with an input FIFO. The 14-bit DAC3171 also supports a DDR 7-bit LVDS interface mode. FIFO input and output pointers can be synchronized across multiple devices for precise signal synchronization. The DAC outputs are current sourcing and terminate to GND with a compliance range of -0.5 to 1V. DAC3151/DAC3161/DAC3171 is pin compatible with the dual-channel, 10-/12-/14-bit, 500MSPS digital-to-analog converter DAC3154/DAC3164/DAC3174.

The device is available in a QFN-64 PowerPAD™ package is specified over the full industrial temperature range (–40°C to 85°C).

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAMS

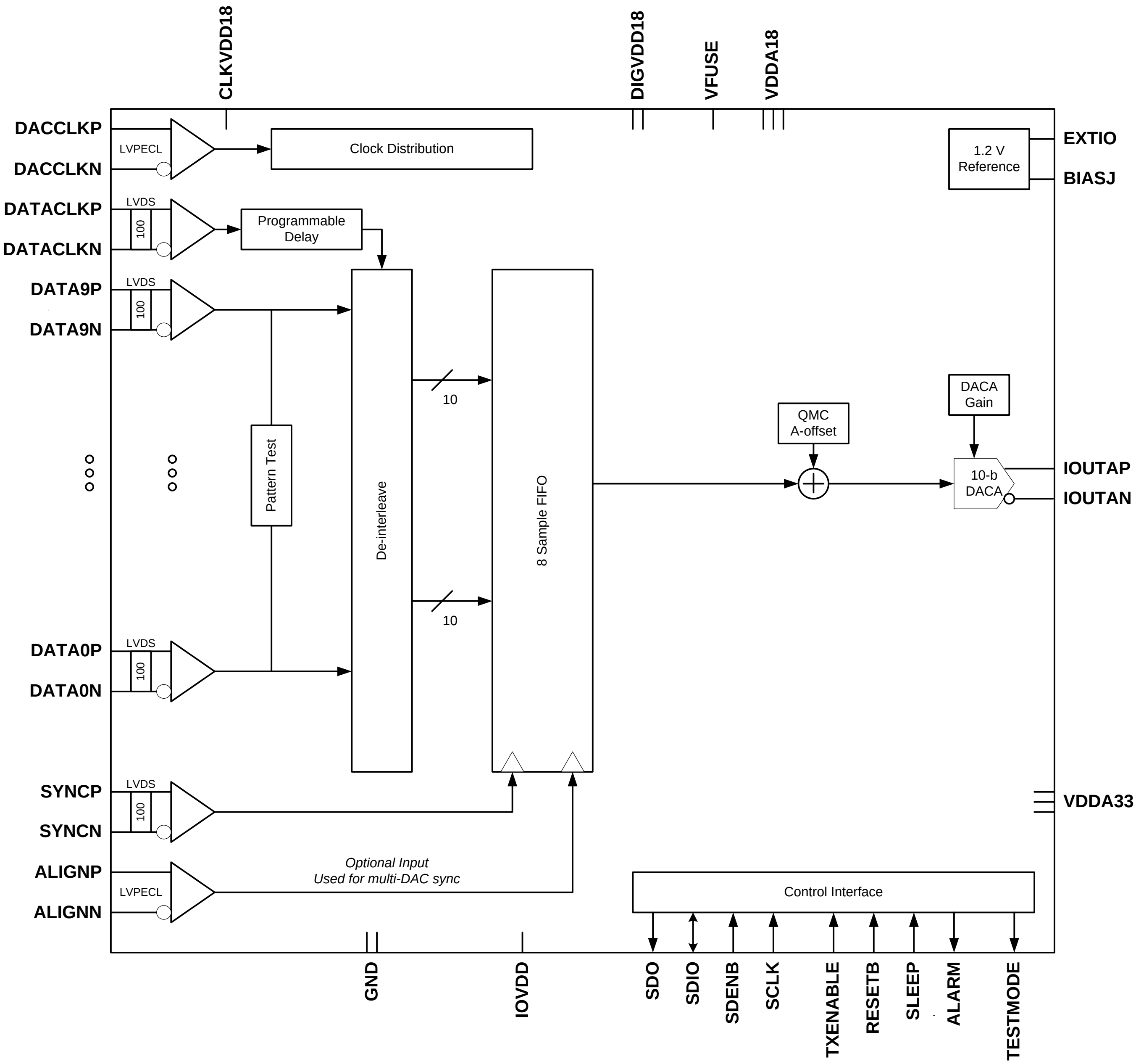

Figure 1. DAC3151 Full Word Interface Mode

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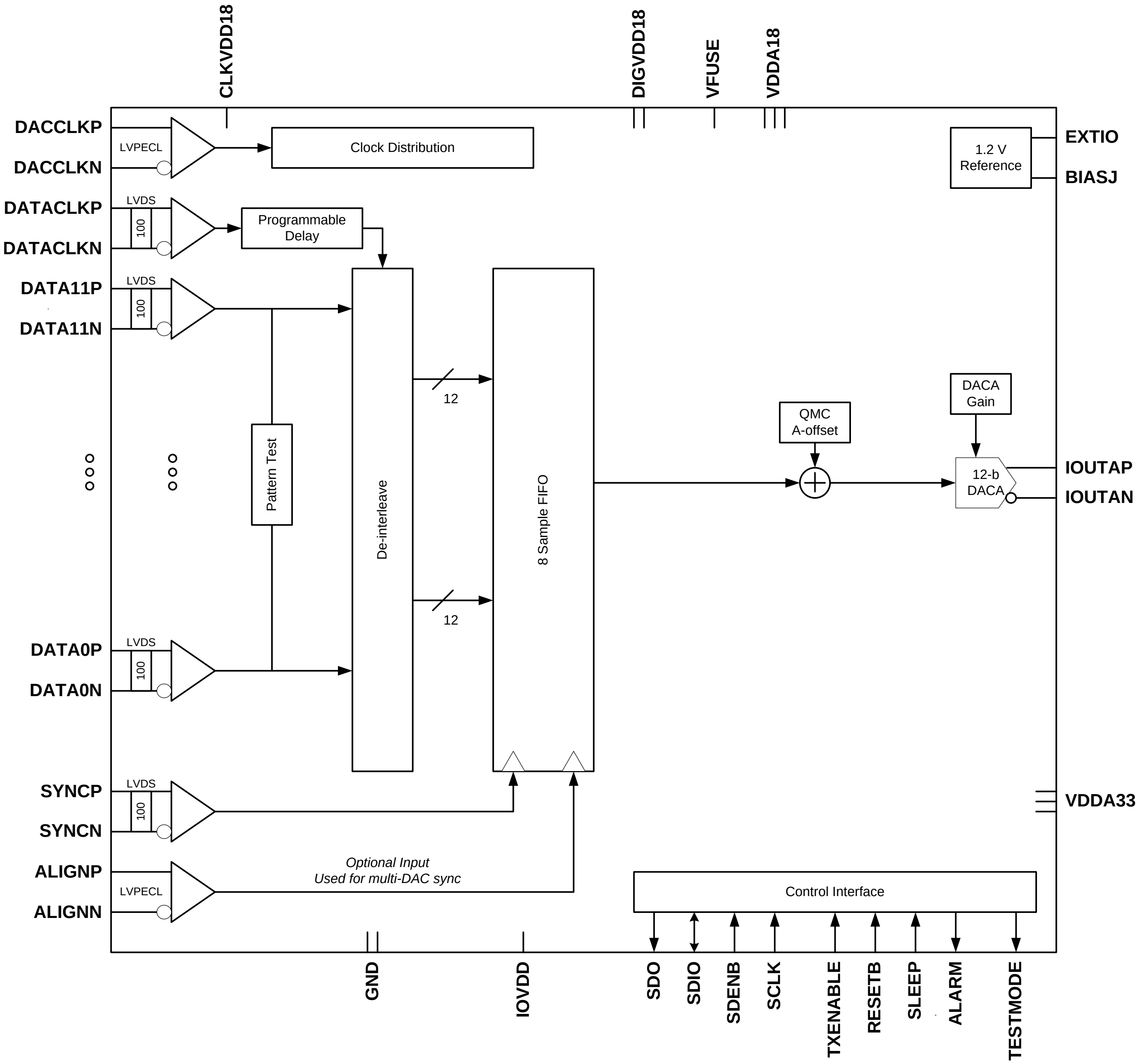

Figure 2. DAC3161 Full Word Interface Mode

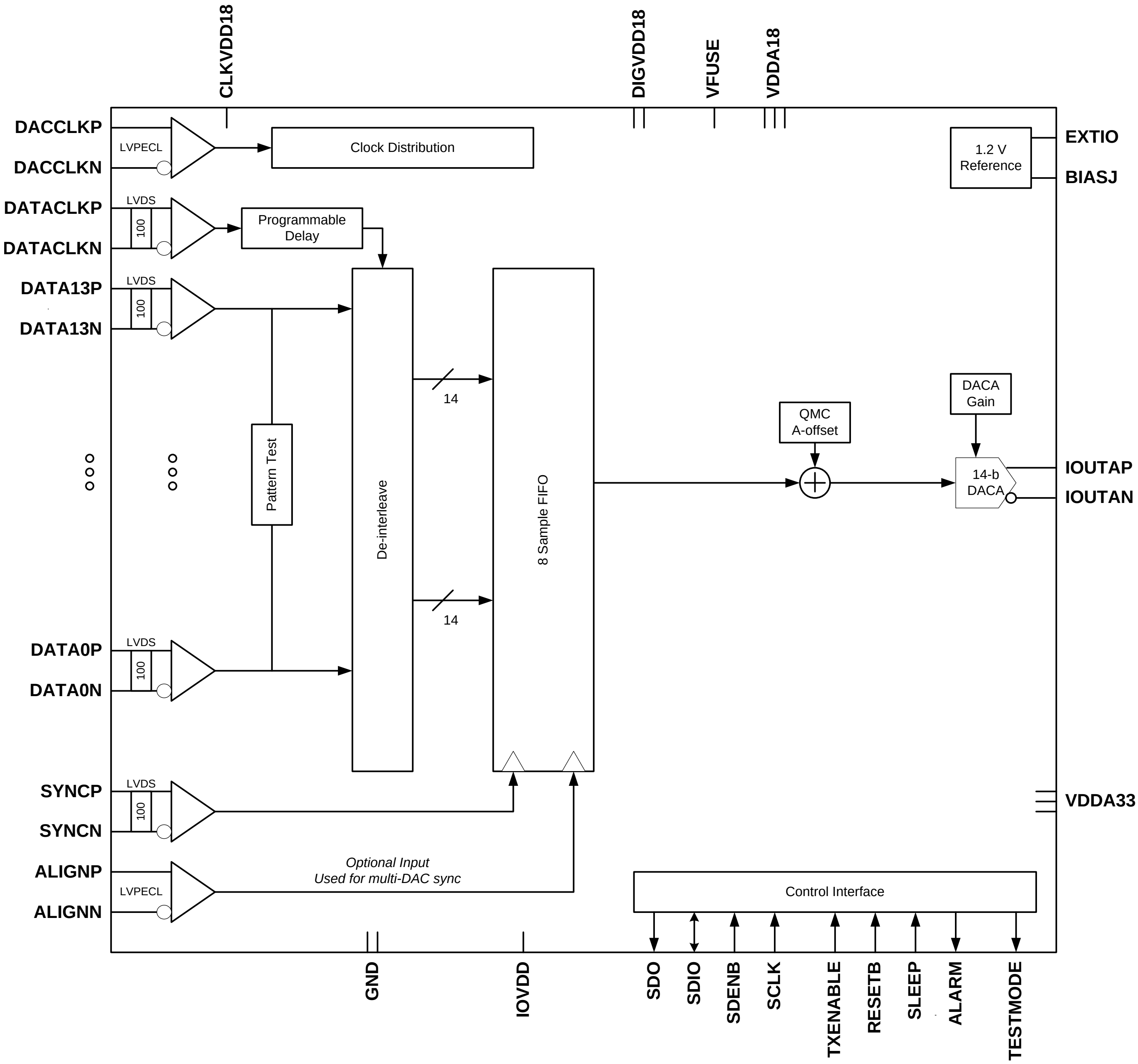

Figure 3. DAC3171 Full Word Interface Mode

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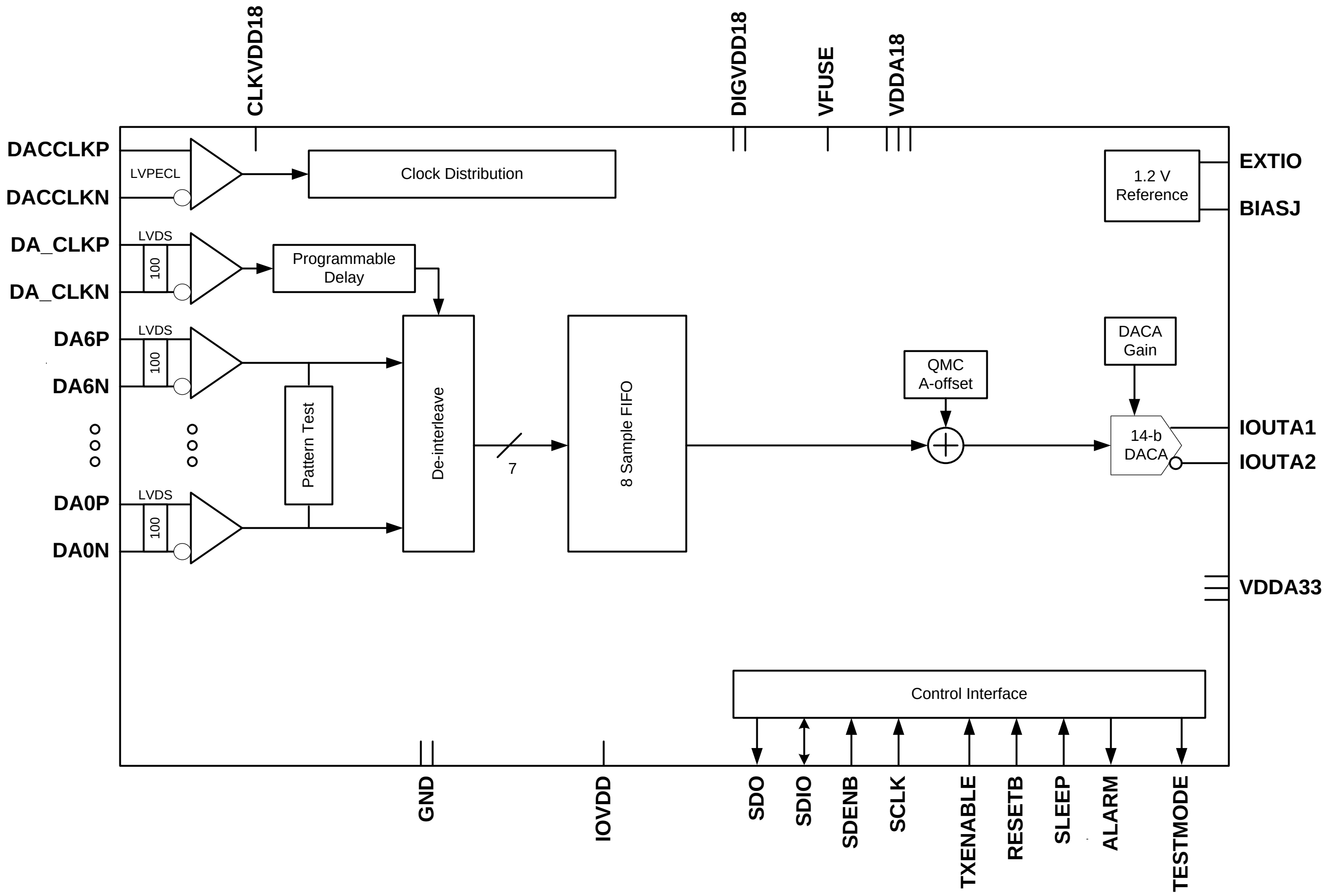
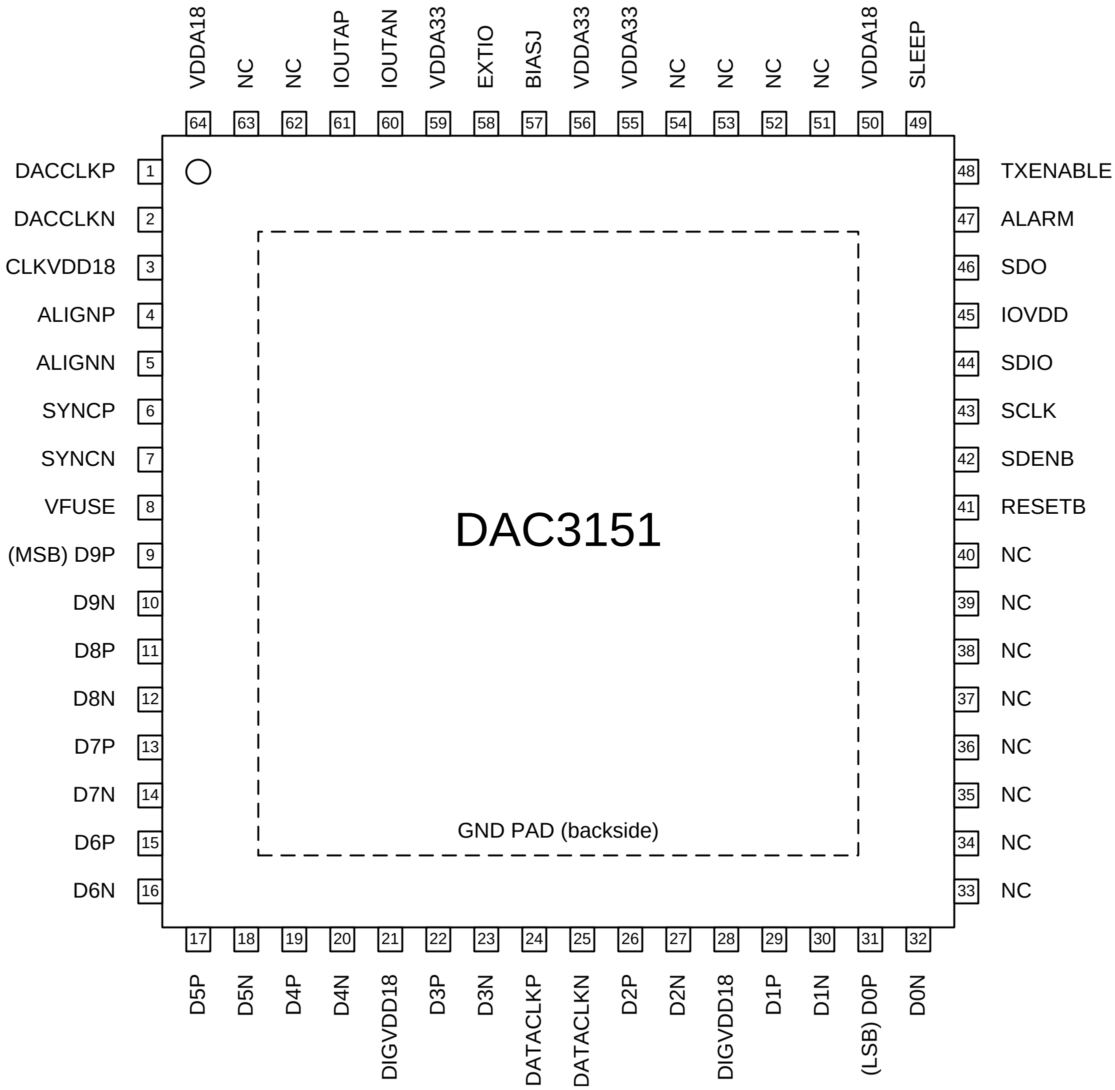


Figure 4. DAC3171 7-bit Interface Mode

PINOUT – DAC3151



PIN ASSIGNMENT TABLE – DAC3151

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL/SERIAL			
SCLK	43	I	Serial interface clock. Internal pull-down.
SDENB	42	I	Serial interface clock. Internal pull-up.
SDIO	44	I/O	Bi-directional serial data in 3 pin mode (default). In 4-pin interface mode (register sif4_ena (config 0, bit 9)), the SDIO pin in an input only. Internal Pull-down.
SDO	46	O	Uni-directional serial interface data in 4 pin mode (register sif4_ena (config 0, bit 9)). The SDO pin is tri-stated in 3-pin interface mode (default). Internal Pulldown.
RESETB	41	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Assynchronous. Internal pull-up.
ALARM	47	O	CMOS output for ALARM condition.
TXENABLE	48	I	Transmit enable active high input. TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data is ignored. Internal pull-down.
SLEEP	49	I	Puts device in sleep, active high. Internal pull-down.

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PIN ASSIGNMENT TABLE – DAC3151 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DATA INTERFACE			
DATA[9:0]P/N	9/10-19/20 22/23 26/27, 29/30, 31/32	I	LVDS input data bits for both channels. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Data format relative to DATACLKP/N clock is Double Data Rate (DDR) with two data transfers per DATACKP/N clock cycle. The data format is interleaved with channel A (rising edge) and channel B falling edge. In the default mode (reverse bus not enabled): DATA13P/N is most significant data bit (MSB) DATA0P/N is most significant data bit (LSB)
DATACLKP/N	24/25	I	DDR differential input data clock. Edge to center nominal timing. Ch A rising edge, Ch B falling edge in multiplexed output mode.
SYNCP/N	6/7	I	Reset the FIFO or to be used as a syncing source. These two functions are captured with the rising edge of DATACLKP/N. The signal captured by the falling edge of DATACLKP/N.
ALIGNP/N	4/5	I	LVPECL FIFO output syncrhonization. This positive/negative pair is captured with the rising edge of DACCLKP/N. It is used to reset the clock dividers and for multiple DAC synchronization. If unused it can be left unconnected.
OUTPUT/CLOCK			
DACCLKP/N	1/2	I	LVPECL clock input for DAC core with a self-bias of approximately CLKVDD18/2.
IOUTAP/N	61/60	O	A-Channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current source and the most positive voltage on the IOUTAP pin. Similarly, a 0xFFFF data input results in a 0 mA current source and the least positive voltage on the IOUTAP pin.
REFERENCE			
EXTIO	58	I/O	Used as external reference input when internal reference is disabled. Requires a 0.1 µF decoupling capacitor to GND when used as reference output.
BIASJ	57	O	Full-scale output current bias. For 20 mA full-scale output current, connect a 960 Ω resistor to GND.
POWER SUPPLY			
IOVDD	45	I	Supply voltage for CMOS IO's. 1.8V – 3.3V.
CLKVDD18	3	I	1.8V clock supply
DIGVDD18	21, 28	I	1.8V digital supply. Also supplies LVDS receivers.
VDDA18	50, 64	I	Analog 1.8V supply
VDDA33	55, 56, 59	I	Analog 3.3V supply
VFUSE	8	I	Digital supply voltage. (1.8V) This supply pin is also used for factory fuse programming. Connect to DVDD pins for normal operation.
NC	33/34-39/40, 51, 52, 53, 54 62, 63		Not Used. These pins can be left open or tied to GROUND in actual application use. It is recommended to turn off pin 33-40 (register lvdsdata_ena) to save power.

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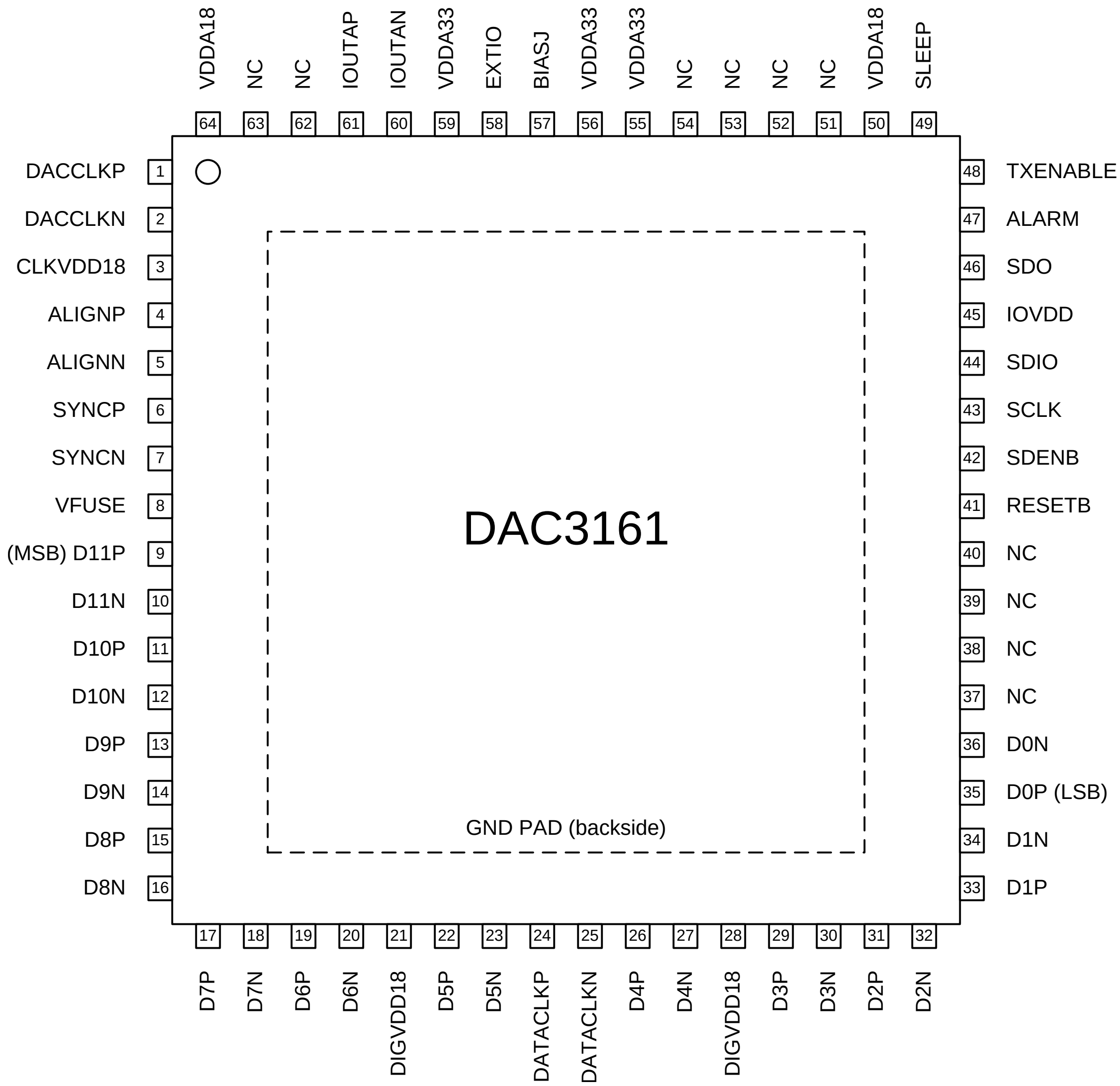
PINOUT – DAC3161



PIN ASSIGNMENT TABLE – DAC3161

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL/SERIAL			
SCLK	43	I	Serial interface clock. Internal pull-down.
SDENB	42	I	Serial interface clock. Internal pull-up.
SDIO	44	I/O	Bi-directional serial data in 3 pin mode (default). In 4-pin interface mode (register sif4_ena (config 0, bit 9)), the SDIO pin in an input only. Internal Pull-down.
SDO	46	O	Uni-directional serial interface data in 4 pin mode (register sif4_ena (config 0, bit 9)). The SDO pin is tri-stated in 3-pin interface mode (default). Internal Pulldown.
RESETB	41	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Assynchronous. Internal pull-up.
ALARM	47	O	CMOS output for ALARM condition.
TXENABLE	48	I	Transmit enable active high input. TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data is ignored. Internal pull-down.
SLEEP	49	I	Puts device in sleep, active high. Internal pull-down.

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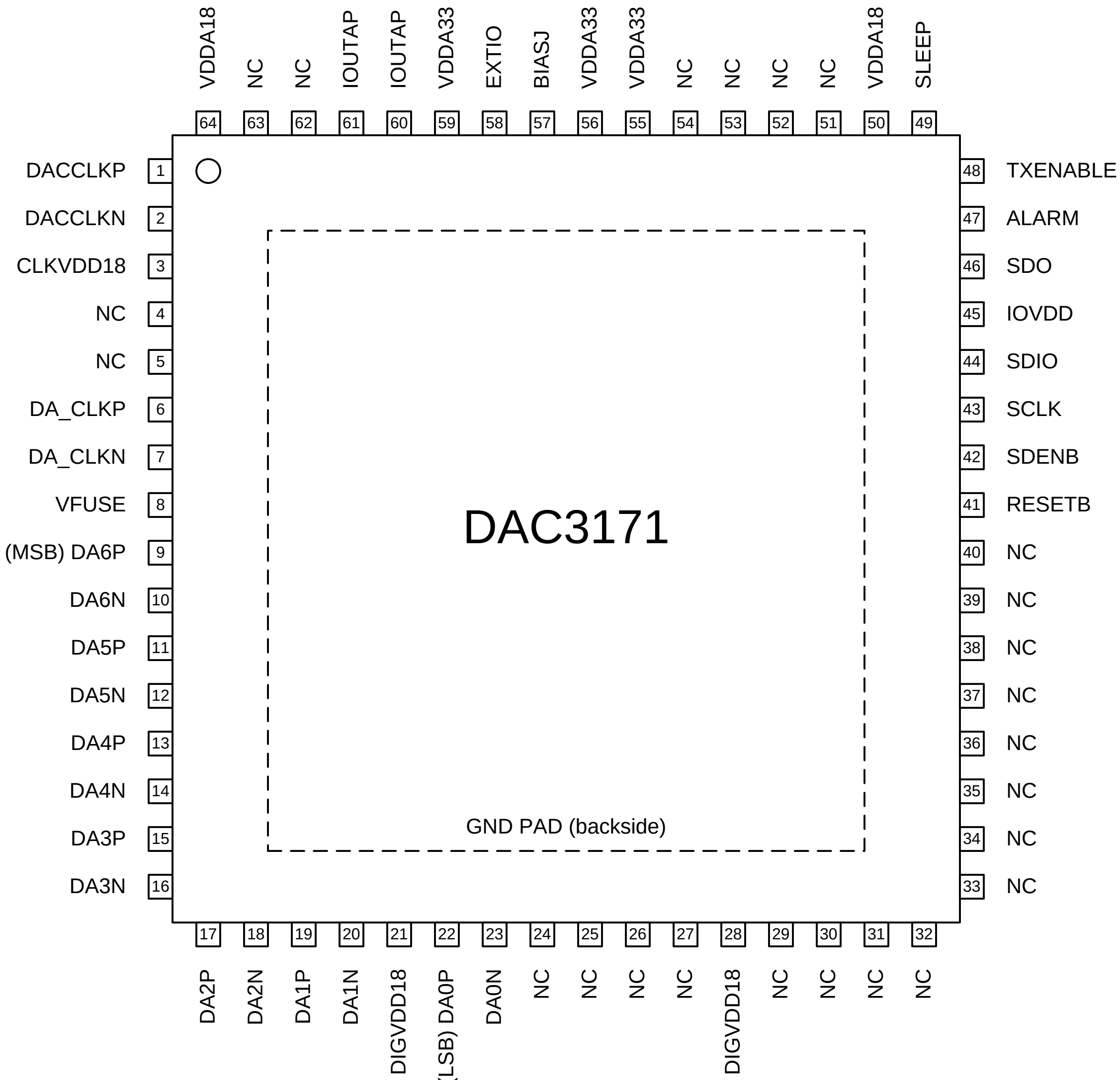
PIN ASSIGNMENT TABLE – DAC3161 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DATA INTERFACE			
DATA[11:0]P/N	9/10-19/20 22/23 26/27, 29/30-35/36	I	LVDS input data bits for both channels. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Data format relative to DATACLKP/N clock is Double Data Rate (DDR) with two data transfers per DATACKP/N clock cycle. The data format is interleaved with channel A (rising edge) and channel B falling edge. In the default mode (reverse bus not enabled): DATA13P/N is most significant data bit (MSB) DATA0P/N is most significant data bit (LSB)
DATACLKP/N	24/25	I	DDR differential input data clock. Edge to center nominal timing. Ch A rising edge, Ch B falling edge in multiplexed output mode.
SYNCP/N	6/7	I	Reset the FIFO or to be used as a syncing source. These two functions are captured with the rising edge of DATACLKP/N. The signal captured by the falling edge of DATACLKP/N.
ALIGNP/N	4/5	I	LVPECL FIFO output syncrhonization. This positive/negative pair is captured with the rising edge of DACCLKP/N. It is used to reset the clock dividers and for multiple DAC synchronization. If unused it can be left unconnected.
OUTPUT/CLOCK			
DACCLKP/N	1/2	I	LVPECL clock input for DAC core with a self-bias of approximately CLKVDD18/2.
IOUTAP/N	61/60	O	A-Channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current source and the most positive voltage on the IOUTAP pin. Similarly, a 0xFFFF data input results in a 0 mA current source and the least positive voltage on the IOUTAP pin.
REFERENCE			
EXTIO	58	I/O	Used as external reference input when internal reference is disabled. Requires a 0.1 µF decoupling capacitor to GND when used as reference output.
BIASJ	57	O	Full-scale output current bias. For 20 mA full-scale output current, connect a 960 Ω resistor to GND.
POWER SUPPLY			
IOVDD	45	I	Supply voltage for CMOS IO's. 1.8V – 3.3V.
CLKVDD18	3	I	1.8V clock supply
DIGVDD18	21, 28	I	1.8V digital supply. Also supplies LVDS receivers.
VDDA18	50, 64	I	Analog 1.8V supply
VDDA33	55, 56, 59	I	Analog 3.3V supply
VFUSE	8	I	Digital supply voltage. (1.8V) This supply pin is also used for factory fuse programming. Connect to DVDD pins for normal operation.
NC	37, 38, 39, 40, 51, 52, 53, 54, 62, 63		Not Used. These pins can be left open or tied to GROUND in actual application use. It is recommended to turn off pin 37-40 (register lvdsdata_ena) to save power.

PIN OUT – DAC3171 7-BIT INTERFACE MODE



PIN ASSIGNMENT TABLE – DAC3171 7-BIT INTERFACE MODE

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL/SERIAL			
SCLK	43	I	Serial interface clock. Internal pull-down.
SDENB	42	I	Serial interface clock. Internal pull-up.
SDIO	44	I/O	Bi-directional serial data in 3 pin mode (default). In 4-pin interface mode (register XYZ), the SDIO pin in an input only. Internal Pull-down.
SDO	46	O	Uni-directional serial interface data in 4 pin mode (register XYZ). The SDO pin is tri-stated in 3-pin interface mode (default). Internal Pulldown.
RESETB	41	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Assynchronous. Internal pull-up.
ALARM	47	O	CMOS output for ALARM condition.
TXENABLE	48	I	Transmit enable active high input. TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data is ignored. Internal pull-down.
SLEEP	49	I	Puts device in sleep, active high. Internal pull-down.

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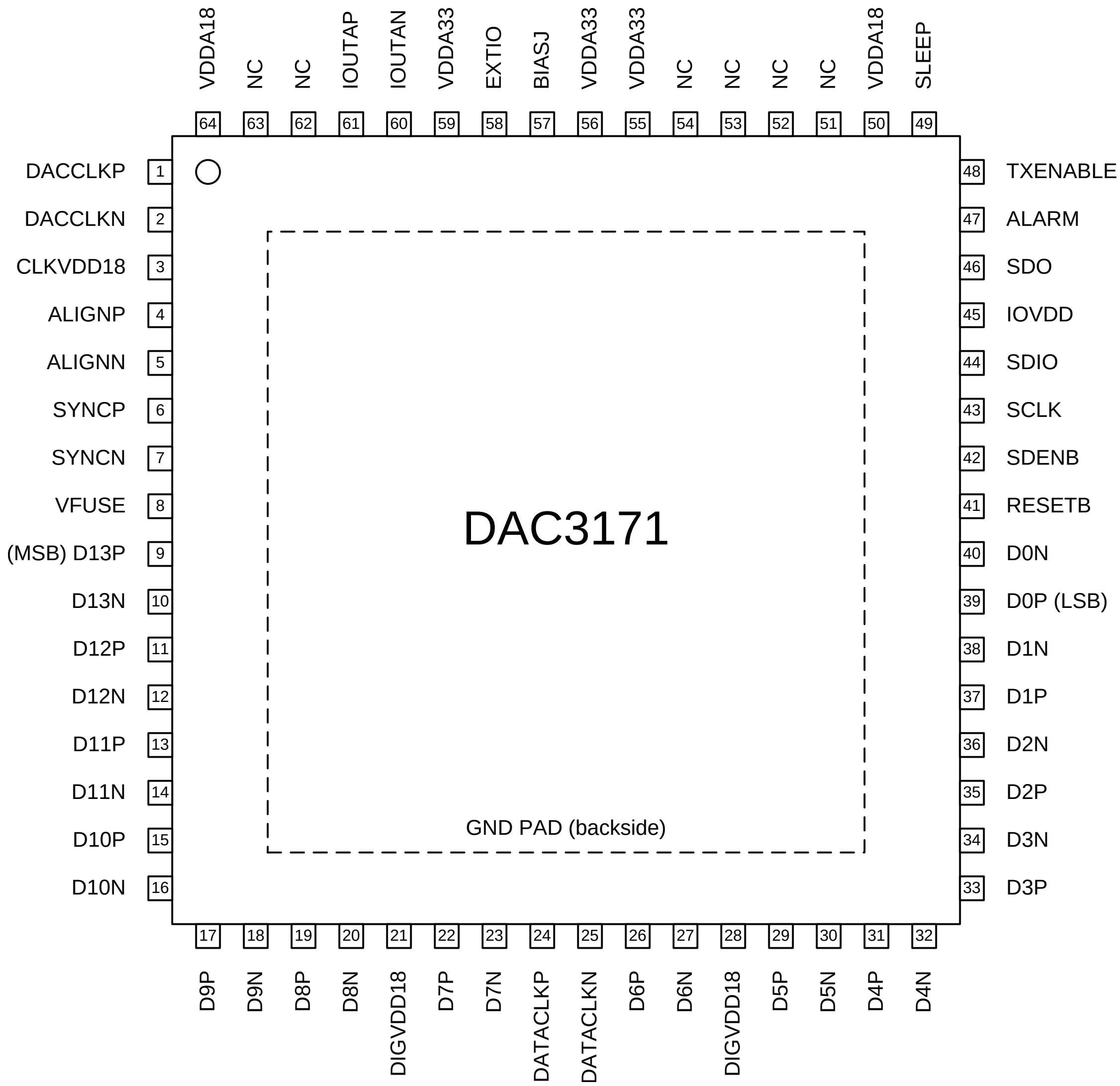
PIN ASSIGNMENT TABLE – DAC3171 7-BIT INTERFACE MODE (continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
DATA INTERFACE			
DA[6:0]P/N	9/10-19/20 22/23	I	LVDS positive input data bits for channel A. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Data format relative to DA_CLKP/N clock is Double Data Rate (DDR) with two data transfers per DA_CLKP/N clock cycle. The data format is 7 MSBs (rising edge)/7 LSBs falling edge. In the default mode (reverse bus not enabled): D6P/N is most significant data bit (MSB) D0P/N is most significant data bit (LSB)
DA_CLKP/N	6/7	I	DDR differential input data clock for channel A. Edge to center nominal timing.
OUTPUT/CLOCK			
DACCLKP/N	1/2	I	LVPECL clock input for DAC core with a self-bias of approximately CLKVDD18/2.
IOUTAP/N	61/60	O	A-Channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current source and the most positive voltage on the IOUTA1 pin. Similarly, a 0xFFFF data input results in a 0 mA current source and the least positive voltage on the IOUTA1 pin. The IOUTA2 pin is the complement of IOUTA1.
REFERENCE			
EXTIO	58	I/O	Used as external reference input when internal reference is disabled. Requires a 0.1 µF decoupling capacitor to GND when used as reference output.
BIASJ	57	O	Full-scale output current bias. For 20 mA full-scale output current, connect a 960 Ω resistor to GND.
POWER SUPPLY			
IOVDD	45		Supply voltage for CMOS IO's. 1.8V – 3.3V.
CLKVDD18	3		1.8V clock supply
DIGVDD18	21, 28		1.8V digital supply. Also supplies LVDS receivers.
VDDA18	50, 64		Analog 1.8V supply
VDDA33	55, 56, 59		Analog 3.3V supply
VFUSE	8		Digital supply voltage. (1.8V) This supply pin is also used for factory fuse programming. Connect to DVDD pins for normal operation.
NC	4,5, 24/25, 26/27 29/30-39/40, 51, 52, 53, 53, 62, 63		Not used. Pin 4 can be left open or tied to DIGVDD18, and other pins can be left open or tied to GROUND in actual application use. It is recommended to turn off pin 24/25, 26/27, 29/30-39/40 (register lvdsdataclk_ena, lvdsdata_ena) to save power.

PINOUT – DAC3171 14-BIT INTERFACE MODE



PIN ASSIGNMENT TABLE – DAC3171 14-BIT INTERFACE MODE

PIN		I/O	DESCRIPTION
NAME	NO.		
CONTROL/SERIAL			
SCLK	43	I	Serial interface clock. Internal pull-down.
SDENB	42	I	Serial interface clock. Internal pull-up.
SDIO	44	I/O	Bi-directional serial data in 3 pin mode (default). In 4-pin interface mode (register sif4_ena (config 0, bit 9)), the SDIO pin in an input only. Internal Pull-down.
SDO	46	O	Uni-directional serial interface data in 4 pin mode (register sif4_ena (config 0, bit 9)). The SDO pin is tri-stated in 3-pin interface mode (default). Internal Pulldown.
RESETB	41	I	Serial interface reset input. Active low. Initialized internal registers during high to low transition. Assynchronous. Internal pull-up.
ALARM	47	O	CMOS output for ALARM condition.
TXENABLE	48	I	Transmit enable active high input. TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data is ignored. Internal pull-down.
SLEEP	49	I	Puts device in sleep, active high. Internal pull-down.

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PIN ASSIGNMENT TABLE – DAC3171 14-BIT INTERFACE MODE (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DATA INTERFACE			
DATA[13:0]P/N	9/10-19/20 22/23 26/27, 29/30-39/40	I	LVDS input data bits for both channels. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Data format relative to DATACLKP/N clock is Double Data Rate (DDR) with two data transfers per DATACKP/N clock cycle. The data format is interleaved with channel A (rising edge) and channel B falling edge. In the default mode (reverse bus not enabled): DATA13P/N is most significant data bit (MSB) DATA0P/N is most significant data bit (LSB)
DATACLKP/N	24/25	I	DDR differential input data clock. Edge to center nominal timing. Ch A rising edge, Ch B falling edge in multiplexed output mode.
SYNCP/N	6/7	I	Reset the FIFO or to be used as a syncing source. These two functions are captured with the rising edge of DATACLKP/N. The signal captured by the falling edge of DATACLKP/N.
ALIGNP/N	4/5	I	LVPECL FIFO output syncrhonization. This positive/negative pair is captured with the rising edge of DACCLKP/N. It is used to reset the clock dividers and for multiple DAC synchronization. If unused it can be left unconnected.
OUTPUT/CLOCK			
DACCLKP/N	1/2	I	LVPECL clock input for DAC core with a self-bias of approximately CLKVDD18/2.
IOUTAP/N	61/60	O	A-Channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current source and the most positive voltage on the IOUTAP pin. Similarly, a 0xFFFF data input results in a 0 mA current source and the least positive voltage on the IOUTAP pin.
REFERENCE			
EXTIO	58	I/O	Used as external reference input when internal reference is disabled. Requires a 0.1 µF decoupling capacitor to GND when used as reference output.
BIASJ	57	O	Full-scale output current bias. For 20 mA full-scale output current, connect a 960 Ω resistor to GND.
POWER SUPPLY			
IOVDD	45	I	Supply voltage for CMOS IO's. 1.8V – 3.3V.
CLKVDD18	3	I	1.8V clock supply
DIGVDD18	21, 28	I	1.8V digital supply. Also supplies LVDS receivers.
VDDA18	50, 64	I	Analog 1.8V supply
VDDA33	55, 56, 59	I	Analog 3.3V supply
VFUSE	8	I	Digital supply voltage. (1.8V) This supply pin is also used for factory fuse programming. Connect to DVDD pins for normal operation.
NC	51, 52, 53, 54 62, 63		Not Used. These pins can be left open or tied to GROUND in actual application use.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN	LEAD/BALL FINISH	ODERING NUMBER	TRANSPORT MEDIA	QUANTITY
DAC3151	QFN-64	RGC	–40°C to 85°C	GREEN (RoHS and no Sb/Br)	NiPdAu	DAC3151IRGCT	Tape and Reel	250
						DAC3151IRGCR		2000
DAC3161						DAC3161IRGCT		250
						DAC3161IRGCR		2000
DAC3171						DAC3171IRGCT		250
						DAC3171IRGCR		2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage	VDDA33 to GND	–0.5 to 4	V
	VDDA18 to GND	–0.5 to 2.3	
	CLKVDD18 to GND	–0.5 to 2.3	
	IOVDD to GND	–0.5 to 4	
	DIGVDD18 to GND	–0.5 to 2.3	
Terminal voltage range	CLKVDD18 to DIGVDD18	–0.5 to 0.5	V
	VDDA18 to DIGVDD18	–0.5 to 0.5	
	DA[6..0]P, DA[6..0]N, D[13..0]P, D[13..0]N, DATACLKP, DATACLKN, DA_CLKP, DA_CLKPN, SYNCP, SYNCN to GND	–0.5 to DIGVDD18 + 0.5	
	DACCLKP, DACCLKN, ALIGNP, ALIGNN	–0.5 to CLKVDD18 + 0.5	
	TXENABLE, ALARM, SDO, SDIO, SCLK, SDENB, RESETB to GND	–0.5 to IOVDD + 0.5	
	IOUTAP, IOUTAN to GND	–0.7 to 1.4	
	EXTIO, BIASJ to GND	–0.5 to VDDA33 + 0.5	
Storage temperature range		–65 to 150	°C
ESD, Human Body Model		2	kV

THERMAL INFORMATION

THERMAL METRIC(1)		DAC3151, DAC3161, DAC3171	UNITS
		QFN (64 PIN)	
θ_{JA}	Junction-to-ambient thermal resistance	23.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	7.6	
θ_{JB}	Junction-to-board thermal resistance	2.8	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	2.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS – DC SPECIFICATIONS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sample rate = 500MSPS, 50% clock duty cycle, VDDA33/IOVDD = 3.3V, VDDA18/CLKVDD18/DIGVDD18 = 1.8V, $IOUT_{FS}$ = 20mA (unless otherwise noted).

PARAMETER	TEST CONDITIONS	DAC3151			DAC3161			DAC3171			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		10			12			14			Bits
DC ACCURACY											
DNL Differential nonlinearity	1 LSB = $IOUT_{FS}/2^{14}$		±0.04			±0.2			±1		LSB
INL Integral nonlinearity			±0.15			±0.5			±2		
ANALOG OUTPUTS											
Coarse gain linearity			±0.4			±0.4			±0.4		LSB
Offset error	Mid code offset		0.01			0.01			0.01		%FSR
Gain error	With external reference		±2			±2			±2		%FSR
	With internal reference		±2			±2			±2		
Gain mismatch	With internal reference	-2		2	-2		2	-2		2	%FSR
Minimum full scale output current	Nominal full-scale current, $IOUT_{FS}$ = 16xIBAIS current		2			2			2		mA
Maximum full scale output current			20			20			20		
Output compliance range	IOUTFS = 20 mA	-0.5		1	-0.5		1	-0.5		1	V
Output resistance			300			300			300		kΩ
Output capacitance				5			5		5		pF
REFERENCE OUTPUT											
V_{REF} Reference output voltage		1.14	1.2	1.26	1.14	1.2	1.26	1.14	1.2	1.26	V
Reference output current			100			100			100		nA
REFERENCE INPUT											
VEXTIO Input voltage range	External reference mode	0.1	1.2	1.25	0.1	1.2	1.25	0.1	1.2	1.25	V
Input resistance			1			1			1		MΩ
Small signal bandwidth			500			500			500		kHz
Input capacitance			100			100			100		pF
TEMPERATURE COEFFICIENTS											
Offset drift			±1			±1			±1		ppm of FSR /°C
Gain drift	With external reference		±15			±15			±15		ppm /°C
	With internal reference		±30			±30			±30		ppm /°C
Reference voltage drift			±8			±8			±8		ppm /°C
POWER SUPPLY											
DIGVDD18, VFUSE, VDDA18, CLKVDD18		1.71	1.8	1.89	1.71	1.8	1.89	1.71	1.8	1.89	V
VDDA33		3.15	3.3	3.45	3.15	3.3	3.45	3.15	3.3	3.45	V
IOVDD	Sets CMOS IO voltage levels. Nominal 1.8V, 2.5V or 3.3V	1.71		3.45	1.71		3.45	1.71		3.45	V

ELECTRICAL CHARACTERISTICS – DC SPECIFICATIONS (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sample rate = 500MSPS, 50% clock duty cycle, VDDA33/IOVDD = 3.3V, VDDA18/CLKVDD18/DIGVDD18 = 1.8V, $IOUT_{FS}$ = 20mA (unless otherwise noted).

PARAMETER		TEST CONDITIONS	DAC3151			DAC3161			DAC3171			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER CONSUMPTION												
I_{VDDA33}	3.3V Analog supply current	MODE 1 f_{DAC} = 491.52 MSPS, QMC on, IF = 20 MHz, Input full word width		28			28			28	35	mA
$I_{CLKVDD18}$	1.8V Clock supply current			47			47			47	56	mA
$I_{DIGVDD18}$	1.8V Digital supply current (DIGVDD18 and VFUSE)			110			110			110	125	mA
I_{IOVDD}	1.8V IO Supply current			0.002			0.002			0.002	0.015	mA
P_{dis}	Total power dissipation			375			375			375	442	mW
I_{VDDA33}	3.3V Analog supply current	MODE 2 f_{DAC} = 320 MSPS, QMC on, IF = 20 MHz, Input full word width		28			28			28		mA
$I_{CLKVDD18}$	1.8V Clock supply current			37			37			37		mA
$I_{DIGVDD18}$	1.8V Digital supply current (DIGVDD18 and VFUSE)			80			80			80		mA
I_{IOVDD}	1.8V IO Supply current			0.002			0.002			0.002		mA
P_{dis}	Total power dissipation			303			303			303		mW
I_{VDDA33}	3.3V Analog supply current	MODE 3 Sleep mode, f_{DAC} = 491.52 MSPS, DAC in sleep mode, Input full word width		2.6			2.6			2.6		mA
$I_{CLKVDD18}$	1.8V Clock supply current			43			43			43		mA
$I_{DIGVDD18}$	1.8V Digital supply current (DIGVDD18 and VFUSE)			106			106			106		mA
I_{IOVDD}	1.8V IO Supply current			0.003			0.003			0.003		mA
P_{dis}	Total power dissipation			277			277			277		mW
I_{VDDA33}	3.3V Analog supply current	MODE 4 Power-down mode, no clock, DAC in sleep mode, Input full word width		1.6	4		1.6	4		1.6	4	mA
$I_{CLKVDD18}$	1.8V Clock supply current			1.8	4		1.8	4		1.8	4	mA
$I_{DIGVDD18}$	1.8V Digital supply current (DIGVDD18 and VFUSE)			0.7	3		0.7	3		0.7	3	mA
I_{IOVDD}	1.8V IO Supply current			0.003	0.015		0.003	0.015		0.003	0.015	mA
P_{dis}	Total power dissipation			10	26		10	26		10	26	mW
PSRR	Power supply rejection ratio	DC tested	–0.4		0.4	–0.4		0.4	–0.4		0.4	%/FSR/V
T	Operating temperature		–40		85	–40		85	–40		85	°C

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ELECTRICAL CHARACTERISTICS – AC SPECIFICATIONS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sample rate = 500MSPS, 50% clock duty cycle, VDDA33/IOVDD = 3.3V, VDDA18/CLKVDD18/DIGVDD18 = 1.8V, $IOUT_{FS}$ = 20mA (unless otherwise noted).

PARAMETER		TEST CONDITIONS	DAC3151			DAC3161			DAC3171			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUT												
f_{DAC}	Maximum sample rate		500			500			500			MSPS
$t_{s(DAC)}$	Output settling time to 0.1%	Transition: Code 0x0000 to 0x3FFF		11			11			11		ns
t_{PD}	Output propagation delay	Does not include digital latency		2			2			2		ns
$t_{r(IOUT)}$	Output rise time 10% to 90%			200			200			200		ps
$t_{f(IOUT)}$	Output fall time 90% to 10%			200			200			200		ps
	Digital Latency	Length of delay from DAC pin inputs to DATA at output pins. In normal operation mode including the latency of FIFO.		26			26			26		µs
AC PERFORMANCE												
SFDR	Spurious free dynamic range	f_{DAC} = 500 MSPS, f_{out} = 10.1 MHz		81			82			82		dBc
		f_{DAC} = 500 MSPS, f_{out} = 20.1 MHz		76			77			78		
		f_{DAC} = 500 MSPS, f_{out} = 70.1 MHz		69			70			74		
IMD3	Intermodulation distortion	f_{DAC} = 500 MSPS, f_{out} = 10.1 ±0.5 MHz		82			83			84		dBc
		f_{DAC} = 500 MSPS, f_{out} = 20.1 ±0.5 MHz		81			82			84		
		f_{DAC} = 500 MSPS, f_{out} = 70.1 ±0.5 MHz		73.5			74			75		
		f_{DAC} = 500 MSPS, f_{out} = 150.1 ±0.5 MHz		61			61			63		
NSD	Noise spectral density	f_{DAC} = 500 MSPS, f_{out} = 10.1 MHz		147			158			160		dBc/Hz
		f_{DAC} = 500 MSPS, f_{out} = 20.1 MHz		146			156			157		
		f_{DAC} = 500 MSPS, f_{out} = 70.1 MHz		146			153			155		
ACLR	Adjacent channel leakage ratio	f_{DAC} = 491.52 MSPS, f_{out} = 30.72 MHz, WCDMA TM1		69			77			78		dBc
		f_{AC} = 491.52 MSPS, f_{out} = 153.6 MHz, WCDMA TM1		68			73			74		

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ELECTRICAL CHARACTERISTICS – DIGITAL SPECIFICATIONS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sample rate = 500MSPS, 50% clock duty cycle, VDDA33/IOVDD = 3.3V, VDDA18/CLKVDD18/DIGVDD18 = 1.8V, $IOUT_{FS}$ = 20mA (unless otherwise noted).

PARAMETER		TEST CONDITIONS	DAC3151			DAC3161			DAC3171			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CMOS DIGITAL INPUTS (RESETB, SDENB, SCLK, SDIO, TXENABLE)												
V_{IH}	High-level input voltage	IOVDD = 3.3 V, 2.5 V or 1.8 V	0.6× IOVDD			0.6× IOVDD			0.6× IOVDD			V
V_{IL}	Low-level input voltage				0.25× IOVDD			0.25× IOVDD			0.25× IOVDD	V
I_{IH}	High-level input current		-40		40				–40		40	μA
I_{IL}	Low-level input current		-40		40				–40		40	μA
DIGITAL OUTPUTS – CMOS INTERFACE (SDOUT, SDIO)												
V_{OH}	High-level output voltage	IOVDD = 3.3 V, 2.5 V, 1.8 V	0.85× IOVDD			0.85× IOVDD			0.85× IOVDD			V
V_{OL}	Low-level output voltage				0.125× IOVDD			0.125× IOVDD			0.125× IOVDD	V
SERIAL PORT TIMING												
$t_{s(SENDB)}$	Setup time, SDENB to rising edge of SCLK		20			20			20			ns
$t_{s(SDIO)}$	Setup time, SDIO to rising edge of SCLK		10			10			10			ns
$t_{h(SDIO)}$	Hold time, SDIO from rising edge of SCLK		5			5			5			ns
$t_{(SCLK)}$	Period of SCLK		100			100			100			ns
$t_{(SCLKH)}$	High time of SCLK		40			40			40			ns
$t_{(SCLKL)}$	Low time of SCLK		40			40			40			ns
$t_{d(DATA)}$	Data output delay after falling edge of SCLK			10			10			10		ns
T_{RESET}	Minimum RESTB pulsewidth			25			25			25		ns
LVDS INTERFACE (D[x..0]P/N, DA[x..0]P/N , DB[x..0]P/N , DA_CLKP/N, DB_CLKP/N, DATACLKP/N, SYNCP/N, ALIGNP/N)												
$V_{A,B+}$	Logic high differential input voltage threshold		175			175			175			mV
$V_{A,B–}$	Logic low differential input voltage threshold				–175			–175			–175	mV
V_{COM}	Input Common Mode Range		1.0	1.2	2.0	1.0	1.2	2.0	1.0	1.2	2.0	V
Z_T	Internal termination		85	110	135	85	110	135	85	110	135	Ω
C_L	LVDS input capacitance			2			2			2		pF

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ELECTRICAL CHARACTERISTICS – DIGITAL SPECIFICATIONS (continued)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, DAC sample rate = 500MSPS, 50% clock duty cycle, VDDA33/IOVDD = 3.3V, VDDA18/CLKVDD18/DIGVDD18 = 1.8V, $IOUT_{FS}$ = 20mA (unless otherwise noted).

PARAMETER			TEST CONDITIONS		DAC3151			DAC3161			DAC3171			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
LVDS INPUT TIMING														
$t_{s(DATA)}$	Setup time	D[x..0] valid to DATACLK rising or falling edge for single bus single clock mode ; DA/DB[x…0] valid to DB_CLK rising or falling edge for dual bus single clock mode; DA[x..0] valid to DA_CLK rising or falling edge, and DB[x…0] valid for DB_CLK rising or falling edge for dual bus dual clock mode	config3 Setting											ps
			datadly	clkdly										
			0	0		-20			-20			-20		
			0	1		-120			-120			-120		
			0	2		-220			-220			-220		
			0	3		-310			-310			-310		
			0	4		-390			-390			-390		
			0	5		-480			-480			-480		
			0	6		-560			-560			-560		
			0	7		-630			-630			-630		
			1	0		70			70			70		
			2	0		150			150			150		
			3	0		230			230			230		
			4	0		330			330			330		
			5	0		430			430			430		
			6	0		530			530			530		
			7	0		620			620			620		
$t_{h(DATA)}$	Hold time	D[x..0] valid to DATACLK rising or falling edge for single bus single clock mode; DA/DB[x…0] valid to DB_CLK rising or falling edge for dual bus single clock mode; DA[x..0] valid to DA_CLK rising or falling edge, and DB[x…0] valid for DB_CLK rising or falling edge for dual bus dual clock mode.	congfig3 Setting											ps
			datadly	clkdly										
			0	0		310			310			310		
			0	1		390			390			390		
			0	2		480			480			480		
			0	3		560			560			560		
			0	4		650			650			650		
			0	5		740			740			740		
			0	6		850			850			850		
			0	7		930			930			930		
			1	0		200			200			200		
			2	0		100			100			100		
			3	0		20			20			20		
			4	0		-60			-60			-60		
			5	0		-140			-140			-140		
			6	0		-220			-220			-220		
			7	0		-290			-290			-290		

TYPICAL CHARACTERISTICS

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

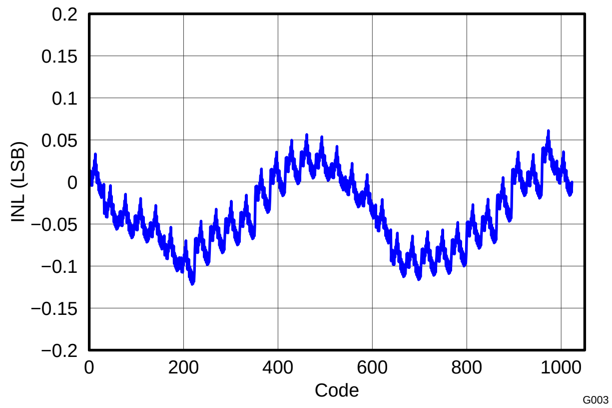

Figure 5. DAC3151 Integral Nonlinearity

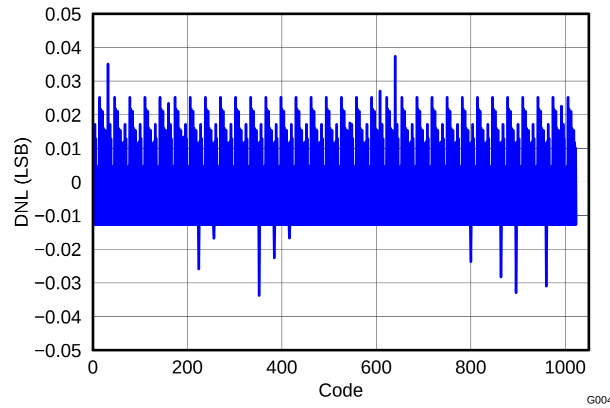

Figure 6. DAC3151 Differential Nonlinearity

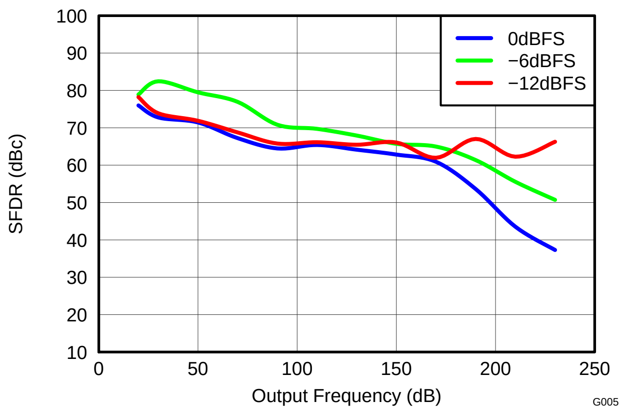

Figure 7. DAC3151 SFDR vs Output Frequency Over Input Scale

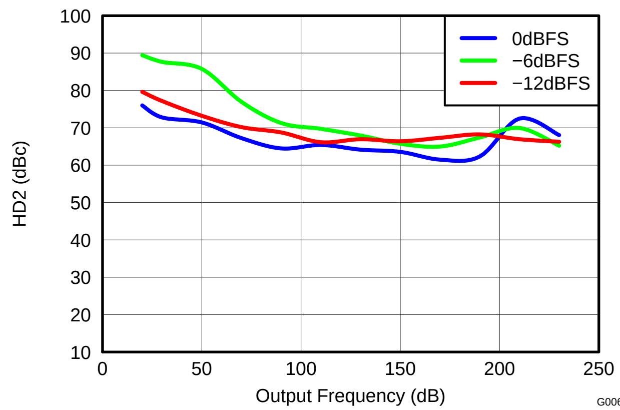

Figure 8. DAC3151 Second-Order Harmonic Distortion vs Output Frequency Over Input Scale

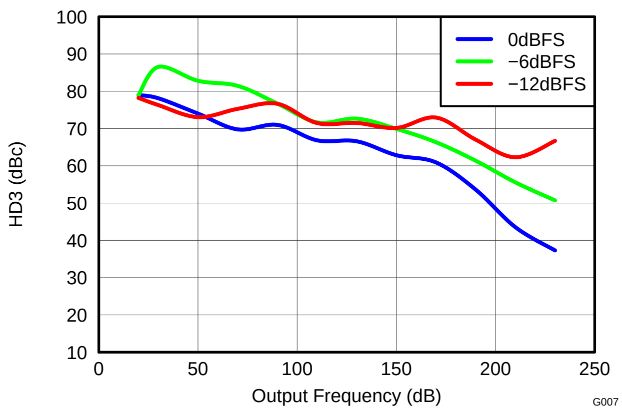

Figure 9. DAC3151 Third-Order Harmonic Distortion vs Output Frequency Over Input Scale

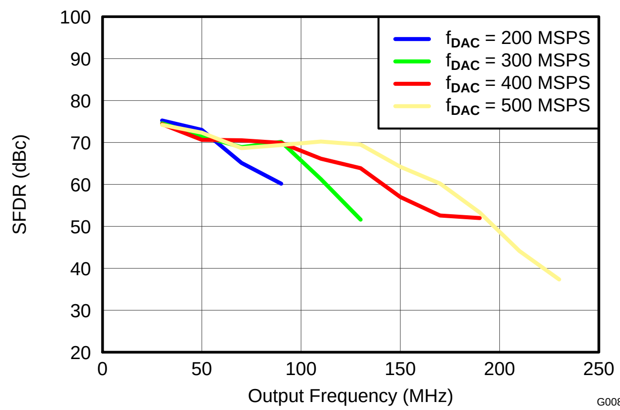

Figure 10. DAC3151 SFDR vs Output Frequency Over f_{DAC}

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TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

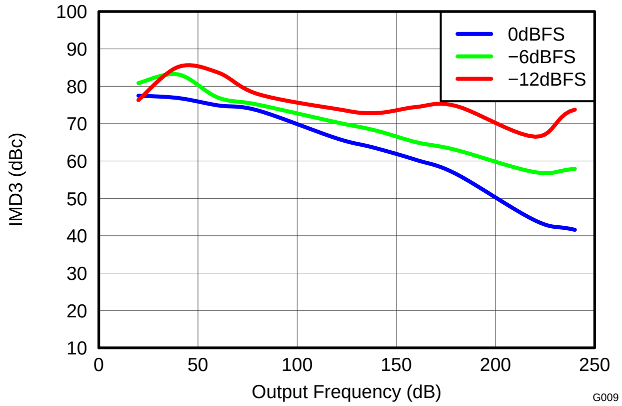

Figure 11. DAC3151 IMD3 vs Output Frequency Over Input Scale

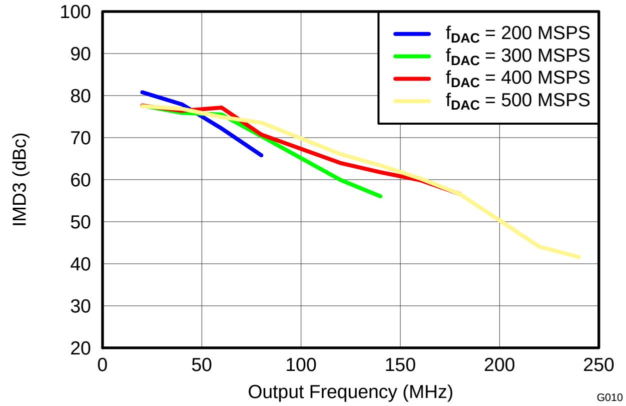

Figure 12. DAC3151 IMD3 vs Output Frequency Over f_{DAC}

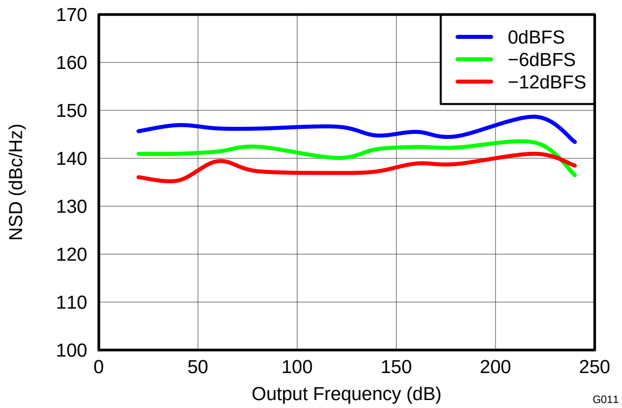

Figure 13. DAC3151 NSD vs Output Frequency Over Input Scale

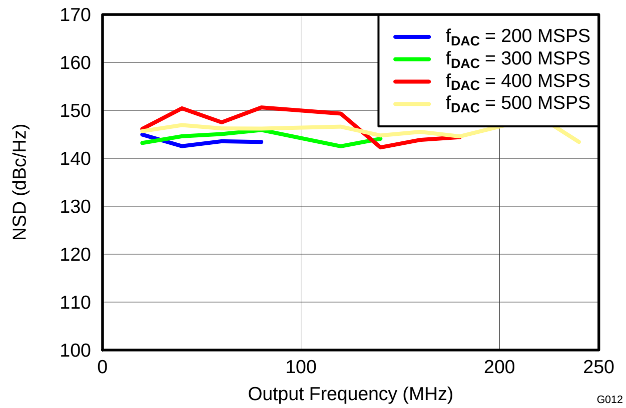

Figure 14. DAC3151 NSD vs Output Frequency Over f_{DAC}

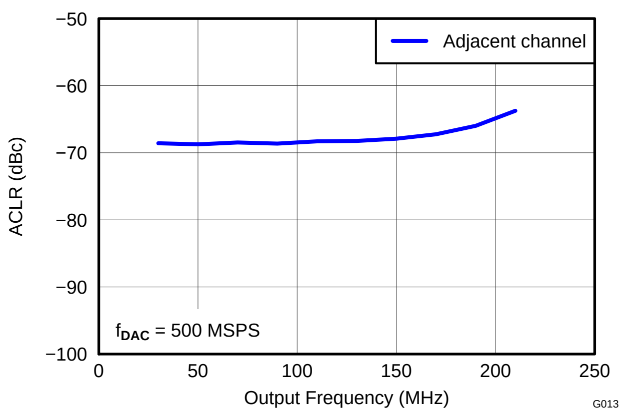

Figure 15. DAC3151 ACLR (Adjacent Channel) vs Output Frequency

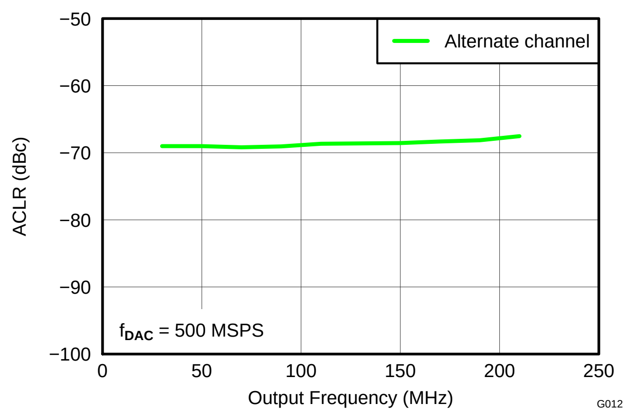

Figure 16. DAC3151 ACLR (Alternate Channel) vs Output Frequency

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

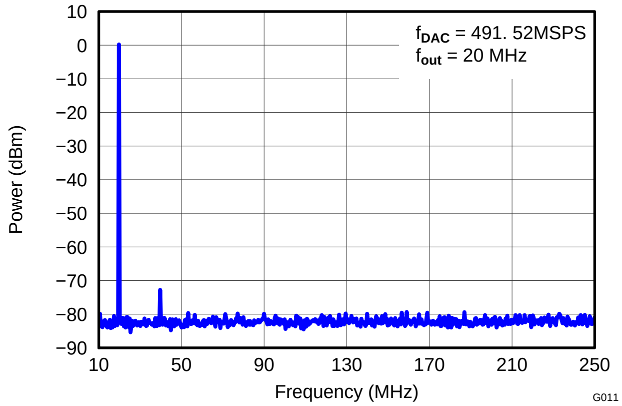

Figure 17. DAC3151 Single-Tone Spectral Plot (IF = 20MHz)

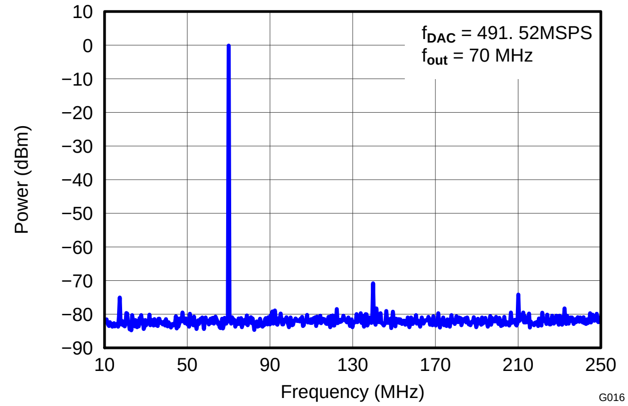

Figure 18. DAC3151 Single-Tone Spectral Plot (IF = 70MHz)

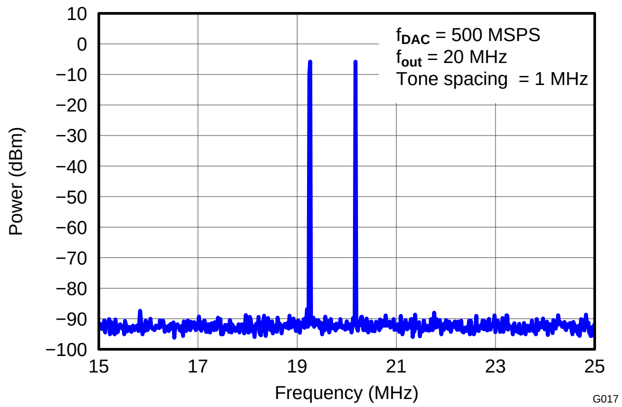

Figure 19. DAC3151 Two-Tone Spectral Plot (IF = 20MHz)

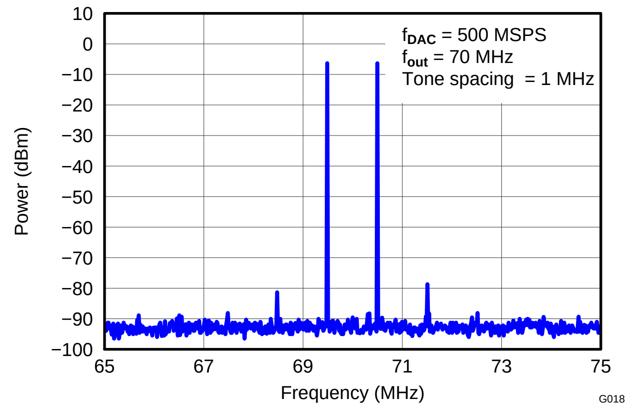

Figure 20. DAC3151 Two-Tone Spectral Plot (IF = 70MHz)

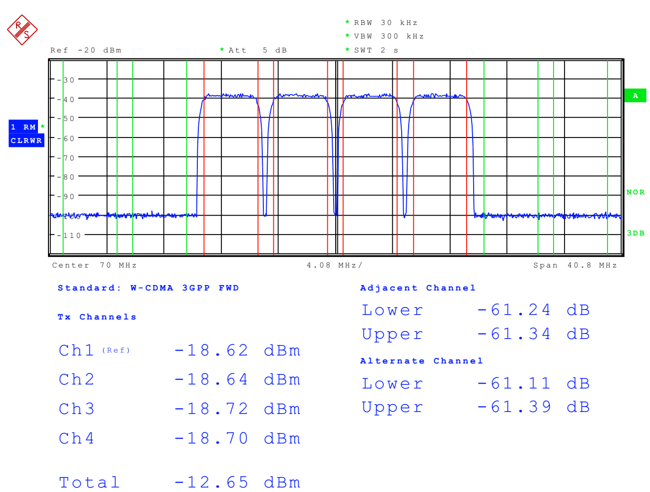

Figure 21. DAC3151 ACPR Four-Carrier WCDMA Test Mode 1

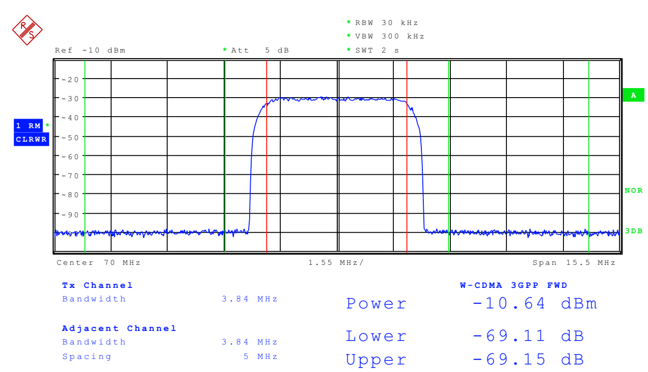

Figure 22. DAC3151 ACPR Single-Carrier WCDMA Test Mode 1

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TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

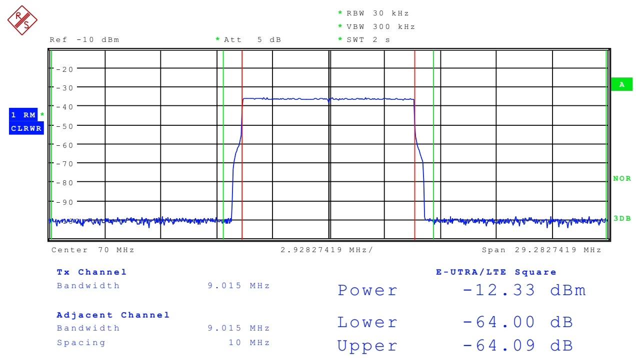

Figure 23. DAC3151 ACPR LTE 10-MHz FDD E-TM 1.1

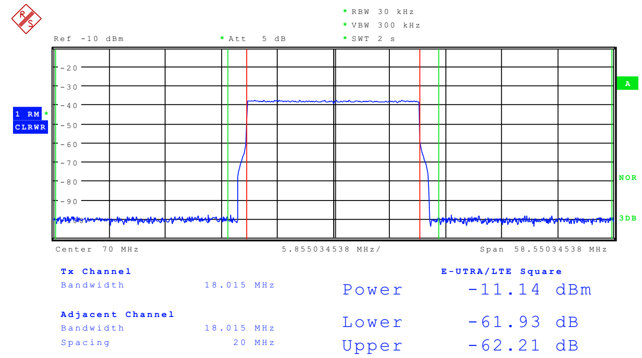

Figure 24. DAC3151 ACPR LTE 20-MHz FDD E-TM 1.1

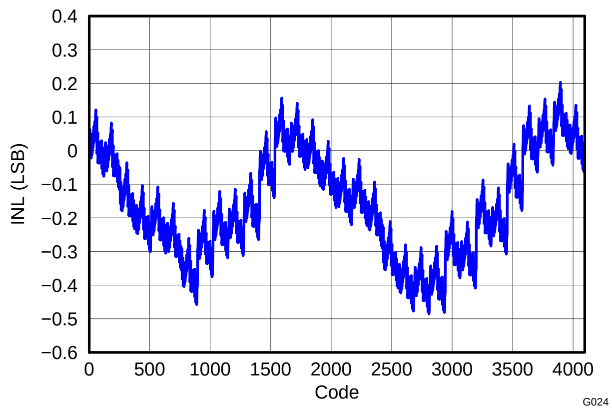

Figure 25. DAC3161 Integral Nonlinearity

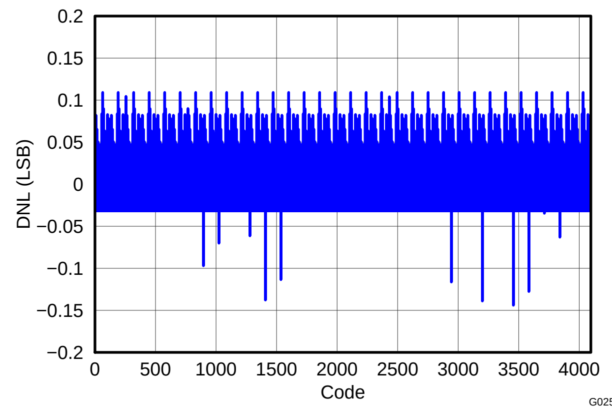

Figure 26. DAC3161 Differential Nonlinearity

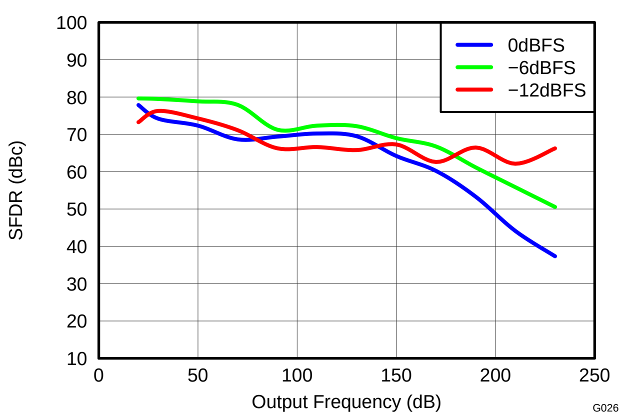

Figure 27. DAC3161 SFDR vs Output Frequency Over Input Scale

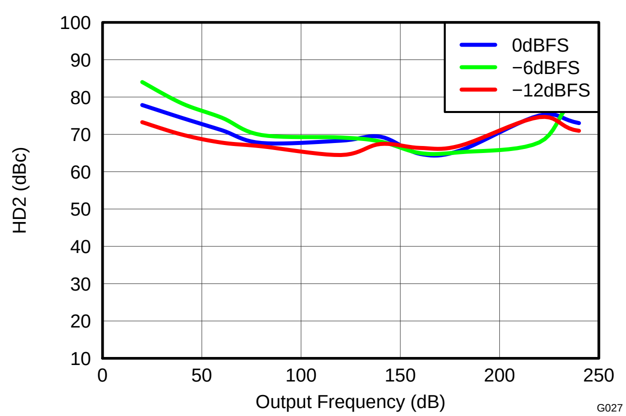

Figure 28. DAC3161 Second-Order Harmonic Distortion vs Output Frequency Over Input Scale

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

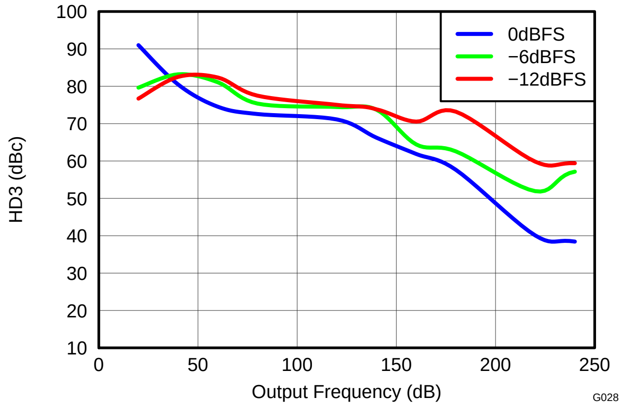

Figure 29. DAC3161 Third-Order Harmonic Distortion vs Output Frequency Over Input Scale

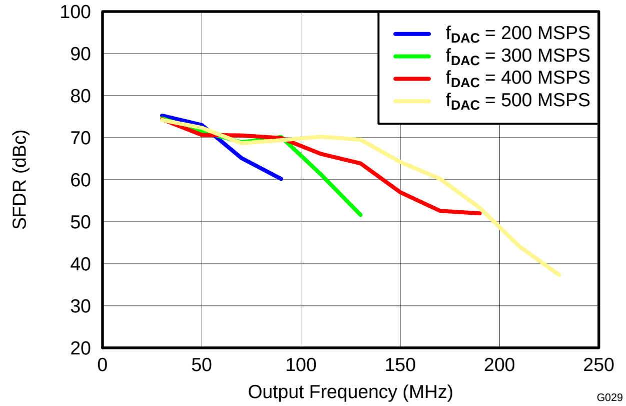

Figure 30. DAC3161 SFDR vs Output Frequency Over f_{DAC}

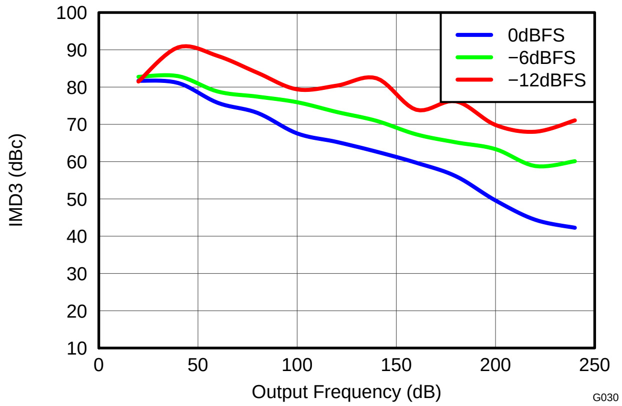

Figure 31. DAC3161 IMD3 vs Output Frequency Over Input Scale

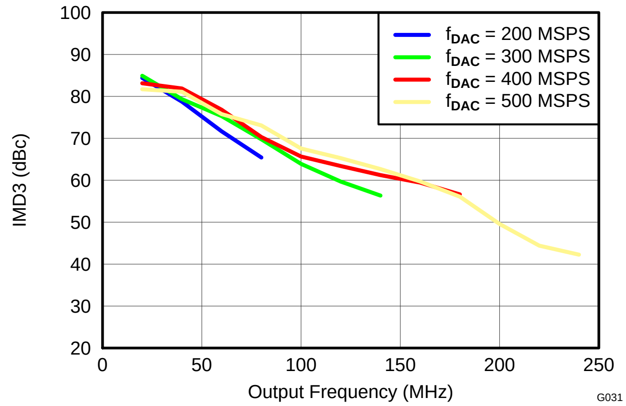

Figure 32. DAC3161 IMD3 vs Output Frequency Over f_{DAC}

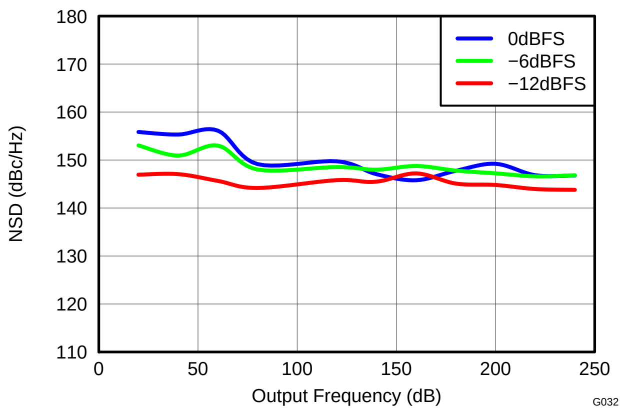

Figure 33. DAC3161 NSD vs Output Frequency Over Input Scale

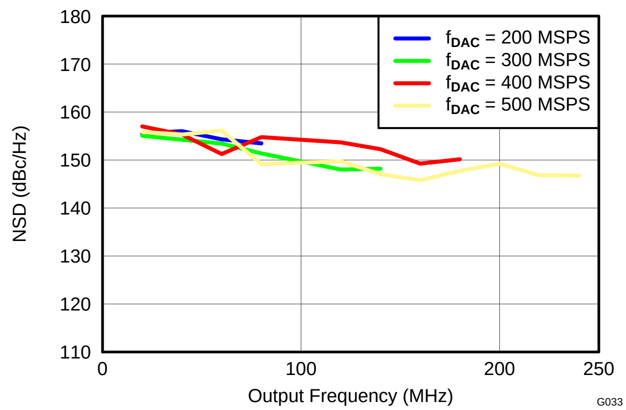

Figure 34. DAC3161 NSD vs Output Frequency Over f_{DAC}

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TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

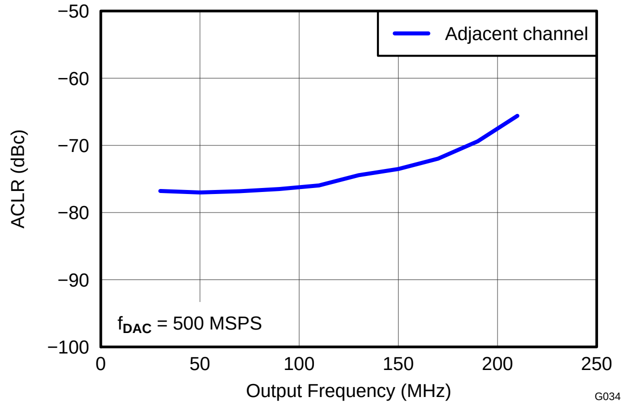

Figure 35. DAC3161 ACLR (Adjacent Channel) vs Output Frequency

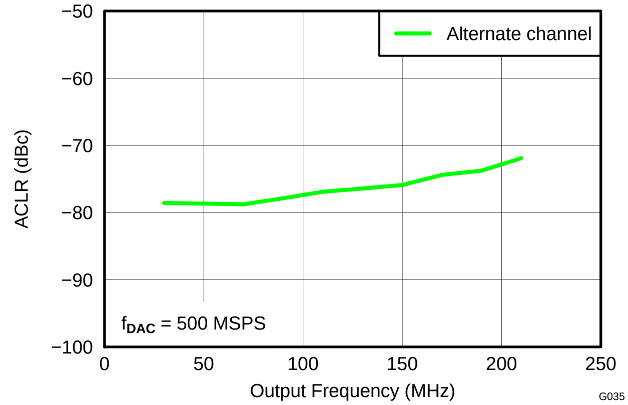

Figure 36. DAC3161 ACLR (Alternate Channel) vs Output Frequency

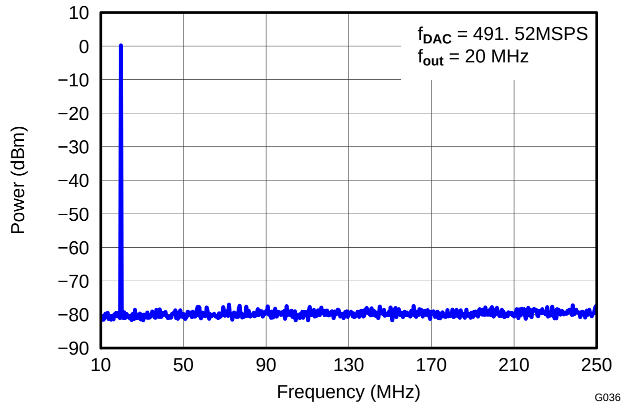

Figure 37. DAC3161 Single-Tone Spectral Plot (IF = 20MHz)

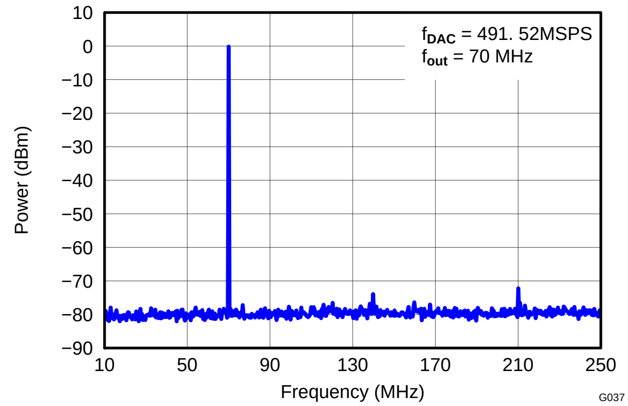

Figure 38. DAC3161 Single-Tone Spectral Plot (IF = 70MHz)

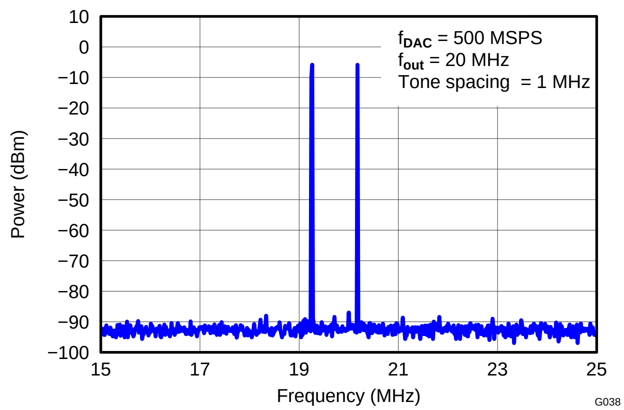

Figure 39. DAC3161 Two-Tone Spectral Plot (IF = 20MHz)

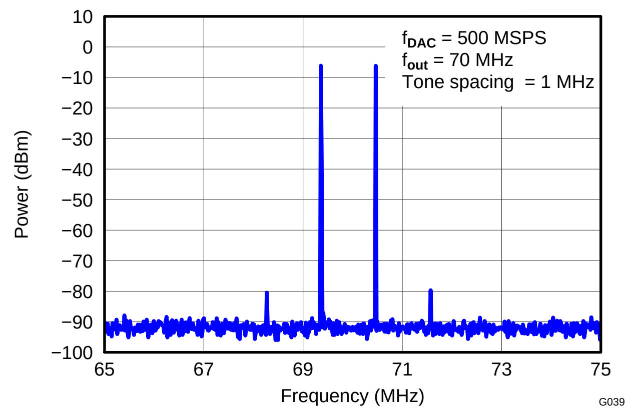

Figure 40. DAC3161 Two-Tone Spectral Plot (IF = 70MHz)

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TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

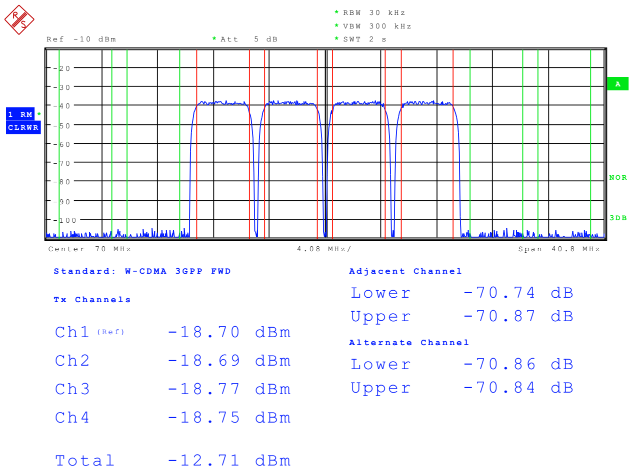

Figure 41. DAC3161 ACPR Four-Carrier WCDMA Test Mode 1

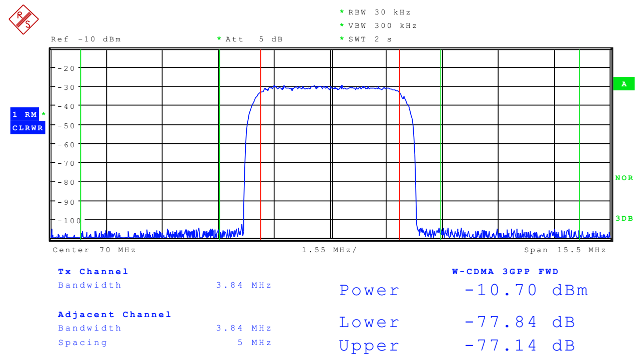

Figure 42. DAC3161 ACPR Single-Carrier WCDMA Test Mode 1

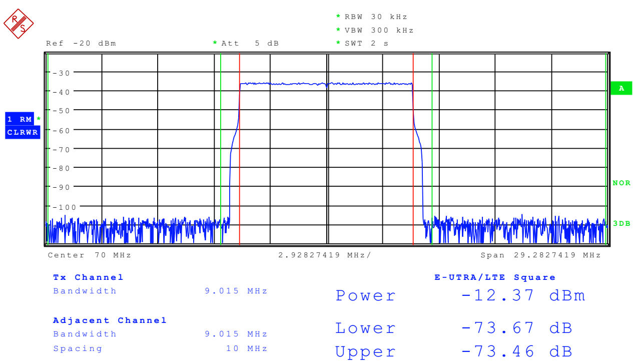

Figure 43. DAC3161 ACPR LTE 10-MHz FDD E-TM 1.1

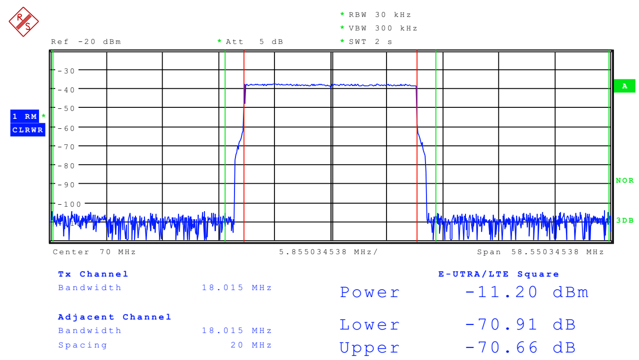

Figure 44. DAC3161 ACPR LTE 20-MHz FDD E-TM 1.1

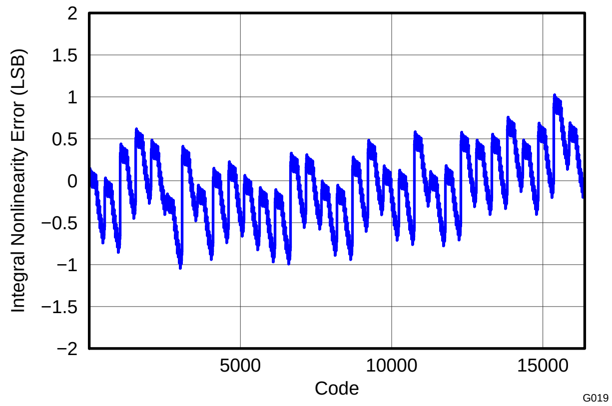

Figure 45. DAC3171 Integral Nonlinearity

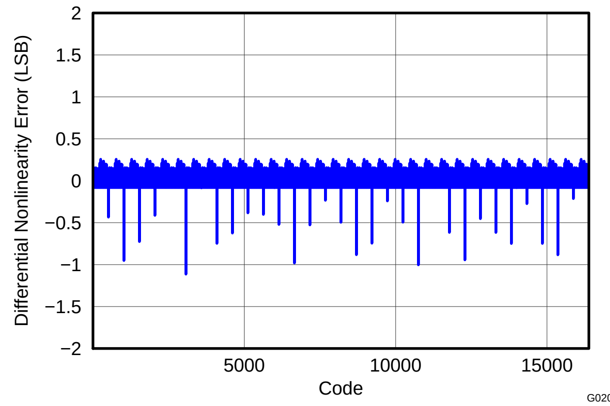

Figure 46. DAC3171 Differential Nonlinearity

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TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

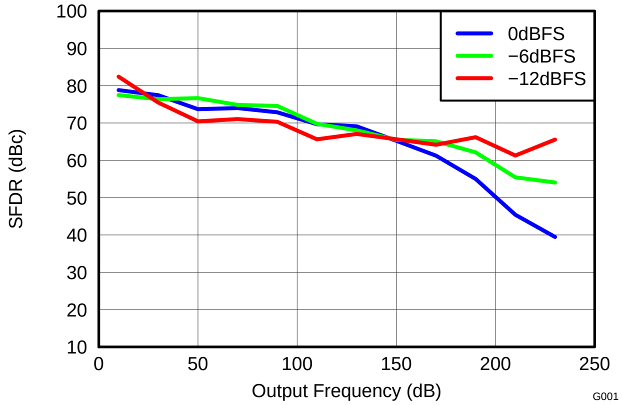

Figure 47. DAC3171 SFDR vs Output Frequency Over Input Scale

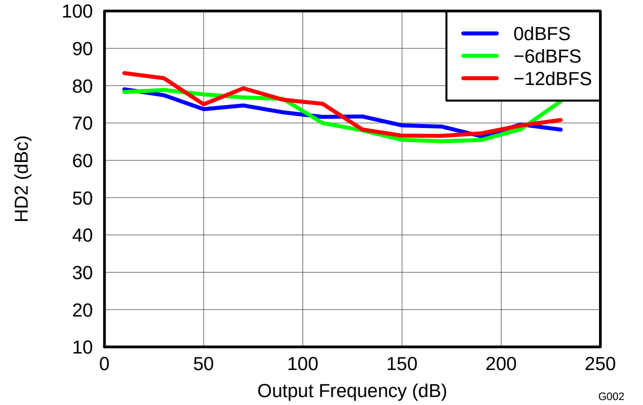

Figure 48. DAC3171 Second-Order Harmonic Distortion vs Output Frequency Over Input Scale

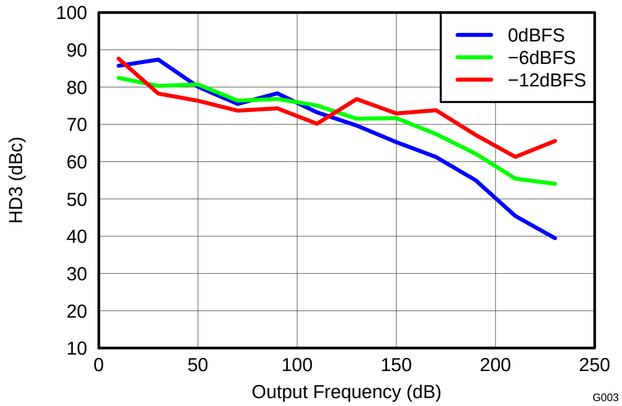

Figure 49. DAC3171 Third-Order Harmonic Distortion vs Output Frequency Over Input Scale

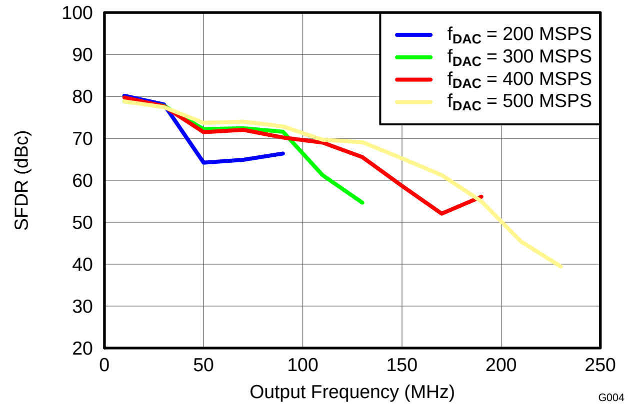

Figure 50. DAC3171 SFDR vs Output Frequency Over f_{DAC}

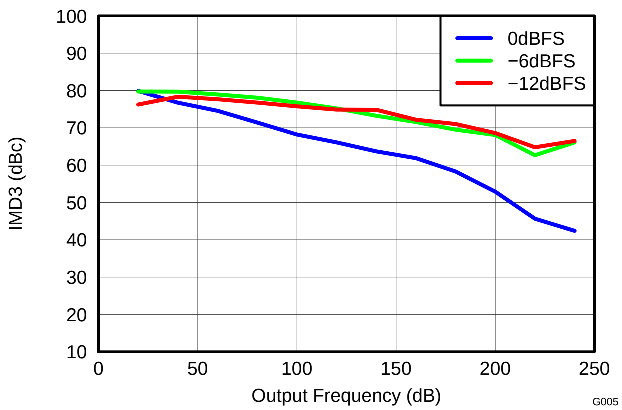

Figure 51. DAC3171 IMD3 vs Output Frequency Over Input Scale

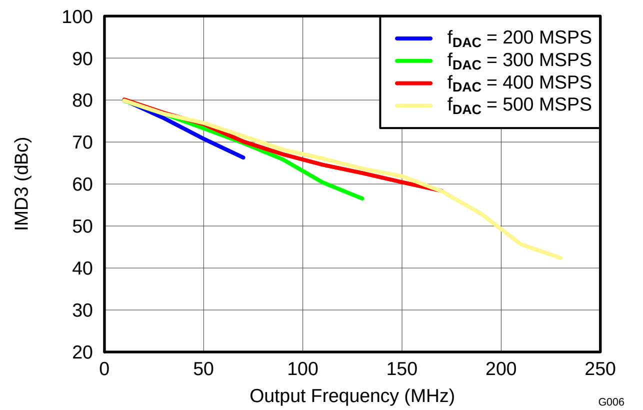

Figure 52. DAC3171 IMD3 vs Output Frequency Over f_{DAC}

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

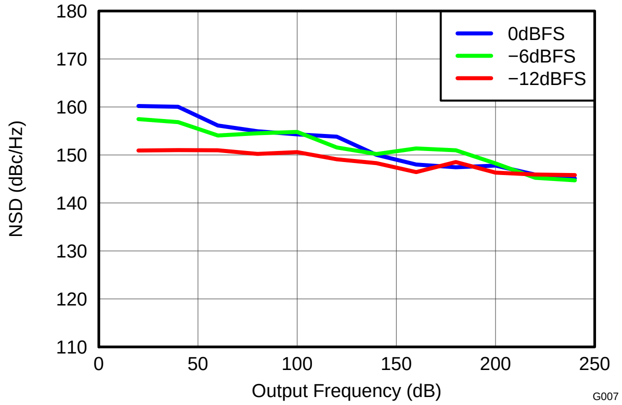

Figure 53. DAC3171 NSD vs Output Frequency Over Input Scale

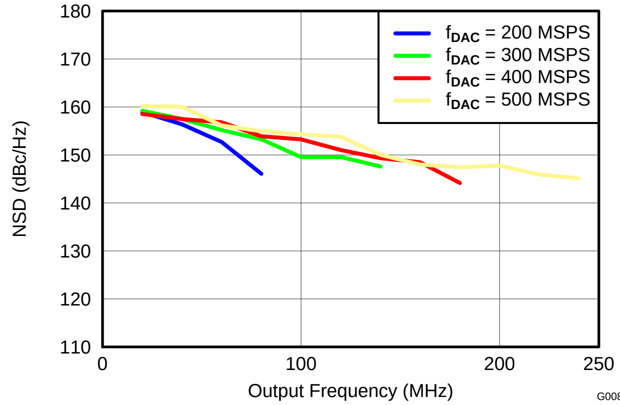

Figure 54. DAC3171 NSD vs Output Frequency Over f_{DAC}

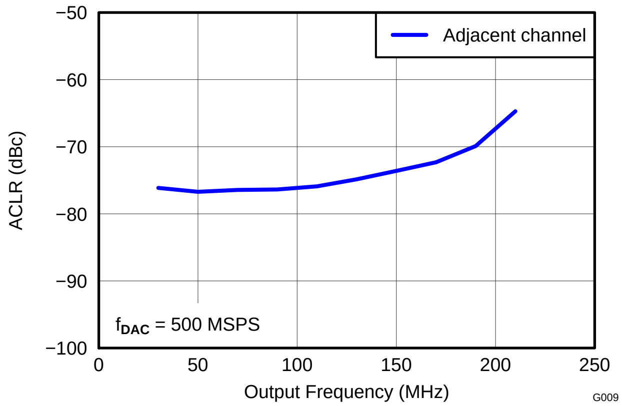

Figure 55. DAC3171 ACLR (Adjacent Channel) vs Output Frequency

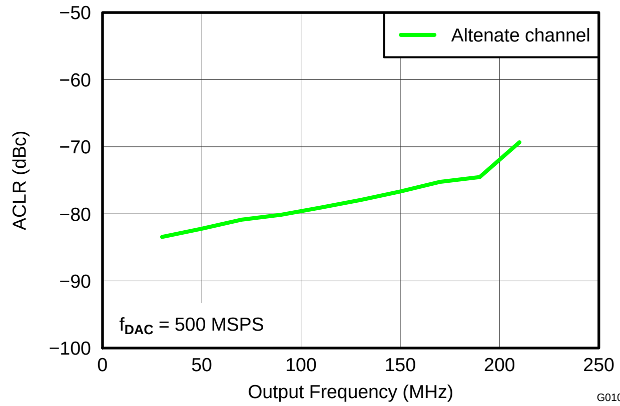

Figure 56. DAC3171 ACLR (Alternate Channel) vs Output Frequency

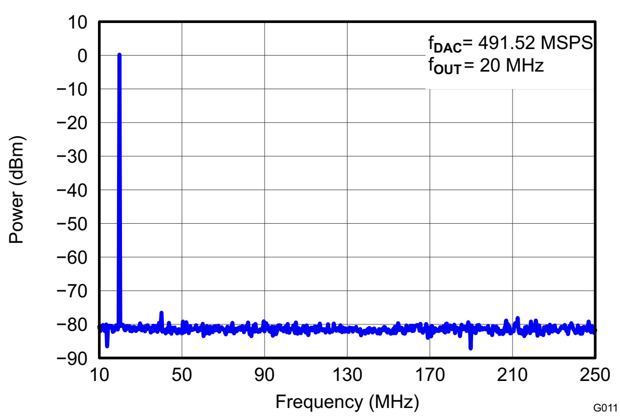

Figure 57. DAC3171 Single-Tone Spectral Plot (IF = 20MHz)

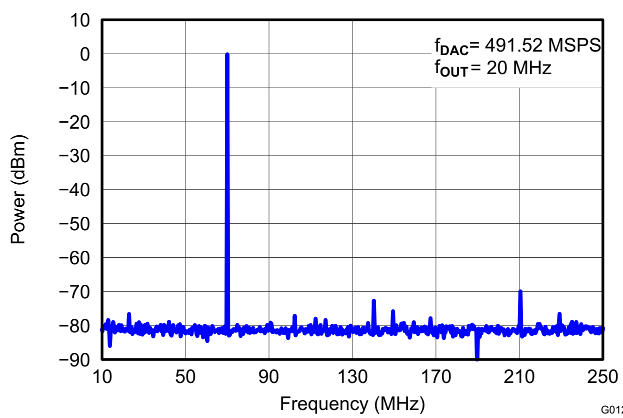

Figure 58. DAC3171 Single-Tone Spectral Plot (IF = 70MHz)

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TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

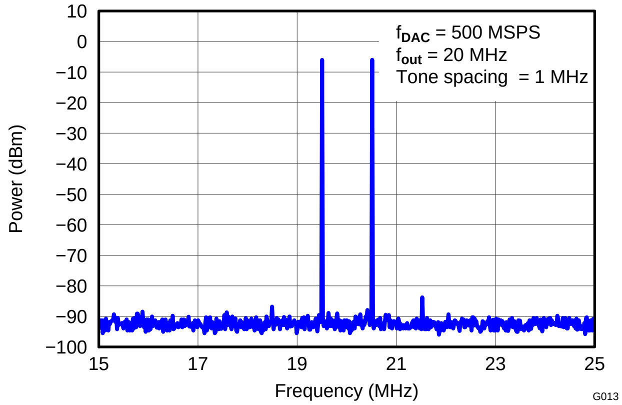

Figure 59. DAC3171 Two-Tone Spectral Plot (IF = 20MHz)

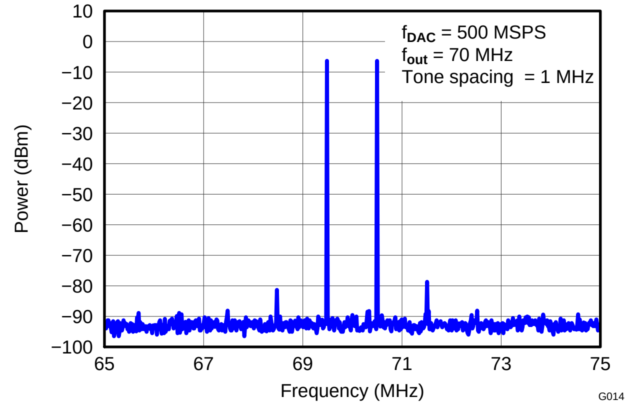

Figure 60. DAC3171 Two-Tone Spectral Plot (IF = 70MHz)

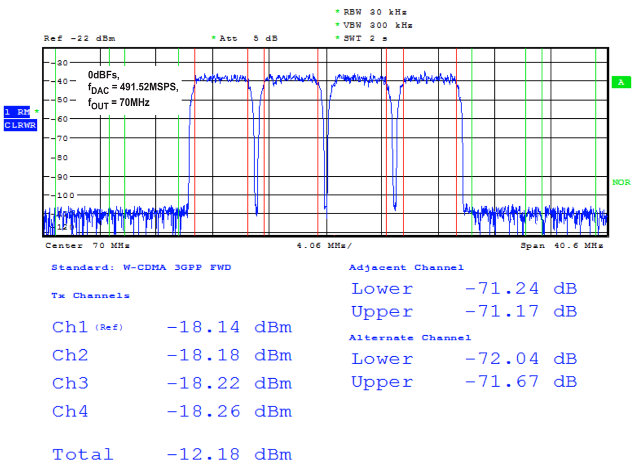

Figure 61. DAC3171 Four-Carrier WCDMA Test Mode 1

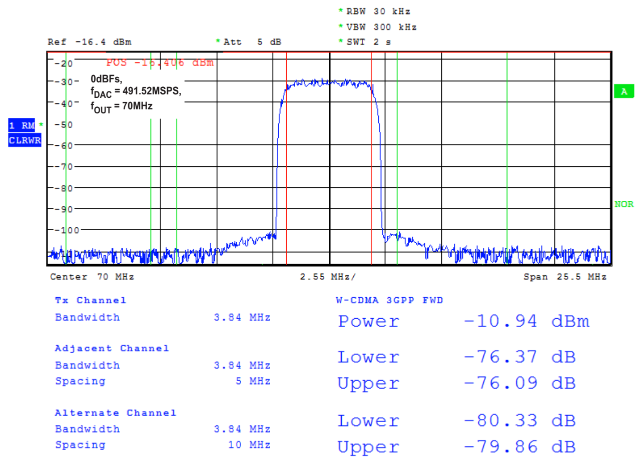

Figure 62. DAC3171 Single-Carrier WCDMA Test Mode 1

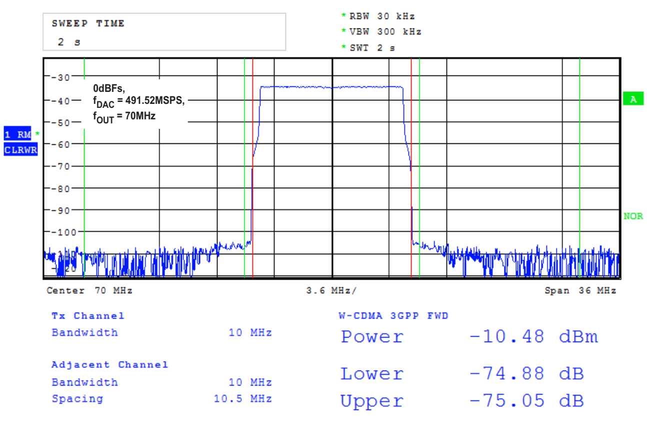

Figure 63. DAC3171 10-MHz Single Carrier LTE Test Mode 3.1

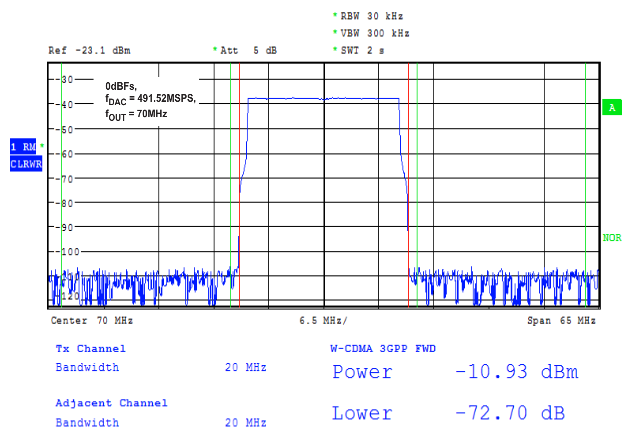

Figure 64. DAC3171 20-MHz Single Carrier LTE Test Mode 3.1

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, nominal supply voltages, f_{DAC} = 500MSPS, 50% clock duty cycle, 0-dBFS input signal and 20mA full-scale output current (unless otherwise noted).

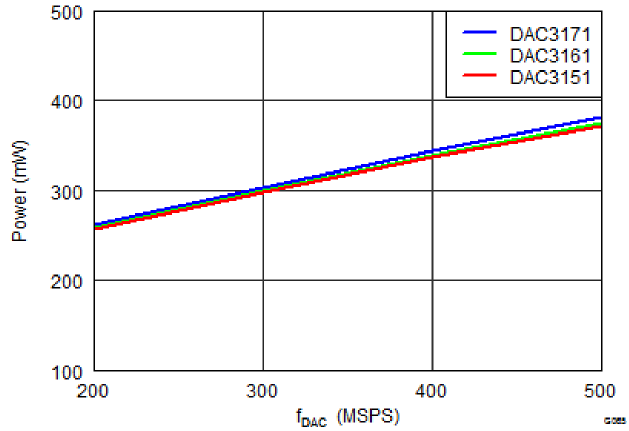

Figure 65. Power Consumption vs f_{DAC}

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DEFINITION OF SPECIFICATIONS

Adjacent Carrier Leakage Ratio (ACLR): Defined as the ratio in decibles relative to the carrier (dBc) between the measured power within a channel and that of an adjacent channel.

Analog and Digital Power Supply Rejection Ratio (APSSR, DPSSR): Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

Differential Nonlinearity (DNL): Defined as the variation in analog output associated with an ideal 1 LSB change in the digital input code.

Gain Drift: Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Gain Error: Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

Integral Nonlinearity (INL): Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Intermodulation Distortion (IMD3): The two-tone IMD3 is defined as the ratio (in dBc) of the 3rd-order intermodulation distortion product to either fundamental output tone.

Offset Drift: Defined as the maximum change in DC offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Offset Error: Defined as the percentage error (in FSR%) for the ratio between the measured mid-scale output current and the ideal mid-scale output current.

Output Compliance Range: Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result reduced reliability of the device or adversely affecting distortion performance.

Reference Voltage Drift: Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

Spurious Free Dynamic Range (SFDR): Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal.

Signal to Noise Ratio (SNR): Defined as the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

TIMING DIAGRAMS

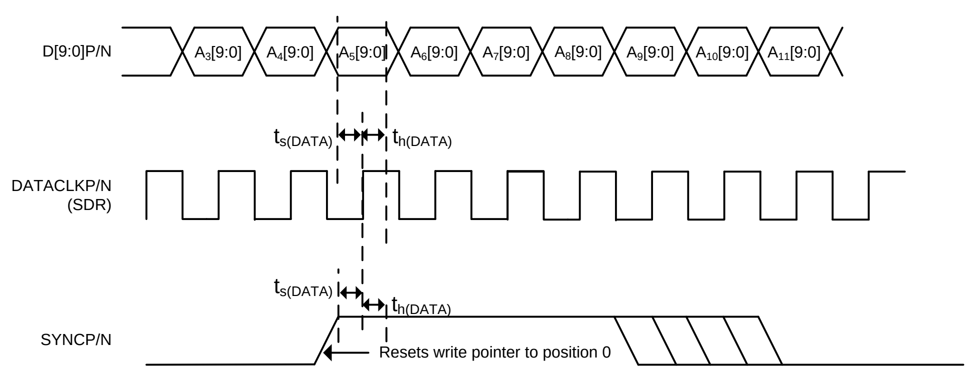

Figure 66. DAC3151 Input Data Timing Diagram

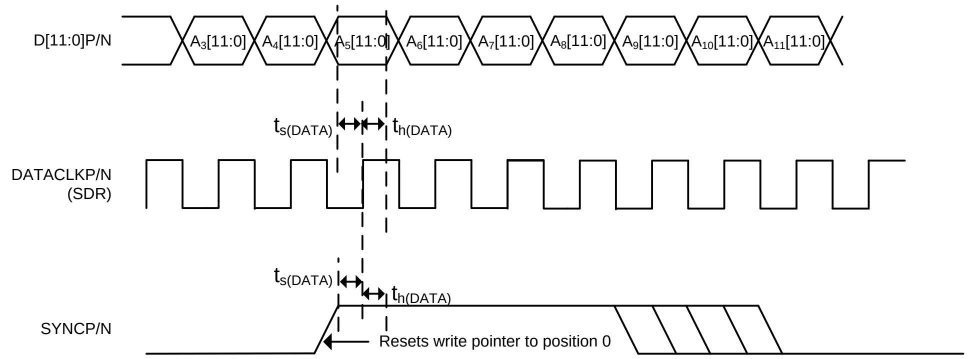

Figure 67. DAC3161 Input Data Timing Diagram

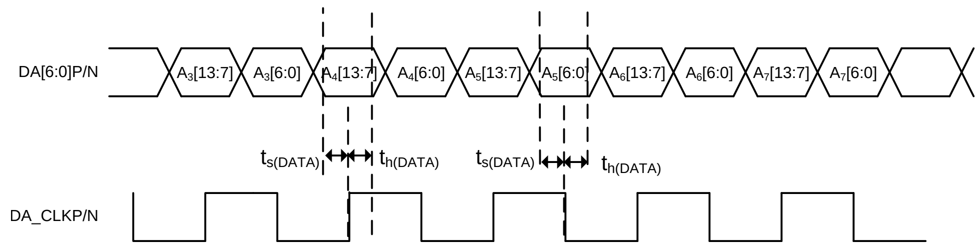

Figure 68. DAC3171 Input Data Timing Diagram for 7-Bit Interface Mode

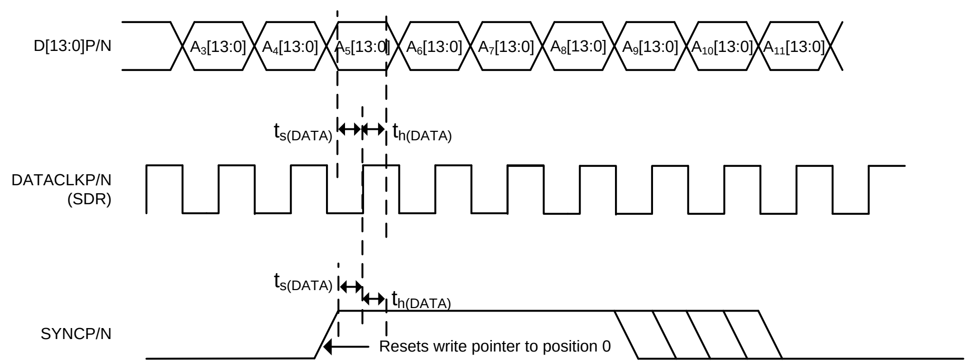

Figure 69. DAC3171 Input Data Timing for 14-Bit Interface Mode

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DATA INPUT FORMATS

Table 1. DAC3151: 10-Bit Interface Mode

	BITS	
DIFFERENTIAL PAIR (P/N)	DATACLK RISING EDGE	DATACLK FALLING EDGE
D9	A9	–
D8	A8	–
D7	A7	–
D6	A6	–
D5	A5	–
D4	A4	–
D3	A3	–
D2	A2	–
D1	A1	–
D0	A0	–
SYNC	FIFO Write Reset	–

Table 2. DAC3161: 12-Bit Interface Mode

	BITS	
DIFFERENTIAL PAIR (P/N)	DATACLK RISING EDGE	DATACLK FALLING EDGE
D11	A11	–
D10	A10	–
D9	A9	–
D8	A8	–
D7	A7	–
D6	A6	–
D5	A5	–
D4	A4	–
D3	A3	–
D2	A2	–
SYNC	FIFO Write Reset	–

Table 3. DAC3171: 7-Bit Interface Mode

DIFFERENTIAL PAIR (P/N)	DA_CLK RISING EDGE	DA_CLK FALLING EDGE
DA6	A13	A6
DA5	A12	A5
DA4	A11	A4
DA3	A10	A3
DA2	A9	A2
DA1	A8	A1
DA0	A7	A0

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Table 4. DAC3171: 14-Bit Interface Mode

	BITS	
DIFFERENTIAL PAIR (P/N)	**DATACLK RISING EDGE**	**DATACLK FALLING EDGE**
D13	A13	–
D12	A12	–
D11	A11	–
D10	A10	–
D9	A9	–
D8	A8	–
D7	A7	–
D6	A6	–
D5	A5	–
D4	A4	–
D3	A3	–
D2	A2	–
D1	A1	–
D0	A0	–
SYNC	FIFO Write Reset	–

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SERIAL INTERFACE DESCRIPTION

The serial port of the DAC3151/DAC3161/DAC3171 is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of DAC3151/DAC3161/DAC3171. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 pin interface by *sif4_ena* in register XYZ. In both configurations, SCLK is the serial interface input clock and SDENB is serial interface enable. For 3 pin configuration, SDIO is a bidirectional pin for both data in and data out. For 4 pin configuration, SDIO is data in only and SDO is data out only. Data is input into the device with the rising edge of SCLK. Data is output from the device on the falling edge of SCLK.

Each read/write operation is framed by signal SDENB (Serial Data Enable Bar) asserted low. The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write as well as the 7-bit address to be accessed. Table 5 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. The data transfer cycle consists of two bytes.

Table 5. Instruction Byte of the Serial interface

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/W	A6	A5	A4	A3	A2	A1	A0

R/W — Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC3151/DAC3161/DAC3171 and a low indicates a write operation to DAC3151/DAC3161/DAC3171.

[A6 : A0] — Identifies the address of the register to be accessed during the read or write operation.

Figure 70 shows the serial interface timing diagram for a DAC3151/DAC3161/DAC3171 write operation. SCLK is the serial interface clock input to DAC3151/DAC3161/DAC3171. Serial data enable SDENB is an active low input to DAC3151/DAC3161/DAC3171. SDIO is serial data in. Input data to DAC3151/DAC3161/DAC3171 is clocked on the rising edges of SCLK.

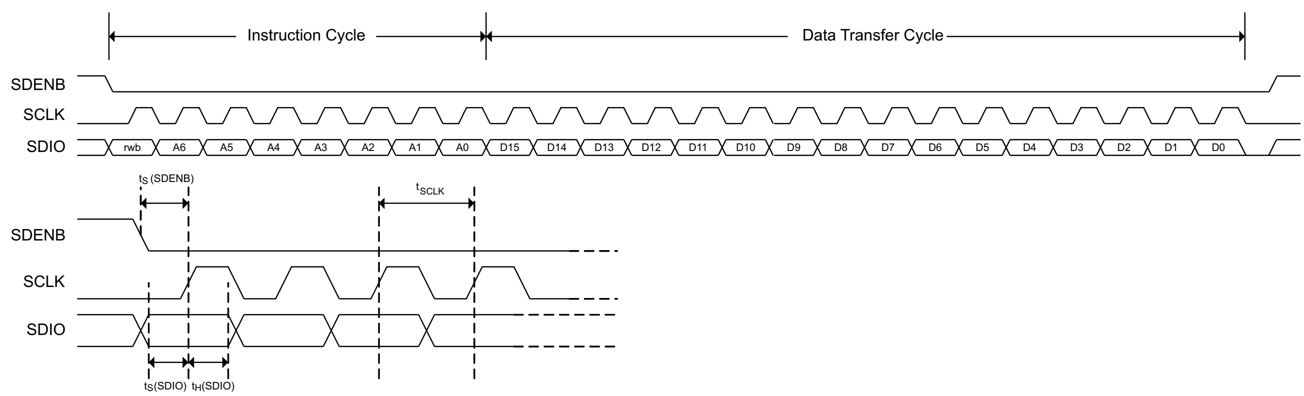

Figure 70. Serial Interface Write Timing Diagram

Figure 71 shows the serial interface timing diagram for a DAC3151/DAC3161/DAC3171 read operation. SCLK is the serial interface clock input to DAC3151/DAC3161/DAC3171. Serial data enable SDENB is an active low input to DAC3151/DAC3161/DAC3171. SDIO is serial data in during the instruction cycle. In 3 pin configuration, SDIO is data out from the DAC3151/DAC3161/DAC3171 during the data transfer cycle, while SDO is in a high-impedance state. In 4 pin configuration, both SDIO and SDO are data out from the DAC3151/DAC3161/DAC3171 during the data transfer cycle. At the end of the data transfer, SDIO and SDO will output low on the final falling edge of SCLK until the rising edge of SDENB when they will 3-state.

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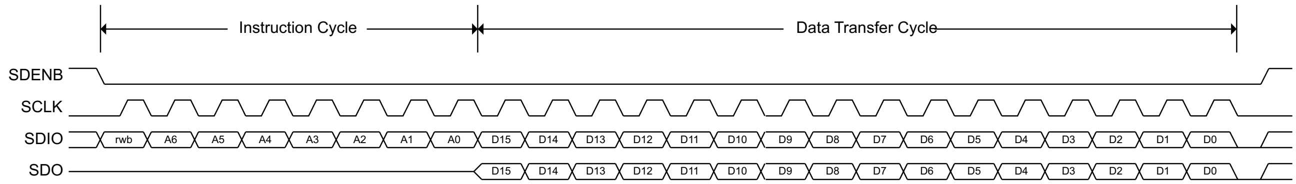

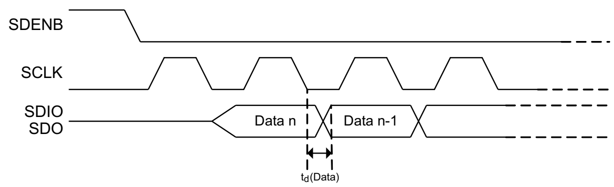

Figure 71. Serial Interface Read Timing Diagram

REGISTER DESCRIPTIONS

In the SIF interface there are four types of registers:

NORMAL: The NORMAL register type allows data to be written and read from. All 16-bits of the data are registered at the same time. There is no synchronizing with an internal clock thus all register writes are asynchronous with respect to internal clocks. There are three subtypes of NORMAL:

- **AUTOSYNC:** A NORMAL register that causes a sync to be generated after the write is finished. These are most commonly used in things like offsets and phaseadd where there is a word or block setup that extends across multiple registers and all of the registers need to be programmed before any take effect on the circuit. For example, the phaseadd is two registers long. It wouldn't serve the user to have the first write 16 of the 32 bits cause a change in the frequency, so the design allows all the registers to be written and then when that last one for this block is finished, an autosync is generated for the mixer telling it to grab all the new SIF values. This will occur on a mixer clock cycle so that no meta-stability errors occur.

- **No RESET Value:** These are NORMAL registers, but for one reason or another reset value can not be guaranteed. This could be because the register has some read_only bits or some internal logic partially controls the bit values. An example is the SIF_CONFIG6 register. The bits come from the temperature sensor and the fuses. Depending on which fuses are blown and what the die temp is the reset value will be different.

- **FUSE controlled:** While this isn't a type of register, you may see this description in the area describing the default value for the register. What is means is that fuses will change the default value and the value shown in the document is for when no fuses are blown.

READ_ONLY: Registers that are internal wires ANDed with the address bus then connected to the SIF output data bus.

WRITE_TO_CLEAR: These registers are just like NORMAL registers with one exception. They can be written and read, however, when the internal logic asynchronously sets a bit high in one of these registers, that bit stays high until it is written to '0'. This way interrupts will be captured and stay constant until cleared by the user.

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Table 6. Register Map

Name	Address	Default	(MSB) Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0
config0	0x00	0x44FC	qmc_offset_ena	dual_ena	chipwidth (1:0)		rev	twos	sif4_ena	reserved	fifo_ena	alarm_out_ena	alarm_out_pol	alignrx_ena	lvdssyncrx_ena	lvdsdataclk_ena	reserved	synconly_ena
config1	0x01	0x600E	iotest_ena	reserved	fullword_interface_ena	64cnt_ena	dacclkgone_ena	dataclkgone_end	collision_ena	reserved	daca_compliment	reserved	sif_sync	sif_sync_ena	alarm_2away_ena	alarm_1away_ena	alarm_collision_ena	reserved
config2	0x02	0x3FFF	reserved	reserved	lvdsdata_ena (13:0)													
config3	0x03	0x0000	datadlya (2:0)			clkdlya (2:0)			reserved			reserved			extref _ena	reserved		reserved
config4	0x04	0x0000	reserved		iotest_results (13:0)													
config5	0x05	0x0000	alarm_from_zerochka	reserved	alarms_from_fifoa (2:0)			reserved			alarm_dacclk_gone	alarm_dataclk_gone	clock_gone	alarm_from_iotesta	reserved	reserved		
config6	0x06	0x0000	tempdata (7:0)								fuse_cntl (5:0)						reserved	
config7	0x07	0xFFFF	alarms_mask (15:0)															
config8	0x08	0x4000	reserved			qmc_offseta (12:0)												
config9	0x09	0x8000	fifo_offset (2:0)			reserved												
config10	0x0A	0xF080	coarse_dac (3:0)				fuse_ sleep	reserved	reserved	tsense_sleep	clkrecv_ena	sleepa	sleepb	reserved				reserved
config11	0x0B	0x1111	reserved				reserved				reserved				reservedspares_west (3:0)			
config12	0x0C	0x3A7A	reserved		iotest_pattern0 (13:0)													
config13	0x0D	0x36B6	reserved		iotest_pattern1 (13:0)													
config14	0x0E	0x2AEA	reserved		iotest_pattern2 (13:0)													
config15	0x0F	0x0545	reserved		iotest_pattern3 (13:0)													
config16	0x10	0x1A1A	reserved		iotest_pattern4 (13:0)													
config17	0x11	0x1616	reserved		iotest_pattern5 (13:0)													
config18	0x12	0x2AAA	reserved		iotest_pattern6 (13:0)													
config19	0x13	0x06C6	reserved		iotest_pattern7 (13:0)													
config20	0x14	0x0000	sifdac_ena	reserved	sifdac (13:0)													
config21	0x15	0xFFFF	sleepcntl (15:0)															
config22	0x16	0x0000	fa002_data(15:0)															
config23	0x17	0x0000	fa002_data(31:16)															
config24	0x18	0x0000	fa002_data(47:32)															
config25	0x19	0x0000	fa002_data(63:48)															
config127	0x7F	0x0044	reserved		reserved		reserved		reserved		reserved	titest_voh	titest_vol	vendorid (1:0)		versionid (2:0)		

Register name: config0 – Address: 0x00, Default: 0x4FC

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config0	0x00	15	qmc_offset_ena	Enable the offset function when asserted.	0
		14	dual_ena	Utilizes both DACs when asserted.	0 FUSE controlled
		13:12	chipwidth	Programmable bits for setting the input interface width. 00: all 14 bits are used. 01: upper 12 bits are used10: upper 10 bits are used 11: upper 10 bits are used	00
		11	rev	Reverses the input bits. When using the 7bit interface, this reverse each 7-bit input, however when using the 14-bit interface, all 14-bits are reversed as one word.	0
		10	twos	When asserted, this bit tells the chip to presume 2's complement data is arriving at the input. Otherwise offset binary is presumed.	1
		9	sif4_ena	When asserted the SIF interface becomes a 4 pin interface. This bit has a lower priority than the **dieid_ena** bit.	0
		8	reserved	reserved	0
		7	fifo_ena	When asserted, the FIFO is absorbing the difference between INPUT clock and DAC clock. If it is not asserted then the FIFO buffering is bypassed but the reversing of bits and handling of offset binary input is still available. **NOTE: When the FIFO is bypassed the DACCCLK and DATACLK must be aligned or there may be timing errors; and, it is not recommended for actual application use.**	1
		6	alarm_out_ena	When asserted the pin alarm becomes an output instead of a tri-stated pin.	1
		5	alarm_out_pol	This bit changes the polarity of the ALARM signal. (0=negative logic, 1=positive logic)	1
		4	alignrx_ena	When asserted the ALIGN pin receiver is powered up. **NOTE: It is recommended to clear this bit when ALIGNP/N are not used (dual bus mode, and SYNC ONLY and SIF_SYNC modes in single bus mode).**	1
		3	lvdssyncrx_ena	When asserted the SYNC pin receiver is powered up. **NOTE: 1 It is recommended to clear this bit when SYNCP/N are not used (dual bus mode, and SIF_SYNC mode in single bus mode.)**	1
		2	lvdsdataclk_ena	When asserted the DATACLK pin receiver is powered up.	1
		1	reserved	reserved	0
		0	synconly_ena	When asserted the chip is put into the SYNC ONLY mode where the SYNC pin is used as the sync input for both the front and back of the FIFO.	0

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Register name: config1 – Address: 0x01, Default: 0x600E

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config1	0x01	15	iotest_ena	Turns on the io-testing circuitry when asserted. This is the circuitry that will compare a 8 sample input pattern to SIF programmed registers to make sure the data coming into the chip meets setup/hold requirements. If this bit is a ‘0’ then the clock to this circuitry is turned off for power savings. **NOTE: Sample 0 should be aligned with the rising edge of SYNC.**	0
		14	reserved	reserved	1
		13	fullwordinterface_ena	When asserted the input interface is changed to use the full 14-bits for each word, instead of dual 8-bit buses for two half words. **Note: fixed to "1" for DAC3151/DAC3161.**	1
		12	64cnt_ena	This enables the resetting of the alarms after 64 good samples with the goal of removing unnecessary errors. For instance on a lab board, when checking the setup/hold through IO TEST, there may initially be errors, but once the test is up and running everything works. Setting this bit removes the need for a SIF write to clear the alarm register.	0
		11	dacclkgone_ena	This allows the DACCLK gone signal from the clock monitor to be used to shut the output off.	0
		10	dataclkgone_ena	This allows the DATACLK gone signal from the clock monitor to be used to shut the output off.	0
		9	collision_ena	This allows the collision alarm from the FIFO to shut the output off	0
		8	reserved	reserved.	0
		7	daca_compliment	When asserted the output to the DACA is complimented. This allows the user of the chip to effectively change the + and – designations of the DAC output pins.	0
		6	reserved	reserved	0
		5	sif_sync	This is the SIF_SYNC signal. Whatever is programmed into this bitwill be used as the chip sync when SIF_SYNC mode is enabled.Design is sensitive to rising edges so programming from 0->1 is when the sync pulse is generated. 1->0 has no effect.	0
		4	sif_sync_ena	When asserted enable SIF_SYNC mode.	0
		3	alarm_2away_ena	When asserted alarms from the FIFO that represent the pointers being 2 away are enabled	1
		2	alarm_1away_ena	When asserted alarms from the FIFO that represent the pointers being 1 away are enabled	1
		1	alarm_collision_ena	When asserted the collision of FIFO pointers causes an alarm to be generated	1
		0	reserved	reserved	0

Register name: config2 – Address: 0x02, Default: 0x3FFF

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config2	0x02	15	reserved	reserved.	0
		14	reserved	reserved.	0
		13:0	lvdsdata_ena	These 14 bits are individual enables for the 14 input pin receivers. **Note: for DAC3171 7-bit input interface mode, it is recommended to turn off bits(6:0).**	0x3FFF

Register name: config3 – Address: 0x03, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config3	0x03	15:13	datadlya	Controls the delay of the A data inputs through the LVDS receivers. 0= no additional delay and each LSB adds a nominal 80ps.	000
		12:10	clkdlya	Controls the delay of the A data clock input through the LVDS receivers. 0= no additional delay and each LSB adds a nominal 80ps.	000
		9:7	reserved	reserved.	000
		6:4	reserved	reserved	000
		3	extref_ ena	Enable external reference for the DAC when set.	0
		2:1	reserved	reserved	00
		0	reserved	reserved	0

Register name: config4 – Address: 0x04, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config4 WRITE TO CLEAR/ No RESET value	0x04	15:14	reserved	reserved	00
		13:0	iotest_ results	The values of these bits tell which bit in the input word failed during the io-test pattern comparison.	0x0000

Register name: config5 – Address: 0x05, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config5 WRITE TO CLEAR	0x05	15	alarm_from_ zerochka	When this bit is asserted the FIFOA write pointer has an all zeros pattern in it. Since this pointer is a shift register, all zeros will cause the input point to be stuck until the next sync. The result could be a repeated 8T pattern at the output if the mixer is off and no syncs occur. Check for this error will tell the user that another sync is necessary to restart the FIFO write pointer.	0
		14	reserved	reserved.	0
		13:11	alarms_from_ fifoa	These bits report the FIFO A pointer status. 000: All fine 001: Pointers are 2 away 01X: Pointers are 1 away 1XX: FIFO Pointer collision	000
		10:8	reserved	reserved	0
		7	alarm_dacclk_ gone	Bit gets asserted when the DACCLK has been stopped long for enough cycles to be caught. The number of cycles varies with interpolation.	0
		6	alarm_dataclk_ gone	Bit gets asserted when the DATACLK has been stopped long for enough cycles to be caught. The number of cycles varies with interpolation.	0
		5	clock_gone	This bit gets set when either alarm_dacclk_gone or alarm_dataclk_gone are asserted. It controls the output of the CDRV_SER block. When high, the CDRV_SER block will output “0x8000” for each output connected to a DAC. The bit must be written to ‘0’ for CDRV_SER outputs to resume normal operation.	0
		4	alarm_from_ iotesta	This is asserted when the input data pattern does not match the pattern in the iotest_pattern registers.	0
		3	reserved	reserved.	0
		2	reserved	reserved	0
		1	reserved	reserved	0
		0	reserved	reserved	0

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Register name: config6 – Address: 0x06, Default: 0x0010(DAC3171); 0x0094(DAC3161); 0x0098(DAC3151)

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config6 No RESET Value	0x06	15:8	tempdata	This the output from the chip temperature sensor. NOTE: when reading these bits the SIF interface must be exteremly slow, 1MHz range.	0x00
		7:2	fuse_cntl	These are the values of the blown fuses and are used to determine the available functionality in the chip. (*** NOTE ***) These bits are READ_ONLY and allow the user to check what features have been disabled in the device. bit5 = 1: Forces Full Word interface bit4 = 0: reserved bit3 = 0: reserved bit2 = 1: Forces Single DAC Mode. **Note: This does not force the channel B in sleep mode. In order to do so, user needs to program the sleepb SPI bit (config10, bit 5) to "1".** bit1:0 : Forces a different bits size. “00” 14bit “01” 12bit “10” 10bit “11” 10bit	0x10 for DAC3171; 0x94 for DAC3161; 0x98 for DAC3151; FUSE controlled
		1	reserved	reserved	0
		0	reserved	reserved	0

Register name: config7 – Address: 0x07, Default: 0xFFFF

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config7	0x07	15:0	alarms_ mask	Each bit is used to mask an alarm. Assertion masks the alarm: bit15 = alarm_mask_zerochka bit14 = alarm_mask_zerochkb bit13 = alarm_mask_fifoa_collision bit12 = alarm_mask_fifoa_1away bit11 = alarm_mask_fifoa_2away bit10 = alarm_mask_fifob_collision bit9 = alarm_mask_fifob_1away bit8 = alarm_mask_fifob_2away bit7 = alarm_mask_dacclk_gone bit6 = alarm_mask_dataclk_gone bit5 = Masks the signal which turns off the DAC output when a clock or collision occurs. This bit has no effect on the PAD_ALARM output. bit4 = alarm_mask_iotesta bit3 = alarm_mask_iotestb bit2 = bit1 = bit0 =	0xFFFF

Register name: config8 – Address: 0x08, Default: 0x4000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config8	0x08	15:13	reserved	reserved	010
		12:0	qmc_ offseta	The DAC A offset correction. The offset is measured in DAC LSBs.	0x0000

Register name: config9 – Address: 0x09, Default: 0x8000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config9 AUTO SYNC	0x09	15:13	fifo_ offset	This is the starting point for the READ_POINTER in the FIFO block. The READ_POINTER is set to this location when a sync occurs on the DACCLK side of the FIFO.	100
		12:0	reserved	reserved	0x0000

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Register name: config10 – Address: 0x0A, Default: 0xF080

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
Config10	0x0A	15:12	coarse_ dac	Scales the output current is 16 equal steps. $\frac{VrefIO}{Rbias} \times (mem\_coarse\_daca + 1)$	1111
		11	fuse_ sleep	Put the fuses to sleep when set high.	0
		10	reserved	reserved	0
		9	reserved	reserved	0
		8	tsense_ sleep	When asserted the temperature sensor is put to sleep.	0
		7	clkrecv_ ena	Turn on the DAC CLOCK receiver block when asserted.	1
		6	sleepa	When asserted DACA is put to sleep.	0
		5	sleepb	When asserted DACB is put to sleep. **Note: This bit needs to be programmed to "1" to save additional power.**	0
		4:0	reserved	reserved	00000

Register name: config11 – Address: 0x0B, Default: 0x1111

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config11	0x0B	15:12	reserved	reserved.	0001
		11:8	reserved	reserved.	0001
		7:4	reserved	reserved.	0001
		3:0	reserved	reserved.	0001

Register name: config12 – Address: 0x0C, Default: 0x3A7A

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config12	0x0C	15:14	reserved	reserved.	00
		13:0	iotest_ pattern0	This is dataword0 in the IO test pattern. It is used with the seven other words to test the input data. (*** NOTE ***) This word should be aligned with the rising edge of SYNC when testing the IO interface.	0x3A7A

Register name: config13 – Address: 0x0D, Default: 0x36B6

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config13	0x0D	15:14	reserved	reserved.	00
		13:0	iotest_ pattern1	This is dataword1 in the IO test pattern. It is used with the seven other words to test the input data.	0x36B6

Register name: config14 – Address: 0x0E, Default: 0x2AEA

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config14	0x0E	15:14	reserved	reserved	00
		13:0	iotest_ pattern2	This is dataword2 in the IO test pattern. It is used with the seven other words to test the input data.	0x2AEA

Register name: config15 – Address: 0x0F, Default: 0x0545

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config15	0x0F	15:14	reserved	reserved	00
		13:0	iotest_ pattern3	This is dataword3 in the IO test pattern. It is used with the seven other words to test the input data.	0x0545

Register name: config16 – Address: 0x10, Default: 0x1A1A

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config16	0x10	15:14	reserved	reserved	00
		13:0	iotest_ pattern4	This is dataword4 in the IO test pattern. It is used with the seven other words to test the input data.	0x1A1A

Register name: config17 – Address: 0x11, Default: 0x1616

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config17	0x11	15:14	reserved	reserved	00
		13:0	iotest_ pattern5	This is dataword5 in the IO test pattern. It is used with the seven other words to test the input data.	0x1616

Register name: config18 – Address: 0x12, Default: 0x2AAA

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config18	0x12	15:14	reserved	reserved	00
		13:0	iotest_ pattern5	This is datawor6 in the IO test pattern. It is used with the seven other words to test the input data.	0x2AAA

Register name: config19 – Address: 0x13, Default: 0x06C6

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config19	0x13	15:14	reserved	reserved	00
		13:0	iotest_ pattern7	This is dataword7 in the IO test pattern. It is used with the seven other words to test the input data.	0x06C6

Register name: config20– Address: 0x14, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config20	0x14	15	sifdac_ ena	When asserted the DAC output is set to the value in sifdac. This can be used for trim setting and other static tests.	0
		14	reserved	reserved	0
		13:0	sifdac	This is the value that is sent to the DACs when sifdac_ena is asserted.	0x0000

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Register name: config21– Address: 0x15, Default: 0xFFFF

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config21	0x15	15:0	sleepcntl	This controls what blocks get sent a SLEEP signal when the PAD_SLEEP pin is asserted. Programming a ‘1’ in a bit will pass the SLEEP signal to the appropriate block. bit15 = DAC A bit14 = DAC B bit13 = FUSE Sleep bit12 = Temperature Sensor bit11 = Clock Receiver bit10 = LVDS DATA Receivers bit9 = LVDS SYNC Receiver bit8 = PECL ALIGN Receiver bit7 = LVDS DATACLK Receiver bit6 = reserved bit5 = reserved bit4 = reserved bit3 = reserved bit2 = reserved bit1 = reserved bit0 = reserved	0xFFFF

Register name: config22– Address: 0x16, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config22 READ ONLY	0x16	15:0	fa002_ data(15:0)	Lower 16bits of the DIE ID word	

Register name: config23– Address: 0x17, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config23 READ ONLY	0x17	15:0	fa002_ data(31:16)	Lower middle 16bits of the DIE ID word	

Register name: config24– Address: 0x18, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config24 READ ONLY	0x18	15:0	fa002_ data(47:32)	Upper middle 16bits of the DIE ID word	

Register name: config25– Address: 0x19, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config25 READ ONLY	0x19	15:0	fa002_ data(63:48)	Upper 16bits of the DIE ID word	

Register name: config127– Address: 0x7F, Default: 0x0045

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config127 READ ONLY/No RESET Value	0x7F	15:14	reserved	reserved	00
		13:12	reserved	reserved	00
		11:10	reserved	reserved	00
		9:8	reserved	reserved	00
		7	reserved	reserved	0
		6	titest_voh	A fixed ‘1’ that can be used to test the Voh at the SIF output.	1
		5	titest_vol	A fixed ‘0’ that can be used to test the Vol at the SIF output.	0
		4:3	vendorid	Fixed at "01".	01
		2:0	versionid	Chip version	001

Synchronization Modes

There are three modes of syncing included in the DAC3151/DAC3161/DAC3171.

- **NORMAL Dual Sync –** The SYNC pin is used to align the input side of the FIFO (write pointers) with the A(0) sample. The ALIGN pin is used to reset the output side of the FIFO (read pointers) to the offset value. Multiple chip alignment can be accomplished with this kind of syncing.
- **SYNC ONLY –** In this mode only the SYNC pin is used to sync both the read and write pointers of the FIFO. There is an asynchronized handoff between the DATACLK and DACCLK when using this mode, therefore it is impossible to accurately align multiple chips closer than 2 or 3T.
- **SIF_SYNC –** When neither SYNC nor ALIGN are used, a programmable SYNC pulse can be used to sync the design. However, the same issues as ISTROBE ONLY apply. There is an asynchronized handoff between the serial clock domain and the two sides of the FIFO. Because of the asynchronous nature of the SIF_SYNC it is impossible to align the sync up with any sample at the input. Note: SIF_SYNC mode is the only synchronisation mode supported in the 7-bit interface mode.

Note: When ALIGNP/N are not used, it is recommended to clear the alignrx_ena register (config1, bit 4), and tie ALIGNP to DIGVDD18 and ALIGNN to GROUND. When SYNCP/N are not used, it is recommended to clear register lvdssyncrx_ena (config0, bit3), and the unused SYNCP/N pins can be left open or tied to GROUND.

Alarm Monitoring

DAC3151/DAC3161/DAC3171 includes flexible alarm monitoring that can be used to alert a possible malfunction scenario. All alarm events can be accessed either through the SIP registers and/or through the ALARM pin. Once an alarm is set, the corresponding alarm bit in register config5 must be reset through the serial interface to allow further testing. The set of alarms includes the following conditions:

Zero check alarm

- Alarm_from_zerochk. Occurs when the FIFO write pointer has an all zeros pattern. Since the write pointer is a shift register, all zeros will cause the input point to be stuck until the next sync event. When this happens a sync to the FIFO block is required.

FIFO alarms

- alarm_from_fifo. Occurs when there is a collision in the FIFO pointers or a collision event is close.
- alarm_fifo_2away. Pointers are within two addresses of each other.
- alarm_fifo_1away. Pointers are within one address of each other.
- alarm_fifo_collision. Pointers are equal to each other.

Clock alarms

- clock_gone. Occurs when either the DACCLK or DATACLOCK have been stopped.
- alarm_dacclk_gone. Occurs when the DACCLK has been stopped.
- alarm_dataclk_gone. Occurs when the DATACLK has been stopped.

Pattern checker alarm

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- alarm_from_iotest. Occurs when the input data pattern does not match the pattern key.

To prevent unexpected DAC outputs from propagating into the transmit channel chain, DAC3151/DAC3161/DAC3171 includes a feature that disables the outputs when a catastrophic alarm occurs. The catastrophic alarms include FIFO pointer collision, the loss DACCLK or the loss of DATACLK. When any of these alarms occur the internal TXenable signal is driven low, causing a zeroing of the data going to the DAC in <10T. One caveat is if both clocks stop, the circuit cannot determine clock loss so no alarms are generated; therefore, no zeroing of output data occurs.

REVISION HISTORY

Changes from Original (August 2013) to Revision A	Page
• Changed from Product Preview to Production Data	1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC3151IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3151I	Samples
DAC3151IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3151I	Samples
DAC3161IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3161I	Samples
DAC3161IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3161I	Samples
DAC3171IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3171I	Samples
DAC3171IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3171I	Samples
DAC3171IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3171I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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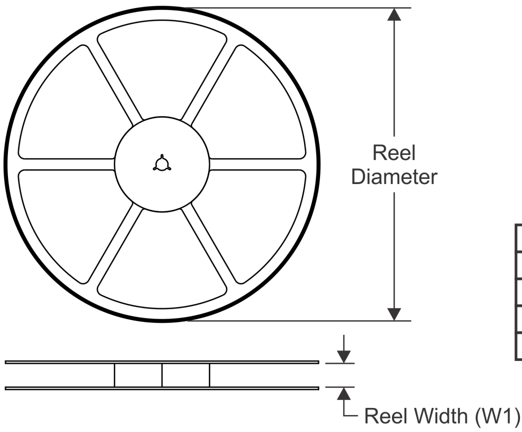
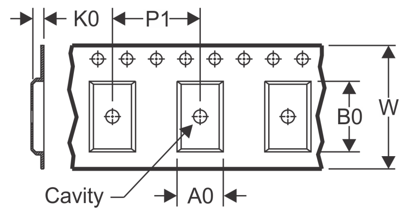
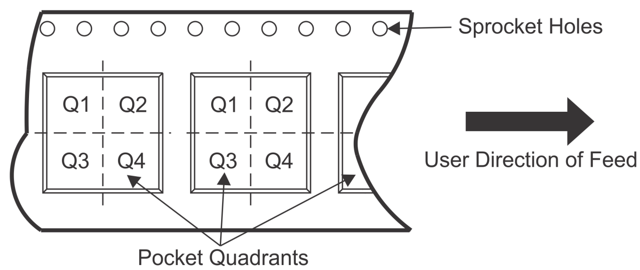
TAPE AND REEL INFORMATION





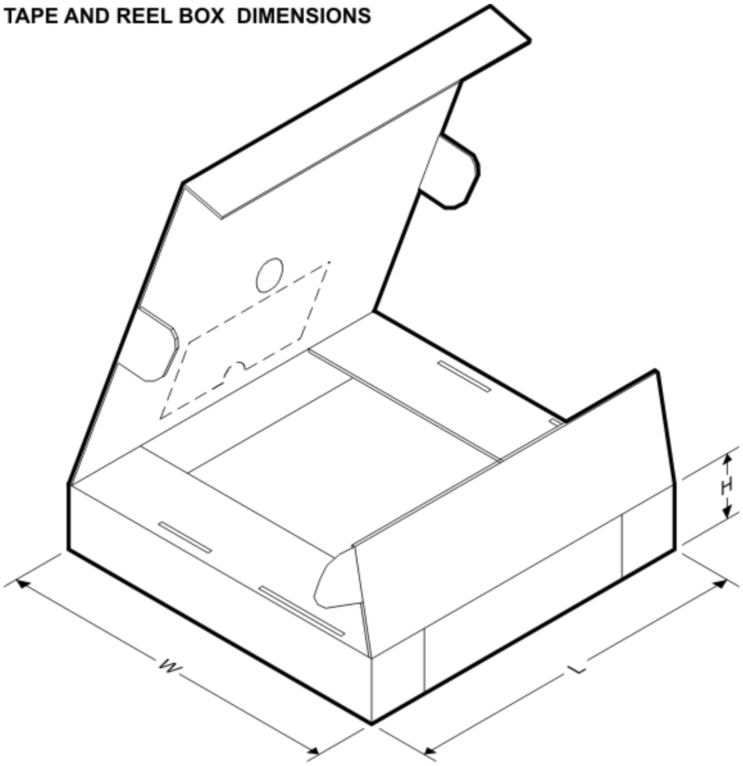
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC3151IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC3151IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC3161IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC3161IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC3171IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
DAC3171IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

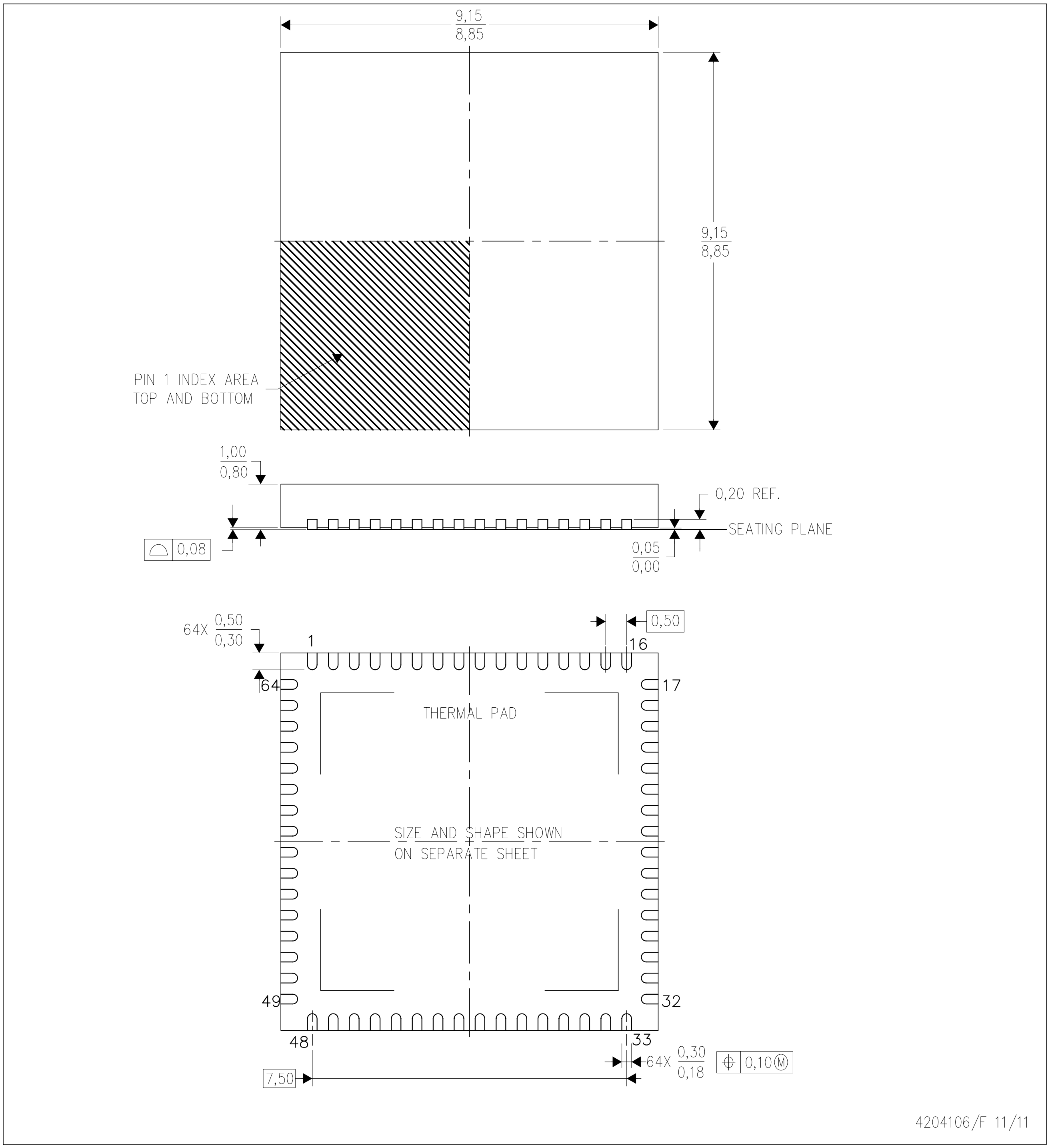
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC3151IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
DAC3151IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6
DAC3161IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
DAC3161IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6
DAC3171IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
DAC3171IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

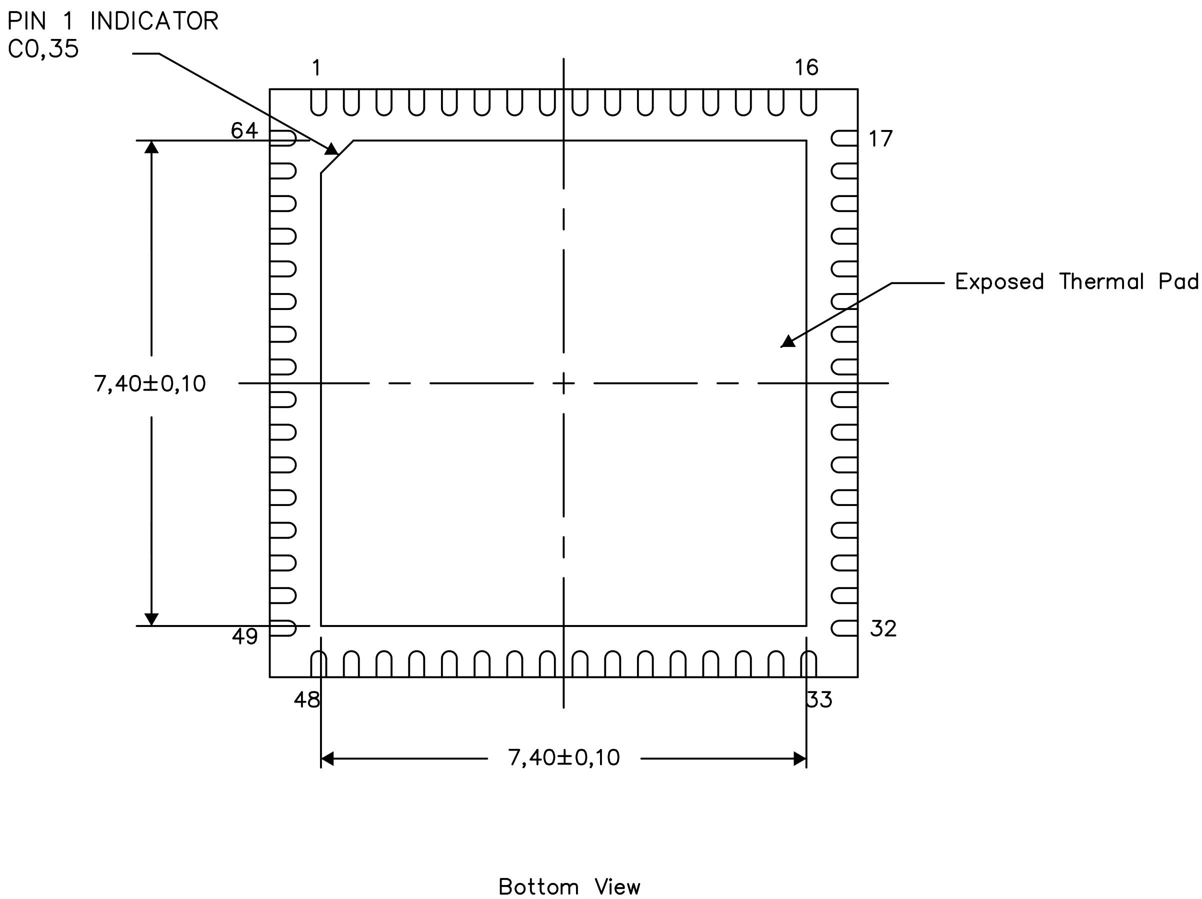
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

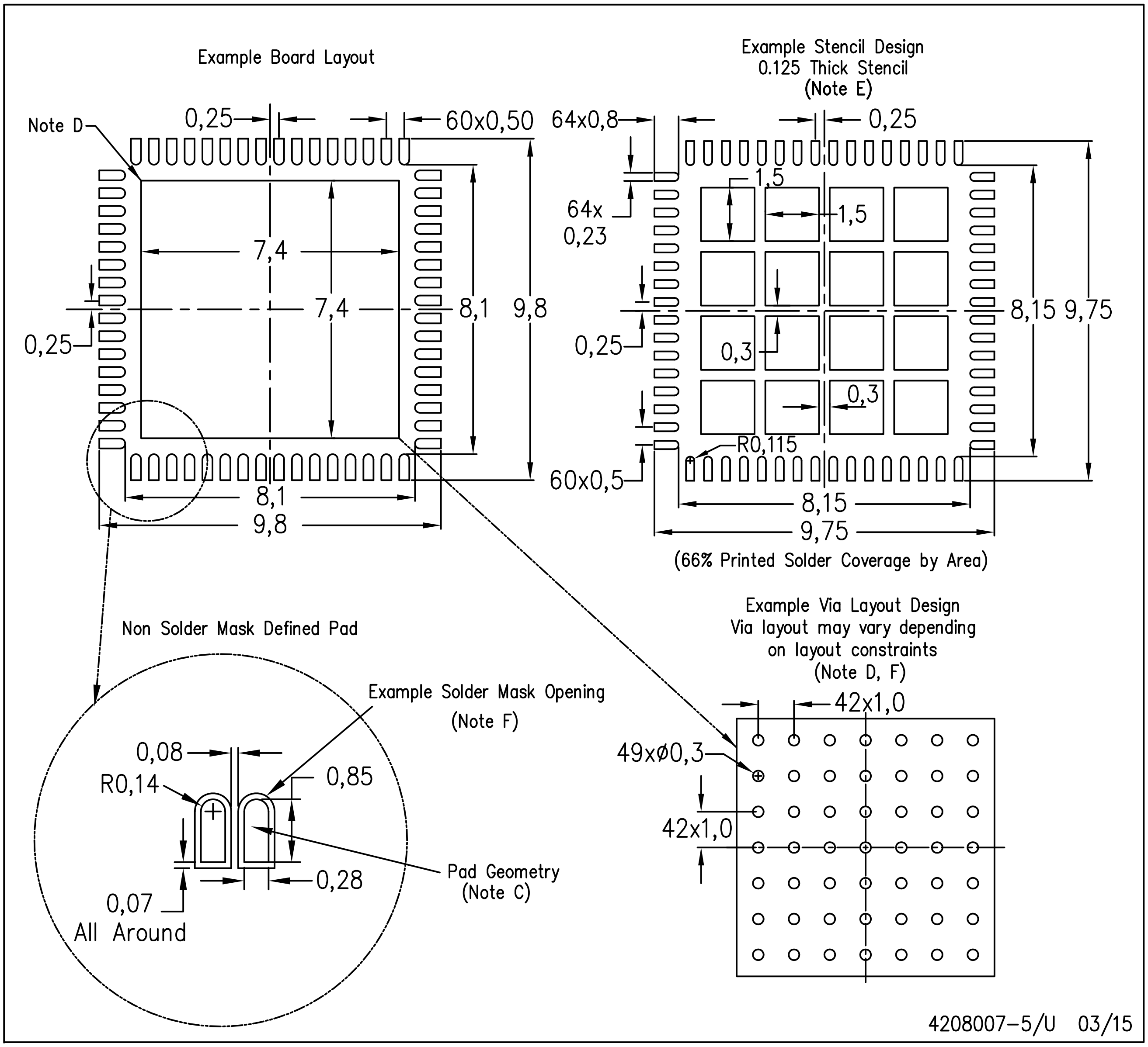


Exposed Thermal Pad Dimensions

4206192–4/AE 03/15

NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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