

General Description

The CYBLE-212020-01 is a fully certified and qualified module supporting Bluetooth® Low Energy (BLE) 4.2 wireless communication. The CYBLE-212020-01 is a turnkey solution and includes onboard crystal oscillators, trace antenna, passive components, and the Cypress PROc™ BLE. Refer to the [CYBL10XX7X datasheet](#) for additional details on the capabilities of the PROc BLE device used on this module.

The CYBLE-212020-01 supports a number of peripheral functions (ADC, timers, counters, PWM) and serial communication protocols (I²C, UART, SPI) through its programmable architecture. The CYBLE-212020-01 includes a royalty-free BLE stack compatible with Bluetooth 4.2 and provides up to 23 GPIOs in a 14.52 × 19.20 × 2.00 mm package.

The CYBLE-212020-01 is drop-in compatible with the CYBLE-01211-00 (128KB BT 4.1) and CYBLE-212019-00 (256KB BT 4.1) EZ-BLE PROc Modules.

The CYBLE-212020-01 is a complete solution targeted at applications requiring cost-optimized BLE wireless connectivity.

Module Description

- Module size: 14.52 mm × 19.20 mm × 2.00 mm (with shield)
- Castelated solder pad connections for ease-of-use
- 256-KB flash memory, 32-KB SRAM memory
- Up to 23 GPIOs configurable as open drain high/low, pull-up/pull-down, Hi-Z analog, Hi-Z digital, or strong output
- Bluetooth 4.2 single-mode module
 - QDID: [82977](#)
 - Declaration ID: [D030800](#)
- Certified to FCC, IC, MIC, KC, and CE regulations
- Industrial temperature range: -40 °C to +85 °C
- 32-bit processor (0.9 DMIPS/MHz) with single-cycle 32-bit multiply, operating at up to 48 MHz
- Watchdog timer with dedicated internal low-speed oscillator (ILO)
- Two-pin SWD for programming

Power Consumption

- TX output power: -18 dbm to +3 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution
- TX current consumption of 15.6 mA (radio only, 0 dbm)

- RX current consumption of 16.4 mA (radio only)
- Low power mode support
 - Deep Sleep: 1.3 µA with watch crystal oscillator (WCO) on
 - Hibernate: 150 nA with SRAM retention
 - Stop: 60 nA with GPIO (P2.2) or XRES wakeup

Functional Capabilities

- Up to 22 capacitive sensors for buttons or sliders with best-in-class signal-to-noise ratio (SNR) and liquid tolerance
- 12-bit, 1-Msps SAR ADC with internal reference, sample-and-hold (S/H), and channel sequencer
- Two serial communication blocks (SCBs) supporting I²C (master/slave), SPI (master/slave), or UART
- Four dedicated 16-bit timer, counter, or PWM (TCPWM) blocks
- LCD drive supported on all GPIOs (common or segment)
- Programmable low-voltage detect (LVD) from 1.8 V to 4.5 V
- I²S master interface
- BLE protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles
- Switches between Central and Peripheral roles on-the-go
- Standard BLE profiles and services for interoperability
- Custom profile and service for specific use cases

Benefits

The CYBLE-212020-01 module is provided as a turnkey solution, including all necessary hardware required to use BLE communication standards.

- Proven hardware design that is ready for use
- Cost-optimized for applications without space constraint
- Reprogrammable architecture
- Fully certified module eliminates the time needed for design, development and certification processes
- Bluetooth SIG qualified with QDID and Declaration ID
- Flexible communication protocol support
- PSoC Creator™ provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test a BLE application

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

■ Overview:

- [EZ-BLE Module Portfolio, Module Roadmap](#)
- [EZ-BLE PSoC Product Overview](#)
- [PSoC BLE Silicon Datasheet](#)

■ Application notes: Cypress offers a number of BLE application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with EZ-BLE modules are:

- [AN96841](#) - Getting Started with EZ-BLE Module
- [AN94020](#) - Getting Started with PSoC BLE
- [AN97060](#) - PSoC® 4 BLE and PSoC™ BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
- [AN91162](#) - Creating a BLE Custom Profile
- [AN91184](#) - PSoC 4 BLE - Designing BLE Applications
- [AN92584](#) - Designing for Low Power and Estimating Battery Life for BLE Applications
- [AN85951](#) - PSoC® 4 and PSoC Analog Coprocessor CapSense® Design Guide
- [AN95089](#) - PSoC® 4/PSoC™ BLE Crystal Oscillator Selection and Tuning Techniques
- [AN91445](#) - Antenna Design and RF Layout Guidelines

■ Technical Reference Manual (TRM):

- PSoC® BLE [Technical Reference Manual](#)

■ Knowledge Base Article

- [KBA212838](#) - Pin Mapping Differences Between the EZ-BLE™ PSoC™ Evaluation Board (CYBLE-212020-EVAL) and the BLE Pioneer Kit (CY8CKIT-042-BLE)
- [KBA97095](#) - EZ-BLE™ Module Placement
- [KBA210638](#) - RF Regulatory Certifications for EZ-BLE™ PSoC™ Module CYBLE-212020-01
- [KBA213976](#) - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
- [KBA210802](#) - Queries on BLE Qualification and Declaration Processes

■ Development Kits:

- CYBLE-212020-EVAL, CYBLE-212020-01 Evaluation Board
- [CY8CKIT-042-BLE](#), Bluetooth® Low Energy (BLE) Pioneer Kit
- [CY8CKIT-002](#), PSoC® MiniProg3 Program and Debug Kit

■ Test and Debug Tools:

- [CYSmart](#), Bluetooth® LE Test and Debug Tool (Windows)
- [CYSmart Mobile](#), Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)

Two Design Environments to Get You Started Quickly

PSoC® Creator™ Integrated Design Environment (IDE)

[PSoC Creator](#) is an Integrated Design Environment (IDE) that enables concurrent hardware and firmware editing, compiling and debugging of PSoC 3, PSoC 4, PSoC 5LP, PSoC 4 BLE, PSoC BLE and EZ-BLE module systems with no code size limitations. PSoC peripherals are designed using schematic capture and simple graphical user interface (GUI) with over 120 pre-verified, production-ready PSoC Components™.

PSoC Components are analog and digital “virtual chips,” represented by an icon that users can drag-and-drop into a design and configure to suit a broad array of application requirements.

Bluetooth Low Energy Component

The [Bluetooth Low Energy Component](#) inside PSoC Creator provides a comprehensive GUI-based configuration window that lets you quickly design BLE applications. The Component incorporates a Bluetooth Core Specification v4.1 compliant BLE protocol stack and provides API functions to enable user applications to interface with the underlying Bluetooth Low Energy Sub-System (BLESS) hardware via the stack.

EZ-Serial™ BLE Firmware Platform

The [EZ-Serial Firmware Platform](#) provides a simple way to access the most common hardware and communication features needed in BLE applications. EZ-Serial implements an intuitive API protocol over the UART interface and exposes various status and control signals through the module's GPIOs, making it easy to add BLE functionality quickly to existing designs.

Use a simple serial terminal and evaluation kit to begin development without requiring an IDE. Refer to the [EZ-Serial webpage](#) for User Manuals and instructions for getting started as well as detailed reference materials.

EZ-BLE modules are pre-flashed with the EZ-Serial Firmware Platform. If you do not have EZ-Serial pre-loaded on your module, you can download each EZ-BLE module's firmware images on the [EZ-Serial webpage](#).

Technical Support

- [Frequently Asked Questions \(FAQs\)](#): Learn more about our BLE ecosystem.
- [Forum](#): See if your question is already answered by fellow developers on the PSoC 4 BLE and PSoC BLE forums.
- Visit our [support](#) page and create a [technical support case](#) or contact a [local sales representative](#). If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

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Overview

Module Description

The CYBLE-212020-01 module is a complete module designed to be soldered to the applications main board.

Module Dimensions and Drawing

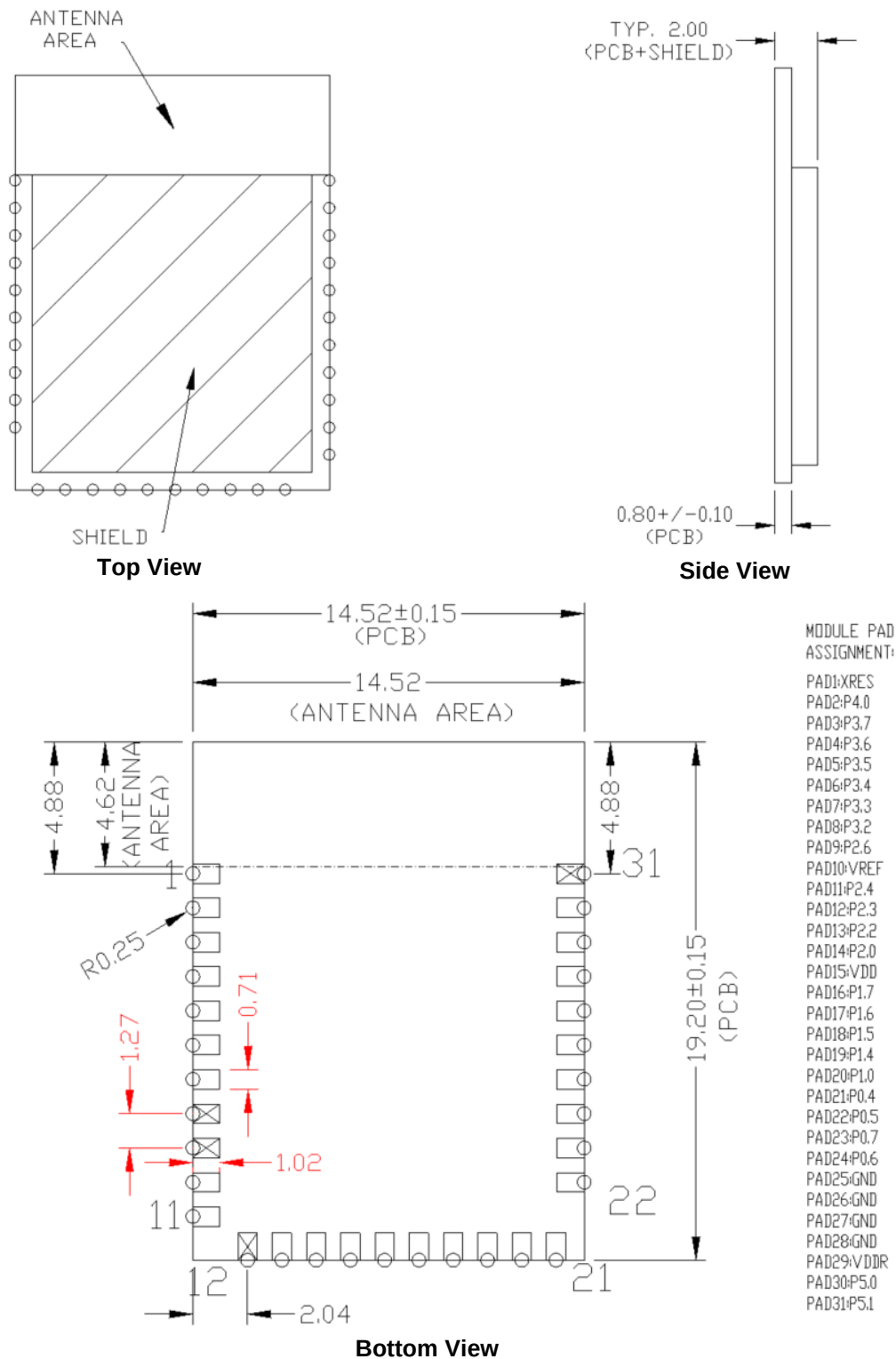
Cypress reserves the right to select components (including the appropriate BLE device) from various vendors to achieve the BLE module functionality. Such selections will still guarantee that all height restrictions of the component area are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in [Figure 1](#) on page 5. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	14.52 ± 0.15 mm
	Width (Y)	19.20 ± 0.15 mm
Antenna location dimensions	Length (X)	11.00 ± 0.15 mm
	Width (Y)	5.00 ± 0.15 mm
PCB thickness	Height (H)	0.80 ± 0.10 mm
Shield height	Height (H)	1.20 ± 0.10 mm
Maximum component height	Height (H)	1.20 mm typical (shield)
Total module thickness (bottom of module to highest component)	Height (H)	2.00 mm typical

See [Figure 1](#) on page 5 for the mechanical reference drawing for CYBLE-212020-01.

Figure 1. Module Mechanical Drawing



Note

1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see [Figure 3](#), [Figure 4](#), [Figure 5](#), and [Figure 6](#) and [Table 3](#).

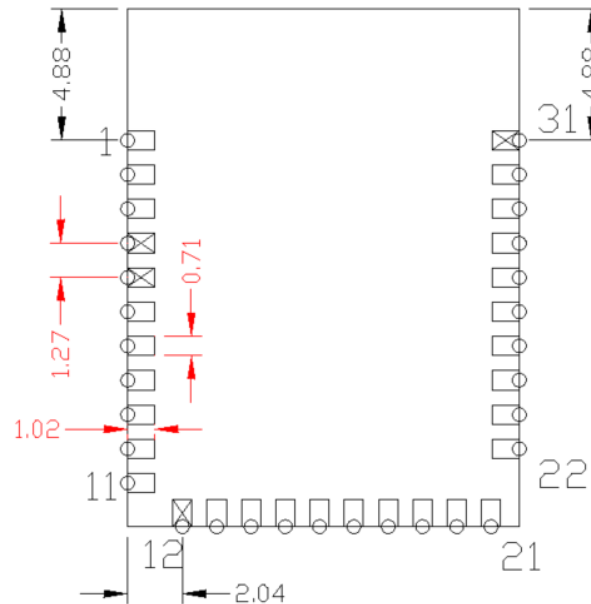
Pad Connection Interface

As shown in the bottom view of [Figure 1](#) on page 5, the CYBLE-212020-01 connects to the host board via solder pads on the back side of the module. [Table 2](#) and [Figure 2](#) detail the solder pad length, width, and pitch dimensions of the CYBLE-212020-01 module.

Table 2. Solder Pad Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	31	Solder Pads	1.02 mm	0.71 mm	1.27 mm

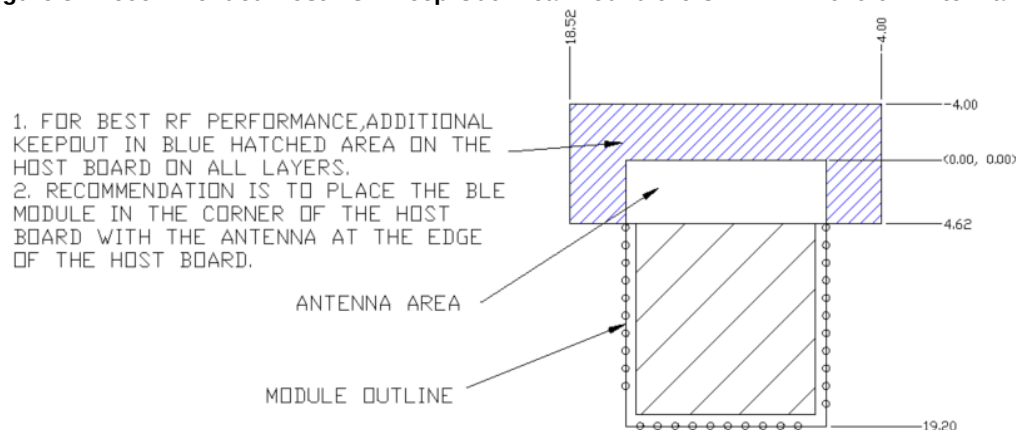
Figure 2. Solder Pad Dimensions (Seen from Bottom)



To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Cypress BLE module is in a corner of the host board with the trace antenna located at the far corner. This placement minimizes the additional recommended keep-out area stated in item 2. Refer to [AN96841](#) for module placement best practices.
2. To maximize RF performance, the area immediately around the Cypress BLE module trace antenna should contain an additional keep-out area, where no grounding or signal trace are contained. The keep-out area applies to all layers of the host board. The recommended dimensions of the host PCB keep-out area are shown in [Figure 3](#) (dimensions are in mm).

Figure 3. Recommended Host PCB Keep-Out Area Around the CYBLE-212020-01 Antenna

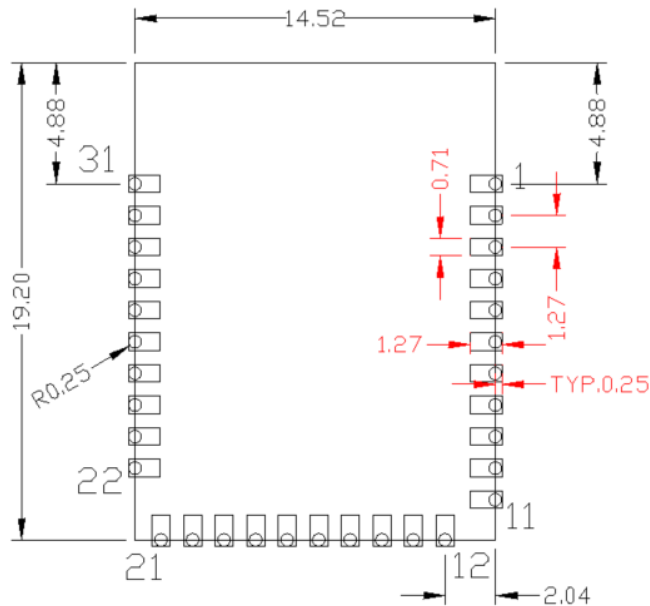


Host PCB Keep-Out Area Around Trace Antenna

Recommended Host PCB Layout

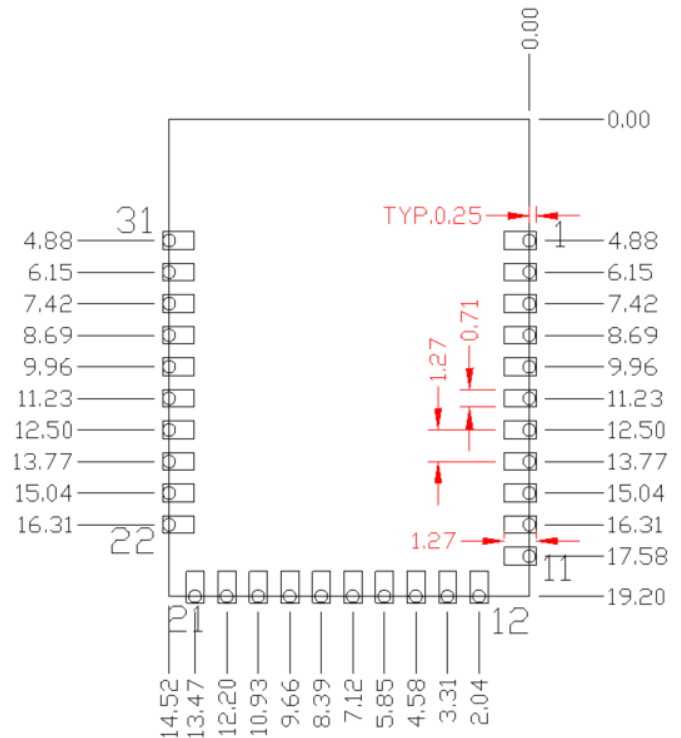
Figure 4, Figure 5, Figure 6, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBLE-212020-01. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.635 mm from center of the pad on either side) shown in Figure 6 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 4, Figure 5, or Figure 6. It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 4. Host Layout Pattern for CYBLE-212020-01



Top View (Seen on Host PCB)

Figure 5. Module Pad Location from Origin



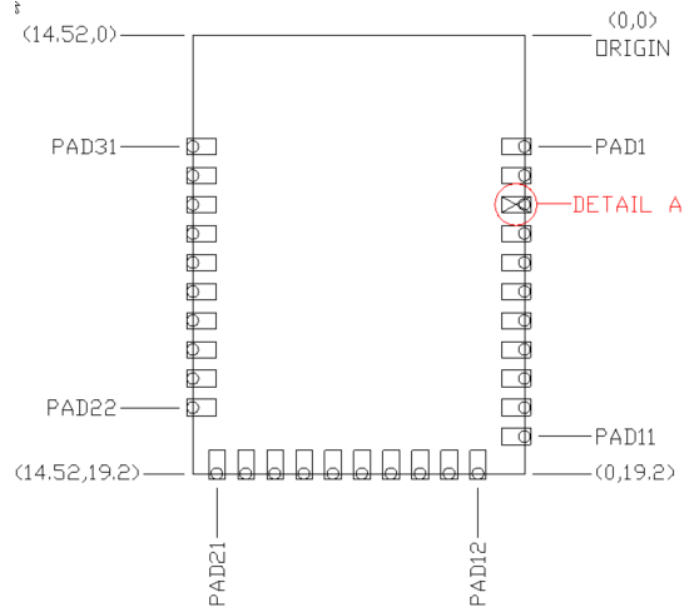
Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBLE-212020-01. All dimensions are referenced to the center of the solder pad. Refer to Figure 6 for the location of each module solder pad.

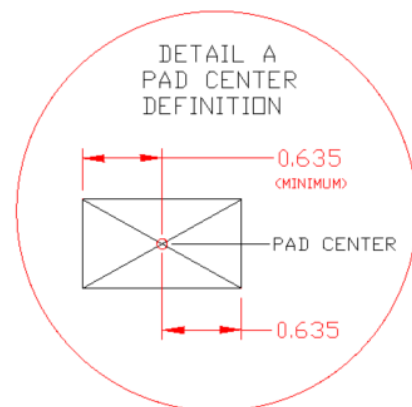
Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Orign (mm)	Dimension from Orign (mils)
1	(0.39, 4.88)	(15.35, 192.13)
2	(0.39, 6.15)	(15.35, 242.13)
3	(0.39, 7.42)	(15.35, 292.13)
4	(0.39, 8.69)	(15.35, 342.13)
5	(0.39, 9.96)	(15.35, 392.13)
6	(0.39, 11.23)	(15.35, 442.13)
7	(0.39, 12.50)	(15.35, 492.13)
8	(0.39, 13.77)	(15.35, 542.13)
9	(0.39, 15.04)	(15.35, 592.13)
10	(0.39, 16.31)	(15.35, 642.13)
11	(0.39, 17.58)	(15.35, 692.13)
12	(2.04, 18.82)	(80.31, 740.94)
13	(3.31, 18.82)	(130.31, 740.94)
14	(4.58, 18.82)	(180.31, 740.94)
15	(5.85, 18.82)	(230.31, 740.94)
16	(7.12, 18.82)	(280.31, 740.94)
17	(8.39, 18.82)	(330.31, 740.94)
18	(9.66, 18.82)	(380.31, 740.94)
19	(10.93, 18.82)	(430.31, 740.94)
20	(12.20, 18.82)	(480.31, 740.94)
21	(13.47, 18.82)	(530.31, 740.94)
22	(14.14, 16.31)	(556.69, 642.12)
23	(14.14, 15.04)	(556.69, 592.12)
24	(14.14, 13.77)	(556.69, 542.12)
25	(14.14, 12.50)	(556.69, 492.12)
26	(14.14, 11.23)	(556.69, 442.12)
27	(14.14, 9.96)	(556.69, 392.12)
28	(14.14, 8.69)	(556.69, 342.12)
29	(14.14, 7.42)	(556.69, 292.12)
30	(14.14, 6.15)	(556.69, 242.12)
31	(14.14, 4.88)	(556.69, 192.12)

Figure 6. Solder Pad Reference Location



Top View (Seen on Host PCB)



Digital and Analog Capabilities and Connections

Table 4 details the solder pad connection definitions and available functions for each connection pad. Table 4 lists the solder pads on CYBLE-212020-01, the BLE device port-pin, and denotes whether the function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

Table 4. Solder Pad Connection Definitions^[2]

Solder Pad Number	Device Port Pin	UART	SPI	I ² C	TCPWM ^[3,4]	CapSense	WCO Out	ECO Out	LCD	SWD	GPIO
1	XRES	External Reset Hardware Connection Input									
2	P4.0 ^[5]	✓(SCB1_RTS)	✓(SCB1_MOSI)		✓(TCPWM0_P)	✓(C _{MOD})			✓		✓
3	P3.7	✓(SCB1_CTS)			✓(TCPWM)	✓(Sensor)	✓		✓		✓
4	P3.6	✓(SCB1_RTS)			✓(TCPWM)	✓(Sensor)			✓		✓
5	P3.5	✓(SCB1_TX)		✓(SCB1_SCL)	✓(TCPWM)	✓(Sensor)			✓		✓
6	P3.4	✓(SCB1_RX)		✓(SCB1_SDA)	✓(TCPWM)	✓(Sensor)			✓		✓
7	P3.3	✓(SCB0_CTS)			✓(TCPWM)	✓(Sensor)			✓		✓
8	P3.2	✓(SCB0_RTS)			✓(TCPWM)	✓(Sensor)			✓		✓
9	P2.6				✓(TCPWM)	✓(Sensor)			✓		✓
10	VREF	Reference Voltage Input (Optional)									
11	P2.4				✓(TCPWM)	✓(Sensor)			✓		✓
12	P2.3				✓(TCPWM)	✓(Sensor)	✓		✓		✓
13	P2.2		✓(SCB0_SS3)		✓(TCPWM)	✓(Sensor)			✓		✓
14	P2.0		✓(SCB0_SS1)		✓(TCPWM)	✓(Sensor)			✓		✓
15	V _{DD}	Digital Power Supply Input (1.8 V to 5.5 V)									
16	P1.7	✓(SCB0_CTS)	✓(SCB0_SCLK)		✓(TCPWM)	✓(Sensor)			✓		✓
17	P1.6	✓(SCB0_RTS)	✓(SCB0_SS0)		✓(TCPWM)	✓(Sensor)			✓		✓
18	P1.5	✓(SCB0_TX)	✓(SCB0_MISO)	✓(SCB0_SCL)	✓(TCPWM)	✓(Sensor)			✓		✓
19	P1.4	✓(SCB0_RX)	✓(SCB0_MOSI)	✓(SCB0_SDA)	✓(TCPWM)	✓(Sensor)			✓		✓
20	P1.0				✓(TCPWM)	✓(Sensor)			✓		✓
21	P0.4	✓(SCB0_RX)	✓(SCB0_MOSI)	✓(SCB0_SDA)	✓(TCPWM)	✓(Sensor)		✓	✓		✓
22	P0.5	✓(SCB0_TX)	✓(SCB0_MISO)	✓(SCB0_SCL)	✓(TCPWM)	✓(Sensor)			✓		✓
23	P0.7	✓(SCB0_CTS)	✓(SCB0_SCLK)		✓(TCPWM)	✓(Sensor)			✓	✓(SWDCLK)	✓
24	P0.6	✓(SCB0_RTS)	✓(SCB0_SS0)		✓(TCPWM)	✓(Sensor)			✓	✓(SWDIO)	✓
25	GND ^[6]	Ground Connection									
26	GND ^[6]	Ground Connection									
27	GND ^[6]	Ground Connection									
28	GND ^[6]	Ground Connection									
29	V _{DDR}	Radio Power Supply (1.9 V to 5.5 V)									
30	P5.0	✓(SCB1_RX)	✓(SCB1_SS0)	✓(SCB1_SDA)	✓(TCPWM3_P)	✓(Sensor)			✓		✓
31	P5.1	✓(SCB1_TX)	✓(SCB1_SCLK)	✓(SCB1_SCL)	✓(TCPWM3_N)	✓(Sensor)		✓	✓		✓

Notes

- If the I²S feature is used in the design, the I²S pins shall be dynamically routed to the appropriate available GPIO by PSoC Creator.
- TCPWM: Timer, Counter, and Pulse Width Modulator. If supported, the pad can be configured to any of these peripheral functions.
- TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.
- When using the capacitive sensing functionality, Pad 2 (P4.0) must be connected to a C_{MOD} capacitor (located off of Cypress BLE Module). The value of this capacitor is 2.2 nF and should be placed as close to the module as possible.
- The main board needs to connect all GND connections (Pad 25/26/27/28) on the module to the common ground of the system.

Power Supply Connections and Recommended External Components

Power Connections

The CYBLE-212020-01 contains two power supply connections, VDD and VDDR. The VDD connection supplies power for both digital and analog device operation. The VDDR connection supplies power for the device radio.

VDD accepts a supply range of 1.71 V to 5.5 V. VDDR accepts a supply range of 1.9 V to 5.5 V. These specifications are listed in Table 9. The maximum power supply ripple for both power connections on the module is 100 mV, as shown in Table 7.

The power supply ramp rate of VDD must be equal to or greater than that of VDDR.

Connection Options

Two connection options are available for any application:

1. Single supply: Connect VDD and VDDR to the same supply.
2. Independent supply: Power VDD and VDDR separately.

External Component Recommendation

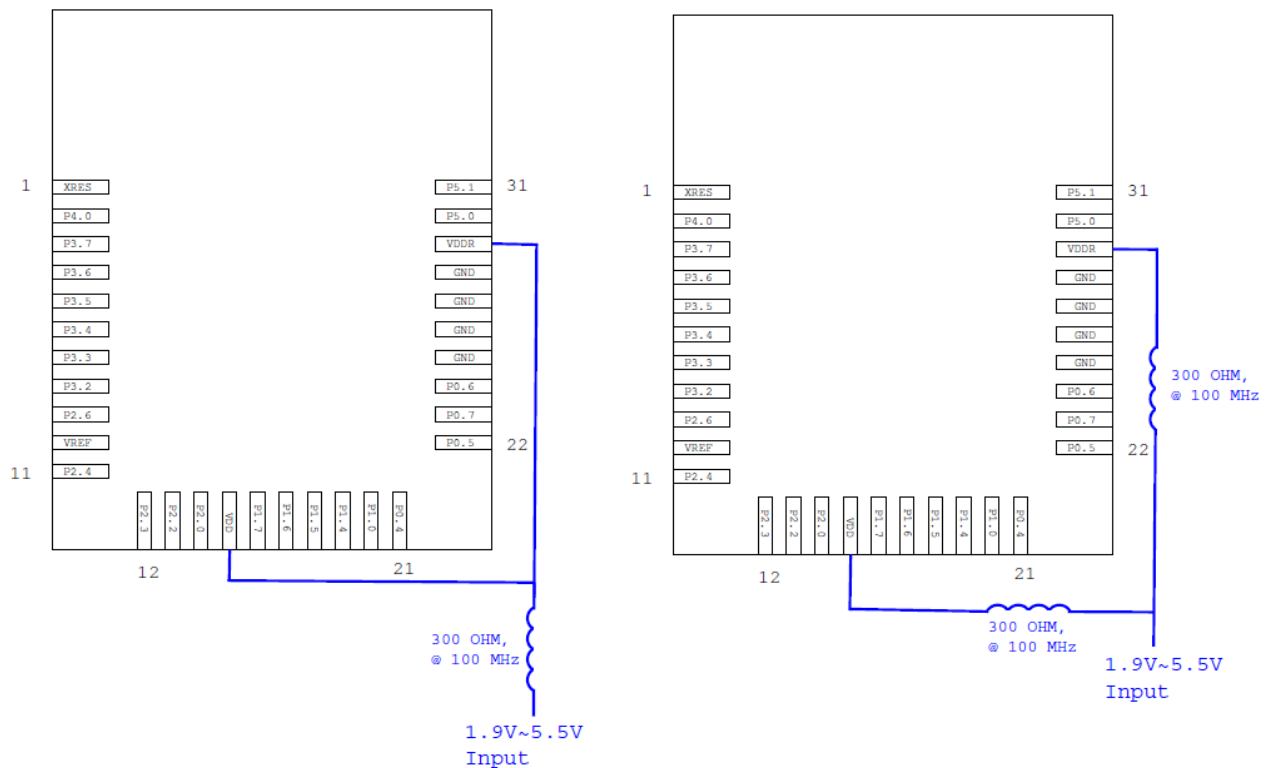
In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pin connection.

Figure 7 details the recommended host schematic options for a single supply scenario. The use of one or two ferrite beads will depend on the specific application and configuration of the CYBLE-212020-01.

Figure 8 details the recommended host schematic for an independent supply scenario.

The recommended ferrite bead value is 330 Ω , 100 MHz. (Murata BLM21PG331SN1D).

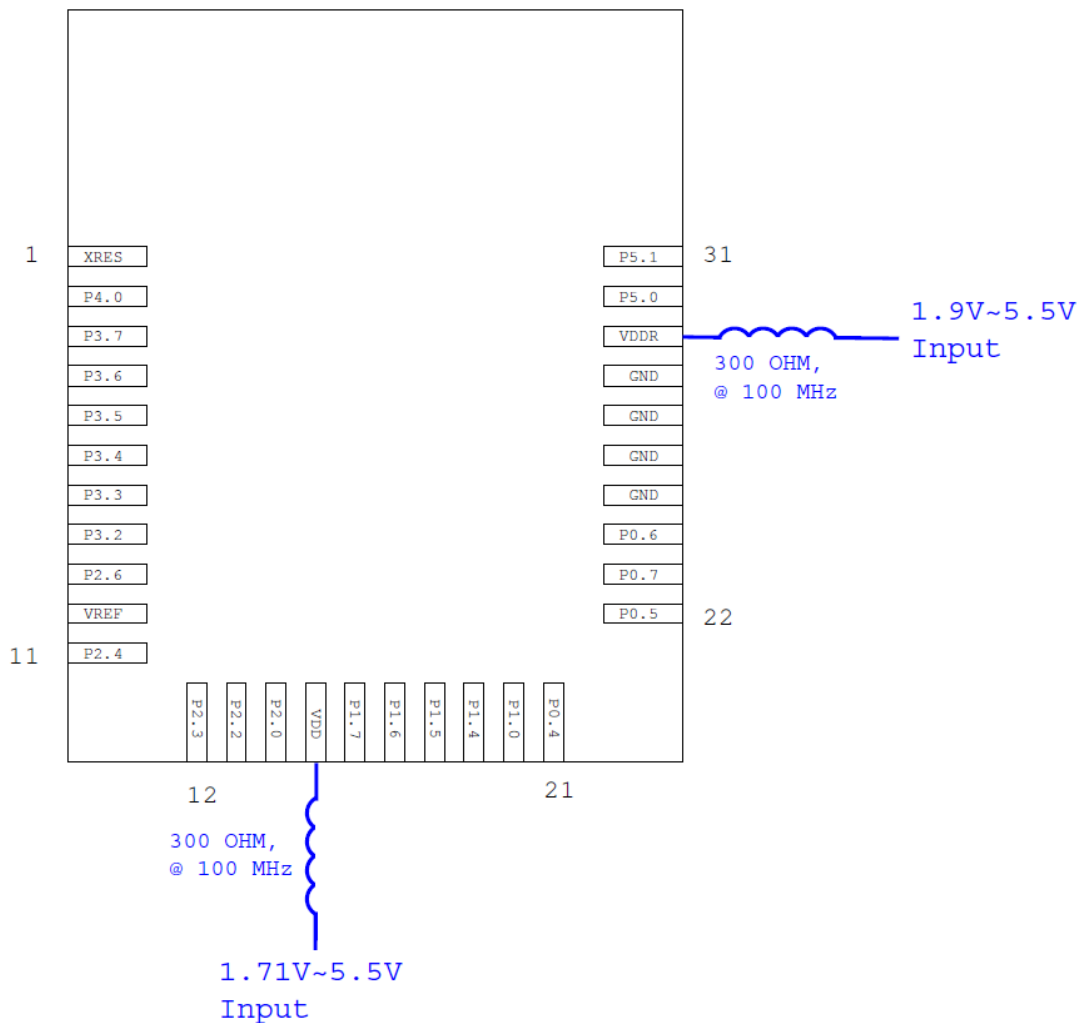
Figure 7. Recommended Host Schematic Options for a Single Supply Option



Single Ferrite Bead Option (Seen from Bottom)

Two Ferrite Bead Option (Seen from Bottom)

Figure 8. Recommended Host Schematic for an Independent Supply Option



Independent Power Supply Option (Seen from Bottom)

Figure 9. CYBLE-212020-01 Schematic Diagram



Critical Components List

Table 5 details the critical components used in the CYBLE-212020-01 module.

Table 5. Critical Component List

Component	Reference Designator	Description
Silicon	U1	56-pin QFN PProC with BLE
Crystal	Y1	24.000 MHz, 12PF
Crystal	Y2	32.768 kHz, 12.5PF

Antenna Design

Table 6 details trace antenna used in the CYBLE-212020-01 module. For more information, see Table 8.

Table 6. Trace Antenna Specifications

Item	Description
Frequency Range	2400–2500 MHz
Peak Gain	0.5-dBi typical
Average Gain	-0.5-dBi typical
Return Loss	10-dB minimum

Electrical Specifications

Table 7 details the absolute maximum electrical characteristics for the Cypress BLE module.

Table 7. CYBLE-212020-01 Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V _{DDD_ABS}	Analog, digital, or radio supply relative to V _{SS} (V _{SSD} = V _{SSA})	−0.5	–	6	V	Absolute maximum
V _{CCD_ABS}	Direct digital core voltage input relative to V _{SSD}	−0.5	–	1.95	V	Absolute maximum
V _{DD_RIPPLE}	Maximum power supply ripple for V _{DD} and V _{DDR} input voltage	–	–	100	mV	3.0-V supply Ripple frequency of 100 kHz to 750 kHz
V _{GPIO_ABS}	GPIO voltage	−0.5	–	V _{DD} + 0.5	V	Absolute maximum
I _{GPIO_ABS}	Maximum current per GPIO	−25	–	25	mA	Absolute maximum
I _{GPIO_injection}	GPIO injection current: Maximum for V _{IH} > V _{DD} and minimum for V _{IL} < V _{SS}	−0.5	–	0.5	mA	Absolute maximum current injected per pin
LU	Pin current for latch-up	−200		200	mA	–

Table 8 details the RF characteristics for the Cypress BLE module.

Table 8. CYBLE-212020-01 RF Performance Characteristics

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
RF _O	RF output power on ANT	−18	0	3	dBm	Configurable via register settings
RX _S	RF receive sensitivity on ANT	–	−87	–	dBm	Guaranteed by design simulation
F _R	Module frequency range	2400	–	2480	MHz	–
G _P	Peak gain	–	0.5	–	dBi	–
G _{Avg}	Average gain	–	−0.5	–	dBi	–
RL	Return loss	–	−10.5	–	dB	–

Table 9 through Table 48 list the module level electrical characteristics for the CYBLE-212020-01. All specifications are valid for −40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 9. CYBLE-212020-01 DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V _{DD1}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
V _{DD2}	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregulated supply
V _{DDR1}	Radio supply voltage (radio on)	1.9	–	5.5	V	–
V _{DDR2}	Radio supply voltage (radio off)	1.71	–	5.5	V	–
Active Mode, V_{DD} = 1.71 V to 5.5 V						
I _{DD3}	Execute from flash; CPU at 3 MHz	–	1.7	–	mA	T = 25 °C, V _{DD} = 3.3 V
I _{DD4}	Execute from flash; CPU at 3 MHz	–	–	–	mA	T = −40 °C to 85 °C
I _{DD5}	Execute from flash; CPU at 6 MHz	–	2.5	–	mA	T = 25 °C, V _{DD} = 3.3 V
I _{DD6}	Execute from flash; CPU at 6 MHz	–	–	–	mA	T = −40 °C to 85 °C
I _{DD7}	Execute from flash; CPU at 12 MHz	–	4	–	mA	T = 25 °C, V _{DD} = 3.3 V
I _{DD8}	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = −40 °C to 85 °C

Table 9. CYBLE-212020-01 DC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I _{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V _{DD} = 3.3 V
I _{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
I _{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V _{DD} = 3.3 V
I _{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
Sleep Mode, V_{DD} = 1.8 V to 5.5 V						
I _{DD13}	IMO on	–	–	–	mA	T = 25 °C, V _{DD} = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 1.9 V to 5.5 V						
I _{DD14}	ECO on	–	–	–	mA	T = 25 °C, V _{DD} = 3.3 V, SYSCLK = 3 MHz
Deep-Sleep Mode, V_{DD} = 1.8 V to 3.6 V						
I _{DD15}	WDT with WCO on	–	1.5	–	μA	T = 25 °C, V _{DD} = 3.3 V
I _{DD16}	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
I _{DD17}	WDT with WCO on	–	–	–	μA	T = 25 °C, V _{DD} = 5 V
I _{DD18}	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
Deep-Sleep Mode, V_{DD} = 1.71 V to 1.89 V (Regulator Bypassed)						
I _{DD19}	WDT with WCO on	–	–	–	μA	T = 25 °C
I _{DD20}	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.8 V to 3.6 V						
I _{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V _{DD} = 3.3 V
I _{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 3.6 V to 5.5 V						
I _{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V _{DD} = 5 V
I _{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.8 V to 3.6 V						
I _{DD33}	Stop-mode current (V _{DD})	–	20	–	nA	T = 25 °C, V _{DD} = 3.3 V
I _{DD34}	Stop-mode current (V _{DDR})	–	40	–	nA	T = 25 °C, V _{DDR} = 3.3 V
I _{DD35}	Stop-mode current (V _{DD})	–	–	–	nA	T = –40 °C to 85 °C
I _{DD36}	Stop-mode current (V _{DDR})	–	–	–	nA	T = –40 °C to 85 °C, V _{DDR} = 1.9 V to 3.6 V
Stop Mode, V_{DD} = 3.6 V to 5.5 V						
I _{DD37}	Stop-mode current (V _{DD})	–	–	–	nA	T = 25 °C, V _{DD} = 5 V
I _{DD38}	Stop-mode current (V _{DDR})	–	–	–	nA	T = 25 °C, V _{DDR} = 5 V
I _{DD39}	Stop-mode current (V _{DD})	–	–	–	nA	T = –40 °C to 85 °C
I _{DD40}	Stop-mode current (V _{DDR})	–	–	–	nA	T = –40 °C to 85 °C

Table 10. AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$
T_{SLEEP}	Wakeup from Sleep mode	–	0	–	μs	Guaranteed by characterization
$T_{DEEPSLEEP}$	Wakeup from Deep-Sleep mode	–	–	25	μs	24-MHz IMO. Guaranteed by characterization
$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	2	ms	Guaranteed by characterization
T_{STOP}	Wakeup from Stop mode	–	–	2	ms	XRES wakeup

GPIO
Table 11. GPIO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{IH}^{[7]}$	Input voltage HIGH threshold	$0.7 \times V_{DD}$	–	–	V	CMOS input
	LVTTL input, $V_{DD} < 2.7\text{ V}$	$0.7 \times V_{DD}$	–	–	V	–
	LVTTL input, $V_{DD} \geq 2.7\text{ V}$	2.0	–	–	V	–
V_{IL}	Input voltage LOW threshold	–	–	$0.3 \times V_{DD}$	V	CMOS input
	LVTTL input, $V_{DD} < 2.7\text{ V}$	–	–	$0.3 \times V_{DD}$	V	–
	LVTTL input, $V_{DD} \geq 2.7\text{ V}$	–	–	0.8	V	–
V_{OH}	Output voltage HIGH level	$V_{DD} - 0.6$	–	–	V	$I_{OH} = 4\text{ mA}$ at 3.3-V V_{DD}
	Output voltage HIGH level	$V_{DD} - 0.5$	–	–	V	$I_{OH} = 1\text{ mA}$ at 1.8-V V_{DD}
V_{OL}	Output voltage LOW level	–	–	0.6	V	$I_{OL} = 8\text{ mA}$ at 3.3-V V_{DD}
	Output voltage LOW level	–	–	0.6	V	$I_{OL} = 4\text{ mA}$ at 1.8-V V_{DD}
	Output voltage LOW level	–	–	0.4	V	$I_{OL} = 3\text{ mA}$ at 3.3-V V_{DD}
R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, $V_{DD} = 3.3\text{ V}$
I_{IL_CTBM}	Input leakage on CTBM input pins	–	–	4	nA	–
C_{IN}	Input capacitance	–	–	7	pF	–
V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DD} > 2.7\text{ V}$
$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–	1	–
I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μA	–
I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Note

 7. V_{IH} must not exceed $V_{DD} + 0.2\text{ V}$.

Table 12. GPIO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RISEF}	Rise time in Fast-Strong mode	2	—	12	ns	3.3-V V_{DD} , $C_{LOAD} = 25$ pF
T_{FALLF}	Fall time in Fast-Strong mode	2	—	12	ns	3.3-V V_{DD} , $C_{LOAD} = 25$ pF
T_{RISES}	Rise time in Slow-Strong mode	10	—	60	ns	3.3-V V_{DD} , $C_{LOAD} = 25$ pF
T_{FALLS}	Fall time in Slow-Strong mode	10	—	60	ns	3.3-V V_{DD} , $C_{LOAD} = 25$ pF
F_{GPIO1}	GPIO F_{OUT} ; $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Fast-Strong mode	—	—	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
F_{GPIO2}	GPIO F_{OUT} ; $1.7\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ Fast-Strong mode	—	—	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
F_{GPIO3}	GPIO F_{OUT} ; $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Slow-Strong mode	—	—	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
F_{GPIO4}	GPIO F_{OUT} ; $1.7\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ Slow-Strong mode	—	—	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
F_{GPIOIN}	GPIO input operating frequency $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	—	—	48	MHz	90/10% V_{IO}

Table 13. OVT GPIO DC Specifications (P5_0 and P5_1 Only)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{IL}	Input leakage (absolute value). $V_{IH} > V_{DD}$	—	—	10	μA	25°C, $V_{DD} = 0\text{ V}$, $V_{IH} = 3.0\text{ V}$
V_{OL}	Output voltage LOW level	—	—	0.4	V	$I_{OL} = 20\text{ mA}$, $V_{DD} > 2.9\text{ V}$

Table 14. OVT GPIO AC Specifications (P5_0 and P5_1 Only)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RISE_OVFS}	Output rise time in Fast-Strong mode	1.5	—	12	ns	25-pF load, 10%–90%, $V_{DD} = 3.3\text{ V}$
T_{FALL_OVFS}	Output fall time in Fast-Strong mode	1.5	—	12	ns	25-pF load, 10%–90%, $V_{DD} = 3.3\text{ V}$
T_{RISESS}	Output rise time in Slow-Strong mode	10	—	60	ns	25-pF load, 10%-90%, $V_{DD} = 3.3\text{ V}$
T_{FALLSS}	Output fall time in Slow-Strong mode	10	—	60	ns	25-pF load, 10%-90%, $V_{DD} = 3.3\text{ V}$
F_{GPIO1}	GPIO F_{OUT} ; $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Fast-Strong mode	—	—	24	MHz	90/10%, 25-pF load, 60/40 duty cycle
F_{GPIO2}	GPIO F_{OUT} ; $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ Fast-Strong mode	—	—	16	MHz	90/10%, 25-pF load, 60/40 duty cycle

XRES

Table 15. XRES DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}	Input voltage HIGH threshold	$0.7 \times V_{DD}$	—	—	V	CMOS input
V_{IL}	Input voltage LOW threshold	—	—	$0.3 \times V_{DD}$	V	CMOS input
R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	—
C_{IN}	Input capacitance	—	3	—	pF	—
$V_{HYSXRES}$	Input voltage hysteresis	—	100	—	mV	—
I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	—	—	100	μA	—

Table 16. XRES AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{RESETWIDTH}	Reset pulse width	1	–	–	μs	–

Temperature Sensor

Table 17. Temperature Sensor Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{SENSACC}	Temperature-sensor accuracy	–5	±1	5	°C	–40 to +85 °C

SAR ADC

Table 18. SAR ADC DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_RES	Resolution	–	–	12	bits	
A_CHNIS_S	Number of channels - single-ended	–	–	8		8 full-speed ^[8]
A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O ^[8]
A-MONO	Monotonicity	–	–	–		Yes
A_GAINERR	Gain error	–	–	±0.1	%	With external reference
A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V _{REF}
A_ISAR	Current consumption	–	–	1	mA	
A_VINS	Input voltage range - single-ended	V _{SS}	–	V _{DDA}	V	
A_VIND	Input voltage range - differential	V _{SS}	–	V _{DDA}	V	
A_INRES	Input resistance	–	–	2.2	kΩ	
A_INCAP	Input capacitance	–	–	10	pF	
VREFSAR	Trimmed internal reference to SAR	–1	–	1	%	Percentage of V _{bg} (1.024 V)

Table 19. SAR ADC AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_PSRR	Power-supply rejection ratio	70	–	–	dB	Measured at 1-V reference
A_CMRR	Common-mode rejection ratio	66	–	–	dB	
A_SAMP	Sample rate	–	–	1	MSPS	
F _{sarintref}	SAR operating speed without external ref. bypass	–	–	100	ksps	12-bit resolution
A_SNR	Signal-to-noise ratio (SNR)	65	–	–	dB	F _{IN} = 10 kHz
A_BW	Input bandwidth without aliasing	–	–	A_SAMP/2	kHz	
A_INL	Integral nonlinearity. V _{DD} = 1.71 V to 5.5 V, 1 MSPS	–1.7	–	2	LSB	V _{REF} = 1 V to V _{DD}
A_INL	Integral nonlinearity. V _{DD} = 1.71 V to 3.6 V, 1 MSPS	–1.5	–	1.7	LSB	V _{REF} = 1.71 V to V _{DD}
A_INL	Integral nonlinearity. V _{DD} = 1.71 V to 5.5 V, 500 ksps	–1.5	–	1.7	LSB	V _{REF} = 1 V to V _{DD}

Note

8. A maximum of eight single-ended ADC Channels can be accomplished only if the AMUX Buses are not being used for other functionality (such as CapSense). If the AMUX Buses are being used for other functions, then the maximum number of single-ended ADC channels is six. Similarly, if the AMUX Buses are being used for other functionality, then the maximum number of differential ADC channels is three.

Table 19. SAR ADC AC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_dnl	Differential nonlinearity. $V_{DD} = 1.71\text{ V}$ to 5.5 V , 1 Msps	-1	—	2.2	LSB	$V_{REF} = 1\text{ V}$ to V_{DD}
A_DNL	Differential nonlinearity. $V_{DD} = 1.71\text{ V}$ to 3.6 V , 1 Msps	-1	—	2	LSB	$V_{REF} = 1.71\text{ V}$ to V_{DD}
A_DNL	Differential nonlinearity. $V_{DD} = 1.71\text{ V}$ to 5.5 V , 500 kps	-1	—	2.2	LSB	$V_{REF} = 1\text{ V}$ to V_{DD}
A_THD	Total harmonic distortion	—	—	-65	dB	$F_{IN} = 10\text{ kHz}$

CSD

CSD Block Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{CSD}	Voltage range of operation	1.71	—	5.5	V	
IDAC1	DNL for 8-bit resolution	-1	—	1	LSB	
IDAC1	INL for 8-bit resolution	-3	—	3	LSB	
IDAC2	DNL for 7-bit resolution	-1	—	1	LSB	
IDAC2	INL for 7-bit resolution	-3	—	3	LSB	
SNR	Ratio of counts of finger to noise	5	—	—	Ratio	Capacitance range of 9 pF to 35 pF, 0.1-pF sensitivity. Radio is not operating during the scan
I_{DAC1_CRT1}	Output current of IDAC1 (8 bits) in High range	—	612	—	μA	
I_{DAC1_CRT2}	Output current of IDAC1 (8 bits) in Low range	—	306	—	μA	
I_{DAC2_CRT1}	Output current of IDAC2 (7 bits) in High range	—	305	—	μA	
I_{DAC2_CRT2}	Output current of IDAC2 (7 bits) in Low range	—	153	—	μA	

Digital Peripherals

Timer

Table 20. Timer DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{TIM1}	Block current consumption at 3 MHz	—	—	42	μA	16-bit timer
I_{TIM2}	Block current consumption at 12 MHz	—	—	130	μA	16-bit timer
I_{TIM3}	Block current consumption at 48 MHz	—	—	535	μA	16-bit timer

Table 21. Timer AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{TIMFREQ}$	Operating frequency	F_{CLK}	—	48	MHz	
$T_{CAPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	—	—	ns	
$T_{CAPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	—	—	ns	
T_{TIMRES}	Timer resolution	T_{CLK}	—	—	ns	
$T_{TENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	—	—	ns	

Table 21. Timer AC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{TENWIDEXT}	Enable pulse width (external)	2 × T _{CLK}	–	–	ns	
T _{TIMRESWINT}	Reset pulse width (internal)	2 × T _{CLK}	–	–	ns	
T _{TIMRESEXT}	Reset pulse width (external)	2 × T _{CLK}	–	–	ns	

Counter

Table 22. Counter DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I _{CTR1}	Block current consumption at 3 MHz	–	–	42	μA	16-bit counter
I _{CTR2}	Block current consumption at 12 MHz	–	–	130	μA	16-bit counter
I _{CTR3}	Block current consumption at 48 MHz	–	–	535	μA	16-bit counter

Table 23. Counter AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{CTRFREQ}	Operating frequency	F _{CLK}	–	48	MHz	
T _{CTRPWINT}	Capture pulse width (internal)	2 × T _{CLK}	–	–	ns	
T _{CTRPWEXT}	Capture pulse width (external)	2 × T _{CLK}	–	–	ns	
T _{CTRES}	Counter Resolution	T _{CLK}	–	–	ns	
T _{CENWIDINT}	Enable pulse width (internal)	2 × T _{CLK}	–	–	ns	
T _{CENWIDEXT}	Enable pulse width (external)	2 × T _{CLK}	–	–	ns	
T _{CTRRESWINT}	Reset pulse width (internal)	2 × T _{CLK}	–	–	ns	
T _{CTRRESWEXT}	Reset pulse width (external)	2 × T _{CLK}	–	–	ns	

Pulse Width Modulation (PWM)

Table 24. PWM DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I _{PWM1}	Block current consumption at 3 MHz	–	–	42	μA	16-bit PWM
I _{PWM2}	Block current consumption at 12 MHz	–	–	130	μA	16-bit PWM
I _{PWM3}	Block current consumption at 48 MHz	–	–	535	μA	16-bit PWM

Table 25. PWM AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{PWMFREQ}	Operating frequency	F _{CLK}	–	48	MHz	
T _{PWMPWINT}	Pulse width (internal)	2 × T _{CLK}	–	–	ns	
T _{PWMEXT}	Pulse width (external)	2 × T _{CLK}	–	–	ns	
T _{PWMKILLINT}	Kill pulse width (internal)	2 × T _{CLK}	–	–	ns	
T _{PWMKILLEXT}	Kill pulse width (external)	2 × T _{CLK}	–	–	ns	
T _{PWMEINT}	Enable pulse width (internal)	2 × T _{CLK}	–	–	ns	
T _{PWMENEXT}	Enable pulse width (external)	2 × T _{CLK}	–	–	ns	
T _{PWMRESWINT}	Reset pulse width (internal)	2 × T _{CLK}	–	–	ns	
T _{PWMRESWEXT}	Reset pulse width (external)	2 × T _{CLK}	–	–	ns	

LCD Direct Drive

Table 26. LCD Direct Drive DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{LCDLOW}	Operating current in low-power mode	–	17.5	–	μA	16 × 4 small segment display at 50 Hz
C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	
LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	
I_{LCDOP1}	LCD system operating current $V_{BIAS} = 5\text{ V}$	–	2	–	mA	32 × 4 segments. 50 Hz at 25 °C
I_{LCDOP2}	LCD system operating current $V_{BIAS} = 3.3\text{ V}$	–	2	–	mA	32 × 4 segments 50 Hz at 25 °C

Table 27. LCD Direct Drive AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{LCD}	LCD frame rate	10	50	150	Hz	

Serial Communication

Table 28. Fixed I²C DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{I2C1}	Block current consumption at 100 kHz	–	–	50	μA	–
I_{I2C2}	Block current consumption at 400 kHz	–	–	155	μA	–
I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	μA	–
I_{I2C4}	I ² C enabled in Deep-Sleep mode	–	–	1.4	μA	–

Table 29. Fixed I²C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{I2C1}	Bit rate	–	–	400	kHz	

Table 30. Fixed UART DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{UART1}	Block current consumption at 100 kbps	–	–	55	μA	–
I_{UART2}	Block current consumption at 1000 kbps	–	–	312	μA	–

Table 31. Fixed UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{UART}	Bit rate	–	–	1	Mbps	–

Table 32. Fixed SPI DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	μA	–
I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	μA	–
I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	μA	–

Table 33. Fixed SPI AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{SPI}	SPI operating frequency (master; 6x over sampling)	–	–	8	MHz	–

Table 34. Fixed SPI Master Mode AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{DMO}	MOSI valid after SCLK driving edge	–	–	18	ns	–
T _{DSI}	MISO valid before SCLK capturing edge Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
T _{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 35. Fixed SPI Slave Mode AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{DMI}	MOSI valid before SCLK capturing edge	40	–	–	ns	
T _{DSO}	MISO valid after SCLK driving edge	–	–	42 + 3 × T _{CPU}	ns	
T _{DSO_ext}	MISO Valid after SCLK driving edge in external clock mode. V _{DD} < 3.0 V	–	–	50	ns	
T _{HSO}	Previous MISO data hold time	0	–	–	ns	
T _{SSELSCK}	SSEL valid to first SCK valid edge	100	–	–	ns	

Memory

Table 36. Flash DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V _{PE}	Erase and program voltage	1.71	–	5.5	V	–
T _{WS48}	Number of Wait states at 32–48 MHz	2	–	–		CPU execution from flash
T _{WS32}	Number of Wait states at 16–32 MHz	1	–	–		CPU execution from flash
T _{WS16}	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

Table 37. Flash AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{ROWWRITE} ^[9]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
T _{ROWERASE} ^[9]	Row erase time	–	–	13	ms	–
T _{ROWPROGRAM} ^[9]	Row program time after erase	–	–	7	ms	–
T _{BULKERASE} ^[9]	Bulk erase time (256 KB)	–	–	35	ms	–
T _{DEVPROG} ^[9]	Total device program time	–	–	25	seconds	–
F _{END}	Flash endurance	100 K	–	–	cycles	–
F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	years	–
F _{RET2}	Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–	years	–

Note

9. It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources

Power-on-Reset (POR)

Table 38. POR DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V _{RISEIPOR}	Rising trip voltage	0.80	–	1.45	V	–
V _{FALLIPOR}	Falling trip voltage	0.75	–	1.40	V	–
V _{IPORHYST}	Hysteresis	15	–	200	mV	–

Table 39. POR AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{PPOR_TR}	Precision power-on reset (PPOR) response time in Active and Sleep modes	–	–	1	μs	–

Table 40. Brown-Out Detect

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V _{FALLPPOR}	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	–
V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.4	–	–	V	–

Table 41. Hibernate Reset

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V _{HBRTRIP}	BOD trip voltage in Hibernate	1.1	–	–	V	–

Voltage Monitors (LVD)

Table 42. Voltage Monitor DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V _{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
V _{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
V _{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
V _{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
V _{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
V _{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
V _{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
V _{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
V _{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
V _{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
V _{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
V _{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
V _{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
V _{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
V _{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
V _{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
LVI_IDD	Block current	–	–	100	μA	–

Table 43. Voltage Monitor AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{MONTRIP}	Voltage monitor trip time	–	–	1	μs	–

SWD Interface

Table 44. SWD Interface Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_SWCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK $\leq$ 1/3 CPU clock frequency
F_SWCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK $\leq$ 1/3 CPU clock frequency
T_SWDI_SETUP	$T = 1/f\text{ SWDCLK}$	$0.25 \times T$	–	–	ns	–
T_SWDI_HOLD	$T = 1/f\text{ SWDCLK}$	$0.25 \times T$	–	–	ns	–
T_SWDO_VALID	$T = 1/f\text{ SWDCLK}$	–	–	$0.5 \times T$	ns	–
T_SWDO_HOLD	$T = 1/f\text{ SWDCLK}$	1	–	–	ns	–

Internal Main Oscillator

Table 45. IMO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I _{IMO1}	IMO operating current at 48 MHz	–	–	1000	μA	–
I _{IMO2}	IMO operating current at 24 MHz	–	–	325	μA	–
I _{IMO3}	IMO operating current at 12 MHz	–	–	225	μA	–
I _{IMO4}	IMO operating current at 6 MHz	–	–	180	μA	–
I _{IMO5}	IMO operating current at 3 MHz	–	–	150	μA	–

Table 46. IMO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F _{IMOTOL3}	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
F _{IMOTOL3}	IMO startup time	–	12	–	μs	–

Internal Low-Speed Oscillator

Table 47. ILO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I _{ILO2}	ILO operating current at 32 kHz	–	0.3	1.05	μA	–

Table 48. ILO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T _{STARTILO1}	ILO startup time	–	–	2	ms	–
F _{ILOTRIM1}	32-kHz trimmed frequency	15	32	50	kHz	–

Table 49. Recommended ECO Trim Value

Parameter	Description	Value	Details/Conditions
ECO _{TRIM}	24-MHz trim value (firmware configuration)	0x0000BCBC	Recommended trim value that needs to be loaded to register CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG

BLE Subsystem

Table 50. BLE Subsystem

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
RF Receiver Specification						
RXS, IDLE	RX sensitivity with idle transmitter	–	–89	–	dBm	
	RX sensitivity with idle transmitter excluding Balun loss	–	–91	–	dBm	Guaranteed by design simulation
RXS, DIRTY	RX sensitivity with dirty transmitter	–	–87	–70	dBm	RF-PHY Specification (RCV-LE/CA/01/C)
RXS, HIGHGAIN	RX sensitivity in high-gain mode with idle transmitter	–	–91	–	dBm	
PRXMAX	Maximum input power	–10	–1	–	dBm	RF-PHY Specification (RCV-LE/CA/06/C)
CI1	Cochannel interference, Wanted signal at –67 dBm and Interferer at FRX	–	9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI2	Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±1 MHz	–	3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI3	Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±2 MHz	–	–29	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI4	Adjacent channel interference Wanted signal at –67 dBm and Interferer at ≥FRX ±3 MHz	–	–39	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI5	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (F _{IMAGE})	–	–20	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI3	Adjacent channel interference Wanted signal at –67 dBm and Interferer at Image frequency (F _{IMAGE} ± 1 MHz)	–	–30	–	dB	RF-PHY Specification (RCV-LE/CA/03/C)
OBB1	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 30–2000 MHz	–30	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
OBB2	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 2003–2399 MHz	–35	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
OBB3	Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 2484–2997 MHz	–35	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
OBB4	Out-of-band blocking, Wanted signal a –67 dBm and Interferer at F = 3000–12750 MHz	–30	–27	–	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
IMD	Intermodulation performance Wanted signal at –64 dBm and 1-Mbps BLE, third, fourth, and fifth offset channel	–50	–	–	dBm	RF-PHY Specification (RCV-LE/CA/05/C)
RXSE1	Receiver spurious emission 30 MHz to 1.0 GHz	–	–	–57	dBm	100-kHz measurement bandwidth ETSI EN300 328 V1.8.1

Table 50. BLE Subsystem (continued)

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
RXSE2	Receiver spurious emission 1.0 GHz to 12.75 GHz	–	–	–47	dBm	1-MHz measurement bandwidth ETSI EN300 328 V1.8.1
RF Transmitter Specifications						
TXP, ACC	RF power accuracy	–	±1	–	dB	
TXP, RANGE	RF power control range	–	20	–	dB	
TXP, 0dBm	Output power, 0-dB Gain setting (PA7)	–	0	–	dBm	
TXP, MAX	Output power, maximum power setting (PA10)	–	3	–	dBm	
TXP, MIN	Output power, minimum power setting (PA1)	–	–18	–	dBm	
F2AVG	Average frequency deviation for 10101010 pattern	185	–	–	kHz	RF-PHY Specification (TRM-LE/CA/05/C)
F1AVG	Average frequency deviation for 11110000 pattern	225	250	275	kHz	RF-PHY Specification (TRM-LE/CA/05/C)
EO	Eye opening = $\Delta F_{2AVG}/\Delta F_{1AVG}$	0.8	–	–		RF-PHY Specification (TRM-LE/CA/05/C)
FTX, ACC	Frequency accuracy	–150	–	150	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
FTX, MAXDR	Maximum frequency drift	–50	–	50	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
FTX, INITDR	Initial frequency drift	–20	–	20	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
FTX, DR	Maximum drift rate	–20	–	20	kHz/ 50 μ s	RF-PHY Specification (TRM-LE/CA/06/C)
IBSE1	In-band spurious emission at 2-MHz offset	–	–	–20	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
IBSE2	In-band spurious emission at ≥ 3 -MHz offset	–	–	–30	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
TXSE1	Transmitter spurious emissions (average), <1.0 GHz	–	–	–55.5	dBm	FCC-15.247
TXSE2	Transmitter spurious emissions (average), >1.0 GHz	–	–	–41.5	dBm	FCC-15.247
RF Current Specifications						
IRX	Receive current in normal mode	–	18.7	–	mA	
IRX_RF	Radio receive current in normal mode	–	16.4	–	mA	Measured at V_{DDR}
IRX, HIGHGAIN	Receive current in high-gain mode	–	21.5	–	mA	
ITX, 3dBm	TX current at 3-dBm setting (PA10)	–	20	–	mA	
ITX, 0dBm	TX current at 0-dBm setting (PA7)	–	16.5	–	mA	
ITX_RF, 0dBm	Radio TX current at 0 dBm setting (PA7)	–	15.6	–	mA	Measured at V_{DDR}
ITX_RF, 0dBm	Radio TX current at 0 dBm excluding Balun loss	–	14.2	–	mA	Guaranteed by design simulation
ITX, –3dBm	TX current at –3-dBm setting (PA4)	–	15.5	–	mA	

Table 50. BLE Subsystem (continued)

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
ITX,-6dBm	TX current at -6-dBm setting (PA3)	–	14.5	–	mA	
ITX,-12dBm	TX current at -12-dBm setting (PA2)	–	13.2	–	mA	
ITX,-18dBm	TX current at -18-dBm setting (PA1)	–	12.5	–	mA	
lavg_1sec, 0dBm	Average current at 1-second BLE connection interval	–	17.1	–	μA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy. For empty PDU exchange
lavg_4sec, 0dBm	Average current at 4-second BLE connection interval	–	6.1	–	μA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy. For empty PDU exchange
General RF Specifications						
FREQ	RF operating frequency	2400	–	2482	MHz	
CHBW	Channel spacing	–	2	–	MHz	
DR	On-air data rate	–	1000	–	kbps	
IDLE2TX	BLE.IDLE to BLE. TX transition time	–	120	140	μs	
IDLE2RX	BLE.IDLE to BLE. RX transition time	–	75	120	μs	
RSSI Specifications						
RSSI, ACC	RSSI accuracy	–	±5	–	dB	
RSSI, RES	RSSI resolution	–	1	–	dB	
RSSI, PER	RSSI sample period	–	6	–	μs	

Environmental Specifications

Environmental Compliance

This Cypress BLE module is built in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

RF Certification

The CYBLE-212020-01 module will be certified under the following RF certification standards at production release.

- FCC: WAP2011
- CE
- IC: 7922A-2011
- MIC: 203-JN0509
- KC: MSIP-CRM-Cyp-2011

Safety Certification

The CYBLE-212020-01 module complies with the following regulations:

- Underwriters Laboratories, Inc. (UL) - Filing E331901
- CSA
- TUV

Environmental Conditions

Table 51 describes the operating and storage conditions for the Cypress BLE module.

Table 51. Environmental Conditions for CYBLE-212020-01

Description	Minimum Specification	Maximum Specification
Operating temperature	−40 °C	85 °C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	–	3 °C/minute
Storage temperature	−40 °C	85 °C
Storage temperature and humidity	–	85 °C at 85%
ESD: Module integrated into system Components ^[10]	–	15 kV Air 2.2 kV Contact

ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

Device Handling: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

Note

10. This does not apply to the RF pins (ANT, XTALI, and XTALO). RF pins (ANT, XTALI, and XTALO) are tested for 500-V HBM.

Regulatory Information

FCC

FCC NOTICE:

The device CYBLE-212020-01 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.

Transmitter operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP2011.

In any case the end product must be labeled exterior with "Contains FCC ID: WAP2011"

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antennas listed below. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in [Table 6](#) on page 13, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBLE-212020-01 with the trace antenna is far below the FCC radio frequency exposure limits. Nevertheless, use CYBLE-212020-01 in such a manner that it minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

Industry Canada (IC) Certification

CYBLE-212020-01 is licensed to meet the regulatory requirements of Industry Canada (IC),

License: IC: 7922A-2011

Manufacturers of mobile, fixed, or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in Table 6 on page 13, having a maximum gain of 0.5 dBi. Antennas not included in this list or having a gain greater than 0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

IC NOTICE:

The device CYBLE-212020-01 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN.

Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

IC RADIATION EXPOSURE STATEMENT FOR CANADA

This device complies with Industry Canada licence-exempt RSS standard(s).

Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that IC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the IC Notice above. The IC identifier is 7922A-2011. In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-2011"

European R&TTE Declaration of Conformity

Hereby, Cypress Semiconductor declares that the Bluetooth module CYBLE-212020-01 complies with the essential requirements and other relevant provisions of Directive 1999/5/EC. As a result of the conformity assessment procedure described in Annex III of the Directive 1999/5/EC, the end-customer equipment should be labeled as follows:



All versions of the CYBLE-212020-01 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

MIC Japan

CYBLE-212020-01 is certified as a module with type certification number 203-JN0509. End products that integrate CYBLE-212020-01 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.

Model Name: EZ-BLE PSoC Module

Part Number: CYBLE-212020-01

Manufactured by Cypress Semiconductor.



[R] 203-JN0509

KC Korea

CYBLE-212020-01 is certified for use in Korea with certificate number MSIP-CRM-Cyp-2011.



1. 제품명(모델명): 특정소출력무선기기(무선데이터통신시스템용 무선기기), CYBLE-212020-01
2. 인증 번호: MSIP-CRM-Cyp-2011
3. 라이선스 소유자: Cypress Semiconductor Corporation
4. 제조일자: 2016.5
5. 제조업체/국가명: Cypress Semiconductor Corporation/ 중국

Packaging

Table 52. Solder Reflow Peak Temperature

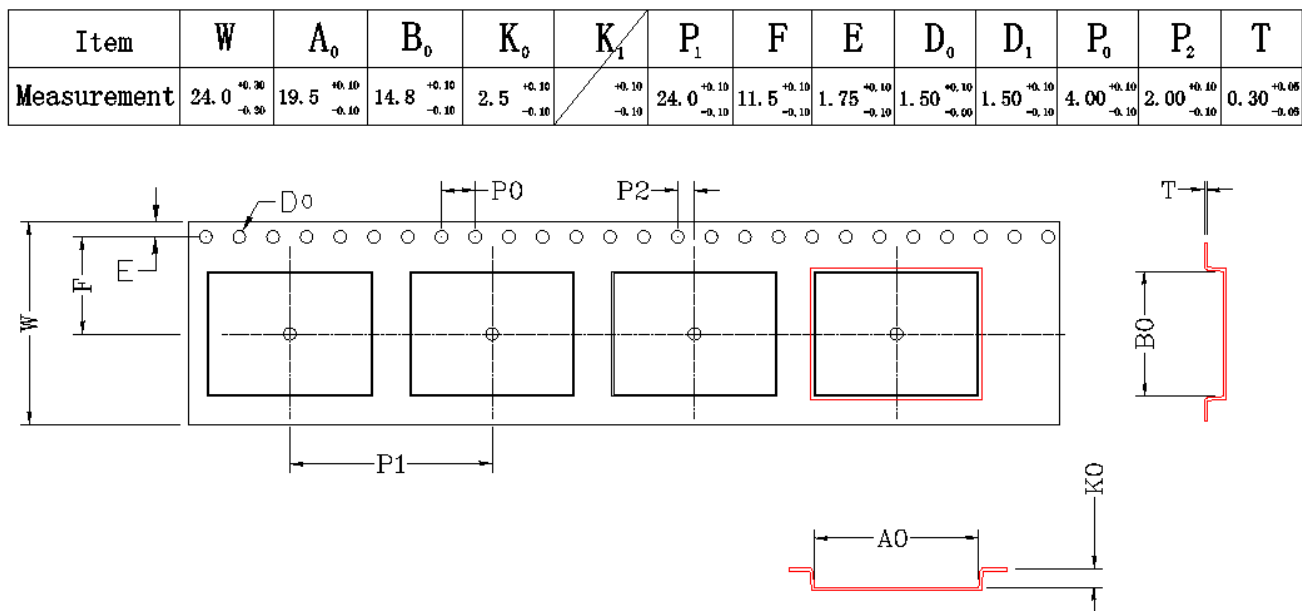
Module Part Number	Package	Maximum Peak Temperature	Maximum Time at Peak Temperature	No. of Cycles
CYBLE-212020-01	31-pad SMT	260 °C	30 seconds	2

Table 53. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Module Part Number	Package	MSL
CYBLE-212020-01	31-pad SMT	MSL 3

The CYBLE-212020-01 is offered in tape and reel packaging. [Figure 10](#) details the tape dimensions used for the CYBLE-212020-01.

Figure 10. CYBLE-212020-01 Tape Dimensions



[Figure 11](#) details the orientation of the CYBLE-212020-01 in the tape as well as the direction for unreeling.

Figure 11. Component Orientation in Tape and Unreeling Direction

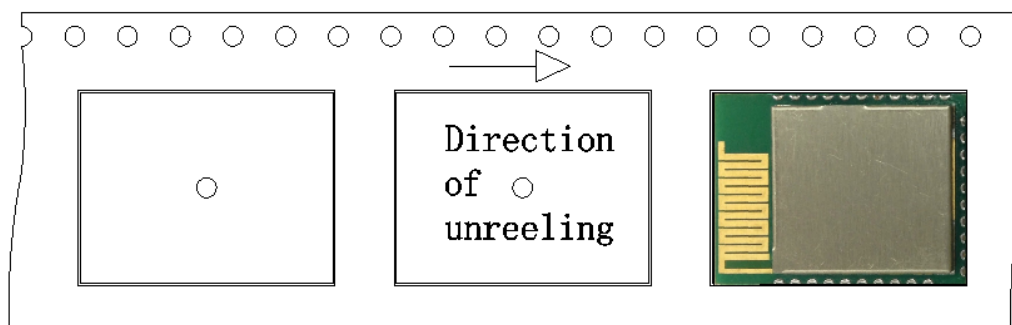
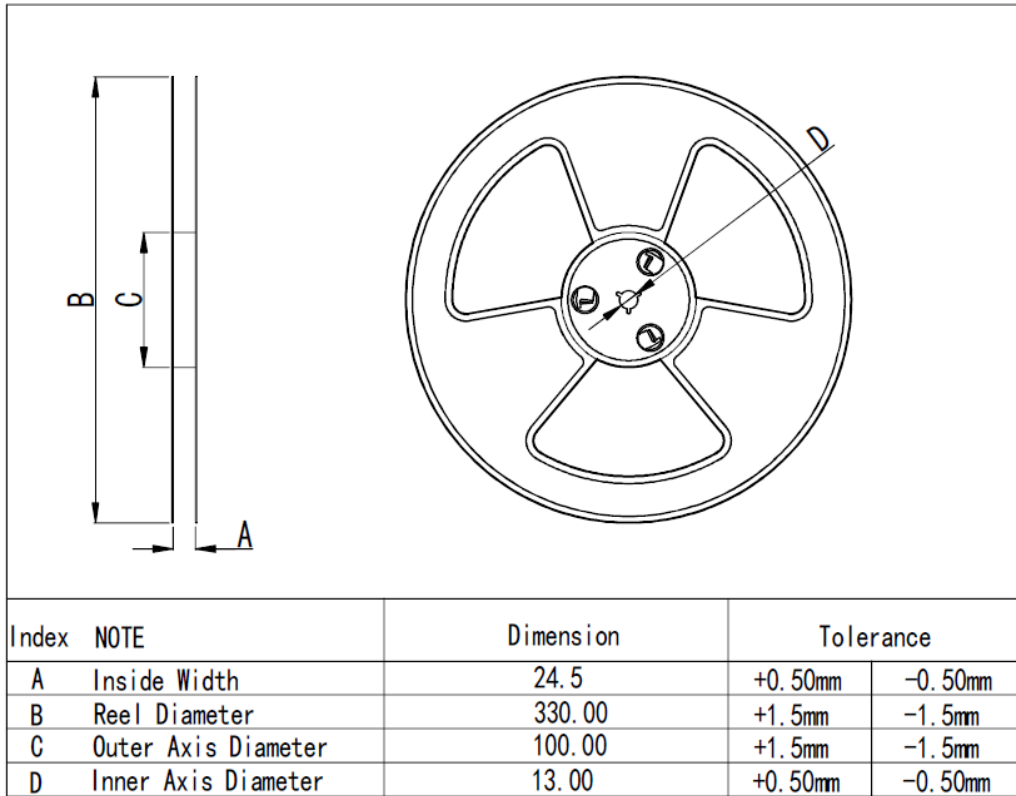


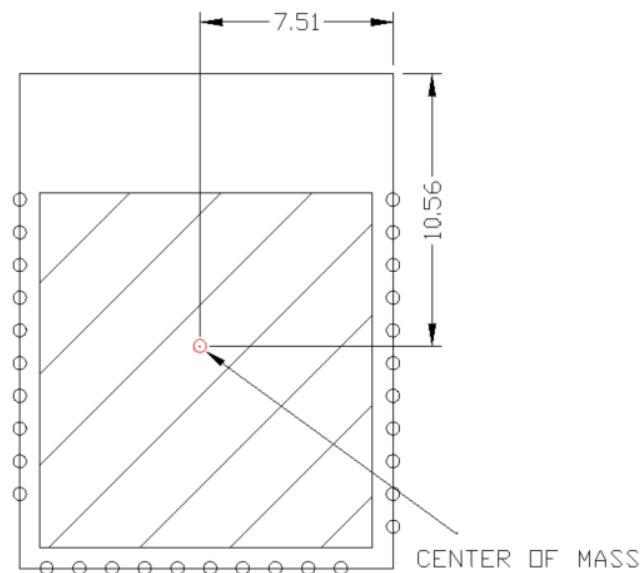
Figure 12 details reel dimensions used for the CYBLE-212020-01.

Figure 12. Reel Dimensions



The CYBLE-212020-01 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBLE-212020-01 is detailed in Figure 13.

Figure 13. CYBLE-212020-01 Center of Mass (Seen from Top)



Ordering Information

Table 54 lists the CYBLE-212020-01 part number and features. Table 55 lists the reel shipment quantities for the CYBLE-212020-01.

Table 54. Ordering Information

Part Number	CPU Speed (MHz)	Flash Size (KB)	CapSense	SCB	TCPWM	12-Bit SAR ADC	I ² S	LCD	Package	Packing	Certified
CYBLE-212020-01	48	256	Yes	2	4	1 Msps	Yes	Yes	31-SMT	Tape and Reel	Yes

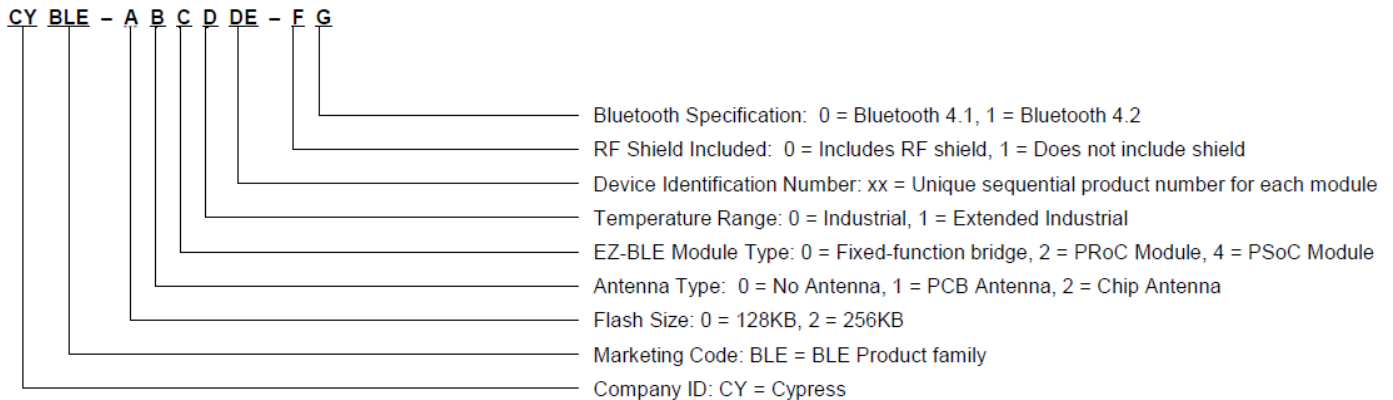
Table 55. Tape and Reel Package Quantity and Minimum Order Amount

Description	Minimum Reel Quantity	Maximum Reel Quantity	Comments
Reel Quantity	500	500	Ships in 500 unit reel quantities.
Minimum Order Quantity (MOQ)	500	–	
Order Increment (OI)	500	–	

The CYBLE-212020-01 is offered in tape and reel packaging. The CYBLE-212020-01 ships with a maximum of 500 units/reel.

Part Numbering Convention

The part numbers are of the form CYBLE-ABCDEF-GH where the fields are defined as follows.



For additional information and a complete list of Cypress Semiconductor BLE products, contact your local Cypress sales representative. To locate the nearest Cypress office, visit our website.

U.S. Cypress Headquarters Address	198 Champion Court, San Jose, CA 95134
U.S. Cypress Headquarter Contact Info	(408) 943-2600
Cypress website address	http://www.cypress.com

Acronyms

Acronym	Description
BLE	Bluetooth Low Energy
Bluetooth SIG	Bluetooth Special Interest Group
CE	European Conformity
CSA	Canadian Standards Association
EMI	electromagnetic interference
ESD	electrostatic discharge
FCC	Federal Communications Commission
GPIO	general-purpose input/output
IC	Industry Canada
IDE	integrated design environment
KC	Korea Certification
MIC	Ministry of Internal Affairs and Communications (Japan)
PCB	printed circuit board
RX	receive
QDID	qualification design ID
SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
TCPWM	timer, counter, pulse width modulator (PWM)
TUV	Germany: Technischer Überwachungs-Verein (Technical Inspection Association)
TX	transmit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilovolt
mA	milliamperes
mm	millimeters
mV	millivolt
μA	microamperes
μm	micrometers
MHz	megahertz
GHz	gigahertz
V	volt

Document History Page

Document Title: CYBLE-212020-01, EZ-BLE™ PSoC™ Bluetooth 4.2 Module				
Document Number: 002-12597				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5285698	MINS	05/26/2016	Preliminary datasheet for CYBLE-212020-01 module.
*A	5418841	DSO	08/31/2016	Changed status from Preliminary to Final. Updated General Description: Replaced "Bluetooth 4.1" with "Bluetooth 4.2". Updated Power Consumption: Replaced "Stop: 60 nA with XRES wakeup" with "Stop: 60 nA with GPIO (P2.2) or XRES wakeup" under "Low power mode support". Updated More Information: Added additional Knowledge Base Article references. Updated Ordering Information: No change in part numbers. Added Table 55 (To specify minimum and maximum reel quantities that ship for orders of the CYBLE-212020-01 module). Updated to new template.
*B	5536076	DSO	11/29/2016	Updated More Information: Added EZ-Serial™ BLE Firmware Platform section. Updated Recommended Host PCB Layout: Updated Figure 4, Figure 5, and Figure 6 captions to specify that these as "Seen on Host PCB". Updated Power Supply Connections and Recommended External Components: Updated Figure 7 and Figure 8 to specify that these are "Seen from Bottom". Updated Digital and Analog Capabilities and Connections: Updated Table 4: Updated TCPWM column to add TCPWM capability on Port 2 pins. Added Footnote 4.
*C	5554670	DSO	12/15/2016	Updated Electrical Specifications: Updated SAR ADC: Updated Table 18 to add Note 8 to specify under what conditions the maximum number of ADC channels can be achieved.

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