# CY7C603xx

# enCoRe™ III Low Voltage

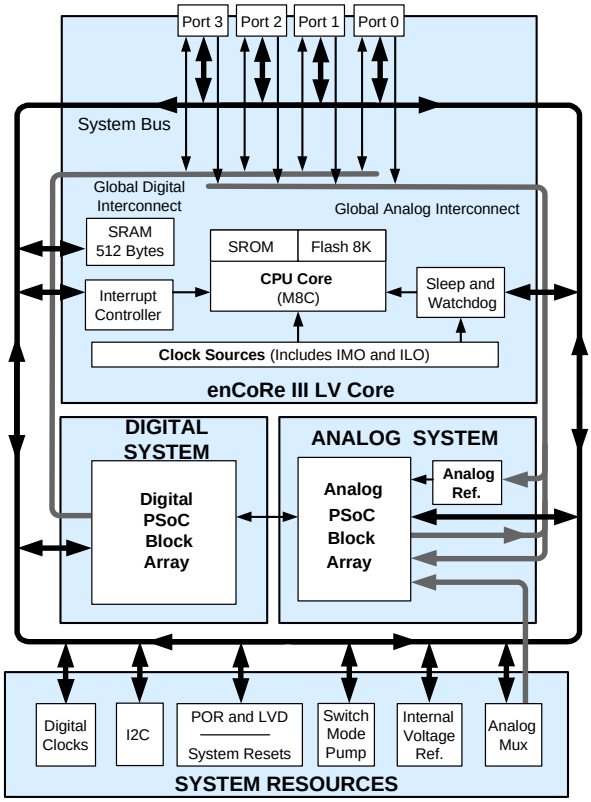
## Features

- Powerful Harvard-architecture processor
  - M8C processor speeds to 12 MHz
  - Low power at high speed
  - 2.4 V to 3.6 V operating voltage
  - Operating voltages down to 1.0 V using on-chip switch mode pump (SMP)
  - Commercial temperature range: 0 °C to +70 °C
- Configurable peripherals
  - 8-bit timers, counters, and PWM
  - Full duplex master or slave SPI
  - 10-bit ADC
  - 8-bit successive approximation ADC
  - Comparator
- Flexible on-chip memory
  - 8K flash program storage 50,000 erase/write cycles
  - 512 bytes SRAM data storage
  - In-System serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- Complete development tools
  - Free development software (PSoC Designer™)
  - Full-featured, In-circuit emulator and programmer
  - Complex breakpoint structure
  - 128K trace memory
- Precision, programmable clocking
  - Internal ±2.5% 24 and 48 MHz oscillator
  - Internal oscillator for watchdog and sleep
- Programmable pin configurations
  - 10 mA drive on all general purpose IO (GPIO)
  - Pull-up, pull-down, high-Z, strong, or open drain drive modes on all GPIO
  - Up to 8 analog inputs on GPIO
  - Configurable interrupt on all GPIO
- Versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of IO combinations
- Additional system resources
  - $I^2C$ master, slave, and Multimaster to 400 kHz
  - Watchdog and sleep timers
  - User-configurable low-voltage detection
  - Integrated supervisory circuit
  - On-chip precision voltage reference

## Applications

- Wireless mice
- Wireless gamepads
- Wireless presenter tools
- Wireless keypads
- PlayStation® 2 wired gamepads
- PlayStation 2 bridges for wireless gamepads
  - Applications requiring a cost effective low voltage 8-bit microcontroller.

## Logic Block Diagram



## Contents

## enCoRe III Low Voltage Functional Overview

The enCoRe III low voltage (enCoRe III LV) Part Number device is based on the flexible PSoC® architecture. This supports a simple set of peripherals that can be configured to match the needs of each application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. A fast CPU, flash program memory, SRAM data memory, and configurable IO are included in both 28-pin SSOP and 32-pin QFN packages.

The enCoRe III LV architecture, as shown in Figure 1, consists of four main areas: the enCoRe III LV Core, the system resources, digital system, and analog system. Configurable global bus resources allow combining all the device resources into a complete custom system. Each enCoRe III LV device supports a limited set of digital and analog peripherals. Depending on the package, up to 28 general purpose IOs (GPIOs) are also included. The GPIOs provide access to the global digital and analog interconnects.

### enCoRe III LV Core

The enCoRe III LV core is a powerful engine that supports a rich feature set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low-speed oscillator).

The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a four MIPS 8-bit Harvard -architecture microprocessor. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

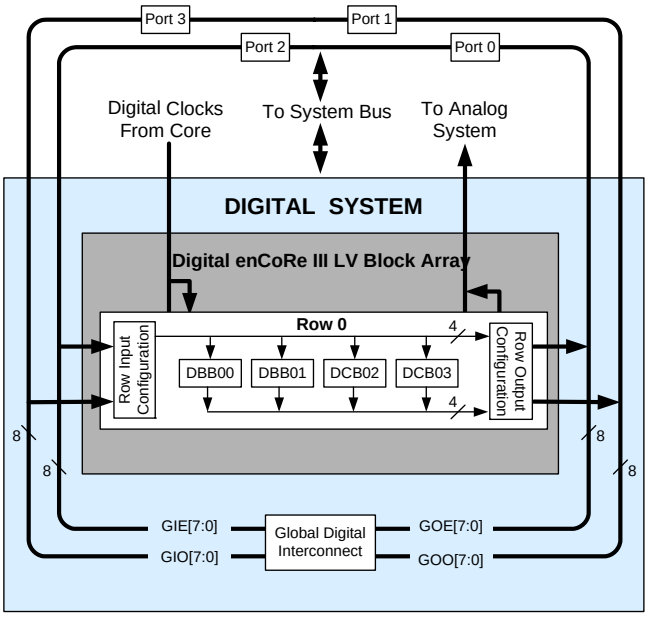
System resources provide additional capability, such as digital clocks to increase flexibility, $I^2C$ functionality for implementing an $I^2C$ master, slave, multi-master, an internal voltage reference that provides an absolute value of 1.3 V to a number of subsystems, a switch mode pump (SMP) that generates normal operating voltages off a single battery cell, and various system resets supported by the M8C.

### The Digital System

The digital system consists of 4 digital enCoRe III LV blocks. Each block is an 8-bit resource. Digital peripheral configurations include the following:

- PWM usable as timer or counter
- SPI master and slave
- I2C slave and multi-master
- CMP
- ADC10
- SARADC

**Figure 1. Digital System Block Diagram**




The digital blocks may be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

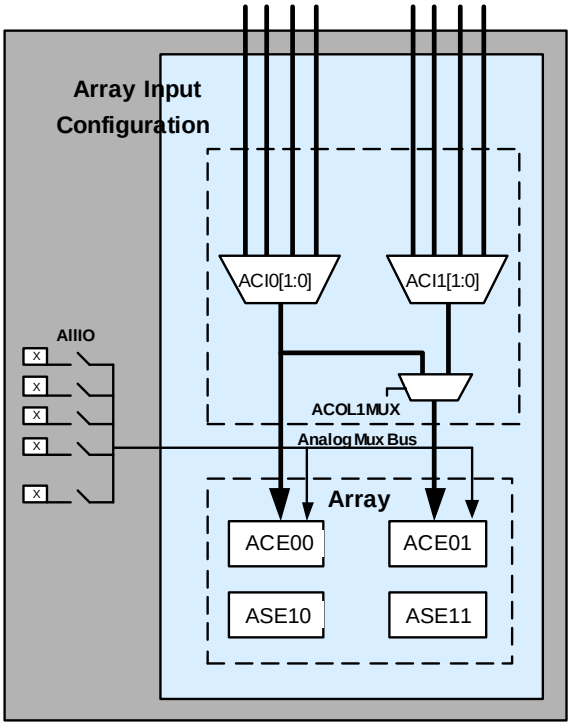
### The Analog System

The analog system consists of two configurable blocks. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the common analog functions for this device (available as user modules) are:

- Analog-to-digital converters (single with 8-bit resolution)
- Pin-to-pin comparators
- Single-ended comparators with absolute (1.3 V) reference
- 1.3 V reference (as a system resource)

Analog blocks are provided in columns of two, which includes one CT (continuous time - ACE00 or ACE01) and one SC (switched capacitor - ASE10 or ASE11) blocks.

**Figure 2. Analog System Block Diagram**




*The Analog Multiplexer System*

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

### Additional System Resources

System resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks may be generated using digital blocks as clock dividers.
- The $I^2C$ module provides 100 kHz and 400 kHz communication over two wires. slave, master, and multi-master modes are all supported.
- Low voltage detection interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system.
- An integrated switch mode pump generates normal operating voltages from a single 1.2 V battery cell, providing a low-cost boost converter.
- Versatile analog multiplexer system.

## enCoRe III LV Device Characteristics

The enCoRe III LV devices have four digital blocks and four analog blocks. Table 1 lists the resources available for specific enCoRe III LV devices.

**Table 1. enCoRe III LV Device Characteristics**

| Part Number | Digital IO | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|---|---|---|---|---|---|---|---|---|---|
| CY7C60323-PVXC | 24 | 1 | 4 | 24 | 0 | 2 | 4 | 512 Bytes | 8K |

## Getting Started

The quickest path to understanding the enCoRe III LV silicon is by reading this data sheet and using the PSoC Designer integrated development environment (IDE). This data sheet is an overview of the enCoRe III LV and presents specific pin, register, and electrical specifications. enCoRe III LV is based on the architecture of the CY8C21x34. For in-depth information, along with detailed programming information, refer to the PSoC Programmable System-on-Chip Technical Reference Manual, which is available at http://www.cypress.com.

For up-to-date ordering, packaging, and electrical specification information, refer to the latest device data sheets on the web at http://www.cypress.com.

### Development Kits

Development kits are available from the following distributors: Digi-key, avnet, arrow, and future. The Cypress online store contains development kits, **C** compilers, and all accessories for enCoRe III LV development. Go to the Cypress online store web site at http://www.cypress.com.

## Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-circuit emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

### PSoC Designer Software Subsystems

*System-Level View*

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system-level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Mixed-Signal Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

*Chip-Level View*

The chip-level view is a more traditional integrated development environment (IDE). Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration enables changing configurations at run time.

*Hybrid Designs*

You can begin in the system-level view, allow it to choose and configure your user modules and routing, and generate code. Then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

*Code Generation Tools*

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

**Assemblers.** The assemblers enable assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products enable you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

*Debugger*

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands enable the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also enables the designer to create a trace buffer of registers and memory locations of interest.

*Online Help System*

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support forum to aid the designer in getting started.

### In-Circuit Emulator

A low-cost, high functionality In-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24-MHz) operation.

## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and connect
4. Generate, verify, and debug

### Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called drivers and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces ($I^2C$-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called user modules. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

### Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that enable you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) user module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in datasheets that are viewed directly in PSoC Designer. These datasheets explain the internal operation of the component and provide performance specifications. Each datasheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

### Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog-to-digital converter (ADC) to convert the potentiometer's output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the Generate Application step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions. This allows you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's debugger subsystem. The debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events. These include monitoring address and data bus values, memory locations and external signals.

## Pin Information

The enCoRe III LV device is available in 28-pin SSOP and 32-pin QFN packages. Every port pin (labeled with a “P”) is capable of Digital IO and connection to the common analog bus. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

### 28-Pin Part Pinout

**Figure 3. CY7C60323-PVXC 28-Pin Device**

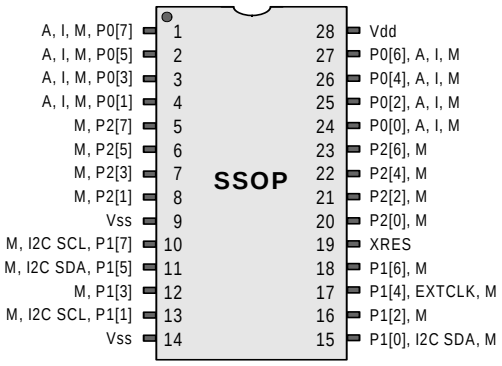



**Table 2. Pin Definitions - CY7C60323-PVXC 28-Pin Device**

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I, M | P0[7] | Analog column mux input. |
| 2 | IO | I, M | P0[5] | Analog column mux input and column output. |
| 3 | IO | I, M | P0[3] | Analog column mux input and column output, integrating input. |
| 4 | IO | I, M | P0[1] | Analog column mux input, integrating input. |
| 5 | IO | M | P2[7] | |
| 6 | IO | M | P2[5] | |
| 7 | IO | I, M | P2[3] | Direct switched capacitor block input. |
| 8 | IO | I, M | P2[1] | Direct switched capacitor block inputt. |
| 9 | Power | | Vss | Ground connection. |
| 10 | IO | M | P1[7] | $I^2C$ serial clock (SCL). |
| 11 | IO | M | P1[5] | $I^2C$ serial data (SDA). |
| 12 | IO | M | P1[3] | |
| 13 | IO | M | P1[1] | $I^2C$ serial clock (SCL), ISSP-SCLK. |
| 14 | Power | | Vss | Ground connection. |
| 15 | IO | M | P1[0] | $I^2C$ serial data (SDA), ISSP-SDATA. |
| 16 | IO | M | P1[2] | |
| 17 | IO | M | P1[4] | Optional external clock input (EXTCLK). |
| 18 | IO | M | P1[6] | |
| 19 | Input | | XRES | Active HIGH external reset with internal pull down. |
| 20 | IO | I, M | P2[0] | Direct switched capacitor block input. |
| 21 | IO | I, M | P2[2] | Direct switched capacitor block input. |
| 22 | IO | M | P2[4] | |
| 23 | IO | M | P2[6] | |
| 24 | IO | I, M | P0[0] | Analog column mux input |
| 25 | IO | I, M | P0[2] | Analog column mux input |
| 26 | IO | I, M | P0[4] | Analog column mux input |
| 27 | IO | I, M | P0[6] | Analog column mux input |
| 28 | Power | | Vdd | Supply voltage. |

**LEGEND** A = analog, I = input, O = output, and M = analog mux input.

## 32-Pin Part Pinout

**Figure 4. CY7C60323-LFXC 32-Pin Device**

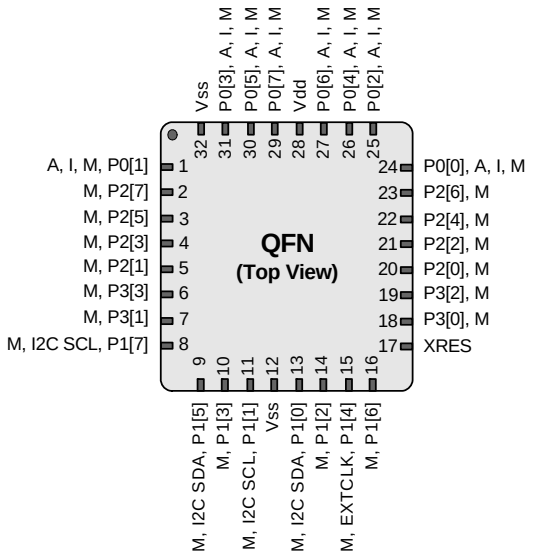



**Figure 4. CY7C60333-LFXC 32-Pin Device**

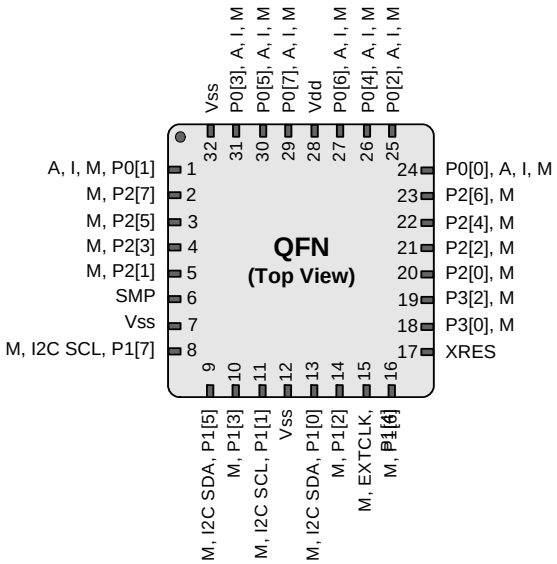



**Figure 8. CY7C60323-LTXC 32-Pin Device**

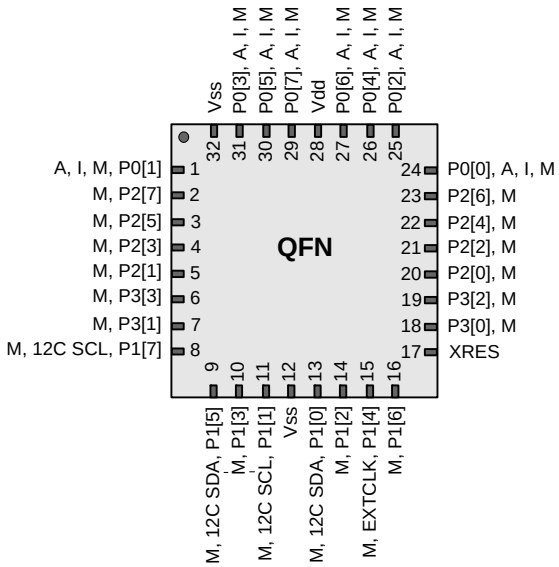



**Figure 9. CY7C60333-LTXC 32-Pin Device**

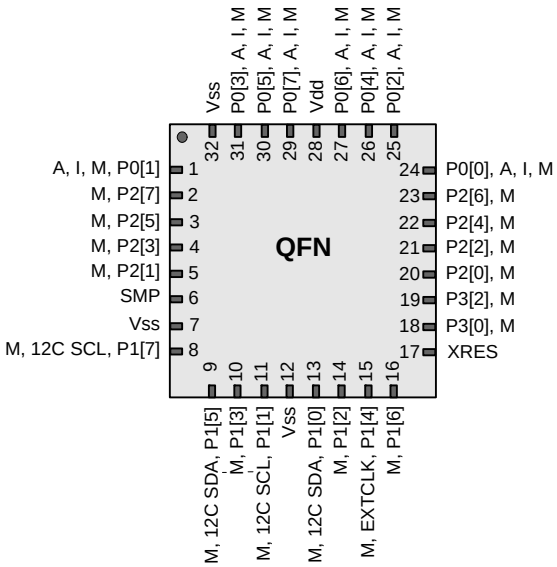


**Table 3. 32-Pin Part Pinout (QFN[1])**

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I, M | P0[1] | Analog column mux input, integrating input. |
| 2 | IO | M | P2[7] | |
| 3 | IO | M | P2[5] | |
| 4 | IO | M | P2[3] | |
| 5 | IO | M | P2[1] | |
| 6 | IO | M | P3[3] | In CY7C60323 part. |
| 6 | Power | | SMP | Switch mode pump (SMP) connection to required external components in CY7C60333 part. |
| 7 | IO | M | P3[1] | In CY7C60323 Part. |
| 7 | Power | | Vss | Ground connection in CY7C60333 part. |
| 8 | IO | M | P1[7] | $I^2C$ serial clock (SCL). |
| 9 | IO | M | P1[5] | $I^2C$ serial data (SDA). |
| 10 | IO | M | P1[3] | |
| 11 | IO | M | P1[1] | $I^2C$ serial clock (SCL), ISSP-SCLK. |
| 12 | Power | | Vss | Ground connection. |
| 13 | IO | M | P1[0] | $I^2C$ serial data (SDA), ISSP-SDATA. |
| 14 | IO | M | P1[2] | |
| 15 | IO | M | P1[4] | Optional external clock input (EXTCLK). |
| 16 | IO | M | P1[6] | |
| 17 | Input | | XRES | Active HIGH external reset with internal pull-down. |
| 18 | IO | M | P3[0] | |
| 19 | IO | M | P3[2] | |
| 20 | IO | M | P2[0] | |
| 21 | IO | M | P2[2] | |
| 22 | IO | M | P2[4] | |
| 23 | IO | M | P2[6] | |
| 24 | IO | I, M | P0[0] | Analog column mux input. |
| 25 | IO | I, M | P0[2] | Analog column mux input. |
| 26 | IO | I, M | P0[4] | Analog column mux input. |
| 27 | IO | I, M | P0[6] | Analog column mux input. |
| 28 | Power | | Vdd | Supply voltage. |
| 29 | IO | I, M | P0[7] | Analog column mux input. |
| 30 | IO | I, M | P0[5] | Analog column mux input |
| 31 | IO | I, M | P0[3] | Analog column mux input, integrating input. |
| 32 | Power | | Vss | Ground connection. |

**LEGEND** A = analog, I = input, O = output, and M = analog mux input.

**Note**
1. The QFN package has a center pad that must be connected to ground (Vss).

## Register Reference

This section lists the registers of the enCoRe III LV device. For detailed register information, refer the PSoC System-on-Chip Technical Reference Manual.

### Register Conventions

The register conventions specific to this section are listed in Table 4.

**Table 4. Register Conventions**

| Convention | Description |
|---|---|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

### Register Mapping Tables

The enCoRe III LV device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to 1 the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are Reserved and must not be accessed.

**Table 5. Register Map 0 Table: User Space**

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1GS | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2IE | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2GS | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | | CB | |
| PRT3DR | 0C | RW | | 4C | | | 8C | | | CC | |
| PRT3IE | 0D | RW | | 4D | | | 8D | | | CD | |
| PRT3GS | 0E | RW | | 4E | | | 8E | | | CE | |
| PRT3DM2 | 0F | RW | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | CUR_PP | D0 | RW |
| | 11 | | | 51 | | | 91 | | STK_PP | D1 | RW |
| | 12 | | | 52 | | | 92 | | | D2 | |
| | 13 | | | 53 | | | 93 | | IDX_PP | D3 | RW |
| | 14 | | | 54 | | | 94 | | MVR_PP | D4 | RW |
| | 15 | | | 55 | | | 95 | | MVW_PP | D5 | RW |
| | 16 | | | 56 | | | 96 | | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | | 97 | | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |

Blank fields are Reserved and must not be accessed. # Access is bit specific.

**Table 5. Register Map 0 Table: User Space** (continued)

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | AMUXCFG | 61 | RW | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | PWM_CR | 62 | RW | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | | 63 | | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | | E4 | |
| DBB01DR1 | 25 | W | | 65 | | | A5 | | | E5 | |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | ADC0_CR | 68 | # | | A8 | | | E8 | |
| DCB02DR1 | 29 | W | ADC1_CR | 69 | # | | A9 | | | E9 | |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | | EA | |
| DCB02CR0 | 2B | # | | 6B | | | AB | | | EB | |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_D | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed. # Access is bit specific.

**Table 6. Register Map 1 Table: Configuration Space**

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DM0 | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DM0 | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | | 8B | | | CB | |
| PRT3DM0 | 0C | RW | | 4C | | | 8C | | | CC | |
| PRT3DM1 | 0D | RW | | 4D | | | 8D | | | CD | |
| PRT3IC0 | 0E | RW | | 4E | | | 8E | | | CE | |
| PRT3IC1 | 0F | RW | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | GDI_O_IN | D0 | RW |
| | 11 | | | 51 | | | 91 | | GDI_E_IN | D1 | RW |
| | 12 | | | 52 | | | 92 | | GDI_O_OU | D2 | RW |
| | 13 | | | 53 | | | 93 | | GDI_E_OU | D3 | RW |
| | 14 | | | 54 | | | 94 | | | D4 | |
| | 15 | | | 55 | | | 95 | | | D5 | |
| | 16 | | | 56 | | | 96 | | | D6 | |
| | 17 | | | 57 | | | 97 | | | D7 | |
| | 18 | | | 58 | | | 98 | | MUX_CR0 | D8 | RW |
| | 19 | | | 59 | | | 99 | | MUX_CR1 | D9 | RW |
| | 1A | | | 5A | | | 9A | | MUX_CR2 | DA | RW |
| | 1B | | | 5B | | | 9B | | MUX_CR3 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | CMP_GO_EN | 64 | RW | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | ADC0_TR | E5 | RW |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | ADC1_TR | E6 | RW |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | CLK_CR3 | 6B | RW | | AB | | ECO_TR | EB | W |

Blank fields are Reserved and must not be accessed. # Access is bit specific.

**Table 6. Register Map 1 Table: Configuration Space** (continued)

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DCB03FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | FLS_PR1 | FA | RW |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_CR | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed. # Access is bit specific.

## Electrical Specifications

This section presents the DC and AC electrical specifications of the enCoRe III LV device. For up-to-date electrical specifications, check the latest data sheet by visiting the web at http://www.cypress.com.

Specifications are valid for 0 °C ≤ $T_A$ ≤ 70 °C and $T_J$ ≤ 85 °C as specified, except where noted.

Refer to Table 19 on page 21 for the electrical specifications for the internal main oscillator (IMO) using SLIMO mode.

**Figure 10. Voltage versus CPU Frequency**

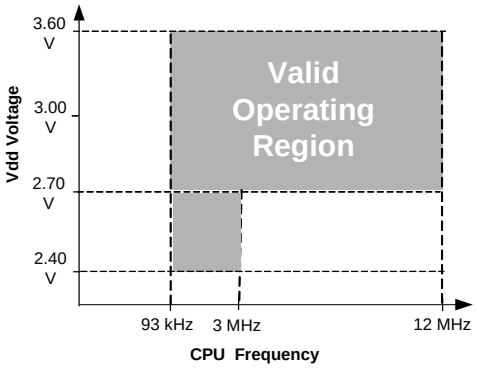
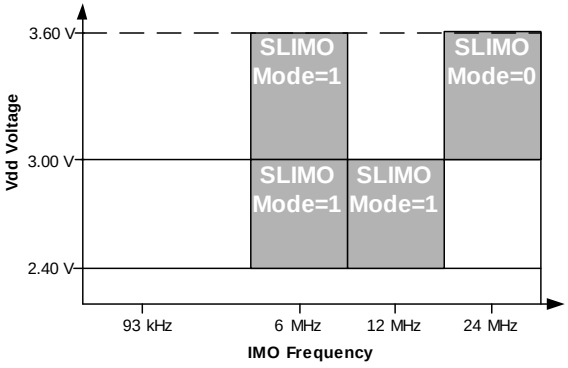



**Figure 11. IMO Frequency Trim Options**




The allowable CPU operating region for 12 MHz has been extended down to 2.7 V from the original 3.0 V design target. The customer's application is responsible for monitoring voltage and throttling back CPU speed in accordance with Figure 10 when voltage approaches 2.7 V. Refer to Table 16 for LVD specifications. Note that the device does not support a preset trip at 2.7 V. To detect Vdd drop at 2.7 V, an external circuit or device such as the WirelessUSB LP - CYRF6936 must be employed; or if the design permits, the nearest LVD trip value at 2.9 V can be used.

## Absolute Maximum Ratings

**Table 7. Absolute Maximum Ratings**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –40 | – | +90 | °C | Higher storage temperatures reduce data retention time. |
| $T_{BAKETEMP}$ | Bake temperature | | 125 | See package label | °C | |
| $T_{BAKETIME}$ | Bake time | See package label | | 72 | Hours | |
| $T_A$ | Ambient temperature with power applied | 0 | – | +70 | °C | |
| Vdd | Supply voltage on Vdd relative to Vss | –0.5 | – | 5 | V | |
| $V_{IO}$ | DC input voltage | Vss – 0.5 | – | Vdd + 0.5 | V | |
| $V_{IOZ}$ | DC voltage applied to tri-state | Vss – 0.5 | – | Vdd + 0.5 | V | |
| $I_{MIO}$ | Maximum current into any port pin | –25 | – | +25 | mA | |
| ESD | Electro static discharge voltage | 2000 | – | – | V | Human body model ESD. |
| LU | Latch up current | – | – | 200 | mA | |

## Operating Temperature

**Table 8. Operating Temperature**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | 0 | – | +70 | °C | |
| $T_J$ | Junction temperature | 0 | – | +85 | °C | The temperature rise from ambient to junction is package specific. See Table 31 on page 29. The user must limit the power consumption to comply with this requirement. |

## DC Electrical Characteristics

*DC Chip-Level Specifications*

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 9. DC Chip-Level Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | 2.40 | – | 3.6 | V | See Table 16 on page 19. |
| $I_{DD3}$ | Supply current, IMO = 6 MHz using SLIMO mode. | – | 1.2 | 2 | mA | Conditions are Vdd = 3.3 V, $T_A$ = 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz. |
| $I_{DD27}$ | Supply current, IMO = 6 MHz using SLIMO mode. | – | 1.1 | 1.5 | mA | Conditions are Vdd = 2.55 V, $T_A$ = 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz. |
| $I_{SB27}$ | Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range. | – | 2.6 | 4. | µA | Vdd = 2.55 V, 0 °C ≤ $T_A$ ≤ 40 °C. |
| $I_{SB}$ | Sleep (Mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. | – | 2.8 | 5 | µA | Vdd = 3.3 V, 0 °C ≤ $T_A$ ≤ 70 °C. |
| $V_{REF}$ | Reference voltage (Bandgap) | 1.28 | 1.30 | 1.32 | V | Trimmed for appropriate Vdd. Vdd = 3.0 V to 3.6 V. |
| $V_{REF27}$ | Reference voltage (Bandgap) | 1.16 | 1.30 | 1.33 | V | Trimmed for appropriate Vdd. Vdd = 2.4 V to 3.0 V. |
| AGND | Analog ground | $V_{REF}$ – 0.003 | $V_{REF}$ | $V_{REF}$ + 0.003 | V | |

*DC GPIO Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

**Table 10. 3.3 V DC GPIO Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull-down resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High output level | Vdd – 1.0 | – | – | V | $I_{OH}$ = 3 mA, $V_{DD}$ > 3.0 V |
| $V_{OL}$ | Low output level | – | – | 0.75 | V | $I_{OL}$ = 10 mA, $V_{DD}$ > 3.0 V |
| $I_{OH}$ | High level source current | 3 | – | – | mA | |
| $I_{OL}$ | Low level sink current | 10 | – | – | mA | |
| $V_{IL}$ | Input low level | – | – | 0.8 | V | Vdd = 3.0 to 3.6. |
| $V_{IH}$ | Input high level | 2.1 | – | | V | Vdd = 3.0 to 3.6. |
| $V_H$ | Input hysteresis | – | 60 | – | mV | |
| $I_{IL}$ | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 µA. |
| $C_{IN}$ | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |
| $C_{OUT}$ | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |

**Table 11. 2.7V DC GPIO Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull-down resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High output level | Vdd – 0.4 | – | – | V | $I_{OH}$ = 2.5 mA (6.25 Typ), $V_{DD}$ = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined $I_{OH}$ budget). |
| $V_{OL}$ | Low output level | – | – | 0.75 | V | $I_{OL}$ = 10 mA, $V_{DD}$ = 2.4 to 3.0 V (90 mA maximum combined $I_{OL}$ budget). |
| $I_{OH}$ | High level source current | 2.5 | – | – | mA | |
| $I_{OL}$ | Low level sink current | 10 | – | – | mA | |
| $V_{IL}$ | Input low level | – | – | 0.75 | V | Vdd = 2.4 to 3.0. |
| $V_{IH}$ | Input high level | 2.0 | – | – | V | Vdd = 2.4 to 3.0. |
| $V_H$ | Input hysteresis | – | 90 | – | mV | |
| $I_{IL}$ | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 µA. |
| $C_{IN}$ | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |
| $C_{OUT}$ | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |

*DC Operational Amplifier Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 12. 3.3-V DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input offset voltage (absolute value) | – | 2.5 | 15 | mV | |
| $TCV_{OSOA}$ | Average input offset voltage drift | – | 10 | – | µV/°C | |
| $I_{EBOA}$ | Input leakage current (Port 0 analog pins) | – | 200 | – | pA | Gross tested to 1 µA |
| $I_{EBOA00}$ | Input leakage current (Port 0, Pin 0 analog pin) | – | 50 | – | nA | Gross tested to 1 µA |
| $C_{INOA}$ | Input capacitance (Port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25 °C |
| $V_{CMOA}$ | Common mode voltage range | 0 | – | $V_{DD}$ – 1 | V | |
| $G_{OLOA}$ | Open loop gain | – | 80 | – | dB | |
| $I_{SOA}$ | Amplifier supply current | – | 10 | 30 | µA | |

**Table 13. 2.7-V DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input offset voltage (absolute value) | – | 2.5 | 15 | mV | |
| $TCV_{OSOA}$ | Average input offset voltage drift | – | 10 | – | µV/°C | |
| $I_{EBOA}$ | Input leakage current (Port 0 analog pins) | – | 200 | – | pA | Gross tested to 1 µA |
| $I_{EBOA00}$ | Input leakage current (Port 0, Pin 0 analog pin) | – | 50 | – | nA | Gross tested to 1 µA |
| $C_{INOA}$ | Input capacitance (Port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25 °C |
| $V_{CMOA}$ | Common mode voltage range | 0 | – | $V_{DD}$ – 1 | V | |
| $G_{OLOA}$ | Open loop gain | – | 80 | – | dB | |
| $I_{SOA}$ | Amplifier supply current | – | 10 | 30 | µA | |

*DC Switch Mode Pump Specifications*

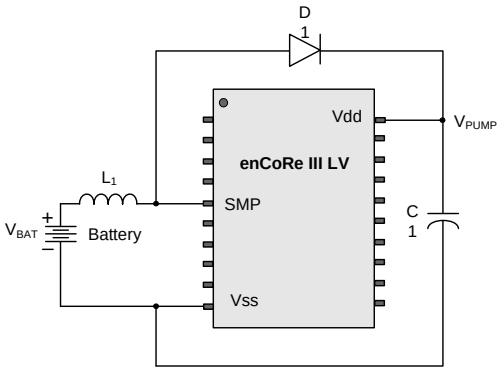
Table 14 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 14. DC Switch Mode Pump (SMP) Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{PUMP3V}$ | 3.3 V output voltage from pump | 3.00 | 3.25 | 3.60 | V | Configuration of footnote.[1] Average, neglecting ripple. SMP trip voltage is set to 3.25 V. |
| $V_{PUMP2V}$ | 2.6 V output voltage from pump | 2.45 | 2.55 | 2.80 | V | Configuration of footnote.[1] average, neglecting ripple. SMP trip voltage is set to 2.55 V. |
| $I_{PUMP}$ | Available output current<br>$V_{BAT}$ = 1.5 V, $V_{PUMP}$ = 3.25 V<br>$V_{BAT}$ = 1.3 V, $V_{PUMP}$ = 2.55 V | <br>8<br>8 | <br>–<br>– | <br>–<br>– | <br>mA<br>mA | Configuration of footnote.[1]<br>SMP trip voltage is set to 3.25 V.<br>SMP trip voltage is set to 2.55 V. |
| $V_{BAT3V}$ | Input voltage range from battery | 1.0 | – | 3.3 | V | Configuration of footnote.[1] SMP trip voltage is set to 3.25 V. |
| $V_{BAT2V}$ | Input voltage range from vattery | 1.0 | – | 2.8 | V | Configuration of footnote.[1] SMP trip voltage is set to 2.55 V. |
| $V_{BATSTART}$ | Minimum input voltage from vattery to start pump | 1.2 | – | – | V | Configuration of footnote.[1] 0 °C ≤ $T_A$ ≤ 100. 1.25 V at $T_A$ = –40 °C. |
| $\Delta V_{PUMP\_Line}$ | Line regulation (over Vi range) | – | 5 | – | $\%V_O$ | Configuration of footnote.[1] $V_O$ is the Vdd value for PUMP trip specified by the VM[2:0] setting in the DC POR and LVD specification, Table 16 on page 19. |
| $\Delta V_{PUMP\_Load}$ | Load regulation | – | 5 | – | $\%V_O$ | Configuration of footnote.[1] $V_O$ is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD specification, Table 16 on page 19. |
| $\Delta V_{PUMP\_Ripple}$ | Output vovltage ripple (depends on cap/load) | – | 100 | – | mVpp | Configuration of footnote.[1] Load is 5 mA. |
| $E_3$ | Efficiency | 35 | 50 | – | % | Configuration of footnote.[1] Load is 5 mA. SMP trip voltage is set to 3.25 V. |
| $E_2$ | Efficiency | 35 | 80 | – | % | For I load = 1 mA, $V_{PUMP}$ = 2.55 V, $V_{BAT}$ = 1.3 V, 10 µH inductor, 1 µF capacitor, and Schottky diode. |
| $F_{PUMP}$ | Switching frequency | – | 1.3 | – | MHz | |
| $DC_{PUMP}$ | Switching duty cycle | – | 50 | – | % | |

**Note**
1. $L_1$ = 2 µH inductor, $C_1$ = 10 µF capacitor, $D_1$ = Schottky diode. See Figure 12 on page 19.

**Figure 12. Basic Switch Mode Pump Circuit**




*DC Analog Mux Bus Specifications*

Table 15 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70° C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 15. DC Analog Mux Bus Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_{SW}$ | Switch resistance to common analog bus | – | – | 400<br>800 | Ω<br>Ω | Vdd ≥ 2.7 V<br>2.4 V ≤ Vdd ≤ 2.7 V |
| $R_{VDD}$ | Resistance of initialization switch to Vdd | – | – | 800 | Ω | |

*DC POR and LVD Specifications*

Table 16 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 16. DC POR and LVD Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{PPOR0}$<br>$V_{PPOR1}$ | Vdd value for PPOR Trip<br>PORLEV[1:0] = 00b<br>PORLEV[1:0] = 01b | – | 2.36<br>2.82 | 2.40<br>2.95 | V<br>V | Vdd must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog. |
| | Vdd value for LVD Trip | | | | | |
| $V_{LVD0}$ | VM[2:0] = 000b | 2.40 | 2.45 | 2.51[2] | V | |
| $V_{LVD1}$ | VM[2:0] = 001b | 2.85 | 2.92 | 2.99[3] | V | |
| $V_{LVD2}$ | VM[2:0] = 010b | 2.95 | 3.02 | 3.09 | V | |
| $V_{LVD37}$ | VM[2:0] = 011b | 3.06 | 3.13 | 3.20 | V | |
| | Vdd value for PUMP Trip | | | | | |
| $V_{PUMP0}$ | VM[2:0] = 000b | 2.45 | 2.55 | 2.62[4] | V | |
| $V_{PUMP1}$ | VM[2:0] = 001b | 2.96 | 3.02 | 3.09 | V | |
| $V_{PUMP2}$ | VM[2:0] = 010b | 3.03 | 3.10 | 3.16 | V | |
| $V_{PUMP3}$ | VM[2:0] = 011b | 3.18 | 3.25 | 3.32[5] | V | |

**Notes**
2. Always greater than 50 mV above VPPOR (PORLEV = 00) for falling supply.
3. Always greater than 50 mV above VPPOR (PORLEV = 01) for falling supply.
4. Always greater than 50 mV above VLVD0.
5. Always greater than 50 mV above VLVD3.

*DC Programming Specifications*

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 17. DC Programming Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DDP}$ | $V_{DD}$ for programming and erase | 4.5 | 5.0 | 5.5 | V | This specification applies to the functional requirements of external programmer tools. |
| $V_{DDLV}$ | Low $V_{DD}$ for verify | 2.4 | 2.5 | 2.6 | V | This specification applies to the functional requirements of external programmer tools. |
| $V_{DDHV}$ | High $V_{DD}$ for verify | 3.5 | 3.6 | 3.7 | V | This specification applies to the functional requirements of external programmer tools. |
| $V_{DDIWRITE}$ | Supply voltage for flash write operation | 2.7 | – | 3.6 | V | This specification applies to this device when it is executing internal flash writes. |
| $I_{DDP}$ | Supply current during programming or verify | – | 5 | 25 | mA | |
| $V_{ILP}$ | Input low voltage during programming or verify | – | – | 0.8 | V | |
| $V_{IHP}$ | Input high voltage during programming or verify | 2.1 | – | – | V | |
| $I_{ILP}$ | Input current when applying Vilp to P1[0] or P1[1] during programming or verify | – | – | 0.2 | mA | Driving internal pull down resistor. |
| $I_{IHP}$ | Input current when applying Vihp to P1[0] or P1[1] during programming or verify | – | – | 1.5 | mA | Driving internal pull down resistor. |
| $V_{OLV}$ | Output low voltage during programming or verify | – | – | Vss + 0.75 | V | |
| $V_{OHV}$ | Output high voltage during programming or verify | Vdd – 1.0 | – | Vdd | V | |
| $Flash_{ENPB}$ | Flash endurance (per block) | 50,000[6] | – | – | – | Erase/write cycles per block. |
| $Flash_{ENT}$ | Flash dndurance (total)[7] | 1,800,000 | – | – | – | Erase/write cycles. |
| $Flash_{DR}$ | Flash data retention | 10 | – | – | Years | |

*DC $I^2C$ Specifications*

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 18. DC $I^2C$ Specifications**[8]

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{ILI2C}$ | Input low level | – | – | 0.3 × $V_{DD}$ | V | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V |
| $V_{IHI2C}$ | Input high level | 0.7 × $V_{DD}$ | – | – | V | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V |

**Notes**

6. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V and 3.0 V to 3.6 V.
7. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
8. All GPIO meet the DC GPIO $V_{IL}$ and $V_{IH}$ specifications found in the DC GPIO Specifications sections. The $I^2C$ GPIO pins also meet the above specs.

## AC Electrical Characteristics

*AC Chip-Level Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 19. 3.3 V AC Chip-Level Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $F_{IMO24}$ | Internal main oscillator frequency for 24 MHz | 23.4 | 24 | 24.6[9, 10] | MHz | Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 14. SLIMO mode = 0. |
| $F_{IMO6}$ | Internal main oscillator frequency for 6 MHz | 5.5 | 6 | 6.5[9, 10] | MHz | Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 14. SLIMO mode = 1. |
| $F_{CPU2}$ | CPU frequency (3.3 V nominal) | 0.093 | 12 | 12.3[9, 10] | MHz | SLIMO mode = 0. |
| $F_{BLK33}$ | Digital block frequency (3.3 V nominal) | 0 | 24 | 24.6[9, 11] | MHz | |
| $F_{32K1}$ | Internal low speed oscillator frequency | 15 | 32 | 64 | kHz | |
| $F_{32K\_U}$ | Internal low speed oscillator untrimmed frequency | 5 | – | 100 | kHz | |
| $DC_{ILO}$ | Internal low speed oscillator duty cycle | 20 | 50 | 80 | % | |
| $T_{XRST}$ | External reset pulse width | 10 | – | – | µs | |
| DC24M | 24 MHz duty cycle | 40 | 50 | 60 | % | |
| Step24M | 24 MHz Trim step size | – | 50 | – | kHz | |
| Fout48M | 48 MHz output frequency | 46.8 | 48.0 | 49.2[10] | MHz | Trimmed. Using factory trim values. |
| $F_{MAX}$ | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | |
| $SR_{POWER\_UP}$ | Power supply slew rate | – | – | 250 | V / ms | |
| $T_{POWERUP}$ | Time from end of POR to CPU executing code | – | 16 | 100 | ms | |
| $t_{jit\_IMO}$ | 24-MHz IMO cycle-to-cycle jitter (RMS)[13] | – | 200 | 700 | ps | |
| | 24-MHz IMO long term N cycle-to-cycle jitter (RMS)[13] | – | 300 | 900 | ps | N = 32 |
| | 24-MHz IMO period jitter (RMS)[13] | – | 100 | 400 | ps | |

**Notes**
9. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
10. 3.0 V < Vdd < 3.6 V.
11. See the individual user module data sheets for information on maximum frequencies for user modules.
12. 2.4 V < Vdd < 3.0 V.
13. Refer to Cypress Jitter Specifications Application Note AN5054 “Understanding Datasheet Jitter Specifications for Cypress Timing Products” at www.cypress.com under Application Notes for more information.

**Table 20. 2.7 V AC Chip-Level Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $F_{IMO12}$ | Internal main oscillator frequency for 12 MHz | 11.5 | 12 | 12.7[9, 12] | MHz | Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 14. SLIMO mode = 1. |
| $F_{IMO6}$ | Internal main oscillator frequency for 6 MHz | 5.5 | 6 | 6.5[9, 12] | MHz | Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 14. SLIMO mode = 1. |
| $F_{CPU1}$ | CPU frequency (2.7 V nominal) | 0.093 | 3 | 3.15[9, 12] | MHz | 12 MHz only for SLIMO mode = 0. |
| $F_{BLK27}$ | Digital block frequency (2.7 V nominal) | 0 | 12 | 12.5[9, 12] | MHz | Refer to the AC digital block specifications. |
| $F_{32K1}$ | Internal low speed oscillator frequency | 8 | 32 | 96 | kHz | |
| $F_{32K\_U}$ | Internal low speed oscillator untrimmed frequency | 5 | – | 100 | kHz | |
| $DC_{ILO}$ | Internal low speed oscillator duty cycle | 20 | 50 | 80 | % | |
| $T_{XRST}$ | External reset pulse width | 10 | – | – | µs | |
| $F_{MAX}$ | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | |
| $SR_{POWER\_UP}$ | Power supply slew rate | – | – | 250 | V / ms | |
| $T_{POWERUP}$ | Time from End of POR to CPU executing code | – | 16 | 100 | ms | |
| $t_{jit\_IMO}$ | 12 MHz IMO cycle-to-cycle jitter (RMS)[14] | – | 400 | 1000 | ps | |
| | 12 MHz IMO long term N cycle-to-cycle jitter (RMS)[14] | – | 600 | 1300 | ps | N = 32 |
| | 12 MHz IMO period jitter (RMS)[14] | – | 100 | 500 | ps | |

**Note**
14. Refer to Cypress Jitter Specifications Application Note AN5054 “Understanding Datasheet Jitter Specifications for Cypress Timing Products” at www.cypress.com under Application Notes for more information.

*AC GPIO Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

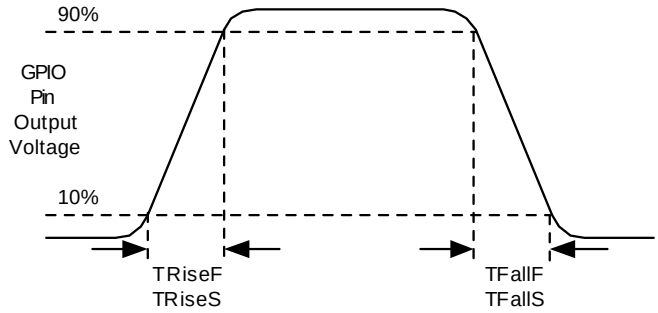
**Table 21. 3.3 V AC GPIO Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO operating frequency | 0 | – | 12 | MHz | Normal Strong Mode |
| TRiseS | Rise time, slow strong mode, cload = 50 pF | 7 | 27 | – | ns | Vdd = 3 to 3.6 V, 10%–90% |
| TFallS | Fall time, slow strong mode, cload = 50 pF | 7 | 22 | – | ns | Vdd = 3 to 3.6 V, 10%–90% |

**Table 22. 2.7 V AC GPIO Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO operating frequency | 0 | – | 3 | MHz | Normal Strong Mode |
| TRiseF | Rise time, normal strong mode, cload = 50 pF | 6 | – | 50 | ns | Vdd = 2.4 to 3.0 V, 10%–90% |
| TFallF | Fall time, normal strong mode, cload = 50 pF | 6 | – | 50 | ns | Vdd = 2.4 to 3.0 V , 10%–90% |
| TRiseS | Rise time, slow strong mode, cload = 50 pF | 18 | 40 | 120 | ns | Vdd = 2.4 to 3.0 V, 10%–90% |
| TFallS | Fall time, slow strong mode, cload = 50 pF | 18 | 40 | 120 | ns | Vdd = 2.4 to 3.0 V, 10%–90% |

**Figure 13. GPIO Timing Diagram**




*AC Operational Amplifier Specifications*

Table 23 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges : 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7V at 25 °C and are for design guidance only.

**Table 23. AC Operational Amplifier Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{COMP}$ | Comparator mode response time, 50 mV overdrive | | | 100<br>200 | ns<br>ns | Vdd ≥ 3.0 V.<br>2.4 V < Vcc < 3.0 V. |

*AC Digital Block Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 24. 3.3 V AC Digital Block Specifications**

| Function | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| All Functions | Block input clock frequency | – | – | 24.6 | MHz | 3.0 V < Vdd < 3.6 V. |
| Timer/ Counter/ PWM | Enable input pulse width | 50[15] | – | – | ns | |
| | Input clock frequency | – | – | 24.6 | MHz | |
| Dead Band | Kill pulse width: | | | | | |
| | Asynchronous restart mode | 20 | – | – | ns | |
| | Synchronous restart mode | 50 | – | – | ns | |
| | Disable mode | 50 | – | – | ns | |
| | Input clock frequency | – | – | 24.6 | MHz | 3.0 V ≤ Vdd ≤ 3.6 V. |
| SPIM | Input clock frequency | – | – | 8.2 | MHz | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2. |
| SPIS | Input clock frequency | – | – | 4.1 | MHz | Note for SPIS Input Clock Frequency: The input clock is the SPI SCLK in SPIS mode. |
| | Width of SS_ Negated between transmissions | 50 | – | – | ns | |
| Transmitter | Input clock frequency | – | – | 24.6 | MHz | The baud rate is equal to the input clock frequency divided by 8. |
| Receiver | Input clock frequency | – | – | 24.6 | MHz | The baud rate is equal to the input clock frequency divided by 8. |

**Table 25. 2.7 V AC Digital Block Specifications**

| Function | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| All Functions | Block input clock frequency | – | – | 12.7 | MHz | 2.4 V ≤ Vdd ≤ 3.0 V. |
| Timer/ Counter/ PWM | Enable input clock width | 100 | – | – | ns | |
| | Input clock frequency | – | – | 12.7 | MHz | |
| Dead Band | Kill pulse width: | | | | | |
| | Asynchronous restart mode | 20 | – | – | ns | |
| | Synchronous restart mode | 100 | – | – | ns | |
| | Disable mode | 100 | – | – | ns | |
| | Input clock frequency | – | – | 12.7 | MHz | 2.4 V ≤ Vdd < 3.0 V. |
| SPIM | Input clock frequency | – | – | 6.35 | MHz | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2. |
| SPIS | Input clock frequency | – | – | 4.1 | MHz | Note for input clock frequency: The input clock is the SPI SCLK in SPIS mode. |
| | Width of SS_ Negated between transmissions | 100 | – | – | ns | |
| Transmitter | Input clock frequency | – | – | 12.7 | MHz | The baud rate is equal to the input clock frequency divided by 8. |
| Receiver | Input clock frequency | – | – | 12.7 | MHz | The baud rate is equal to the input clock frequency divided by 8. |

**Note**
15. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 26. 3.3 V AC External Clock Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency with CPU clock divide by 1 | 0.093 | – | 12.3 | MHz | Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements. |
| $F_{OSCEXT}$ | Frequency with CPU clock divide by 2 or greater | 0.186 | – | 24.6 | MHz | If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met. |
| – | High period with CPU clock divide by 1 | 41.7 | – | 5300 | ns | |
| – | Low period with CPU clock divide by 1 | 41.7 | – | – | ns | |
| – | Power-up IMO to switch | 150 | – | – | µs | |

**Table 27. 2.7 V AC External Clock Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency with CPU clock divide by 1 | 0.093 | – | 3.08 | MHz | Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements. |
| $F_{OSCEXT}$ | Frequency with CPU clock divide by 2 or greater | 0.186 | – | 6.35 | MHz | If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met. |
| – | High period with CPU clock divide by 1 | 160 | – | 5300 | ns | |
| – | Low period with CPU clock divide by 1 | 160 | – | – | ns | |
| – | Power-up IMO to switch | 150 | – | – | µs | |

*AC Programming Specifications*

Table 28 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 28. AC Programming Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{RSCLK}$ | Rise time of SCLK | 1 | – | 20 | ns | |
| $T_{FSCLK}$ | Fall time of SCLK | 1 | – | 20 | ns | |
| $T_{SSCLK}$ | Data set up time to falling edge of SCLK | 40 | – | – | ns | |
| $T_{HSCLK}$ | Data hold time from falling edge of SCLK | 40 | – | – | ns | |
| $F_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $T_{ERASEB}$ | Flash erase time (Block) | – | 10 | – | ms | |
| $T_{WRITE}$ | Flash block write time | – | 40 | – | ms | |
| $T_{DSCLK3}$ | Data out delay from falling edge of SCLK | – | – | 50 | ns | 3.0 ≤ Vdd ≤ 3.6 |
| $T_{DSCLK2}$ | Data out delay from falling edge of SCLK | – | – | 70 | ns | 2.4 ≤ Vdd ≤ 3.0 |
| $T_{ERASEALL}$ | Flash erase time (Bulk) | – | 20 | – | ms | Erase all blocks and protection fields at once. |
| $T_{PROGRAM\_HOT}$ | Flash block erase + flash block write time | – | – | 100 | ms | 0 °C ≤ $T_J$ ≤ 100 °C |
| $T_{PROGRAM\_COLD}$ | Flash block erase + flash block write time | – | – | 200 | ms | -40 °C ≤ $T_J$ ≤ 0 °C |

*AC I²C Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 3.6 V and 0 °C ≤ $T_A$ ≤ 70 °C, or 2.4 V to 3.0 V and 0 °C ≤ $T_A$ ≤ 70 °C, respectively. Typical parameters apply to 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 29. AC Characteristics of the I²C SDA and SCL Pins for Vdd ≥ 3.0 V**

| Parameter | Description | Standard-Mode | | Fast-Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $F_{SCLI2C}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $T_{HDSTAI2C}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | µs |
| $T_{LOWI2C}$ | LOW period of the SCL clock | 4.7 | – | 1.3 | – | µs |
| $T_{HIGHI2C}$ | HIGH period of the SCL clock | 4.0 | – | 0.6 | – | µs |
| $T_{SUSTAI2C}$ | Set up time for a repeated START condition | 4.7 | – | 0.6 | – | µs |
| $T_{HDDATI2C}$ | Data hold time | 0 | – | 0 | – | µs |
| $T_{SUDATI2C}$ | Data setup time | 250 | – | 100[16] | – | ns |
| $T_{SUSTOI2C}$ | Set up time for STOP condition | 4.0 | – | 0.6 | – | µs |
| $T_{BUFI2C}$ | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | µs |
| $T_{SPI2C}$ | Pulse width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns |

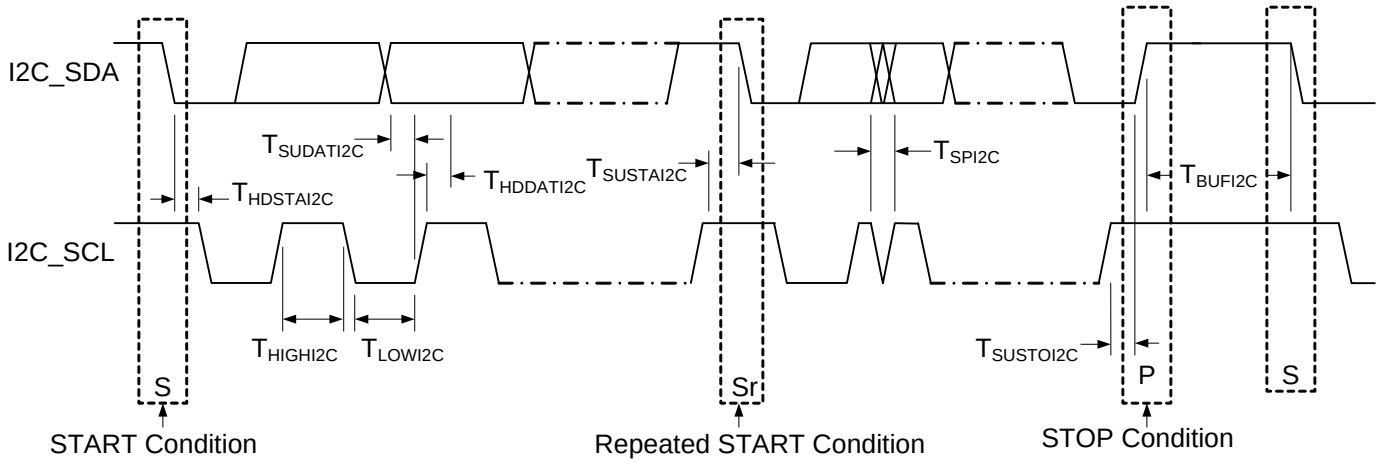
**Table 30. 2.7 V AC Characteristics of the I²C SDA and SCL Pins (Fast-Mode not Supported)**

| Parameter | Description | Standard-Mode | | Fast-Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $F_{SCLI2C}$ | SCL clock frequency | 0 | 100 | – | – | kHz |
| $T_{HDSTAI2C}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0 | – | – | – | µs |
| $T_{LOWI2C}$ | LOW period of the SCL clock | 4.7 | – | – | – | µs |
| $T_{HIGHI2C}$ | HIGH period of the SCL clock | 4.0 | – | – | – | µs |
| $T_{SUSTAI2C}$ | Setup time for a repeated START condition | 4.7 | – | – | – | µs |
| $T_{HDDATI2C}$ | Data hold time | 0 | – | – | – | µs |
| $T_{SUDATI2C}$ | Data setup time | 250 | – | – | – | ns |
| $T_{SUSTOI2C}$ | Setup Time for STOP Condition | 4.0 | – | – | – | µs |
| $T_{BUFI2C}$ | Bus free time between a STOP and START condition | 4.7 | – | – | – | µs |
| $T_{SPI2C}$ | Pulse width of spikes are suppressed by the input filter. | – | – | – | – | ns |

**Note**

16. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

**Figure 14. Definition of Timing for Fast-/Standard-Mode on the I²C Bus**




## Packaging Information

This section illustrates the packaging specifications for the Part Number device, along with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled PSoC Emulator Pod Dimensions at http://www.cypress.com.

### Packaging Dimensions

**Figure 15. 28-Pin (210-Mil) SSOP**

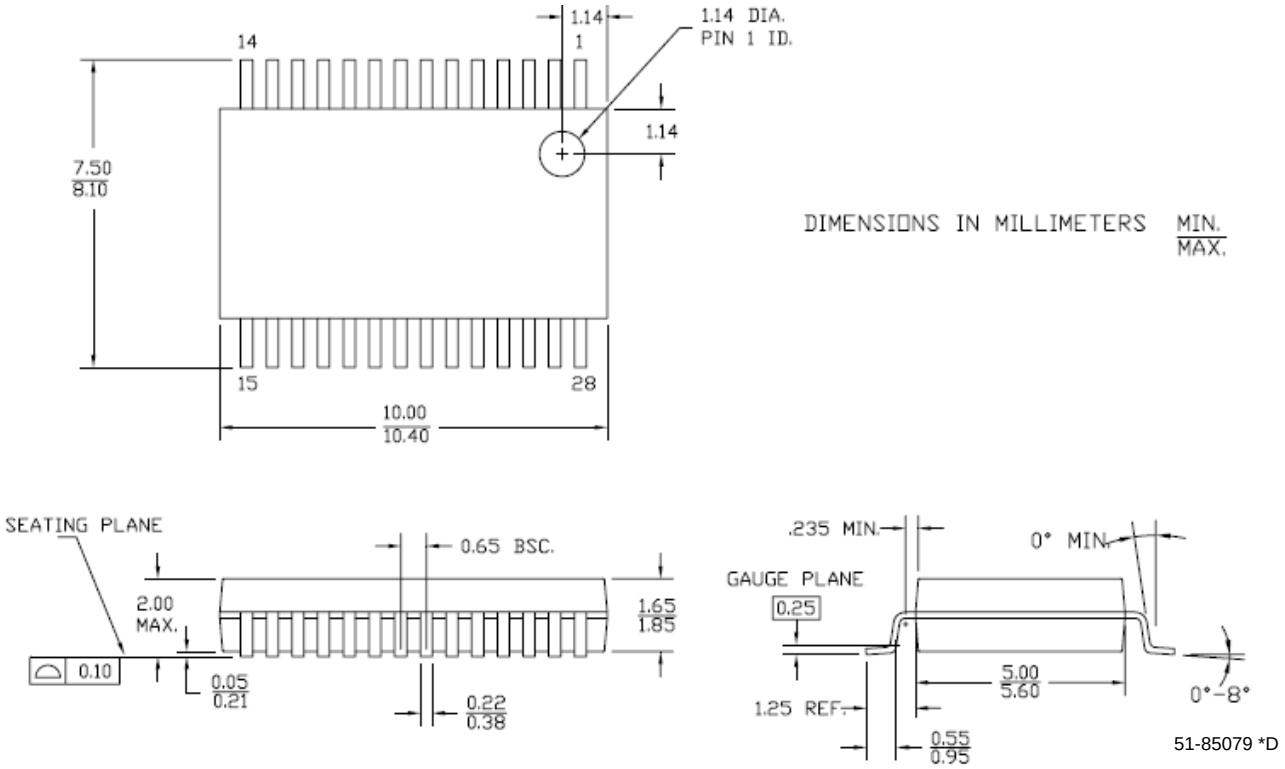
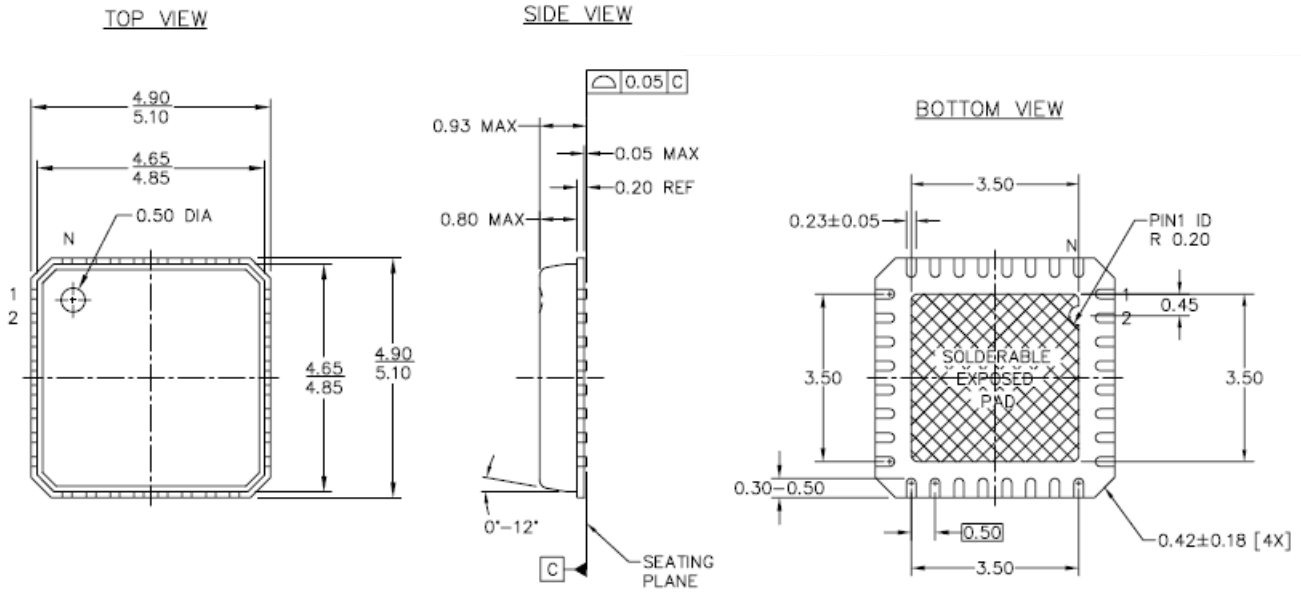


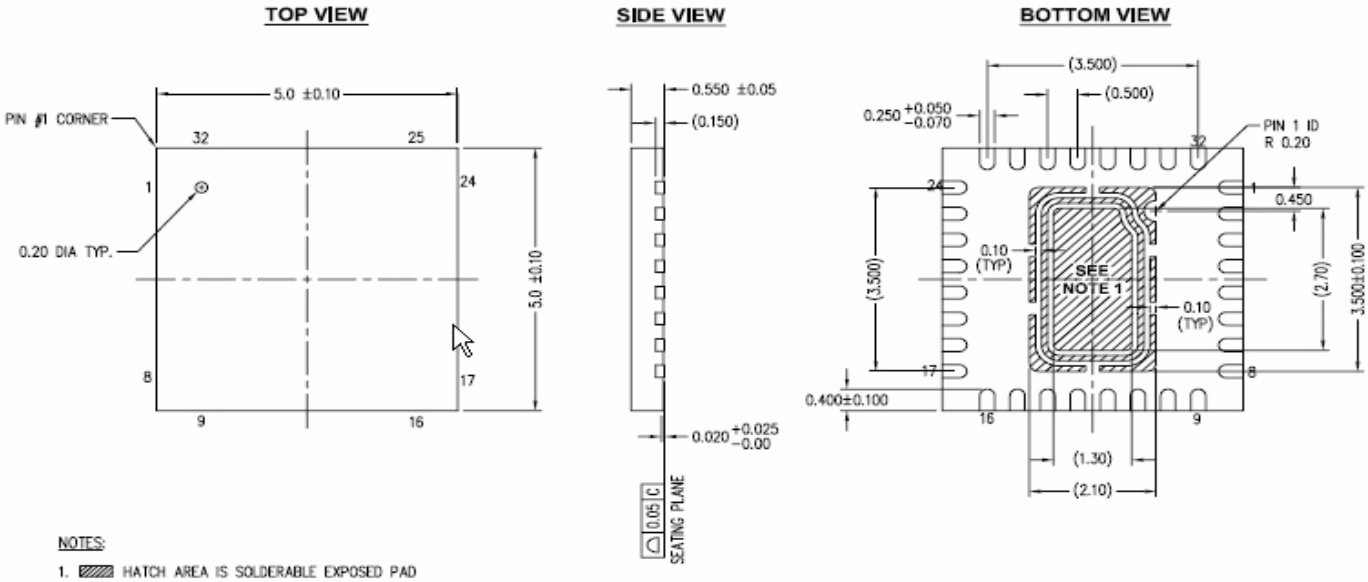
**Figure 16. 32-Pin QFN (5 x 5 mm) (PUNCH)**




NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD.
2. REFERENCE JEDEC#: MO–220
3. PACKAGE WEIGHT: 0.054g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

51-85188 *D

**Figure 17. 32-Pin QFN (5 x 5 mm) (SAWN)**




NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO–248
3. PACKAGE WEIGHT: 0.0388g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 *B

## Thermal Impedances

**Table 31. Thermal Impedances per Package**

| Package | Typical $\theta_{JA}$ [17] | Typical $\theta_{JC}$ |
|---|---|---|
| 28 SSOP | 96 °C / W | 39 °C / W |
| 32 QFN [19] | 22 °C / W | 12 °C / W |

## Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

**Table 32. Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature | Time at Maximum Peak Temperature |
|---|---|---|
| 28 SSOP | 260 °C | 20 s |
| 32 QFN | 260 °C | 20 s |

**Notes**

17. $T_J = T_A + \text{Power} \times \theta_{JA}$
18. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220±5 °C with Sn-Pb or 245±5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.
19. To achieve the thermal impedance specified for the QFN package, refer to "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" available at http://www.amkor.com.

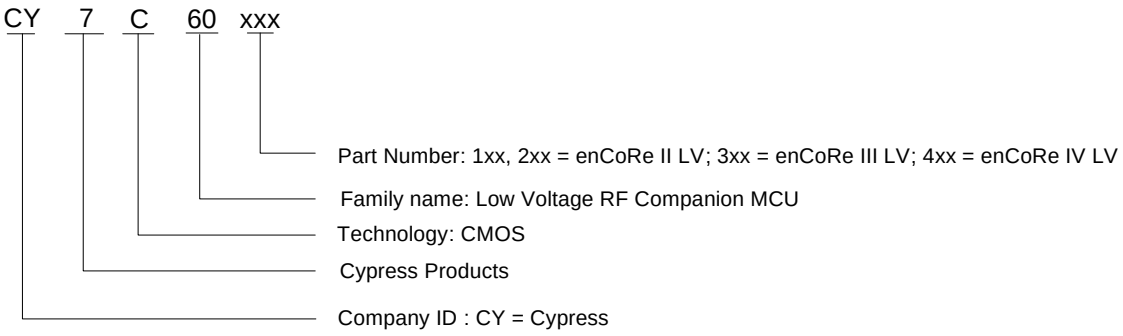
## Ordering Information

The following table lists the Part Number device's key package features and ordering codes

**Table 33. Part Number Device Key Features and Ordering Information**

| Package Type | Ordering Part Number | Flash Size | RAM Size | SMP | I/O |
|---|---|---|---|---|---|
| 28-SSOP | CY7C60323-PVXC | 8K | 512 | No | 24 |
| 28-SSOP Tape and Reel | CY7C60323-PVXCT | 8K | 512 | No | 24 |
| 32-QFN SAWN | CY7C60323-LTXC | 8K | 512 | No | 28 |
| 32-QFN SAWN Tape and Reel | CY7C60323-LTXCT | 8K | 512 | No | 28 |
| 32-QFN SAWN | CY7C60333-LTXC | 8K | 512 | Yes | 26 |
| 32-QFN SAWN Tape and Reel | CY7C60333-LTXCT | 8K | 512 | Yes | 26 |

### Ordering Code Definitions



# Acronyms

## Acronyms Used

Table 34 lists the acronyms that are used in this document.

**Table 34. Acronyms Used in this Datasheet**

| Acronym | Description | Acronym | Description |
|---|---|---|---|
| AC | alternating current | MIPS | million instructions per second |
| ADC | analog-to-digital converter | PCB | printed circuit board |
| API | application programming interface | PGA | programmable gain amplifier |
| CPU | central processing unit | PLL | phase-locked loop |
| CT | continuous time | POR | power on reset |
| DAC | digital-to-analog converter | PPOR | precision power on reset |
| DC | direct current | PSoC® | Programmable System-on-Chip |
| DTMF | dual-tone multi-frequency | PWM | pulse width modulator |
| ECO | external crystal oscillator | QFN | quad flat no leads |
| EEPROM | electrically erasable programmable read-only memory | RTC | real time clock |
| GPIO | general purpose I/O | SAR | successive approximation |
| ICE | in-circuit emulator | SC | switched capacitor |
| IDE | integrated development environment | SLIMO | slow IMO |
| ILO | internal low speed oscillator | SMP | switch-mode pump |
| IMO | internal main oscillator | SPI™ | serial peripheral interface |
| I/O | input/output | SRAM | static random access memory |
| ISSP | in-system serial programming | SROM | supervisory read only memory |
| LCD | liquid crystal display | SSOP | shrink small-outline package |
| LPC | low power comparator | USB | universal serial bus |
| LVD | low voltage detect | WDT | watchdog timer |
| MAC | multiply-accumulate | XRES | external reset |

# Reference Documents

*CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM)* (001-14463)

*Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054* (001-14503)

*Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* – available at http://www.amkor.com.

# Document Conventions

## Units of Measure

Table 35 lists the units of measures.

**Table 35. Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| kB | 1024 bytes | µH | microhenry |
| dB | decibels | µs | microsecond |
| °C | degree Celsius | ms | millisecond |
| µF | microfarad | ns | nanosecond |
| fF | femto farad | ps | picosecond |
| pF | picofarad | µV | microvolts |
| kHz | kilohertz | mV | millivolts |
| MHz | megahertz | mVpp | millivolts peak-to-peak |
| rt-Hz | root hertz | nV | nanovolts |
| kΩ | kilohm | V | volts |
| Ω | ohm | µW | microwatts |
| µA | microampere | W | watt |
| mA | milliampere | mm | millimeter |
| nA | nanoampere | ppm | parts per million |
| pA | pikoampere | % | percent |

## Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

# Glossary

| | |
|---|---|
| active high | 5. A logic signal having its asserted state as the logic 1 state.<br>6. A logic signal having the logic 1 state as the higher voltage of the two states. |
| analog blocks | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more. |
| analog-to-digital (ADC) | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation. |
| API (Application Programming Interface) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications. |
| asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |
| bandgap reference | A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference. |

## Glossary (continued)

| | |
|---|---|
| bandwidth | 1. The frequency range of a message or information processing system measured in hertz.<br>2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum. |
| bias | 1. A systematic deviation of a value from a reference value.<br>2. The amount by which the average of a set of values departs from a reference value.<br>3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |
| block | 1. A functional unit that performs a single function, such as an oscillator.<br>2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block. |
| buffer | 1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.<br>2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.<br>3. An amplifier used to lower the output impedance of a system. |
| bus | 1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.<br>2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].<br>3. One or more conductors that serve as a common connection for a group of related devices. |
| clock | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks. |
| comparator | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements. |
| compiler | A program that translates a high level language, such as C, into machine language. |
| configuration space | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’. |
| crystal oscillator | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components. |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression. |
| data bus | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions. |
| debugger | A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory. |
| dead band | A period of time when neither of two or more signals are in their active state or in transition. |

## Glossary (continued)

| | |
|---|---|
| digital blocks | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI. |
| digital-to-analog (DAC) | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation. |
| duty cycle | The relationship of a clock period high time to its low time, expressed as a percent. |
| emulator | Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system. |
| external reset (XRES) | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state. |
| flash | An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off. |
| Flash block | The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes. |
| frequency | The number of cycles or events per unit of time, for a periodic function. |
| gain | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB. |
| $I^2C$ | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE | The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer). |
| input/output (I/O) | A device that introduces data into or extracts data from a system. |
| interrupt | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution. |
| jitter | 1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams.<br>2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. |
| low-voltage detect (LVD) | A circuit that senses Vdd and provides an interrupt to the system when Vdd falls below a selected threshold. |

## Glossary (continued)

| | |
|---|---|
| M8C | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space. |
| master device | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device*.** |
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |
| modulator | A device that imposes a signal on a carrier. |
| noise | 1. A disturbance that affects a signal and that may distort the information carried by the signal.<br>2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| phase-locked loop (PLL) | An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| power on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset. |
| PSoC® | Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress. |
| PSoC Designer™ | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied measurand |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a know state. See hardware reset and software reset. |

## Glossary (continued)

| | |
|---|---|
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |
| serial | 1. Pertaining to a process in which all events occur one after the other.<br>2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |
| SRAM | An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device. |
| SROM | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash. |
| stop bit | A signal following a character or block that prepares the receiving device to receive the next character or block. |
| synchronous | 1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.<br>2. A system whose operation is synchronized by a clock signal. |
| tri-state | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net. |
| UART | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits. |
| user modules | Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function. |
| user space | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program. |
| $V_{DD}$ | A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V. |
| $V_{SS}$ | A name for a power net meaning "voltage source." The most negative power supply signal. |
| watchdog timer | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time. |

## Document History Page

| Description Title: CY7C603xx, enCore™ III Low Voltage<br>Document Number: 38-16018 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 339394 | BON | See ECN | New Advance Data Sheet. |
| *A | 399556 | BHA | See ECN | Changed from Advance Information to Preliminary.<br>Changed data sheet format.<br>Removed CY7C604xx. |
| *B | 461240 | TYJ | See ECN | Modified Figure 10 to include 2.7 V Vdd at 12 MHz operation. |
| *C | 470485 | TYJ | See ECN | Corrected part numbers in section 4 to match with part numbers in Ordering Information. From CY7C60323-28PVXC, CY7C60323-56LFXC and CY7C60333-56LFXC to CY7C60323-PVXC, CY7C60323-LFXC and CY7C60333-LFXC respectively.<br>Changed from Preliminary to Final data sheet. |
| *D | 513713 | KKVTMP | See ECN | Change title from Wireless enCoRe II to enCoRe III Low Voltage.<br>Applied new template formatting. |
| *E | 2197567 | UVS/AESA | See ECN | Added 32-Pin Sawn QFN Pin Diagram, package diagram, and ordering information. |
| *F | 2620679 | CMCC/PYRS | 12/12/2008 | Added Packaging Handling information.<br>Deleted note regarding link to amkor.com for MLF package dimensions. |
| *G | 2852393 | XUT | 01/15/2010 | Added Table of Contents.<br>Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows:<br>Replaced TRAMP (time) with SRPOWER_UP (slew rate) specification.<br>Added $I_{OH}$, $I_{OL}$, DCILO, F32K_U, TPOWERUP, TERASEALL, TPROGRAM_HOT, and TPROGRAM_COLD specifications.<br>Updated copyright and Sales, Solutions, and Legal Information URLs.<br>Updated 28-Pin SSOP and 32-Pin QFN (PUNCH and SAWN) package diagrams. |
| *H | 2892683 | NJF | 03/15/2010 | Updated Cypress website links.<br>Updated Development Kits.<br>Updated 3.3 V AC Chip-Level Specifications and 2.7 V AC Chip-Level Specifications.<br>Removed AC Analog Mux Bus Specs section.<br>Updated 32-pin Sawn QFN package diagram.<br>Removed inactive parts from Ordering Information. |
| *I | 2911952 | GNKK | 04/13/2010 | Updated revision in the footer. |
| *J | 3014656 | BHA | 09/15/2010 | Updated Logic Block Diagram to enCore III LV.<br>Added Ordering Code Definitions<br>Added Acronyms and Units of Measure table.<br>Datasheet updated as per latest Template. |
| *K | 3114976 | NJF | 12/19/10 | Updated 3.3-V and 2.7-V AC Digital Block Specifications.<br>Updated DC Operational Amplifier Specifications.<br>Updated $I^2C$ Timing Diagram.<br>Added DC $I^2C$ Specifications.<br>Added UILO max limit.<br>Added Tjit_IMO specification, removed existing jitter specifications.<br>Updated Units of Measure, Acronyms, Glossary, and References sections.<br>Updated solder reflow specifications. |

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