CY7C199

32K x 8 Static RAM

Features

- **High speed**
  - **— 12 ns**
- **Fast t_{DOE}**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 495 mW (Max, “L” version)**
- **Low standby power**
  - **— 0.275 mW (Max, “L” version)**
- **2V data retention (“L” version only)**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **Available in pb-free 28-pin TSOP I and 28-pin (300-Mil) Molded DIP**

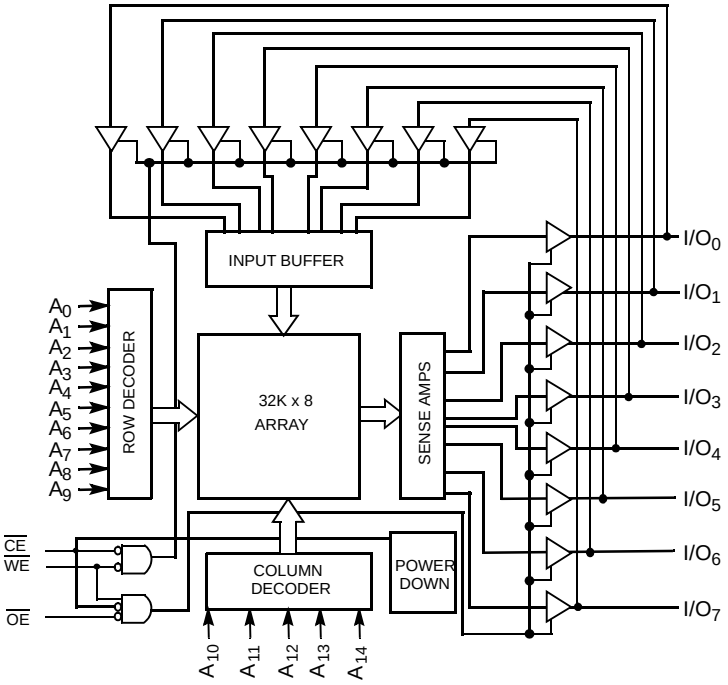
Functional Description

The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and active LOW Output Enable ($\overline{OE}$) and tri-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW Write Enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

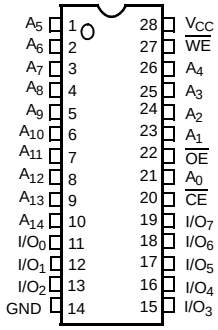
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ($\overline{WE}$) is HIGH. A die coat is used to improve alpha immunity.

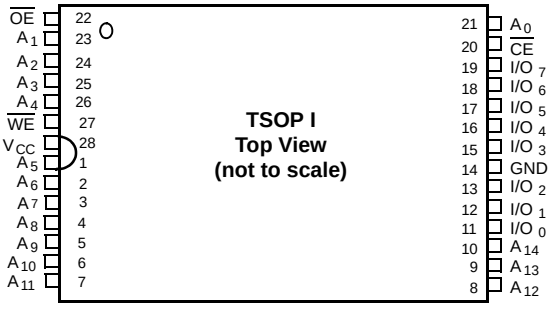
Logic Block Diagram



Pin Configurations

DIP
Top View





Selection Guide

		–12	–15	–20	Unit
Maximum Access Time		12	15	20	ns
Maximum Operating Current		160	155	150	mA
	L		90		
Maximum CMOS Standby Current		10	10	10	mA
	L		0.05		

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[1] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range [3]

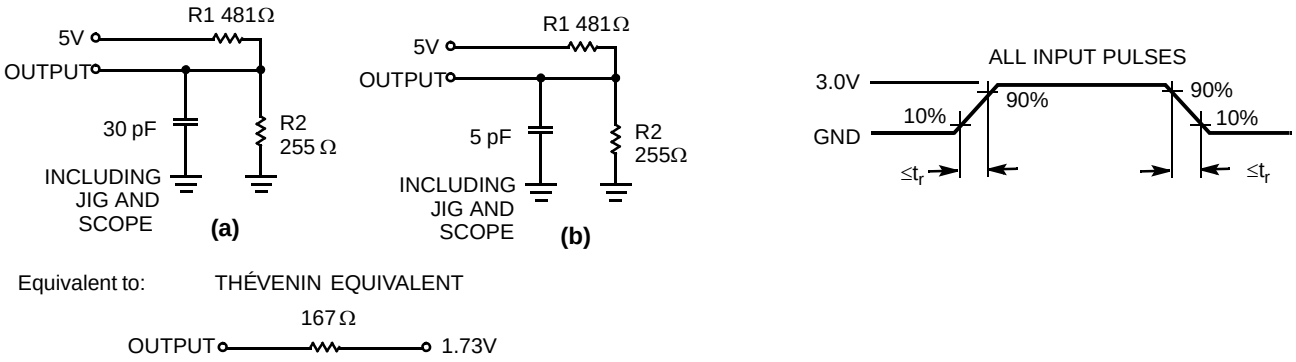
Parameter	Description	Test Conditions		-12		-15		-20		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH}=–4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL}=8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage			–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–5	+5	–5	+5	–5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	–5	+5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		160		155		150	mA
			L				90			mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		30		30	mA
			L				5			mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		10		10		10	mA
			L				0.05			mA

Notes:
1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	8	pF
C_{OUT}	Output Capacitance		8	pF

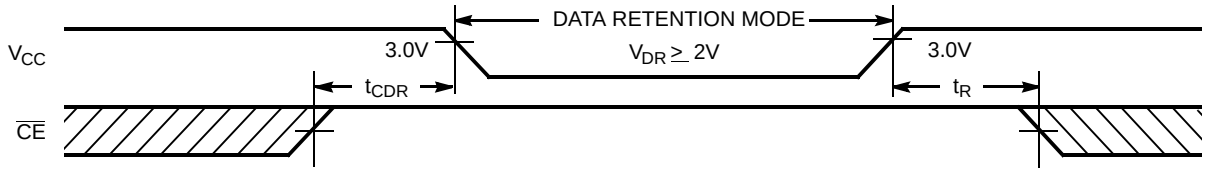
AC Test Loads and Waveforms[5]



Data Retention Characteristics Over the Operating Range (L-version only)

Parameter	Description	Conditions[6]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		10	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time		0		ns
t_R[5]	Operation Recovery Time		200		µs

Data Retention Waveform



Notes:
4. Tested initially and after any design or process changes that may affect these parameters.
5. $t_R \leq 3$ ns for the -12 and the -15 speeds. $t_R \leq 5$ ns for the -20 and slower speeds.
6. No input may exceed V_{CC} + 0.5V.

Switching Characteristics Over the Operating Range [3,7]

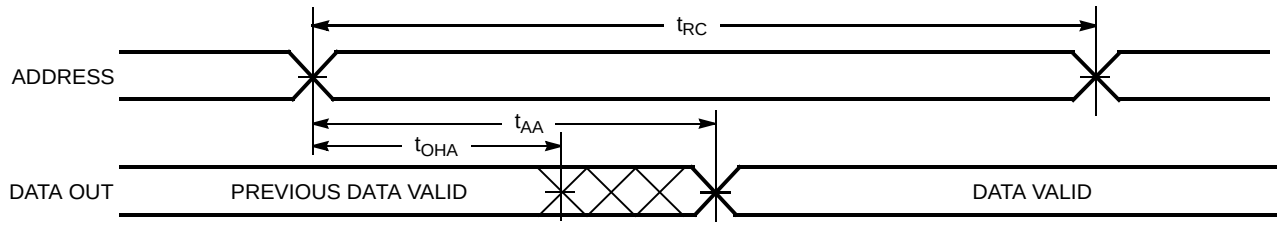
Parameter	Description	-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		7		9	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[8]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8, 9]		5		7		9	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[8]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[8, 9]		5		7		9	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		12		15		20	ns
Write Cycle[10, 11]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		ns
t_{AW}	Address Set-up to Write End	9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		15		ns
t_{SD}	Data Set-up to Write End	8		9		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[9]		7		7		10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[8]	3		3		3		ns

Notes:

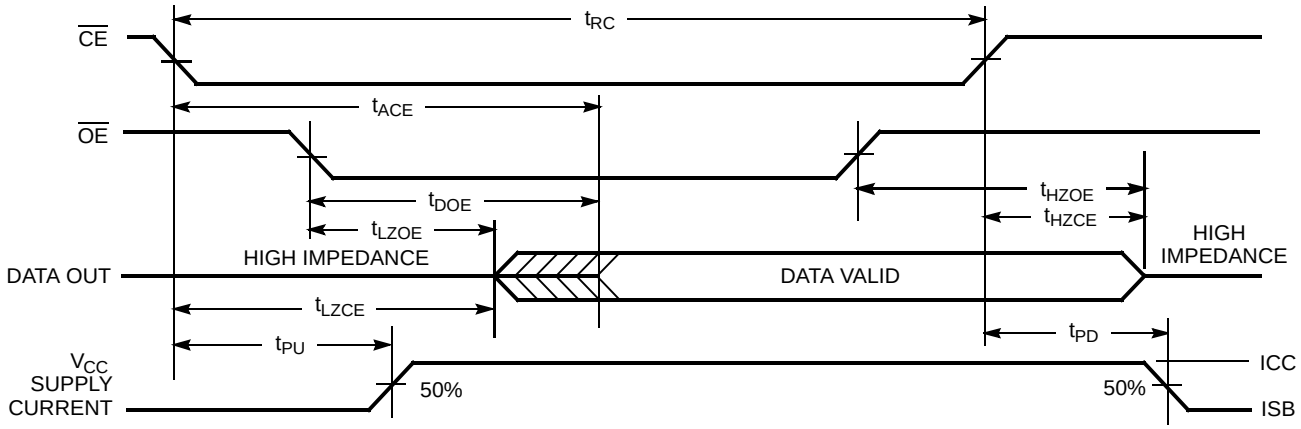
7. Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Read Cycle No. 1[12, 13]



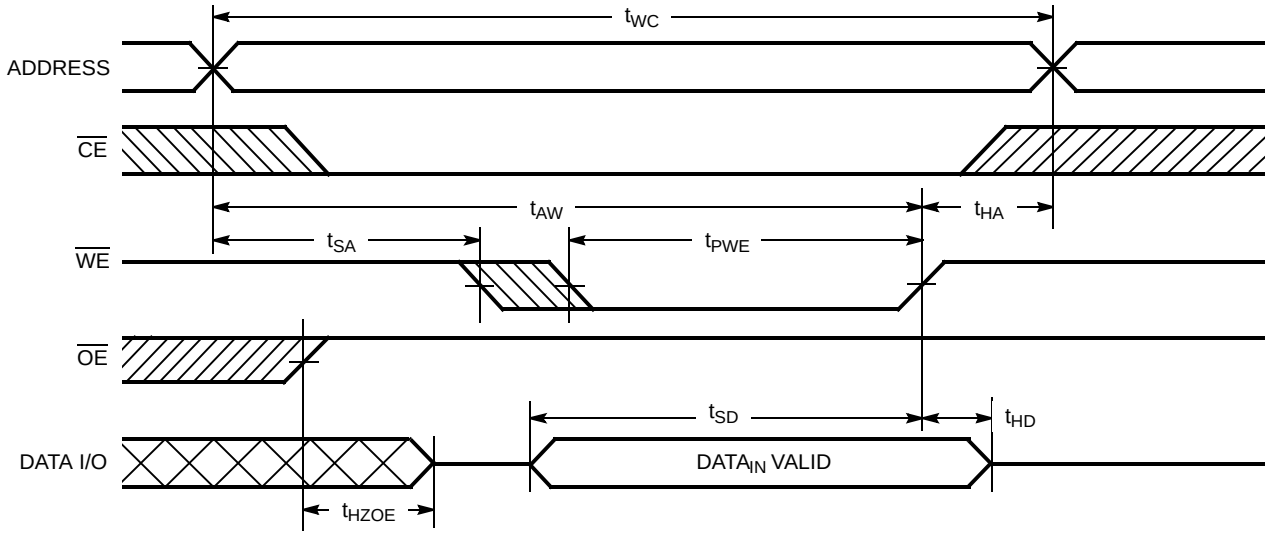
Read Cycle No. 2 [13, 14]



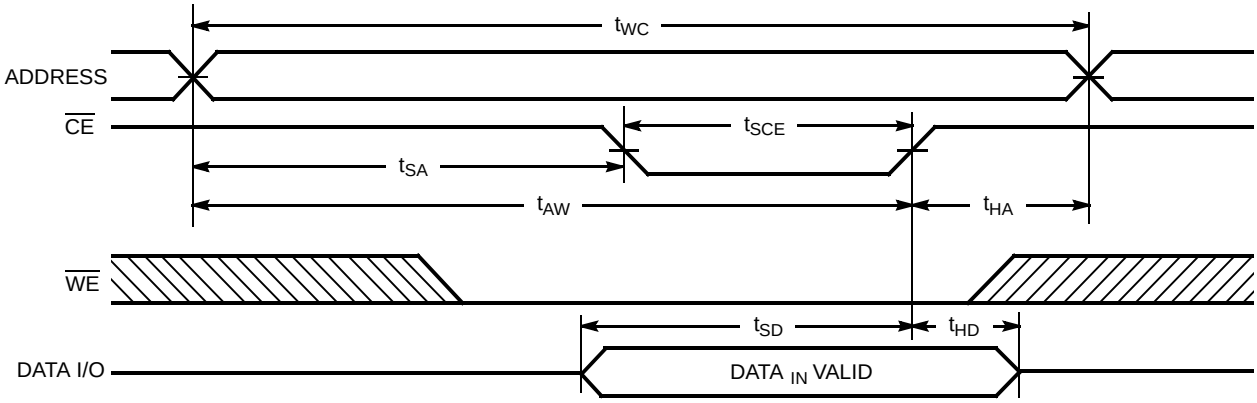
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)[10, 15, 16]



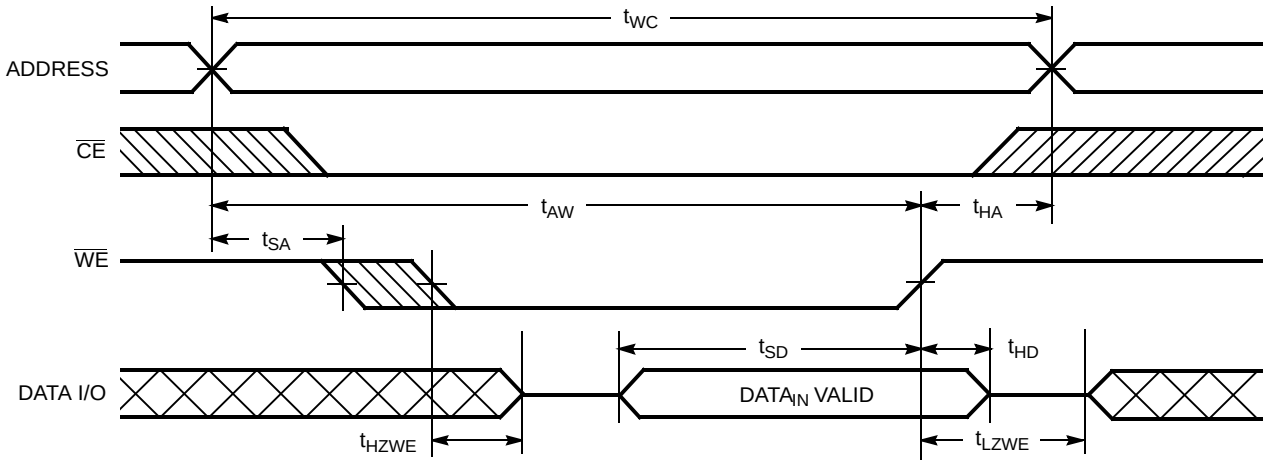
Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 15, 16]



Notes:
15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

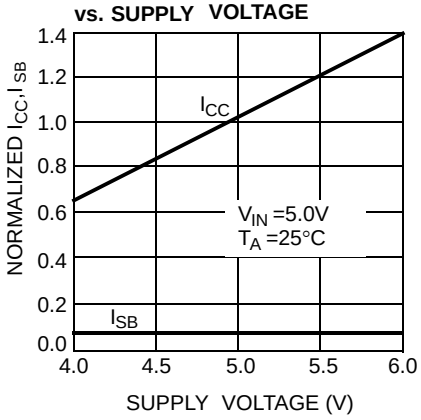
Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled $\overline{OE}$ LOW)[11, 16]

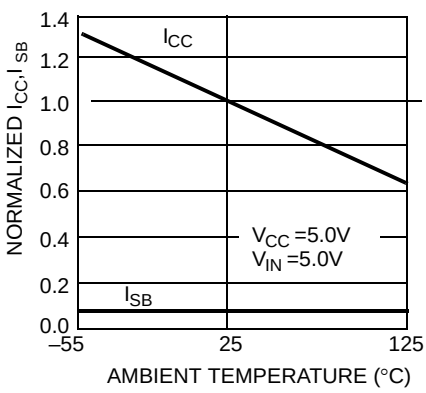


Typical DC and AC Characteristics

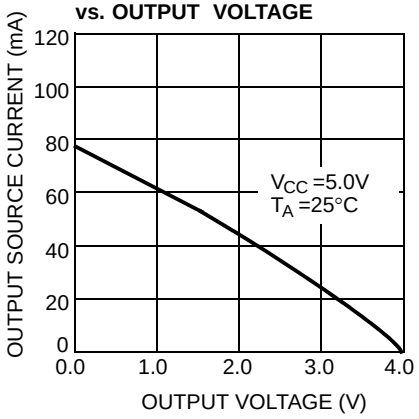
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



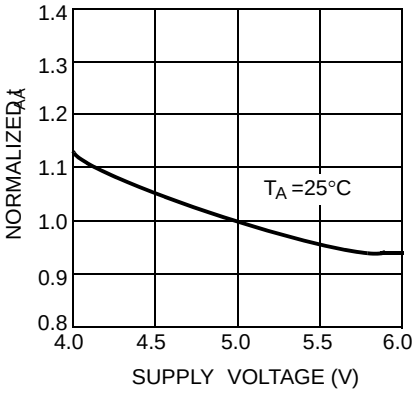
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



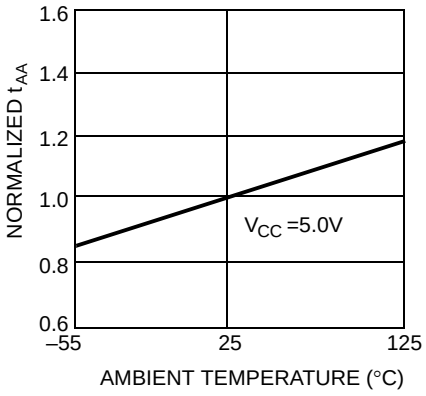
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



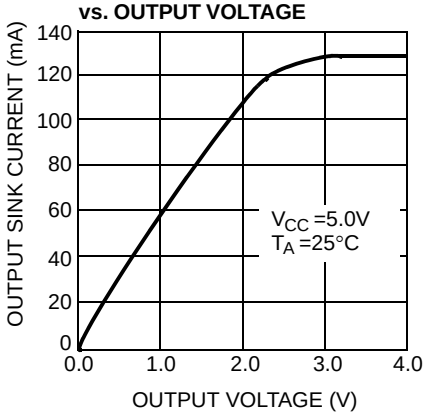
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



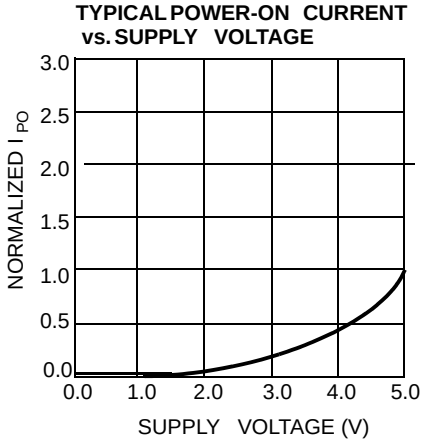
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

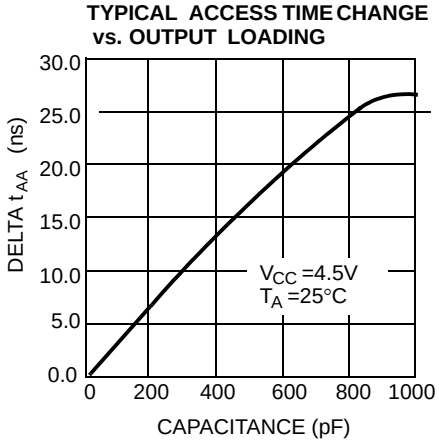


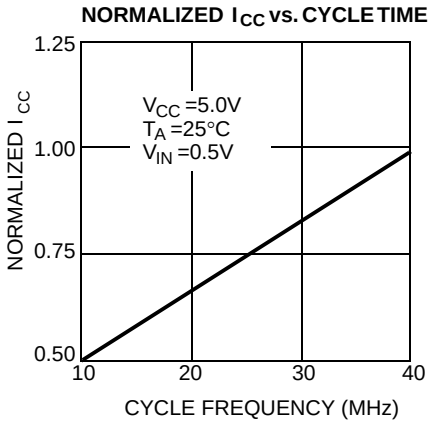
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Typical DC and AC Characteristics (continued)







Truth Table

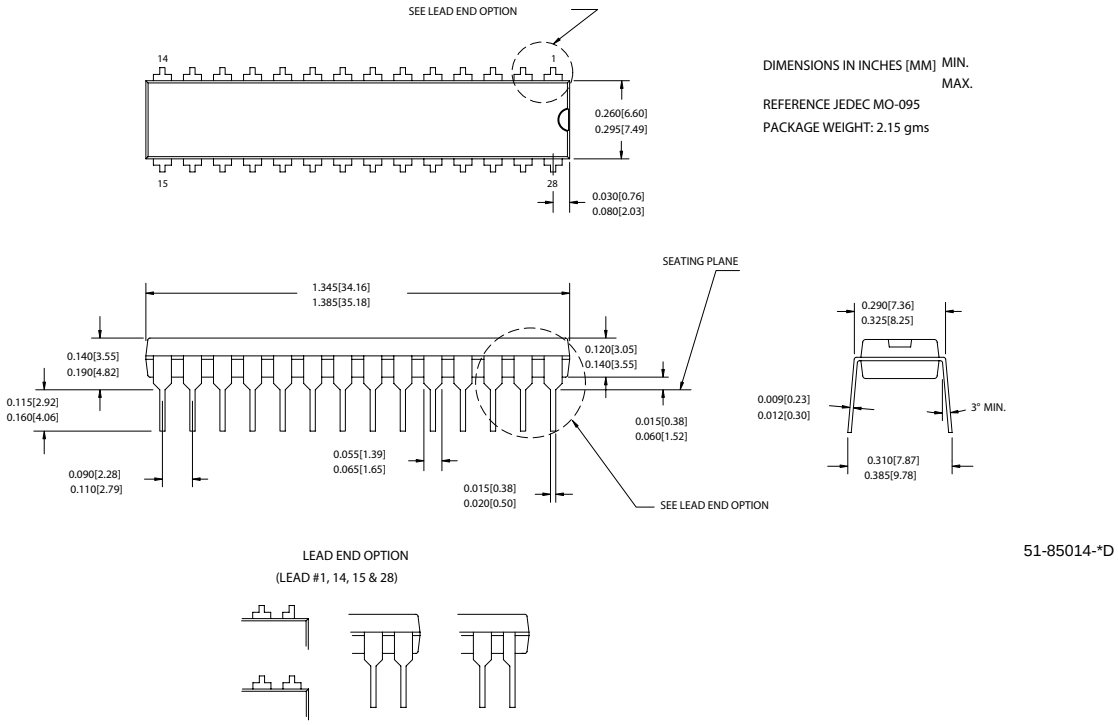
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C199-12ZXC	51-85071	28-pin TSOP I (Pb-free)	Commercial
15	CY7C199-15ZXC	51-85071	28-pin TSOP I (Pb-free)	Commercial
	CY7C199L-15ZXC			
20	CY7C199-20PXC	51-85014	28-pin (300-Mil) Molded DIP (Pb-free)	Commercial

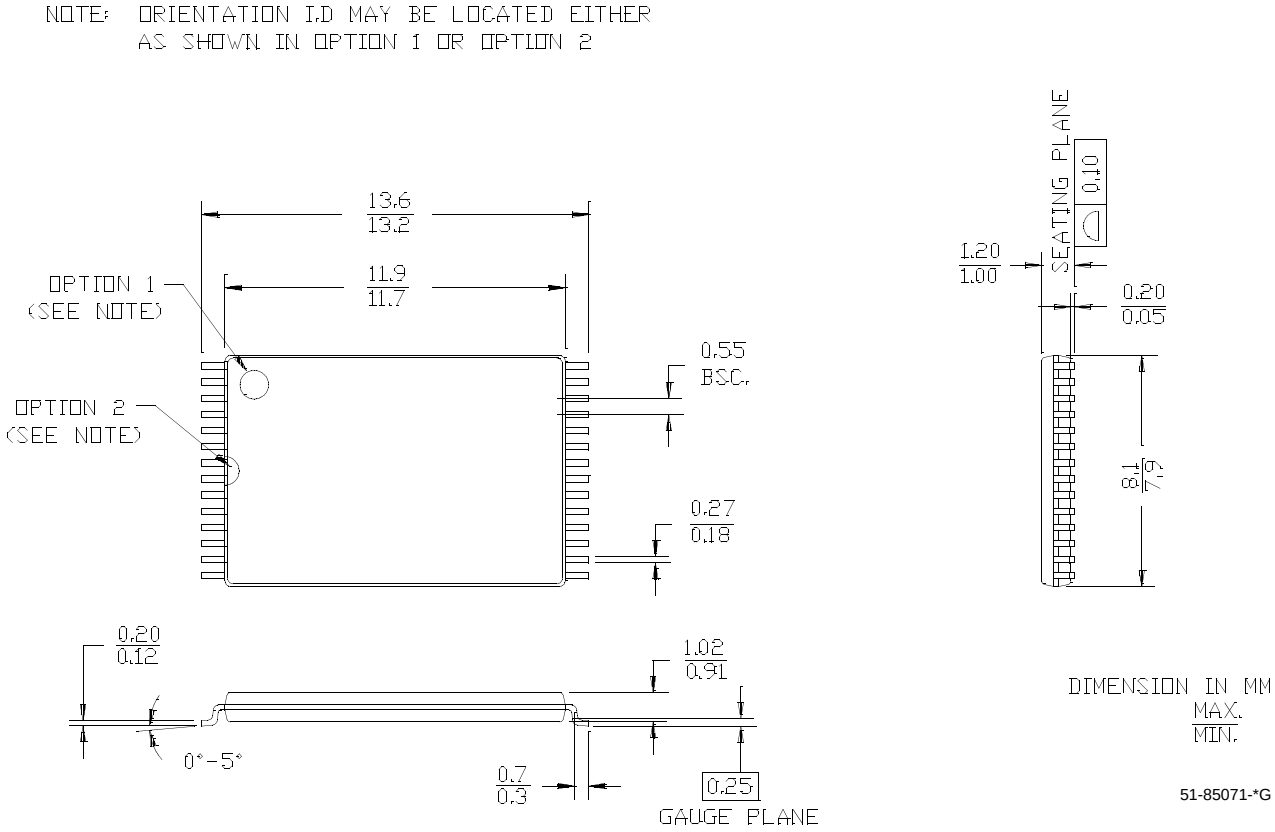
Package Diagrams

28-pin (300-Mil) PDIP (51-85014)



Package Diagrams (continued)

28-pin TSOP Type 1 (8x13.4 mm) (51-85071)



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Document History Page

Document Title: CY7C199 32K x 8 Static RAM Document Number: 38-05160				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109971	10/28/01	SZV	Change from Spec number: 38-00239 to 38-05160
*A	121730	01/09/02	DFP	Updated Product Offering table
*B	492500	See ECN	NXR	Removed 8 ns, 10 ns, 25 ns , 35 ns, 45 ns speed bins Removed 28-Lead (300-Mil) CerDIP, 28-Pin Rectangular Leadless Chip Carrier, 28-Lead Molded SOIC, 28-Lead Molded SOJ packages from product offering Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics Table Updated Ordering Information Table