BlueCore® CSR8811™ A08 0.5mm WLCSP

Bluetooth v4.0

Bluetooth low energy

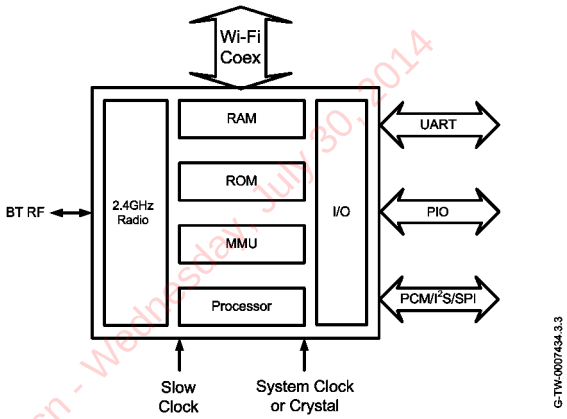
Production Information

CSR8811A08-ICXR-R

Issue 3

Features

- Dual-mode Bluetooth®/Bluetooth low energy radio
- Fully qualified Bluetooth v4.0 IC
- Bluetooth Smart Ready
- Can form part of Bluetooth v4.0 + HS system
- Class 1 or Class 2 Bluetooth power levels
- High-sensitivity Bluetooth and Bluetooth low energy receiver
- Full-speed Bluetooth operation with full piconet and scatternet support
- On-chip balun and minimal BOM
- Low-power selectable 1.2 to 3.6V I/O
- Integrated I/O and core regulators
- High-speed UART port (up to 4Mbps)
- HFP v1.6 wide-band speech supported on-chip
- On-chip encoding of SBC and aptX® codecs for A2DP music streaming
- PCM/I²S digital audio interface
- Support for IEEE 802.11 coexistence
- Green (RoHS and no antimony or halogenated flame retardants)
- Optimised for use on low-cost PCBs



General Description

The CSR8811™ is a product from CSR's Connectivity Centre. It is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including EDR to 3Mbits/s and Bluetooth low energy.

CSR8811's dual-mode radio enables it to connect to the billions of Bluetooth products already on the market, as well as a new generation of Bluetooth low energy devices.

Bluetooth low energy allows mobile devices to exchange simple data sets with very low consumption. Example use cases include watches, medical sensors and fitness trainers that can operate for many years from a small coin cell battery. CSR8811 brings Bluetooth low energy to the mobile phone, allowing it to connect to this new class of devices.

When used with CSR Synergy Software™ and a CSR UniFi ® wireless chip, CSR8811 provides a system fully qualifiable to the Bluetooth v4.0 + HS system for faster file transfer.

This family of Bluetooth products includes:

- CSR8311™ A08 for automotive applications
- CSR8510™ A06 for PCs and USB dongles

Products requiring a standalone Bluetooth low energy radio should use CSR1000™ or CSR1001™ ICs.

Applications

- Low-cost phones, Feature phones, Smartphones
- Personal Navigation Devices (PNDs)
- Portable media Players (PMPs)

CSR designed CSR8811 to reduce PCB area and the number of external components:

- The high-power Class 1 Bluetooth transmitter removes the requirement for external amplification.
- The balun is integrated, which results in a single-ended 50Ω port that does not require additional matching components.
- Integrated LDOs, with minimum decoupling components, allow the chip to be operated directly from the battery or a regulated supply.
- No requirement for external inductors.

This ensures that production costs are minimised.

The device incorporates auto-calibration and BIST routines to simplify development, type approval and production test.

To improve the performance of both Bluetooth and IEEE 802.11b/g/n co-located systems a wide range of coexistence features are supported.

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Device Details

Bluetooth low energy

- Dual mode Bluetooth low energy radio
- Supports simultaneous Bluetooth BR/EDR and multiple low energy connections
- Support for on-chip AES encryption
- Adaptive Bluetooth/Bluetooth low energy scheduler
- On-chip whitelist support

Bluetooth Radio

- On-chip balun (50Ω impedance in TX and RX modes)
- No external trimming is required in production
- Bluetooth v4.0 specification compliant

Bluetooth Transmitter

- Class 1, Class 2 and Class 3 support without need for external power amplifier or TX/RX switch
- DQPSK and 8DPSK

Bluetooth Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Channel classification for AFH
- DQPSK and 8DPSK

Baseband and Software

- Internal RAM allows full-speed data transfer, mixed voice and data, and full piconet operation, including all medium rate packet types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Includes support for eSCO and AFH
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Bluetooth Stack

- CSR's Bluetooth Protocol Stack runs on the on-chip MCU in the configuration Standard HCI over UART

Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter
- Compatible with external clock 19.2MHz to 40MHz
- Can be operated from external crystal

Physical Interfaces

- UART interface with programmable baud rate up to 4Mbits/s
- BCSP, H4, H4DS and H5 support
- PCM/I^2S interface
- Synchronous serial interface up to 4Mbits/s for system debugging

Auxiliary Features

- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low power Park/Sniff/Hold mode
- Auto Baud Rate setting, depending on host interface
- On-chip linear regulators:
  - 1.8V output from typical 2.5 to 4.8V (5.5V for short periods) input (load current 100mA)
  - Low dropout linear regulators producing internal supply voltages from 1.8V, and allowing operation directly from a battery
- Power-on-reset cell detects low supply voltage
- Arbitrary sequencing of power supplies is permitted

Package

- 28-ball 2.57 x 3.21 x 0.6mm, 0.5mm pitch WLCSP

  Note:

  This IC has the same package size as the previous CSR8811 WLCSP 0.5mm pitch versions and the CSR8810 WLCSP 0.5mm pitch ICs.
- Can be used on low-cost PCBs without the need for blind vias

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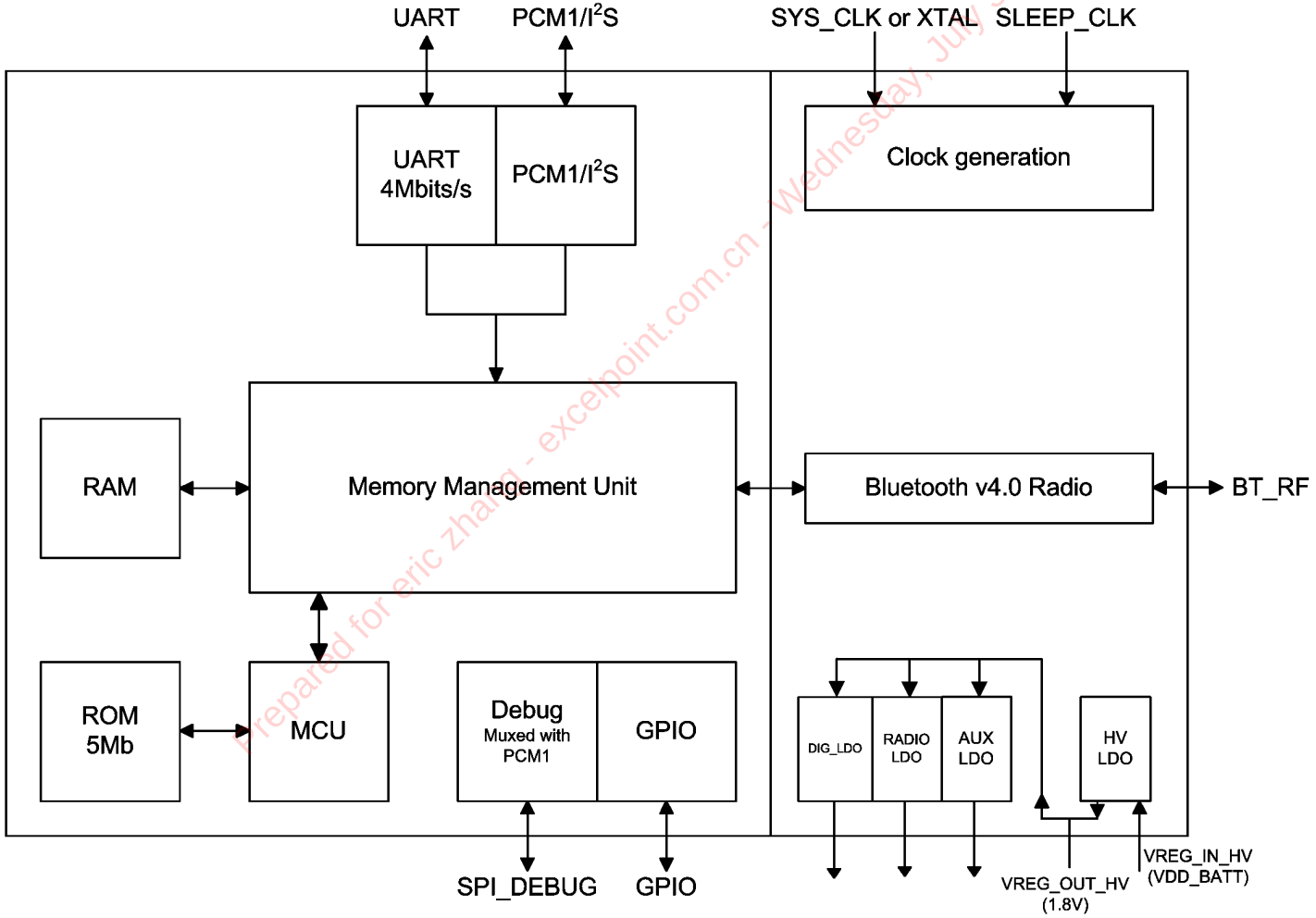
Functional Block Diagram



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Document History

Revision	Date	Change Reason
1	20 JAN 12	Original publication of this document.
2	13 SEP 12	Not released.
3	02 OCT 12	Updated High-voltage Linear Regulator section, Negative Resistance Model section, RoHS/Green information and package dimensions image. Removed VDD_HOST. If you have any comments about this document, email Comments@csr.com giving the number, title and section with your feedback.

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Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

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Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

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1 Package Information

1.1 Pinout Diagram

Orientation from top of device

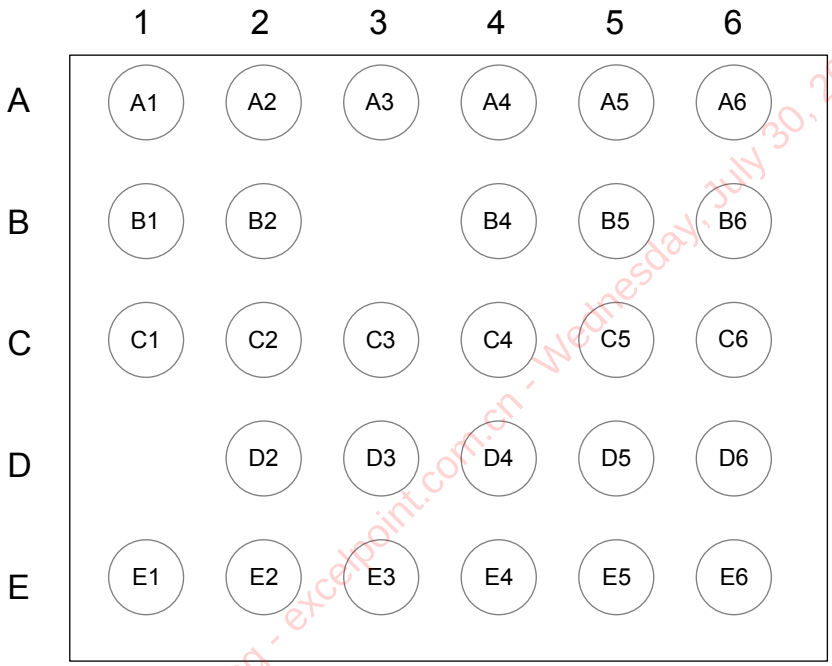

Figure 1.1: Pinout Diagram

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1.2 Device Terminal Functions

Bluetooth RF	Ball	Pad Type	Supply Domain	Description
BT_RF	B1	RF	VDD_RADIO	Bluetooth transmitter/receiver

Synthesisor and Oscillator	Ball	Pad Type	Supply Domain	Description
SYS_CLK XTAL_IN	A3	Analogue	VDD_AUX	For external system clock input or crystal
XTAL_OUT	A2			Ground connections drive for crystal

UART Interface	Ball	Pad Type	Supply Domain	Description
UART_TX	A6	Bidirectional, tristate, with weak internal pull-up	VDD_PADS	UART data output, active high
UART_RX	B5			UART data input, active high
UART_CTS	C5			UART clear to send, active low
UART_RTS	B6			UART request to send, active low

PCM Interface	Ball	Pad Type	Supply Domain	Description
PCM_OUT	E2	Output, tristate, with weak internal pull-down	VDD_PADS	PCM synchronous data output
SPI_MISO				SPI data output
PCM_IN	D4	Input, tristate, with weak internal pull-down		PCM synchronous data input
SPI_MOSI				SPI data input
PCM_SYNC	D2	Bidirectional, tristate, with weak internal pull-down		PCM synchronous data sync
SPI_CS#				SPI chip select, active low
PCM_CLK	D3	Bidirectional, tristate, with weak internal pull-down		PCM synchronous data clock
SPI_CLK				SPI clock
SPI_PCM#_SEL	E6	Input with weak internal pull-down		Control line to select SPI or PCM interface, high = SPI, low = PCM

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PIO Port	Ball	Pad Type	Supply Domain	Description
PIO[0]	E1	Bidirectional, tristate, with weak internal pull-down	VDD_PADS	Programmable input/output line and 32kHz sleep clock input
PIO[1]	E4			Programmable input/output line
PIO[2]	D5			Programmable input/output line, clock REQ out
PIO[3]	E3			Programmable input/output line, clock REQ in
PIO[4]	E5			Programmable input/output line
PIO[9]	C6			Programmable input/output line

Power Supplies	Ball	Pad Type	Description
VREG_EN_RST#	A5	Input with strong internal pull-down	Take high to enable internal regulators. Also acts as active low reset
VREG_IN_HV	B4	Analogue regulator input	Input to internal high-voltage regulator
VREG_OUT_HV	A4	Analogue regulator output	Output from internal high-voltage regulator and input to low-voltage internal regulators
VDD_DIG	D6	VDD	Power supply from digital regulator
VDD_RADIO	B2	VDD	Power supply for Bluetooth radio and LO.
VDD_AUX	C2	VDD	Output capacitor for internal auxiliary regulator
VDD_PADS	C3	VDD	Power supply for digital input/output pads
VSS_DIG	C4	VSS	Ground connections for digital I/O circuitry
VSS_AUX	A1	VSS	Ground connections for LO and auxiliary regulator
VSS_RADIO	C1	VSS	Ground connections for Bluetooth radio

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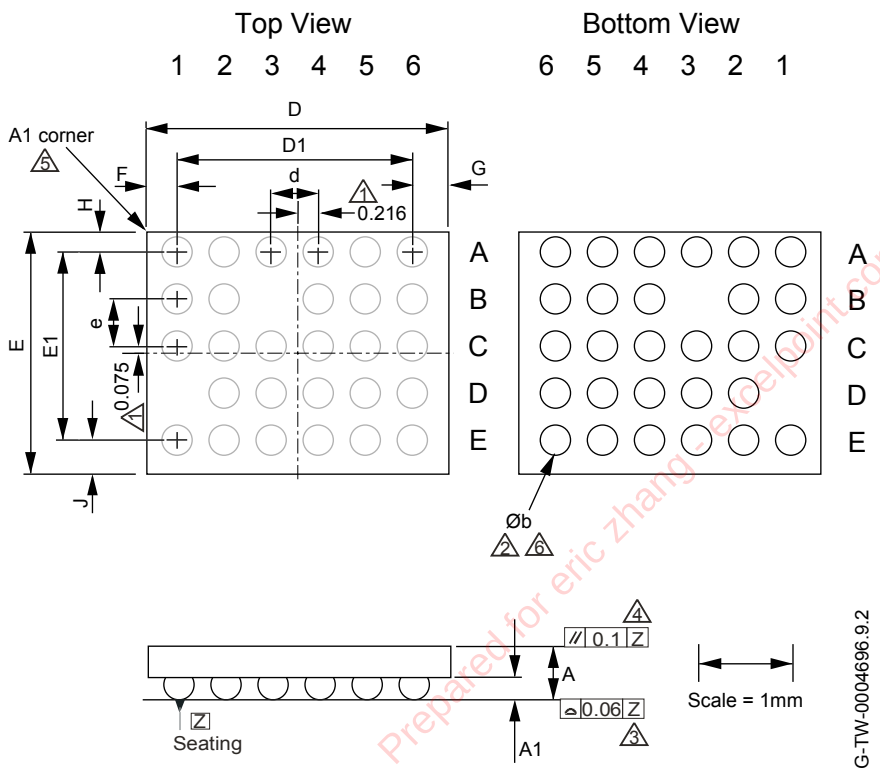
1.3 Package Dimensions



Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.54	0.57	0.60	d	-	0.50	-
A1	0.21	0.24	0.27	e	-	0.50	-
b	0.30	0.32	0.34	F	0.295	0.315	0.335
D	3.169	3.208	3.248	G	0.375	0.395	0.415
E	2.529	2.569	2.609	H	0.185	0.205	0.225
D1	-	2.50	-	J	0.345	0.365	0.385
E1	-	2.00	-				

Notes

1. Midpoint of ball array is offset to centre of component
2. Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
3. Datum Z is defined by spherical crowns of the solder balls
4. Parallelism measurement shall exclude any effect of mark on top surface of package
5. Pin A1 polarity mark
6. UBM is 300µm

Description	28-ball WLCSP		
Size	2.57 x 3.21 x 0.6mm	**JEDEC**	Non JEDEC
Pitch	0.5mm pitch	**Units**	mm

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1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 2.57 x 3.21 x 0.6mm WLCSP 28-ball package:

- NSMD lands (that is, lands smaller than the solder mask aperture) are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- Ideally, use via-in-pad technology to achieve truly NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred and this trace should be as thin as possible, this needs to take into consideration its current carrying and the RF requirements.
- 35µm thick (1oz) copper lands are recommended rather than 17µm thick (0.5oz). This results in a greater standoff which has been proven to provide greater reliability during thermal cycling.
- Use 300µm ±10µm land diameters to achieve optimum reliability.
- Solder paste is preferred to flux during the assembly process, because this adds to the final volume of solder in the joint, increasing its reliability.
- When using a nickel gold plating finish, keep the gold thickness below 0.5µm to prevent brittle gold/tin intermetallics forming in the solder.
- The WLCSP is designed so that ball lands do not lie on top of sensitive areas of the active silicon.
- WLCSP components often have the ball array mid-point offset to the centre of the component outline. This requires careful consideration during component PCB footprint design.

1.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

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2 Bluetooth Modem

2.1 Bluetooth Radio Ports

2.1.1 BT_RF

CSR8811 contains an on-chip balun which combines the balanced outputs of the PA on transmit and produces the balanced input signals for the LNA required on receive. No matching components are needed as the receive mode impedance is 50Ω and the transmitter has been optimised to deliver power in a 50Ω load.

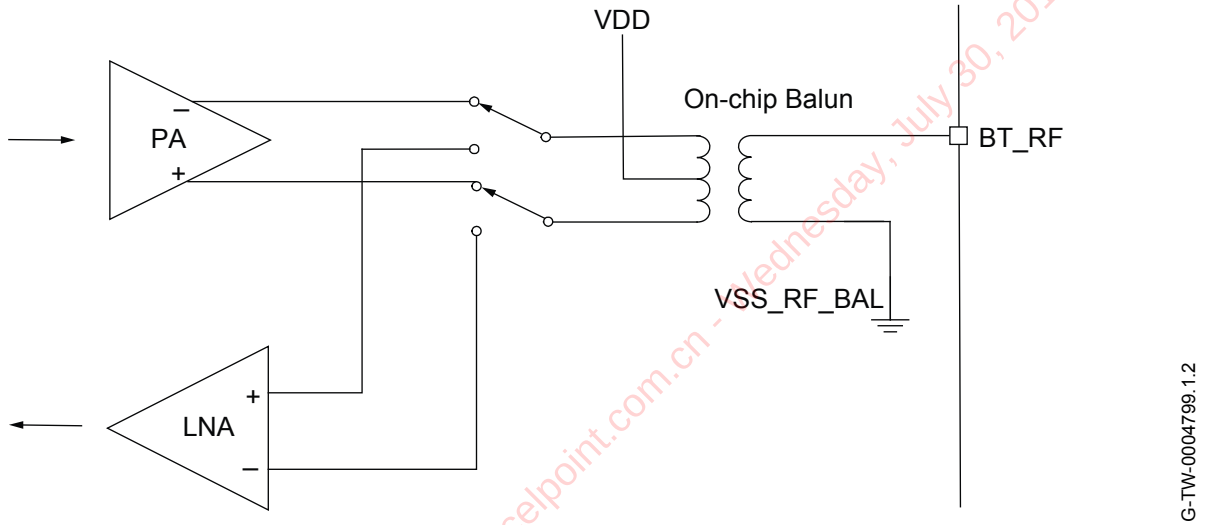

Figure 2.1: Simplified Circuit BT_RF

2.2 Bluetooth Receiver

The receiver features a near-zero IF architecture that enables the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input enables the receiver to operate in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised.

For both basic rate and EDR, an ADC digitises the IF received signal.

2.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the balanced port of the on-chip balun.

2.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the mixer input signal within a limited range. This improves the dynamic range of the receiver, so improving performance in interference limited environments.

2.3 RF Transmitter

2.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

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2.3.2 Power Amplifier

The internal PA output power is software controlled and configured through a PS Key. The internal PA on the CSR8811 has a maximum output power that enables it to operate as a Class 1, Class 2 and Class 3 Bluetooth radio without requiring an external RF PA.

2.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v4.0 specification.

2.5 Baseband

2.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

2.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatches

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3 Clock Input and Generation

The Bluetooth reference clock for the system is generated from an external clock source frequency of between 19.2 and 40MHz, or an external crystal.

All CSR8811 internal digital clocks are generated using a phase locked loop, which is locked to the frequency of the clock source.

3.1 Input Frequencies

CSR8811 must be configured to operate with the chosen reference frequency (using the appropriate PS Key, etc.). This can be any reference frequency between 19.2 and 40MHz. Until a clock reference frequency has been explicitly set from an off-chip source no radio operation is possible. This can be done using the debug and programming interface. Otherwise the default, along with various internal firmware checks, enables communication over the host interface for a limited range of baud rates. Once a host communication is established, PS Keys pertaining to the clock scheme can be configured. This depends on the firmware build. Full details are in the *Release Note* for the CSR8811 firmware build on www.csrsupport.com.

3.2 External Reference Clock

3.2.1 Input: XTAL_IN

CSR8811 can use a TCXO reference clock input into XTAL_IN. In this mode, ground XTAL_OUT.

The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion. If peaks of the reference clock are either below VSS or above VDD_AUX, it must be driven through a DC blocking capacitor (approximately 33 to 100pF) connected to XTAL_IN.

Table 3.1 lists the specification for the external reference clock signal.

	Min	Typ	Max	Unit
Frequency[a]	19.2	26	40	MHz
Frequency tolerance	-20	-	20	ppm
Duty cycle	30:70	50:50	70:30	%
Edge jitter (at zero crossing)	-	-	1.6	ps rms

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CSR8811 A08 0.5mm pitch WLCSP Data Sheet

			Min	Typ	Max	Unit
Phase noise	f_{ref} = 26MHz	1kHz offset	-	-	-120	dBc/Hz
		10kHz offset	-	-	-130	
		100kHz offset	-	-	-135	
Signal level	AC coupled sinusoidal		200	-	VDD_AUX[b]	mV pk-pk
	DC coupled digital	V_{IL}	-	VSS[c]	-	V
		V_{IH}	-	VDD_AUX[b] [c]	-	V

Table 3.1: External Clock Specifications

[a] The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

[b] VDD_AUX is 1.35V nominal

[c] If driven via a DC blocking capacitor max amplitude is reduced to 700mV pk-pk for non 50:50 duty cycle

3.2.2 XTAL_IN Impedance in External Mode

The impedance of XTAL_IN does not change significantly between deep sleep and active modes.

3.2.3 Clock Start-up Delay

CSR8811 hardware incorporates a default 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there are scenarios where the clock is not guaranteed to either exist or be stable after this period. Under these conditions, CSR8811 firmware provides a software function that extends the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 1ms to 31ms. Zero is the default for 5ms delay.

This PS Key enables system optimisation where clock stability latencies are longer or shorter than 5ms, keeping the current consumption of CSR8811 as low as possible. CSR8811 consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

Clock accuracy must be within 20ppm after the delay specified in PSKEY_CLOCK_STARTUP_DELAY. This is to ensure that the radio meets the RF specification. Refer to your product software documentation for a description of PSKEY_CLOCK_STARTUP_DELAY.

3.3 Crystal Oscillator: SYS_CLK and XTAL_OUT

CSR8811 contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. Figure 3.1 shows the external crystal is connected to pins XTAL_IN, XTAL_OUT.

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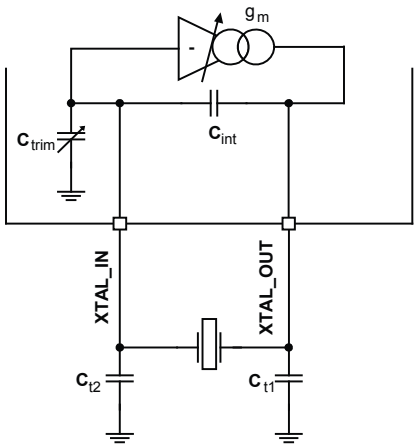

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Figure 3.1: Crystal Driver Circuit

Figure 3.2 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

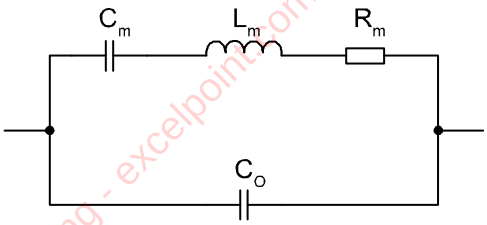

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Figure 3.2: Crystal Equivalent Circuit

The resonant frequency is trimmable with the crystal load capacitance. CSR8811 contains variable internal capacitors to provide a fine trim.

Parameter	Min	Typ	Max	Unit
Frequency	19.2	26	32	MHz
Initial frequency tolerance	-25	-	25	ppm
Pullability	10	15	30	ppm/pF
Amplifier transconductance	2	-	-	mA/V

Table 3.2: Crystal Specification

The CSR8811 driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT.

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CSR8811 A08 0.5mm pitch WLCSP Data Sheet

3.3.1 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. CSR8811 provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing and slew rate at XTAL_IN (to which all on-chip clocks are referred).

Crystal load capacitance, C_l is calculated using Equation 3.1:

$$C_l = C_{int} + \frac{(C_{t2} + C_{trim})\ C_{t1}}{C_{t2} + C_{trim} + C_{t1}}$$

Equation 3.1: Load Capacitance

Note:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

3.3.2 Frequency Trim

CSR8811 enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with an on-chip trim capacitor, C_{trim}. The value of C_{trim} is set by a 6-bit word in PSKEY_ANA_FTRIM. Its value is calculated as follows:

$$C_{trim} = 125fF \times PSKEY_ANA_FTRIM$$

Equation 3.2: Trim Capacitance

The C_{trim} capacitor is connected between XTAL_IN and ground. When viewed from the crystal terminals, the combination of the tank capacitors and the trim capacitor presents a load across the terminals of the crystal which varies in steps of typically 125fF for each least significant bit increment of PSKEY_ANA_FTRIM.

Equation 3.3 describes the frequency trim.

$$\frac{\Delta(F_x)}{F_x} = pullability \times 0.110 \times \left(\frac{C_{t1}}{C_{t1} + C_{t2} + C_{trim}}\right)(ppm/LSB)$$

Equation 3.3: Frequency Trim

Note:

F_x = crystal frequency

Pullability is a crystal parameter with units of ppm/pF

Total trim range is 0 to 63

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 3.4.

$$\frac{\partial(F_X)}{\partial(C_l)} = F_X \bullet \frac{C_m}{2(C_l + C_O)^2}$$

Equation 3.4: Pullability

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Note:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model), see Figure 3.2

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

3.3.3 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in CSR8811 uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit oscillates if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 3.5.

$$g_m > 3\ \frac{(2\pi F_x)^2\ R_m\ ((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + C_{t1}\ (C_{t2} + C_{trim}))}{C_{t1}\ (C_{t2} + C_{trim})}$$

Equation 3.5: Transconductance Required for Oscillation

CSR8811 guarantees a transconductance value of at least 2mA/V at maximum drive level.

Note:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance.

3.3.4 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is as a frequency dependent resistive element. Consider the driver amplifier as a circuit that provides negative resistance. For oscillation, the value of the negative resistance is greater than that of the crystal circuit equivalent resistance. Although the CSR8811 crystal driver circuit is based on a transimpedance amplifier, it is possible to calculate an equivalent negative resistance for it using the formula in Equation 3.6.

$$R_{neg} = \frac{-g_m C_{in} C_{out}}{(2\pi F_x)^2 (C_{in} C_{out} + (C_o + C_{int})(C_{in} + C_{out}))^2}$$

Equation 3.6: Equivalent Negative Resistance

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Note:

g_m is the transconductance of the crystal oscillator amplifier and can be set in a typical range 420 µA/V to 1.65 mA/V typical, dependent on level control 0:15.

C_o is the static capacitance of the crystal, sometimes referred to as the shunt or case capacitance. This parameter is manaufacturer/device-dependent.

$C_{int} = C_{t2} + C_{trim}$, where:

- C_{int} is on-chip parasitic capacitance between the input and output of the crystal amplifier.
- C_{int} <1.5 pF.
- C_{t2} is the external capacitance on the input of the xtal amplifier.
- C_{trim} is on-chip capacitance in parallel with C_{t2} used to trim the xtal on to frequency and has a range 7.5 pF to 11 pF.

$C_{out} = C_{t1}$, where:

- C_{t1} is the external capacitance on the output of the crystal amplifier.

Equation 3.6 shows the negative resistance of the CSR8811 driver as a function of its drive strength.

The value of the driver negative resistance is easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

3.3.5 Crystal PS Key Settings

The CSR8811 firmware automatically controls the drive level on the crystal circuit to achieve optimum input swing. PSKEY_XTAL_TARGET_AMPLITUDE is used by the firmware to servo the required amplitude of crystal oscillation. Refer to the software build release note for a detailed description.

Configure the CSR8811 to operate with the chosen reference frequency.

3.4 Timing for Frequency

Clock accuracy must be 20ppm after the delay specified by the PS Keys configuring the clock startup delay. This assumes PSKEY_CLOCK_STARTUP_DELAY is set to give a 5ms delay (the default). If not, the accuracy must be 20ppm at the point after the delay specified by that PS Key. For more information see the software documentation for a description of PSKEY_CLOCK_STARTUP_DELAY.

3.5 Sleep Clock

The sleep clock is an external 32.768kHz clock for deep sleep and other low-power modes. The sleep clock is required when CSR8811 uses an external reference clock, see Section 3.2. When the CSR8811 uses a crystal oscillator, see Section 3.3, an external sleep clock is not required but would significantly reduce system power consumption.

Note:

Sleep clock can be input on either PIO[0] or PIO[7].

Figure 3.3 shows a typical application.

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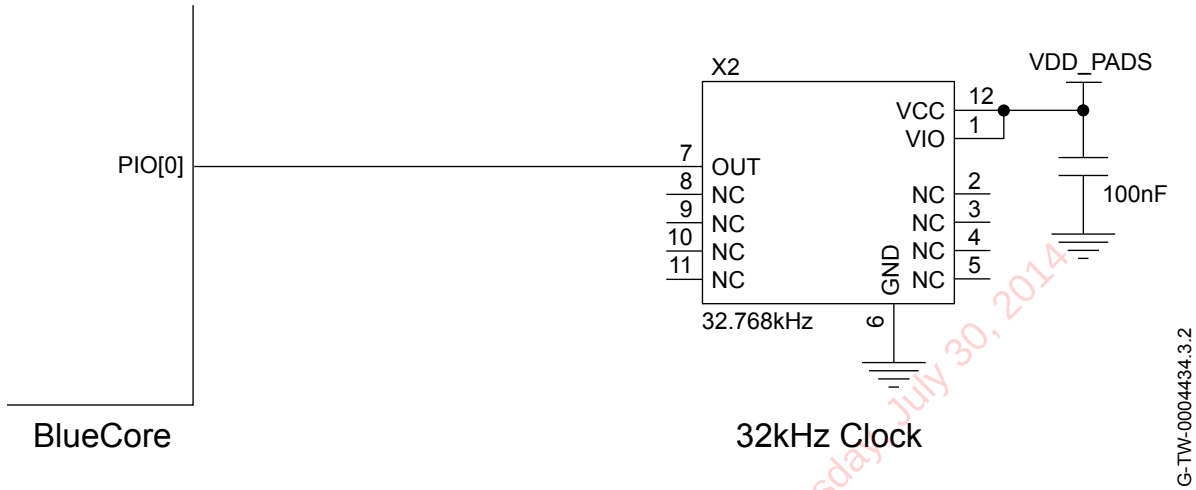

Figure 3.3: Example Sleep Clock Application Circuit

Section 11.3.7 lists the requirements for the sleep clock.

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4 Bluetooth Stack Microcontroller

CSR8811 uses a 16-bit RISC MCU for low power consumption and efficient use of memory.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

4.1 Programmable I/O Ports

See the *Device Terminal Functions* section for the list of supplies to the PIOs.

PIO lines are configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset and have additional individual bus keeper configuration.

See the CSR8811 software release note for the default function of PIO lines, as they are firmware build-specific.

4.2 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of WLAN coexistence schemes. There is support for:

- Channel skipping AFH
- Priority signalling
- Channel signalling
- Host passing of channel instructions

The CSR8811 supports the WLAN coexistence schemes:

- Unity 3e+
- Unity-3+
- Unity-3
- Unity-3e
- Unity+

For more information see *CSR8810 Hardware Design Guidelines (0.4mm WLCSP)* and *Bluetooth and IEEE 802.11 b/g Co-existence Solutions Overview*.

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5 Memory Interface and Management

5.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

5.2 System RAM

56KB of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

5.3 Internal ROM Memory (5Mb)

5Mb of Internal ROM memory is available on CSR8811. This memory is provided for system firmware, storing CSR8811 settings and program code.

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6 Host Interface

Use the host interface to:

- Configure CSR8811 to suit the target platform requirements
- Transfer data to and from other Bluetooth devices.

CSR8811 has a new automatic host transport selection scheme that does not require the use of PIOs.

6.1 UART Interface

This is a standard UART interface for communicating with other serial devices.

CSR8811 UART interface provides a simple mechanism for communicating with other serial devices using the RS-232 protocol.

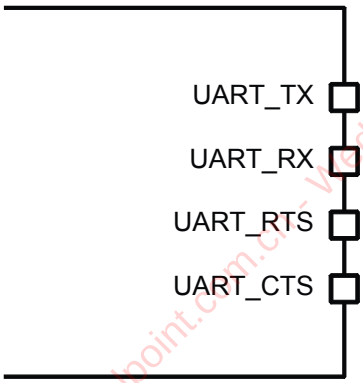

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Figure 6.1: Universal Asynchronous Receiver Transmitter (UART)

Figure 6.1 shows the 4 signals that implement the UART function. When CSR8811 is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, implement RS232 hardware flow control where both are active low indicators.

If UART_CTS and UART_RTS are not required for hardware flow control, they are reconfigurable as PIO.

UART configuration parameters, such as baud rate and packet format, are set using CSR8811 firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Table 6.1 shows the possible UART settings.

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Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 6.1: Possible UART Settings

The UART interface resets CSR8811 on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as Figure 6.2 shows. If t_{BRK} is longer than the value defined by the PSKEY_HOSTIO_UART_RESET_TIMEOUT, a reset occurs. This feature enables a host to initialise the system to a known state. Also, CSR8811 can issue a break character for waking the host.

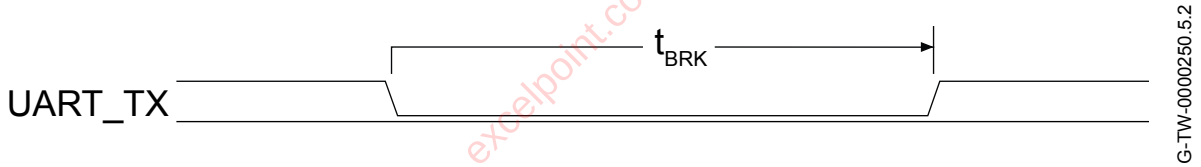

Figure 6.2: Break Signal

Refer to PSKEY_UART_BITRATE for more information about the baud rates and their values.

Generated baud rate is independent of selected incoming clock frequency.

6.1.1 UART Configuration While Reset is Active

The UART interface for CSR8811 is tri-state while the chip is being held in reset. This enables the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when CSR8811 reset is de-asserted and the firmware begins to run.

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7 Programming and Debug Interface

Important Note:

This interface can be used to configure and debug the CSR8811. For debug purposes CSR strongly recommends that the 4 debug and programming signals are brought out to either test points or a header.

CSR provides development and production tools to communicate over this interface from a PC, although a level translator circuit is often required. All are available from CSR.

CSR8811 uses a 16-bit data and 16-bit address programming and debug interface. Transactions occur when the internal processor is running or is stopped.

Data is written or read one word at a time, or the auto-increment feature is available for block access.

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8 Audio Interfaces

CSR8811 has a digital audio interface that is configurable as either a PCM or I²S port.

8.1 PCM Interface

The audio PCM interface on the CSR8811 supports:

- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data.
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
- Hardware on CSR8811 for sending data to and from a SCO connection.
- Up to 3 SCO connections on the PCM interface at any one time.
- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
  - Long Frame Sync
  - Short Frame Sync
  - GCI timing environments
- 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats.
- Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting PSKEY_PCM_CONFIG32.

8.1.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, CSR8811 generates PCM_CLK and PCM_SYNC.

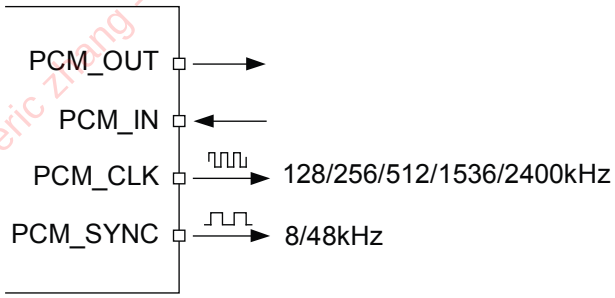

Figure 8.1: PCM Interface Master

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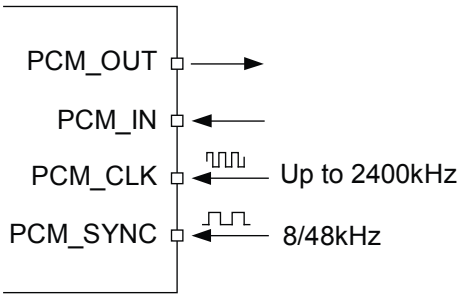

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Figure 8.2: PCM Interface Slave

8.1.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When CSR8811 is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8 bits long. When CSR8811 is configured as PCM Slave, PCM_SYNC is from 1 cycle PCM_CLK to half the PCM_SYNC rate.

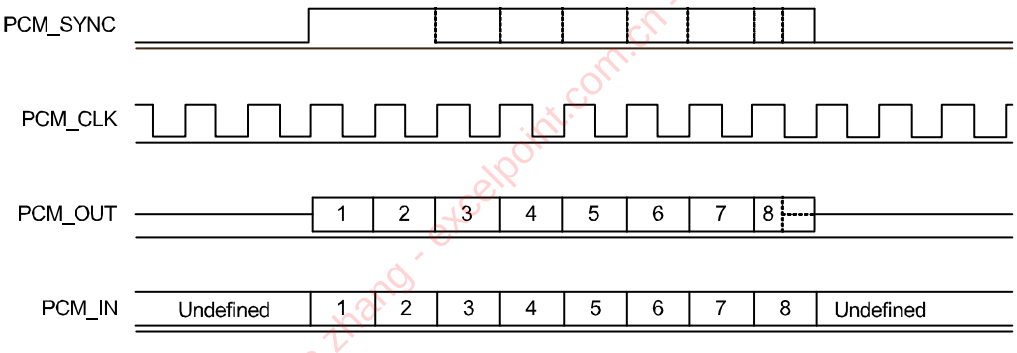

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Figure 8.3: Long Frame Sync (Shown with 8-bit Companded Sample)

CSR8811 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

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8.1.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always 1 clock cycle long.

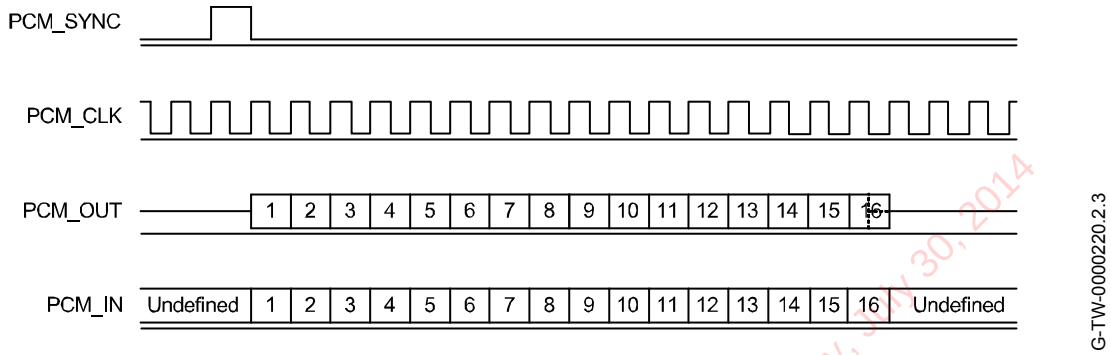

Figure 8.4: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, CSR8811 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable as high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

8.1.4 Multi-slot Operation

More than 1 SCO connection over the PCM interface is supported using multiple slots. Up to 3 SCO connections are carried over any of the first 4 slots.

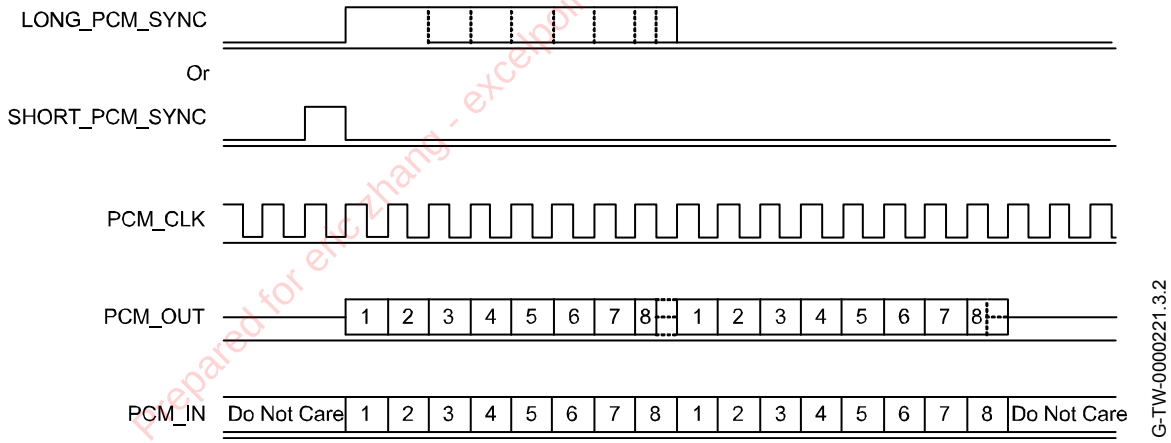

Figure 8.5: Multi-slot Operation with 2 Slots and 8-bit Companded Samples

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8.1.5 GCI Interface

CSR8811 is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The 2 64kbps B channels are accessed when this mode is configured.

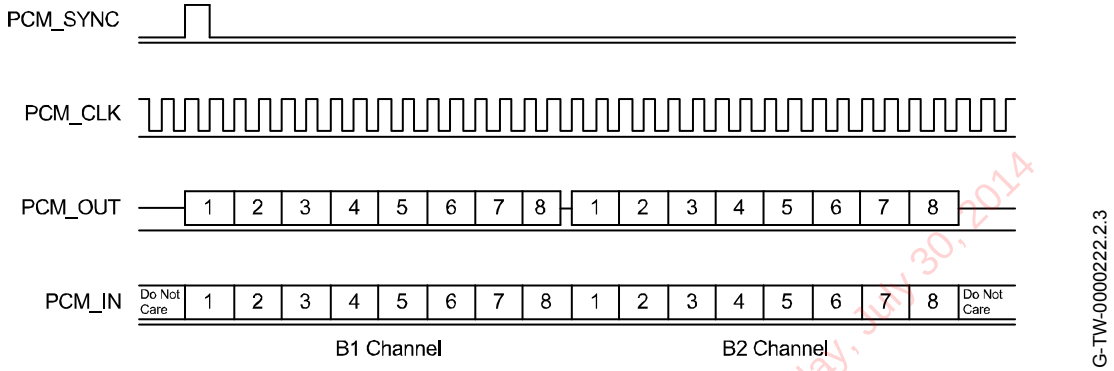

Figure 8.6: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz.

8.1.6 Slots and Sample Formats

CSR8811 receives and transmits on any selection of the first 4 slots following each sync pulse. Slot durations are either 8 or 16 clock cycles:

- 8 clock cycles for 8-bit sample formats.
- 16 clock cycles for 8-bit, 13-bit or 16-bit sample formats.

CSR8811 supports:

- 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats.
- A sample rate of 8ksps.
- Little or big endian bit order.
- For 16-bit slots, the 3 or 8 unused bits in each slot are filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some codecs.

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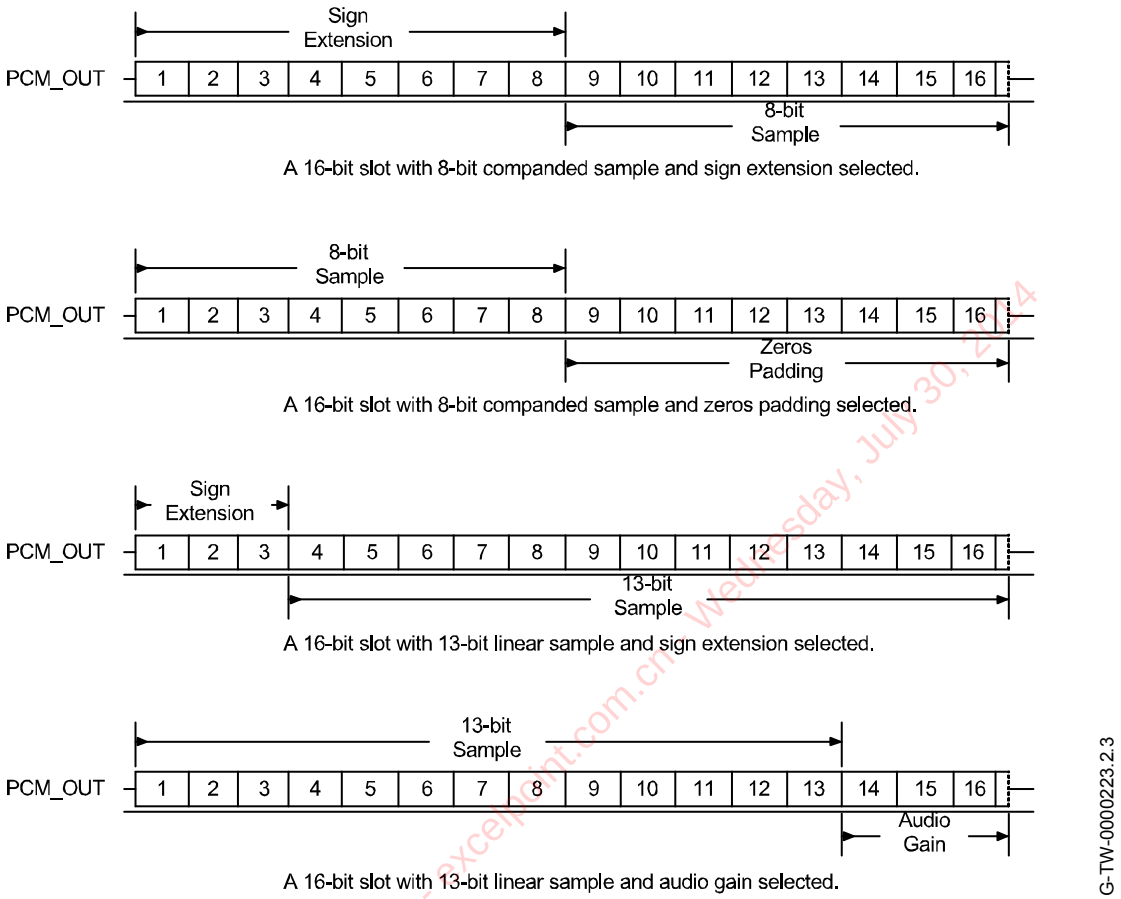

Figure 8.7: 16-bit Slot Length and Sample Formats

8.1.7 Additional Features

CSR8811 has a mute facility that forces PCM_OUT to be 0. In master mode, CSR8811 is compatible with some codecs which control power down by forcing PCM_SYNC to 0 while keeping PCM_CLK running.

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8.1.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Frequency selection is programmable.	-	128	-	kHz
				256		
				512		
		48MHz DDS generation. Frequency selection is programmable.	2.9	-	-	kHz
-	PCM_SYNC frequency for SCO connection		-	8	-	kHz
t_{mclkh} [(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} [(a)]	PCM_CLK low	4MHz DDS generation	730	-	-	ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk

Table 8.1: PCM Master Timing

[(a)] Assumes normal system clock operation. Figures vary during low-power modes, when system clock speeds are reduced.

Symbol	Parameter		Min	Typ	Max	Unit
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high	4MHz DDS generation	-	-	20	ns
		48MHz DDS generation	-	-	40.83	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (long frame sync only)	4MHz DDS generation	-	-	20	ns
		48MHz DDS generation	-	-	40.83	ns

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Symbol	Parameter		Min	Typ	Max	Unit
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low	4MHz DDS generation	-	-	20	ns
		48MHz DDS generation	-	-	40.83	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		20	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		0	-	-	ns

Table 8.2: PCM Master Mode Timing Parameters

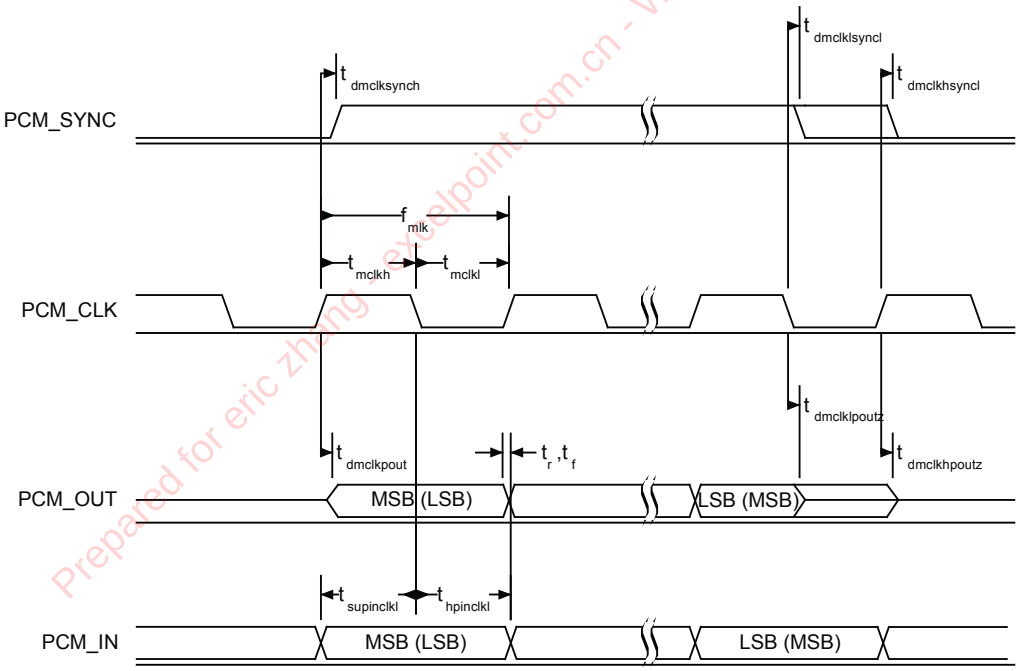

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Figure 8.8: PCM Master Timing Long Frame Sync

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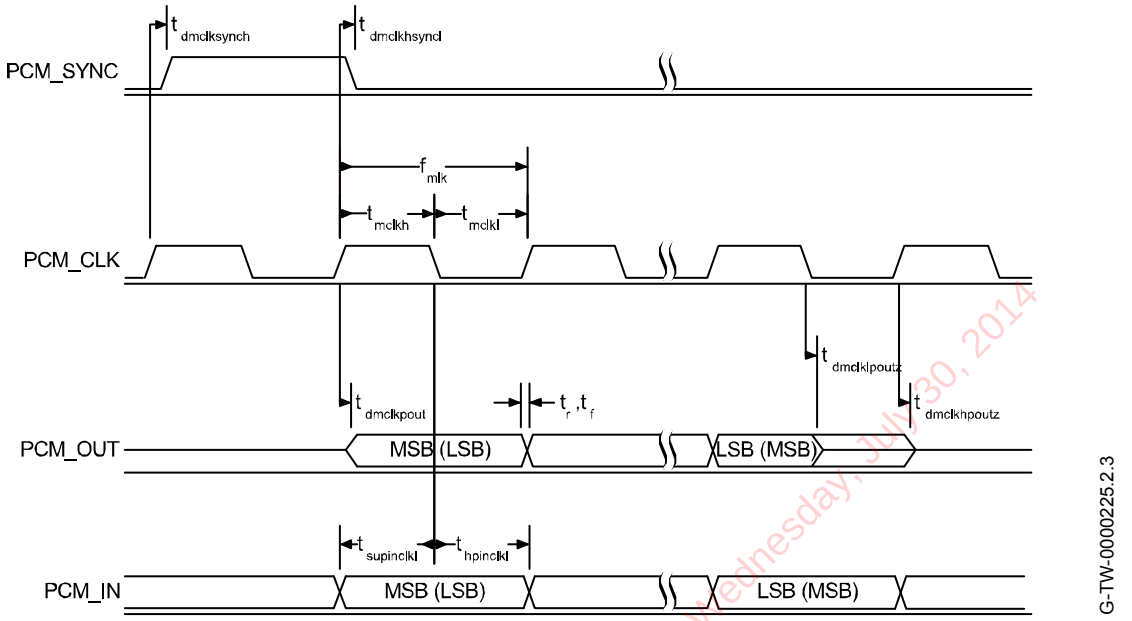

Figure 8.9: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns

Table 8.3: PCM Slave Timing

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Symbol	Parameter	Min	Typ	Max	Unit
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	2	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	20	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (long frame sync only)	-	-	15	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	15	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	20	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	2	-	-	ns

Table 8.4: PCM Slave Mode Timing Parameters

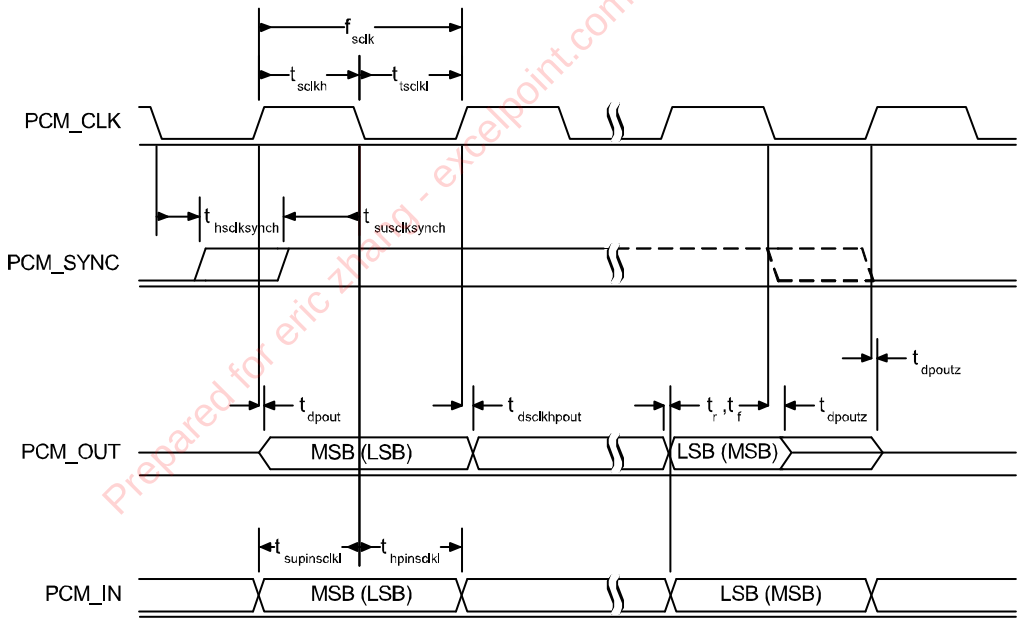

Figure 8.10: PCM Slave Timing Long Frame Sync

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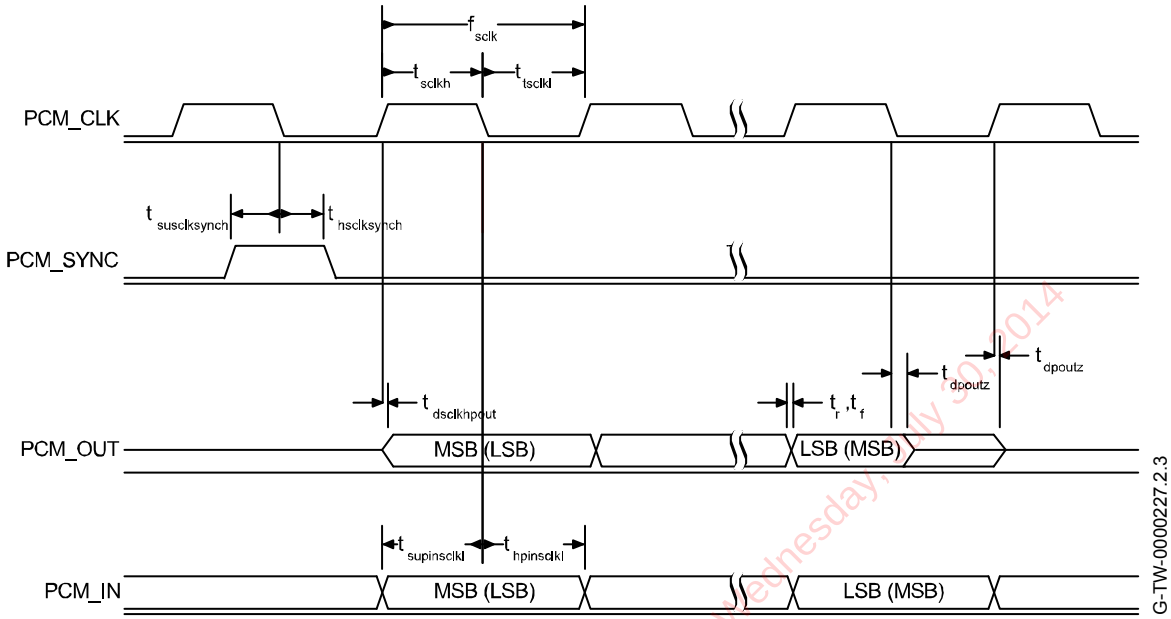

Figure 8.11: PCM Slave Timing Short Frame Sync

8.1.9 PCM_CLK and PCM_SYNC Generation

CSR8811 has 2 methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from CSR8811 internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating these signals by DDS from an internal 48MHz clock, which enables a greater range of frequencies to be generated with low jitter but consumes more power. To select this second method set bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC is either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 8.1 describes PCM_CLK frequency when generated from the internal 48MHz clock:

$$f = \frac{CNT_RATE}{CNT_LIMIT} \times 24MHz$$

Equation 8.1: PCM_CLK Frequency Generated Using the Internal 48MHz Clock

Set the frequency of PCM_SYNC relative to PCM_CLK using Equation 8.2:

$$f = \frac{PCM_CLK}{SYNC_LIMIT \times 8}$$

Equation 8.2: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to `0x08080177`.

8.1.10 PCM Configuration

Configure the PCM by using the PS Keys PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristate of PCM_OUT.

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Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 8.5: PSKEY_PCM_LOW_JITTER_CONFIG Description

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Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tristate PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tristate PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tristate PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC while keeping PCM_CLK running. Some codecs use this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode.
MUTE_EN	10	1 = force PCM_OUT to 0.

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Name	Bit Position	Description
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16-cycle slot duration or 8 (0b11) bit sample with 8-cycle slot duration.

Table 8.6: PSKEY_PCM_CONFIG32 Description

8.2 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 8.7 lists these alternative functions. Figure 8.12 shows the timing diagram.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 8.7: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Table 8.8 describes the values for the PS Key (PSKEY_DIGITAL_AUDIO_CONFIG) that is used to set-up the digital audio interface. For example, to configure an I²S interface with 16-bit SD data set PSKEY_DIGITAL_CONFIG to 0x0406.

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Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17 bit SD data is rounded down to 16 bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00F0	CONFIG_AUDIO_ATTEN	Attenuation in 6 dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16 bit, 01=20 bit, 10=24 bit, 11=Reserved. This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17 bit SD_IN data is rounded down to 16 bits. For 1 only the most significant 16 bits of data are received.
D[11]	0x0800	CONFIG_AUDIO_SLOT_SEL	0: Select slots 0 and 1 for audio data. 1: Select slots 2 and 3 for audio data.
D[12]	0x1000	CONFIG_SYNC_MULT_ENB	0: Enable *8 multiplier for sync limit multiplier. 1: Disable multiplier.
D[13]	0x2000	CONFIG_TX_START_RISING	Start I^2S sampling during low wclk phase (0) or high wclk phase (1)
D[14]	0x4000	CONFIG_RX_START_RISING	Start I^2S sampling during low wclk phase (0) or high wclk phase (1)

Table 8.8: PSKEY_DIGITAL_AUDIO_CONFIG

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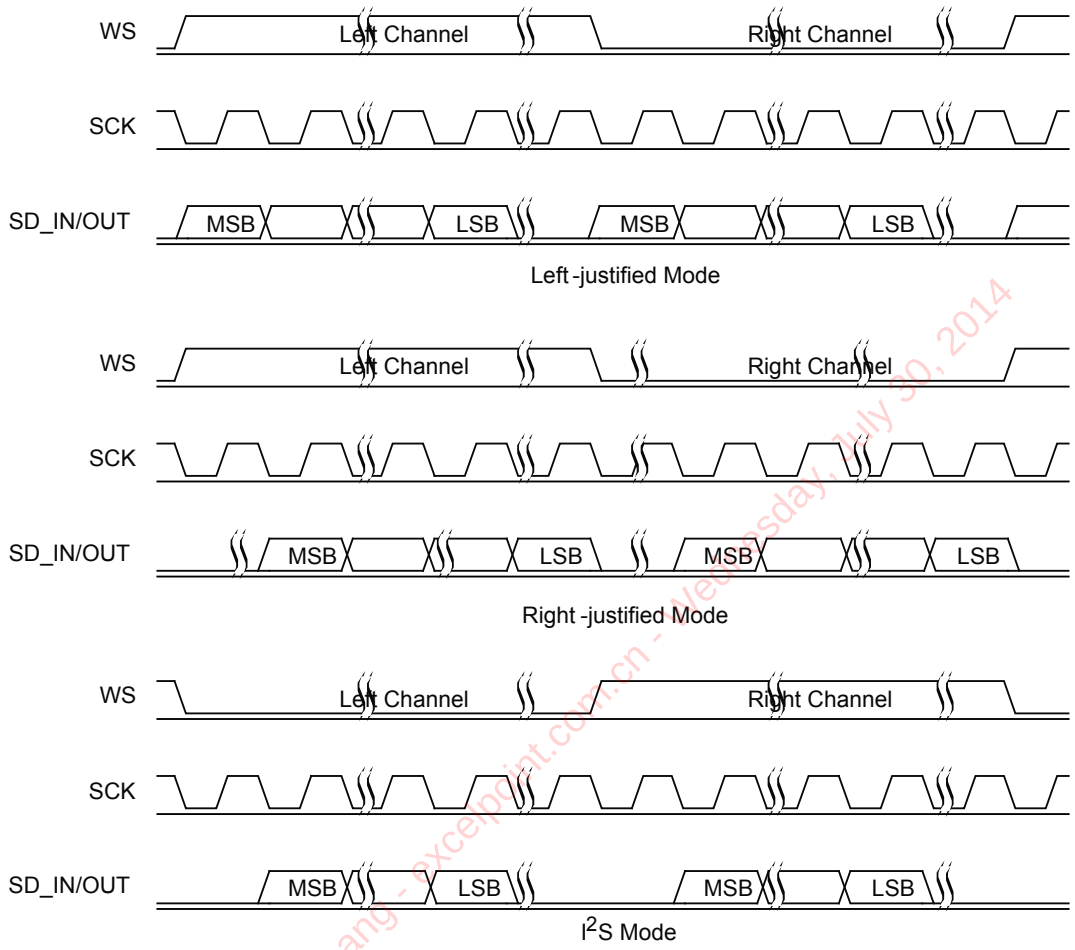

Figure 8.12: Digital Audio Interface Modes

The internal representation of audio samples within CSR8811 is 16-bit and data on SD_OUT is limited to 16-bit per channel.

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Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns

Table 8.9: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{ssu}	WS valid to SCK high set-up time	20	-	-	ns
t_{sh}	SCK high to WS invalid hold time	2.5	-	-	ns
t_{opd}	SCK low to SD_OUT valid delay time	-	-	20	ns
t_{isu}	SD_IN valid to SCK high set-up time	20	-	-	ns
t_{ih}	SCK high to SD_IN invalid hold time	2.5	-	-	ns

Table 8.10: I²S Slave Mode Timing

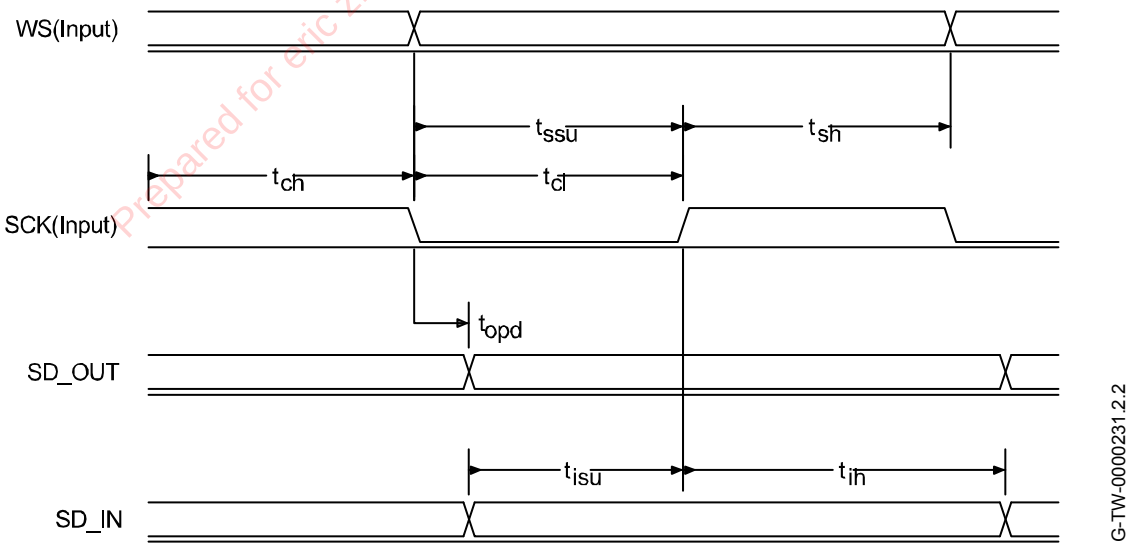

Figure 8.13: Digital Audio Interface Slave Timing

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Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz

Table 8.11: Digital Audio Interface Master Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{spd}	SCK low to WS valid delay time	-	-	39.27	ns
t_{opd}	SCK low to SD_OUT valid delay time	-	-	18.44	ns
t_{isu}	SD_IN valid to SCK high set-up time	18.44	-	-	ns
t_{ih}	SCK high to SD_IN invalid hold time	0	-	-	ns

Table 8.12: I²S Master Mode Timing Parameters, WS and SCK as Outputs

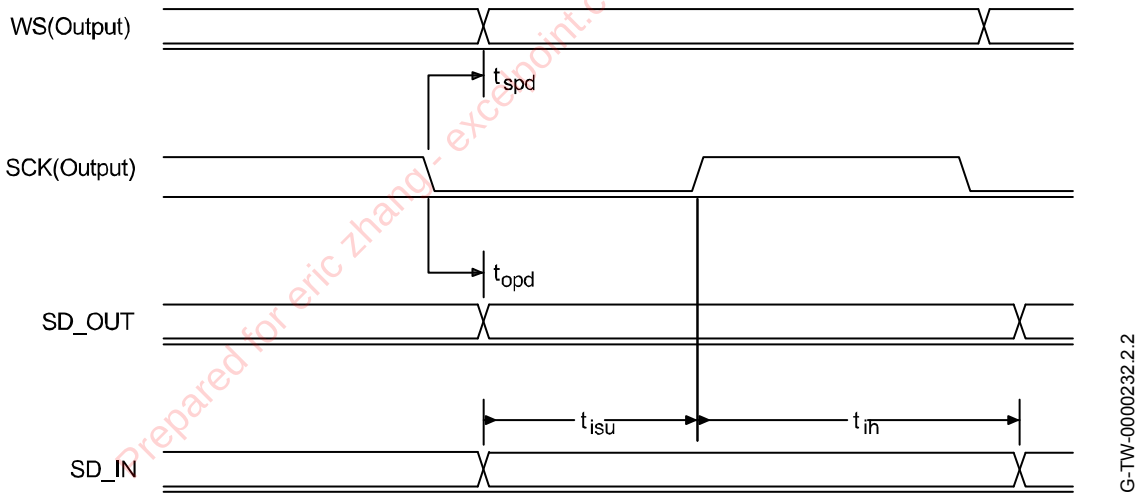

Figure 8.14: Digital Audio Interface Master Timing

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9 Power Control and Regulation

See the Example Application Schematic for the regulator configuration.

The high-voltage regulator generates the main 1.8V rail from the battery supply. This then supplies 3 lower voltage linear regulators:

- A programmable low-voltage regulator to supply the 0.9V to 1.25V digital supply, VDD_DIG
- A low-voltage regulator to supply the 1.35V VDD_RADIO rail
- An always-on regulator to supply 1.35V to auxiliary and reference circuitry, VDD_AUX

9.1 High-voltage Linear Regulator

The on-chip high-voltage regulator is designed to power the main 1.8V rail from a typical Lithium Ion / Lithium Polymer cell. The input voltage should be 2.3V to 4.8V. The maximum current output from this regulator is 100mA.

A minimum 1.5µF capacitor must be connected to the VREG_OUT_HV pin. Low ESR capacitors such as multilayer ceramic types should be used.

The High Voltage internal regulator can be bypassed and an external supply used. The transient response of any external regulator used should be 5µs or less. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels.

When this regulator is not used the VREG_IN_HV pin must be left unconnected or tied to VREG_OUT_HV. The VREG_EN_RST# pin remains active controlling the reset function if the HV linear regulator is not used so the pin must be driven high to take the device out of reset.

CSR recommends that the supplies are all powered at the same time. The order of powering the supplies relative to the other I/O supply (VDD_PADS) is not important. If the I/O supply is powered before the supplies all digital I/Os will have a weak pull-down irrespective of the reset state.

9.1.1 Regulator Control

The regulator is enabled by taking the VREG_EN_RST# pin above 1V. The regulator can also be controlled by the software.

The VREG_EN_RST# is also connected internally to the reset function, and is powered from the VDD_PADS supply, so voltages above VDD_PADS must not be applied to this pin. The VREG_EN_RST# pin is pulled down internally.

9.2 Low-voltage VDD_DIG Linear Regulator

The on-chip low-voltage VDD_DIG regulator powers the CSR8811 WLCSP digital circuits.

A minimum 1.5µF capacitor must be connected to the VDD_DIG pin. Low ESR capacitors such as multilayer ceramic types should be used.

The regulator enable and output voltage is controlled by the firmware.

9.3 Low-voltage VDD_ANA Linear Regulator

The on-chip low-voltage VDD_ANA regulator powers the internal radio circuits of the CSR8811.

A minimum 1.5µF capacitor must be connected to the VDD_ANA pin. Low ESR capacitors such as multilayer ceramic types should be used.

The regulator is controlled by the firmware. The regulator is disabled when the device is in deep-sleep mode or in reset.

9.4 Low-voltage VDD_AUX Linear Regulator

The on-board low-voltage VDD_AUX regulator powers the CSR8811 1.35V VDD_AUX supply.

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The output of this regulator must be decoupled externally using a minimum 470nF capacitor connected to the VDD_AUX pin. Low ESR capacitors such as multilayer ceramic types should be used.

The regulator is controlled by the firmware.

9.5 Reset

CSR8811 the reset function is internally tied to the VREG_EN_RST# pin. The CSR8811 may be reset from several sources:

- VREG_EN_RST# pin
- Power-on reset
- A UART break character
- Via a software-configured watchdog timer

The VREG_EN_RST# pin is an active low reset. To ensure a full reset the reset signal should be asserted for a period greater than 5ms.

A warm reset function is also available under software control. After a warm reset the RAM data remains available.

9.6 Power-on Sequencing

CSR8811 does not have any strict relative timing requirements for clock and power supply sequencing during reset or power-on. Follow this sequence of operation to ensure that the initial cold boot is completed successfully:

1. All external power supplies should be stable and the sleep clock should be present.
2. VREG_EN_RST# should be driven high.
3. The external reference clock must be present and stable a variable number of milliseconds after the CSR8811 asserts its clock request signal. The default value is 5ms. You can modify this using the persistent store configuration key PSKEY_CLOCK_STARTUP_DELAY.

It is then possible to establish host communications with the CSR8811 in order to set further configuration values. When you have set configuration values, perform a warm reset so that they take effect and normal radio operation can begin.

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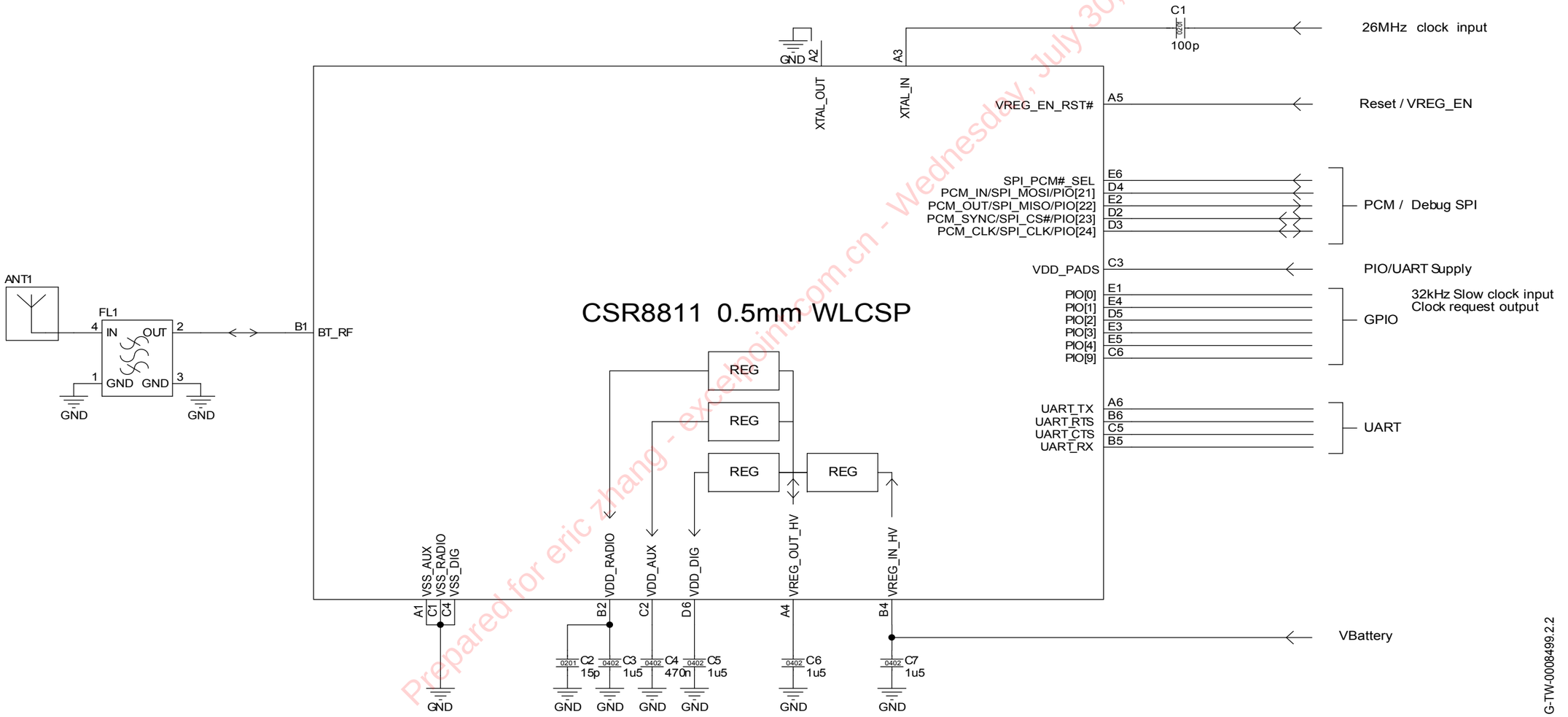
10 Example Application Schematic



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11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Rating	Min	Max
Storage temperature	-40°C	85°C
VBAT operation[a]	2.3V	4.8V
Low-voltage operation (bypassing high-voltage linear regulator)	1.7V	2.0V
I/O supply voltage	-0.4V	3.6V
Other terminal voltages	VSS - 0.4V	VDD + 0.4V

[a] Short-term operation up to a maximum of 10% of product lifetime is permissible without damage, but output regulation and other specifications are not gauranteed in excess of 4.8V.

11.2 Recommended Operating Conditions

Operating Condition	Min	Max
Operating temperature range	-30°C	85°C
VBAT operation	2.3V	4.8V
Low Voltage Operation (Bypassing high-voltage linear regulator)	1.75V	1.95V
I/O supply voltage (VDD_PADS)	1.2V	3.6V
VREG_EN_RST#	VSS_PADS	VDD_PADS

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11.3 Input/Output Terminal Characteristics

11.3.1 High-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	2.3	3.3	4.8	V
Output voltage	1.75	1.85	1.95	V
Temperature coefficient	-200	-	200	ppm/°C
Output noise (frequency range 100Hz to 100kHz)	-	-	0.4	mV rms
Settling time (settling to within 10% of final value)	-	-	5	µs
Output current	-	-	100	mA

11.3.2 Low-voltage VDD_DIG Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Output voltage	0.90	-	1.25	V
Output current	-	-	30	mA

11.3.3 Low-voltage VDD_AUX Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Output voltage	1.30	1.35	1.40	V
Output current	-	-	5	mA

11.3.4 Low-voltage VDD_RADIO Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Output voltage	1.30	1.35	1.45	V
Output current	-	-	60	mA

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11.3.5 Digital

Digital Terminals	Min	Typ	Max	Unit
Input Voltage				
V_{IL} input logic level low	-0.4	-	0.4	V
V_{IH} input logic level high	0.7 x VDD	-	VDD + 0.4	V
Output Voltage				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75 X VDD	-	-	V
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	µA
Strong pull-down	10	40	150	µA
Weak pull-up	-5	-1.0	-0.33	µA
Weak pull-down	0.33	1.0	5.0	µA
C_I input capacitance	1.0	-	5.0	pF

11.3.6 Clock

Clock Source	Min	Typ	Max	Unit
External Clock				
SYS_CLK input resistance	30	-	-	kΩ
SYS_CLK input capacitance	-	-	4	pF

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11.3.7 Sleep Clock

Sleep Clock			Min	Typ	Max	Units
Frequency[a]			30	32.768	35	kHz
Frequency tolerance[b]			-	-	250	±ppm
Duty cycle			5:95	50:50	95:5	%
Jitter Integrated rms jitter 10Hz to 20kHz		f_{ref} = 32.768kHz	-	-	20	ns rms
Phase noise	f_{ref} = 32.768kHz	1kHz offset	-	-	-100	dBc/ Hz
		10kHz offset	-	-	-120	
Digital input, values as Section 11.3.5						

Table 11.1: Sleep Clock Specification

[a] Stability is most important as frequency is calibrated against the system clock.

[b] The frequency of the slow clock is periodically calibrated against the system clock, as a result the rate of change of the frequency is more important than the maximum deviation.

11.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 11.2 shows the ESD handling maximum ratings.

Condition	Note	Max Rating
Human Body Model Contact Discharge per JEDEC EIA/JESD22-A114	ESD_HAND_HBM	2000V (all pins)
Machine Model Contact Discharge per JEDEC EIA/ JESD22-A115	ESD_HAND_MM	200V (except XTAL_IN = 190V)
Charged Device Model Contact Discharge per JEDEC EIA/JESD22-C101	ESD_HAND_CDM	500V (all pins)

Table 11.2: ESD Handling Ratings

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12 Software

CSR8811:

- Is supplied with on-chip Bluetooth v4.0 specification qualified HCI stack firmware
- Can be shipped with CSR's off-chip software package, CSR Synergy, that runs on the host.

12.1 On-chip Software

12.1.1 BlueCore HCI Stack

Figure 12.1 shows an example implementation. An internal processor runs the Bluetooth stack up to the HCI. The host processor must provide all upper layers including the application.

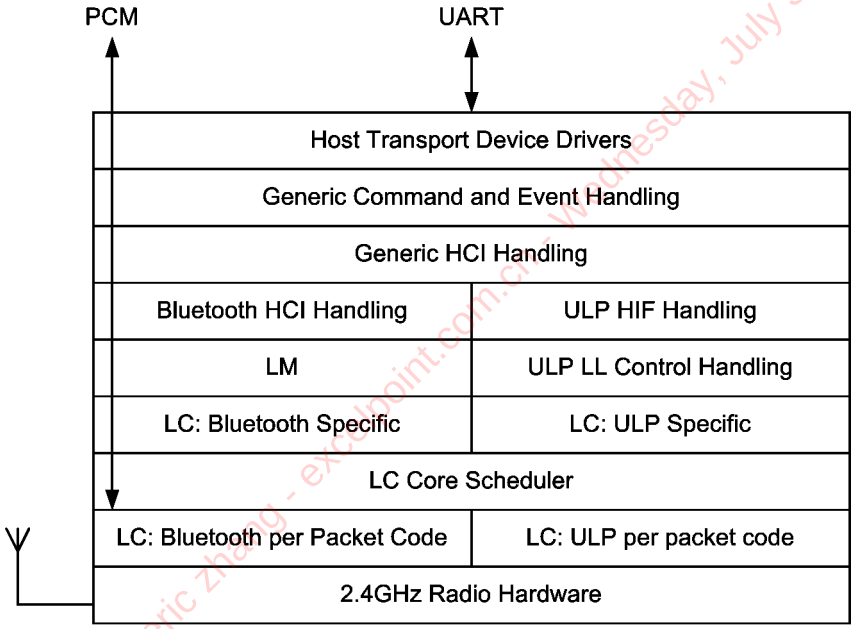

Figure 12.1: Example Firmware Architecture

12.1.1.1 Latest Features of the HCI Stack

CSR8811 is qualified to Bluetooth v4.0 specification. This introduces the following features:

- Generic Alternate MAC/PHY (AMP)
- Generic Test Methodology for AMP
- 802.11 Protocol Adaptation Layer
- Enhanced Power Control
- Enhanced USB and SDIO HCI Transports
- HCI Read Encryption Key Size command
- Unicast Connectionless Data

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12.2 Off-chip Software

12.2.1 CSR Synergy

CSR Synergy is a product from CSR that aids software development. It integrates all Host software for the wireless technologies into one package and can support Bluetooth, Bluetooth low energy, Wi-Fi, eGPS, FM TX/RX, NFC and UWB as Figure 12.2 shows.

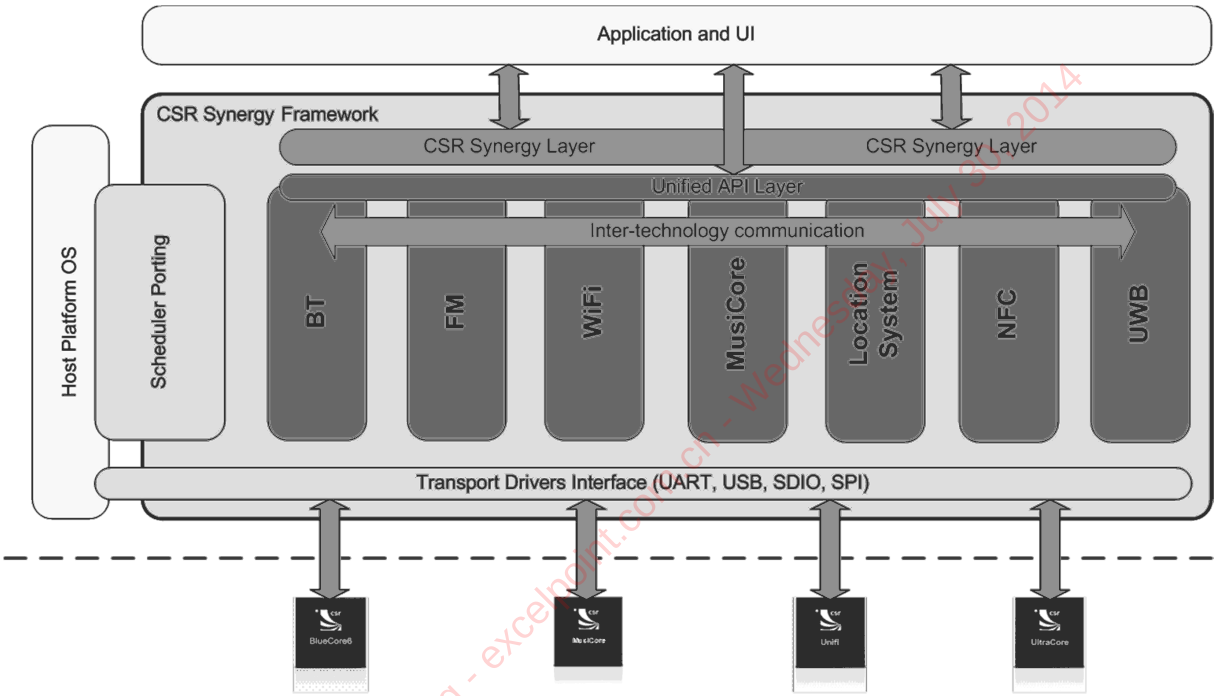

Figure 12.2: CSR Synergy Framework

Each technology in CSR Synergy is released as an individual component running in the common environment, the CSR Synergy Framework. This framework operates as a virtual OS for the components. Technologies can be removed and added easily to fit the hardware configuration, leaving no overhead in terms of MIPS and memory usage when a technology is not used.

See http://www.csr.com/products/19/csr-synergy for more information.

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13 CSR Green Semiconductor Products and RoHS Compliance

CSR confirms that CSR Green semiconductor products comply with the following regulatory requirements:

- Restriction on Hazardous Substances directive guidelines in the EU RoHS Directive 2002/95/EC and RoHS recast 2011/65/EU[1] from 3 Jan 2013.
- EU REACH, Regulation (EC) No 1907/2006[1]:
  - List of substances subject to authorisation (Annex XIV)
  - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations and articles (Annex XVII). This Annex now includes requirements that were contained within EU Directive, 76/769/EEC. There are many substance restrictions within this Annex, including, but not limited to, the control of use of Perfluorooctane sulfonates (PFOS).
  - When requested by customers, notification of substances identified on the Candidate List as Substances of Very High Concern (SVHC)[1].
- POP regulation (EC) No 850/2004[1]
- EU Packaging and Packaging Waste, Directive 94/62/EC[1]
- Montreal Protocol on substances that deplete the ozone layer.
- Conflict minerals, Section 1502, Dodd-Frank Wall Street Reform and Consumer Protection act, which affects columbite-tantalite (coltan / tantalum), cassiterite (tin), gold, wolframite (tungsten) or their derivatives. CSR is a fabless semiconductor company: all manufacturing is performed by key suppliers. CSR have mandated that the suppliers shall not use materials that are sourced from "conflict zone mines" but understand that this requires accurate data from the EICC programme. CSR shall provide a complete EICC / GeSI template upon request.

CSR has defined the "CSR Green" standard based on current regulatory and customer requirements incuding free from bromine, chlorine and antimony trioxide.

Products and shipment packaging are marked and labelled with applicable environmental marking symbols in accordance with relevant regulatory requirements.

This identifies the main environmental compliance regulatory restrictions CSR specify. For more information on the full "CSR Green" standard, contact product.compliance@csr.com.

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CSR8811 A08 0.5mm pitch WLCSP Data Sheet

[1] Including applicable ammendments to EU law which are published in the EU Official Journal, or SVHC Candidate List updates published by the European Chemicals Agency (ECHA).

14 Ordering Information

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART	WLCSP 28-ball Green	2.57 x 3.21 x 0.6mm, 0.5mm pitch	Tape and reel	CSR8811A08-ICXR-R

Note:

At **Production** status minimum order quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

To contact a CSR representative, send e-mail to sales@csr.com or go to www.csr.com/contacts.htm.

14.1 Chip Marking

Figure 14.1 shows the product marking for CSR8811A08-ICXR-R 28-ball WLCSP 2.57 x 3.21 x 0.6mm.

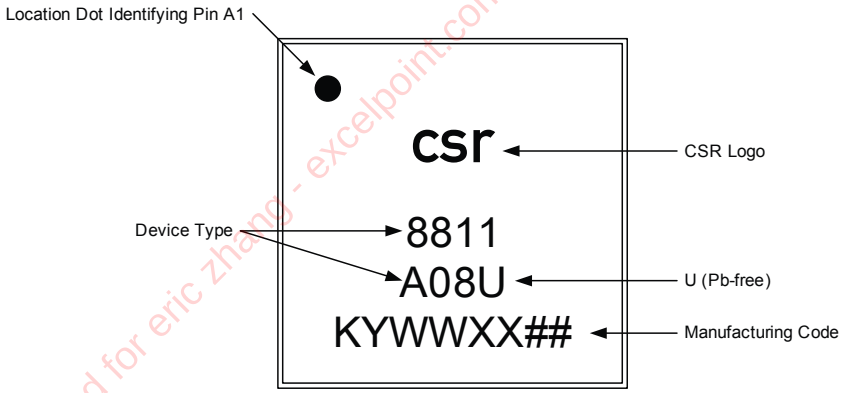

Figure 14.1: CSR8811A08 Chip Marking

4th line is the manufacturing code:

- Assembly subcontractor code: K
- Date code: YWWXX

  Note:

  Y is year of assembly

  WW is week of assembly

  XX is lot designator
- ## is wafer ID

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G-TW-0010189.1.2

15 Tape and Reel Information

The tape and reel are in accordance with EIA-763-2. For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

15.1 Tape Orientation

Figure 15.1 shows the general orientation of the CSR8811 package in the carrier tape.

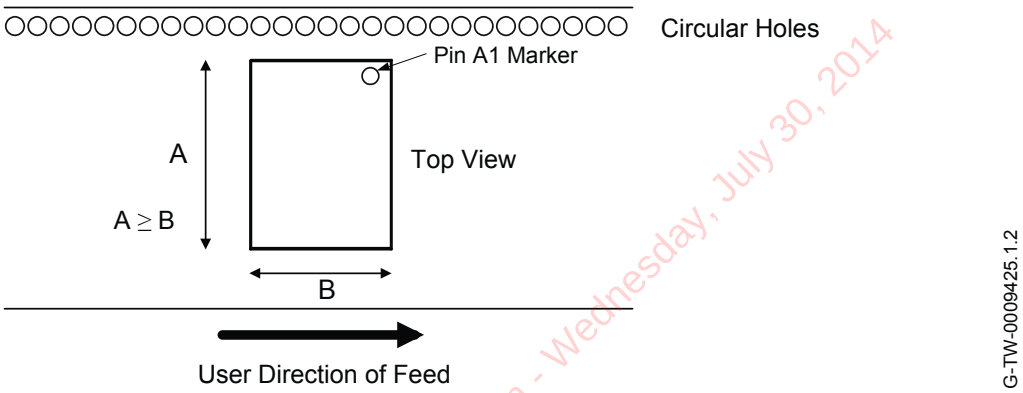

Figure 15.1: Tape Orientation

15.2 Tape Dimensions

Figure 15.2 shows the dimensions of the tape for the CSR8811.

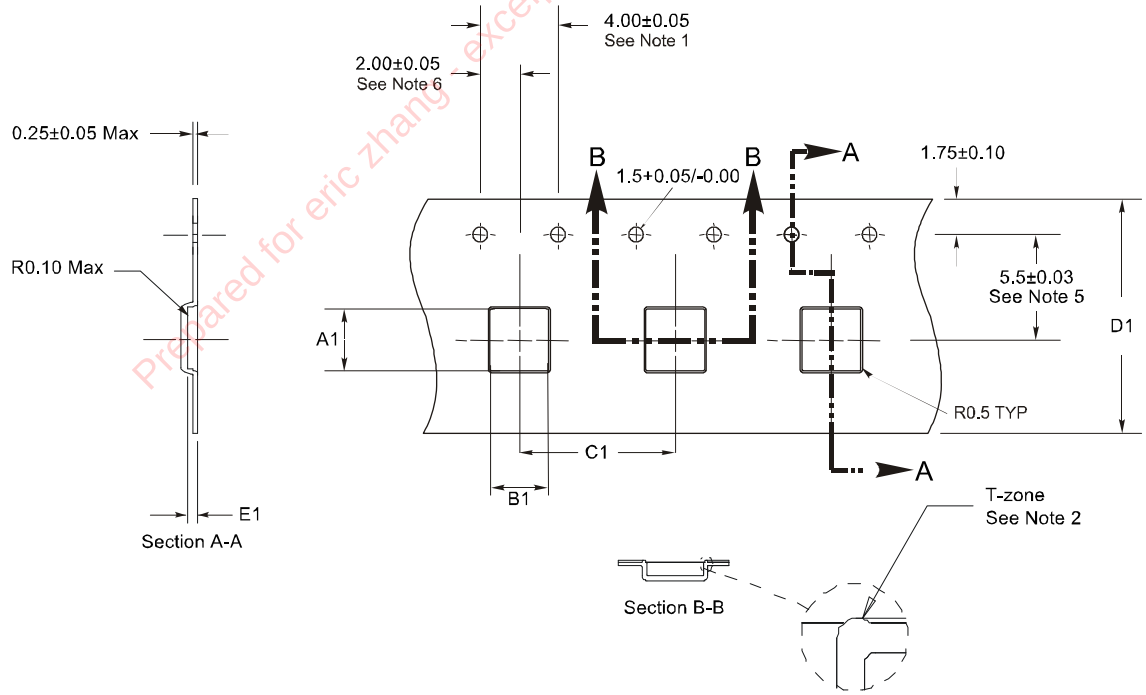

Figure 15.2: Tape Dimensions

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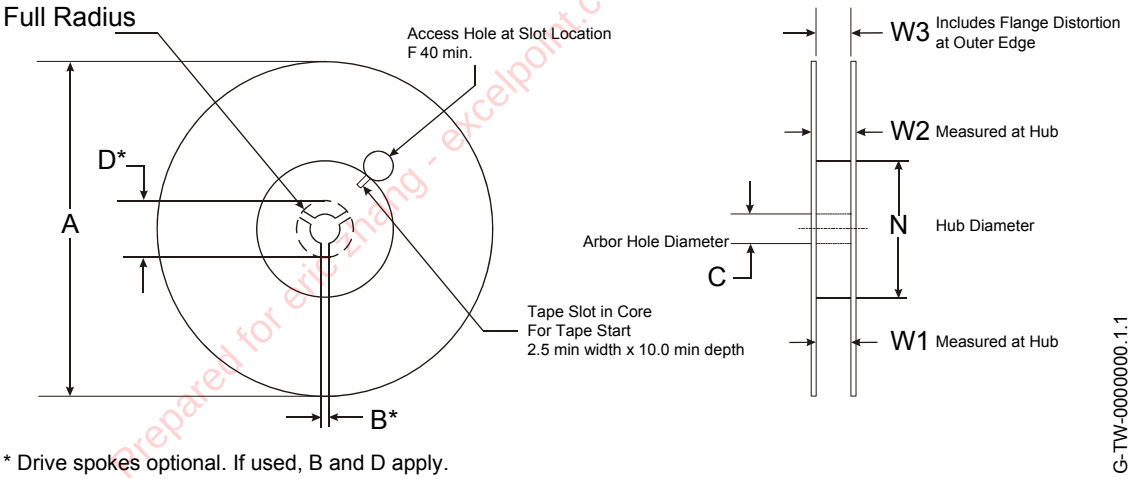
Package	A1	B1	C1	D1	E1	Unit	Notes
CSR8811 28-ball	3.7 ± 0.05	3.35 ± 0.05	8 ± 0.05	12 ± 0.10	0.82 ± 0.05	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.1mm. 2. Carrier camber in compliance with EIA 763. 3. A1 and B1 measured on a plane 0.3mm above the bottom of the pocket. 4. E1 measured from a plane on the inside bottom of the pocket to top surface of carrier. 5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole. 6. Surface resistivity = 1.0 x 10^5 and < 1.0 x $10^{12}\Omega$/sq.

Table 15.1: Tape Dimensions

15.3 Reel Information

Reel Dimensions

All dimensions in mm



* Drive spokes optional. If used, B and D apply.

Figure 15.3: Reel Dimensions

Package Type	Tape Width	A Max	B	C	D Min	N Min	W1	W2 Max	W3		Units
									Min	Max	
2.57 x 3.21 x 0.6mm WLCSP	12	330	1.5	13.0 (0.5/-0.2)	20.2	50	12.4 (2.0/-0.0)	18.4	11.9	15.4	mm

Table 15.2: Reel Dimensions

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15.4 Moisture Sensitivity Level

CSR8811 is qualified to moisture sensitivity level MSL1 in accordance with JEDEC J-STD-020.

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16 Document References

Document	Reference, Date
BCCMD Commands	CS-101482-SP
CSR8810 Hardware Design Guidelines (0.4mm WLCSP)	CS-210416-DD
Environmental Compliance Statement for CSR Green Semiconductor Products	CB-001036-ST, 27 September 2007
HQ Commands	CS-101677-SP
IC Packing and Labelling Specification	CS-112584-SP
Specification of the Bluetooth System	v4.0, 6 July 2010
Typical Solder Reflow Profile for Lead-free Devices	CS-116434-AN

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Terms and Definitions

Term	Definition
3G	3rd Generation of mobile communications technology
802.11™	WLAN specification defined by a working group within the IEEE
µ-law	Audio companding standard (G.711)
A-law	Audio companding standard (G.711)
A2DP	Advanced Audio Distribution Profile
AC	Alternating Current
ADC	Analogue to Digital Converter
AES	Advanced Encryption Standard
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AMP	Alternate MAC/PHY
balun	balanced/unbalanced interface or device that changes a balanced output to an unbalanced input or vice versa
BIST	Built-In Self-Test
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
CDMA	Code Division Multiple Access
codec	Coder decoder
CRC	Cyclic Redundancy Check
CSR	Cambridge Silicon Radio
CVSD	Continuous Variable Slope Delta Modulation
DC	Direct Current
DDS	Direct Digital Synthesis
EBU	European Broadcasting Union
EDR	Enhanced Data Rate
eGPS®	enhanced GPS
EIA	Electronic Industries Alliance
eSCO	Extended SCO
ESD	Electrostatic Discharge

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Term	Definition
FM	Frequency Modulation
GCI	General Circuit Interface
GSM	Global System for Mobile communications
HCI	Host Controller Interface
HFP	Hands-Free Profile
I²S	Inter-Integrated Circuit Sound
i.e.	*Id est*, that is
I/O	Input/Output
IC	Integrated Circuit
IEEE	Institute of Electronic and Electrical Engineers
IF	Intermediate Frequency
IQ	In-Phase and Quadrature
ISDN	Integrated Services Digital Network
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
Kb	Kilobit
KB	Kilobyte
LC	An inductor (L) and capacitor (C) network
LNA	Low Noise Amplifier
LSB	Least Significant Bit (or Byte)
MAC	Medium Access Control
Mb	Megabit
MB	Megabyte
MCU	MicroController Unit
MIPS	Million Instructions Per Second
MMU	Memory Management Unit
MSB	Most Significant Bit (or Byte)
NFC	Near Field Communication
NSMD	Non Solder Mask Defined
OS	Operating System
PA	Power Amplifier

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Term	Definition
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PHY	Physical (layer)
PIO	Programmable Input/Output, also known as general purpose I/O
pk-pk	peak-to-peak
plc	Public Limited Company
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
RS-232	Recommended Standard-232, a TIA/EIA standard for serial transmission between computers and peripheral devices (modem, mouse, etc.)
RSSI	Received Signal Strength Indication
RX	Receive or Receiver
SBC	Sub-Band Coding
SCO	Synchronous Connection-Oriented
SDIO	Secure Digital Input/Output
SIG	(Bluetooth) Special Interest Group
S/PDIF	Sony/Philips Digital InterFace (also IEC 958 type II, part of IEC-60958). An interface designed to transfer stereo digital audio signals between various devices and stereo components with minimal loss.
TCXO	Temperature Compensated crystal Oscillator
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UniFi®	Group term for CSR's range of ICs designed to meet IEEE 802.11 standards
Unity	Collective name for CSR's Bluetooth/Wi-Fi coexistence schemes

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Term	Definition
Unity+	CSR's advanced coexistence scheme. Extra signalling wire used in conjunction with Unity-3 or Unity-3e for improved coexistence with periodic Bluetooth activity.
Unity-3	De facto industry standard 3-wire coexistence signalling scheme
USB	Universal Serial Bus
UWB	Ultra-wideband
VCO	Voltage Controlled Oscillator
W-CDMA	Wideband Code Division Multiple Access
Wi-Fi®	Wireless Fidelity (IEEE 802.11 wireless networking)
WLAN	Wireless Local Area Network
WLCSP	Wafer Level Chip Scale Package

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