Main Specifications

■ General Specifications (Power Supplies and CPU Units)

Item	CQM1-PA203	CQM1-PA206	CQM1-PA216	CQM1-PD026
Supply voltage	100 to 240 V AC, 50/60 Hz		100 or 230 V AC (selectable), 50/60 Hz	24 V DC
Operating voltage range	85 to 264 V AC		85 to 132 V AC or 170 to 264 V AC	20 to 28 V DC
Operating frequency range	47 to 63 Hz			---
Power consumption	60 VA max.	120 VA max.		50 W max.
Inrush current	30 A max.			
Output capacity	5 V DC: 3.6 A (18 W)	5 V DC: 6 A 24 V DC: 0.5 A (30 W total)		5 V DC: 6 A (30 W)
Insulation resistance	20 MΩ min. (at 500 V DC) between AC external terminals and GR terminals			
Dielectric strength	2,300 V AC 50/60 Hz for 1 min between AC external and GR terminals, leakage current: 10 mA max. 1,000 V AC 50/60 Hz for 1 min between DC external and GR terminals, leakage current: 20 mA max.			
Noise immunity	Conforms to IEC61000-4-4, 2 kV (power lines)			
Vibration resistance	10 to 57 Hz with an amplitude of 0.075 mm, and 57 to 150 Hz with an acceleration of 9.8 m/s^2 in the X, Y, and Z directions for 80 minutes each (i.e., swept for 8 minutes, 10 times).			
Shock resistance	147 m/s^2 (118 m/s^2 for Contact Output Units) 3 times each in X, Y, and Z directions			
Ambient temperature	Operating: 0 to 55 °C Storage: –20 to 75 °C (except battery)			
Ambient operating humidity	10% to 90% (no condensation)			
Operating environment	No corrosive gas			
Ground	Less than 100 Ω			
Construction	Panel mounted			
Weight	5 kg max.			
Internal current consumption	CQM1H-CPU11: 820 mA max. at 5 V DC CQM1H-CPU21/51/61: 840 mA max. at 5 V DC			
Dimensions (without cables)	CQM1H-CPU11/21: 187 to 571 × 110 × 107 mm (W×H×D) CQM1H-CPU51/61: 187 to 603 × 110 × 107 mm (W×H×D)			
Accessories	RS-232C connector (one XM2A-0901 Plug and one XM2S-0911-E Hood) (except CQM1H-CPU11) CPM2A-BAT01 Battery Set (installed in CPU Unit when shipped)			

■ CPU Unit Specifications

Characteristics

Item		Specifications
Control method		Stored program method
I/O control method		Cyclic scan and direct output/immediate interrupt processing
Programming language		Ladder-diagram programming
I/O capacity		CQM1H-CPU11/21: 256 CQM1H-CPU51/61: 512
Program capacity		CQM1H-CPU11/21 : 3.2 Kwords CQM1H-CPU51 : 7.2 Kwords CQM1H-CPU61 : 15.2 Kwords
Data memory capacity		CQM1H-CPU11/21 : 3 Kwords CQM1H-CPU51 : 6 Kwords CQM1H-CPU61 : 12 Kwords (DM: 6 Kwords; EM: 6 Kwords)
Instruction length		1 step per instruction, 1 to 4 words per instruction
Number of instructions		162 (14 basic, 148 special instructions)
Instruction execution times		Basic instructions: 0.375 to 1.125 μs Special instructions: 17.7 μs (MOV instruction)
Overseeing time		0.70 ms
Mounting structure		No Backplane (Units are joined horizontally using connectors)
Mounting		DIN Track mounting (screw mounting not possible)
CPU Unit built-in DC input points		16
Maximum number of Units		CPU Block only: 11 Units (I/O Units and Dedicated I/O Units) max. CPU Block and Expansion I/O Block CPU Block: 5 Units max. Expansion I/O Block: 11 Units max.
Inner Boards		CQM1H-CPU11/21: None CQM1H-CPU51/61: 2 Boards
Communications Units (Controller Link Unit)		CQM1H-CPU11/21: None CQM1H-CPU51/61: 1 Unit
Types of interrupts	Input interrupts (4 inputs max.)	Input Interrupt Mode: Interrupts are executed in response to inputs from external sources to the CPU Unit's built-in input points. Counter Mode: Interrupts are executed in response to reception of a set number of pulses (counted down) via the CPU Unit's internal built-in input points (4 points).
	Interval timer interrupts (3 timers max.)	Scheduled Interrupt Mode: Program is interrupted at regular intervals measured by one of the CPU Unit's internal timers. One-shot Interrupt Mode: An interrupt is executed after a set time, measured by one of the CPU Unit's internal timers.
	High-speed counter interrupts	Target Value Comparison: Interrupt is executed when the high-speed counter PV is equal to a specified value. Range Comparison: Interrupt is executed when the high-speed counter PV lies within a specified range. **Note** Counting is possible for high-speed counter inputs from the CPU Unit's internal input points, Pulse I/O Boards, or Absolute Encoder Interface Boards. (The High-speed Counter Board has no interrupt function, but can output bit patterns internally and externally.)
I/O allocations		I/O is automatically allocated in order from the Unit nearest to the CPU Unit. (Because there are no I/O tables, it is not necessary, and not possible, to create I/O tables from a Programming Device.)

Note: Analog Power Supply Units must also be counted.

Main Specifications

Memory Area Structure

Data area		Size	Words	Bits	Function
IR area	Input area	256 bits	IR 000 to IR 015	IR 00000 to IR 01515	Input bits are allocated to Input Units or Dedicated I/O Units. The 16 bits in IR 000 are always allocated to the CPU Unit's built-in inputs. Bits in IR 001 to IR 015 are allocated to I/O or Dedicated I/O Units connected to the CPU Unit.
	Output area	256 bits	IR 100 to IR 115	IR 10000 to IR 11515	Output bits are allocated to Output Units or Dedicated I/O Units connected to the CPU Unit.
	Work areas	2,528 bits min.	IR 016 to IR 089	IR 01600 to IR 08915	Work bits do not have any specific function and they can be freely used within the program. (A minimum 2,528 bits are available as work bits. Most bits in the IR and LR areas can be used as work bits when they are not used for their allocated functions, so the total number of available work bits depends on the configuration of the PLC.)
			IR 116 to IR 189	IR 11600 to IR 18915	
			IR 216 to IR 219	IR 21600 to IR 21915	
			IR 224 to IR 229	IR 22400 to IR 22915	
Controller Link status areas		96 bits	IR 090 to IR 095	IR 09000 to IR 09515	Status Area 1: Stores the Controller Link data link status information.
		96 bits	IR 190 to IR 195	IR 19000 to IR 19515	Status Area 2: Stores the Controller Link error and network participation information.
MACRO operand area	Input area	64 bits	IR 096 to IR 099	IR 09600 to IR 09915	Used when the MACRO instruction, MCRO(99), is used.
	Output area	64 bits	IR 196 to IR 199	IR 19600 to IR 19915	
Inner Board slot 1 area		256 bits	IR 200 to IR 215	IR 20000 to IR 21515	These bits are allocated to the Inner Board mounted in slot 1 of a CQM1H-CPU51/61. High-speed Counter Board: IR 200 to IR 213 Serial Communications Board: IR 200 to IR 207
Analog settings area		64 bits	IR 220 to IR 223	IR 22000 to IR 22315	Used to store the analog settings when a CQM1H-AVB41 Analog Setting Board is mounted.
High-speed Counter 0 PV		32 bits	IR 230 to IR 231	IR 23000 to IR 23115	Used to store the present values of high-speed counter 0.
Inner Board slot 2 area		192 bits	IR 232 to IR 243	IR 23200 to IR 24315	These bits are allocated to the Inner Board mounted in slot 2. High-speed Counter Board: IR 232 to IR 243 Absolute Encoder Interface Board: IR 232 to IR 239 Pulse I/O Board: IR 232 to IR 239 Analog I/O Board: IR 232 to IR 239
SR area		184 bits	SR 244 to SR 255	SR 24400 to SR 25507	These bits serve specific functions such as flags and control bits.
HR area		1,600 bits	HR 00 to HR 99	HR 0000 to HR 9915	These bits store data and retain their ON/OFF status when power is turned OFF or when the operating mode is changed.
AR area		448 bits	AR 00 to AR 27	AR 0000 to AR 2715	These bits serve specific functions such as flags and control bits.
TR area		8 bits	---	TR 0 to TR 7	These bits are used to temporarily store ON/OFF status at program branches.
LR area		1,024 bits	LR 00 to LR 63	LR 0000 to LR 6315	Used for 1:1 data link through the RS-232 port or through a Controller Link Unit.
Timer/Counter area		512 bits	TIM/CNT 000 to TIM/CNT 511 (timer/counter numbers)		The same numbers are used for both timers and counters. Timer numbers 000 to 015 can be used with TIMH(15) for interrupt-refreshed PVs to ensure proper timing without inaccuracy being caused by the cycle time.

Data area		Size	Words	Bits	Function
DM area	Read/ write	3,072 words	DM 0000 to DM 3071	---	DM area data can be accessed in word units only. Word values are retained when the power is turned OFF.
		3,072 words	DM 3072 to DM 6143	---	Available in CQM1H-CPU51/61 CPU Units only.
	Read-only[4]	425 words	DM 6144 to DM 6568	---	Cannot be written from the program (only from a Programming Device). DM 6400 to DM 6409: Controller Link parameters DM 6450 to DM 6499: Routing tables DM 6550 to DM 6559: Serial Communications Board Setup
	Error history area[4]	31 words	DM 6569 to DM 6599	---	Cannot be written from the program (only from a Programming Device). Stores the time of occurrence and error code of errors that occur.
	PLC Setup[4]	56 words	DM 6600 to DM 6655	---	Cannot be written from the program (only from a Programming Device). Stores various parameters that control PLC operation.
EM area		6,144 words	EM 0000 to EM 6143	---	EM area data can be accessed in word units only. Word values are retained when the power is turned OFF or the operating mode is changed. (CQM1H-CPU61 CPU Unit only.)

Memory Cassette Specifications

Item	Details
Memory Cassette (EEPROM or flash memory)	Mounted from the front of the CPU Unit and used to store and read the user's program, DM (read-only DM and PLC Setup), and expansion instruction information as one block. It is possible to set the CPU Unit so that data stored in the Memory Cassette (user's program, DM, expansion instruction information) is automatically sent to the CPU Unit (auto-boot) at startup. Transfer and comparison of data between the CPU Unit and Memory Cassette are possible using AR area control bits.

Other Functions

Item	Specification
Macro instructions	Subroutines called by instructions containing arguments.
Min. cycle time	1 to 9,999 ms (Unit: 1 ms)
Cycle time monitoring	When the cycle time exceeds 100 ms, the Cycle Time Over Flag turns ON, and operation continues. (A setting can be made in the PLC Setup so that this error is not generated.) When the cycle time exceeds the cycle monitor time, operation is stopped. Cycle monitor time settings: 0 to 990 ms in 10-ms units, 0 to 9,900 ms in 100-ms units, 0 to 99 s in 1-s units. **Note** The maximum and current values of the cycle time are stored in the AR area.
I/O refreshing	Cyclic refreshing, refreshing by IORF(97), direct output refreshing (set in the PLC Setup), interrupt input refreshing. (The inputs that are refreshed can be set separately for input interrupts, high-speed counter interrupts, and interval timer interrupts in the PLC Setup.)
I/O memory status when changing operating mode	Depends on the ON/OFF status of the I/O Hold Bit (SR 25212).
Load OFF	All outputs on Output Units can be turned OFF when the CPU Unit is operating in RUN, MONITOR, or PROGRAM mode. (Used for stopping output in emergencies, for debugging, etc.)
User-customized DIP switch setting	A pin setting on the DIP switch on the front of the CPU Unit is stored in AR 0712. This setting can be used as an ON/OFF condition (e.g., to switch between trial operation and actual operation).
Mode setting at power-up	Possible
Debugging	Forced set/reset, differential monitoring, data tracing (scheduled, cyclic, or when instruction is executed).
Online editing	User programs can be overwritten in program-block units when the CPU Unit is in MONITOR mode. With the CX-Programmer, more than one program block can be edited at the same time.
Program protection	Write-protection of user program and data memory (DM 6144 to DM 6655: read-only DM): Set using pin 1 of the DIP switch.
Error check	User-defined errors (i.e., user can define fatal errors and non-fatal errors using the FAL(06) and FALS(07) instructions.) (It is possible to stop operation using FALS(07) for fatal errors. User-defined error logs can be created in specific bits (logging) when using FAL(06).
Error log	Up to 10 errors (including user-defined errors) are stored in the error log. Information includes the error code, error details, and the time the error occurred.

Main Specifications

Item	Specification			
Serial communications	Built-in peripheral port: Programming Device (including Programming Console) connections, Host Links, no-protocol communications Built-in RS-232C port: Programming Device (excluding Programming Console) connections, Host Links, no-protocol communications, NT Links (1:1 mode), 1:1 Data LInks			
	RS-232C port and RS-422A/485 port on Serial Communications Board (sold separately): Programming Device (excluding Programming Console) connections, Host Links, no-protocol communications, NT Links (1:1 mode, 1:N mode), 1:1 Data LInks, protocol macros			
Serial communications modes	CQM1H CPU Unit's built-in port	Built-in peripheral port	Built-in RS-232C port	Serial Communications Board ports
Programming Console bus	Connects to Programming Console.	YES (pin 7 OFF)	No	No
Peripheral bus	Connects to a computer running CX-Programmer or other Support Software. (Automatically used if the network type is set to peripheral bus on the Support Software.)	YES (pin 7 ON)	No	No
Host Link (SYSMAC WAY)	Enables reading/writing CPU Unit I/O memory or program using Host Link commands. Computers running Support Software or OMRON Programmable Terminals can also be connected. PLC-initiated communications are possible.	YES (pin 7 ON)	YES	YES
No-protocol	Enables sending or receiving up to 256 bytes of data without a protocol or data conversion. A start code, end code, and transmission delay can be set.	YES (pin 7 ON)	YES	YES
1:1 data link	Enables 1:1 data link with a CQM1H, CQM1, CPM-series, C200HX/HG/HE, C200HS, or SRM1 PLC.	No	YES	YES
NT links (1:1 and 1:N)	Enables 1:1 or 1:N communications with OMRON Programmable Terminals without additional programming.	No	YES (1:1 only)	YES (1:1 and 1:N)
Protocol macros	Enables user-created protocols to communicate with essential any device equipped with a serial communications port (e.g., RS-232C). Standard protocols are also provided.	No	No	YES
Clock	Some Memory Cassette are equipped with a clock. (The time of the error will recorded if a clock is used.			
Input time constants	Used to set the ON (or OFF) response times for DC Input Units. Settings: 1, 2, 4, 8, 16, 32, 64, and 128 ms.			
Power OFF detection time	AC power supply: 10 to 25 ms (not fixed), DC power supply: 5 to 25 ms (not fixed)			
Memory protection	Held Areas: Holding bits, contents of Data Memory and Extended Data Memory, and status of the counter Completion Flags and present values. **Note** If the I/O Hold Bit (SR 25212) is turned ON, and the PLC Setup is set to maintain the I/O Hold Bit status when power is turned ON, the contents of the IR area and the LR area will be saved.			
Commands to a host computer	Host Link command responses can be sent to a computer connected via the Host Link System using the TXD(—) (communications port output) instruction.			
Remote programming and monitoring	Host Link or peripheral bus communications via a CPU Unit's serial communications port can be used for remote programming and remote monitoring of the PLC through a Controller Link System. (This function is, however, not supported for the serial communications ports on the Serial Communications Board.)			
Program check	Program is checked at the beginning of operation for items such as no END(01) instruction and instruction errors. CX-Programmer can also check programs. (The level of program checking can be set.)			
Battery life	5 years at 25°C (Depends on the ambient temperature and power supply conditions. Min.: 1 yr) Battery replacement must be performed within 5 minutes.			
Errors from self-diagnostics	CPU (watchdog timer), I/O verification, I/O bus, memory, FALS system (FALS execution or cycle monitor time over), FAL system (FAL execution or PLC Setup error etc.), battery, cycle time over and communications port.			
Other functions	Storage of number of times power has been interrupted. (Stored in AR area.)			