

## 2.5-V TO 3.3-V HIGH-PERFORMANCE CLOCK BUFFER

Check for Samples: [CDCVF2310-EP](#)

### FEATURES

- High-Performance 1:10 Clock Driver
- Operates up to 200 MHz at  $V_{DD}$  3.3 V
- Pin-to-Pin Skew < 100 ps at  $V_{DD}$  3.3 V
- $V_{DD}$  Range: 2.3 V to 3.6 V
- Output Enable Glitch Suppression
- Distributes One Clock Input to Two Banks of Five Outputs
- 25- $\Omega$  On-Chip Series Damping Resistors
- Packaged in 24-Pin TSSOP

### APPLICATIONS

- General-Purpose Applications

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military ( $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) Temperature Range <sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

(1) Custom temperature ranges available

### DESCRIPTION

The CDCVF2310 is a high-performance, low-skew clock buffer that operates up to 200 MHz. Two banks of five outputs each provide low-skew copies of CLK. After power up, the default state of the outputs is low regardless of the state of the control pins. For normal operation, the outputs of bank 1Y[0:4] or 2Y[0:4] can be placed in a low state when the control pins (1G or 2G, respectively) are held low and a negative clock edge is detected on the CLK input. The outputs of bank 1Y[0:4] or 2Y[0:4] can be switched into the buffer mode when the control pins (1G and 2G) are held high and a negative clock edge is detected on the CLK input. The device operates in a 2.5-V and 3.3-V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

The CDCVF2310 is characterized for operation from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

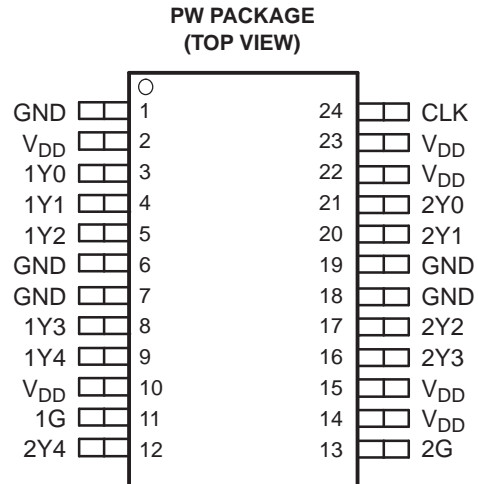
**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

$T_J$	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	TSSOP - PW	CDCVF2310MPWREP	CKV2310EP	V62/13603-01XE
		CDCVF2310MPWEP	CKV2310EP	V62/13603-01XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

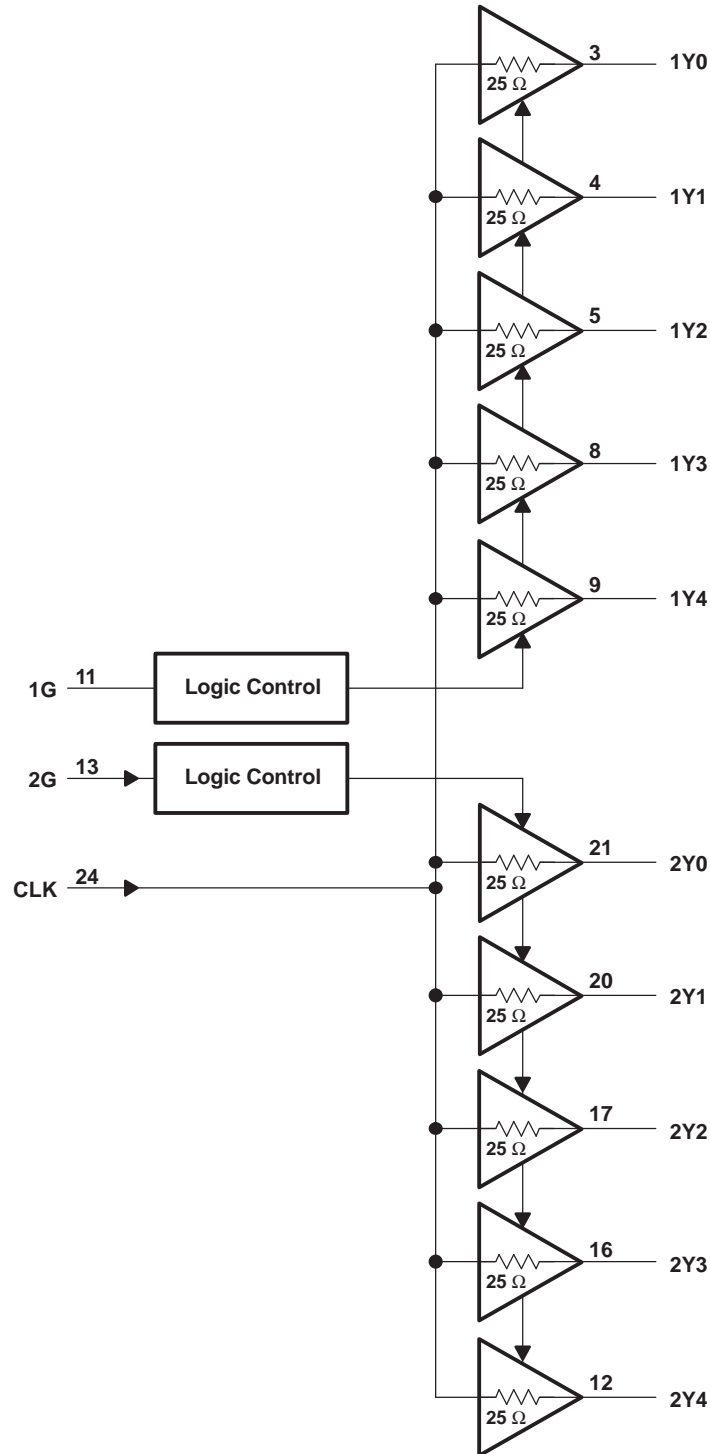




This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**FUNCTIONAL BLOCK DIAGRAM**



**Table 2. FUNCTION TABLE**

INPUT			OUTPUT	
1G	2G	CLK	1Y[0:4]	2Y[0:4]
L	L	↓	L	L
H	L	↓	CLK <sup>(1)</sup>	L
L	H	↓	L	CLK <sup>(1)</sup>
H	H	↓	CLK <sup>(1)</sup>	CLK <sup>(1)</sup>

- (1) After detecting one negative edge on the CLK input, the output follows the input CLK if the control pin is held high.

**Terminal Functions**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
1G	11	I	Output enable control for 1Y[0:4] outputs. This output enable is active-high, meaning the 1Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
2G	13	I	Output enable control for 2Y[0:4] outputs. This output enable is active-high, meaning the 2Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
1Y[0:4]	3, 4, 5, 8, 9	O	Buffered output clocks
2Y[0:4]	21, 20, 17, 16, 12	O	Buffered output clocks
CLK	24	I	Input reference frequency
GND	1, 6, 7, 18, 19		Ground
V <sub>DD</sub>	2, 10, 14, 15, 22, 23		DC power supply, 2.3 V – 3.6 V

**ABSOLUTE MAXIMUM RATINGS**

over operating junction temperature range (unless otherwise noted) <sup>(1)</sup>

Supply voltage range, V <sub>DD</sub>	–0.5 V to 4.6 V
Input voltage range, V <sub>I</sub> <sup>(2)</sup> <sup>(3)</sup>	–0.5 V to V <sub>DD</sub> + 0.5 V
Output voltage range, V <sub>O</sub> <sup>(2)</sup> <sup>(3)</sup>	–0.5 V to V <sub>DD</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DD</sub> )	±50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub> )	±50 mA
Continuous total output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>DD</sub> )	±50 mA
Storage temperature range T <sub>stg</sub>	–65°C to 150°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 4.6 V maximum.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		CDCVF2310		UNITS
		PW		
		24 PINS		
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	91.7		°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance <sup>(3)</sup>	31.2		
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	46.4		
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	1.5		
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	45.8		
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	N/A		

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

### RECOMMENDED OPERATING CONDITIONS <sup>(1)</sup>

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}$		2.3	2.5		V
			3.3	3.6	
Low-level input voltage, $V_{IL}$	$V_{DD} = 3\text{ V to }3.6\text{ V}$			0.8	V
	$V_{DD} = 2.3\text{ V to }2.7\text{ V}$			0.7	
High-level input voltage, $V_{IH}$	$V_{DD} = 3\text{ V to }3.6\text{ V}$	2			V
	$V_{DD} = 2.3\text{ V to }2.7\text{ V}$	1.7			
Input voltage, $V_i$		0		$V_{DD}$	V
High-level output current, $I_{OH}$	$V_{DD} = 3\text{ V to }3.6\text{ V}$			12	mA
	$V_{DD} = 2.3\text{ V to }2.7\text{ V}$			6	
Low-level output current, $I_{OL}$	$V_{DD} = 3\text{ V to }3.6\text{ V}$			12	mA
	$V_{DD} = 2.3\text{ V to }2.7\text{ V}$			6	
Operating junction temperature, $T_J$		-55		125	°C

- (1) Unused inputs must be held high or low to prevent them from floating.

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$	Input voltage	$V_{DD} = 3\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$I_I$	Input current	$V_I = 0\text{ V}$ or $V_{DD}$				$\pm 5$	$\mu\text{A}$
$I_{DD}^{(2)}$	Static device current	$\text{CLK} = 0\text{ V}$ or $V_{DD}$ ,	$I_O = 0\text{ mA}$			100	$\mu\text{A}$
$C_I$	Input capacitance	$V_{DD} = 2.3\text{ V}$ to $3.6\text{ V}$ ,	$V_I = 0\text{ V}$ or $V_{DD}$		2.5		pF
$C_O$	Output capacitance	$V_{DD} = 2.3\text{ V}$ to $3.6\text{ V}$ ,	$V_I = 0\text{ V}$ or $V_{DD}$		2.8		pF
<b><math>V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}</math></b>							
$V_{OH}$	High-level output voltage	$V_{DD} = \text{min to max}$ ,	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{DD} - 0.2$			V
		$V_{DD} = 3\text{ V}$	$I_{OH} = -12\text{ mA}$ $I_{OH} = -6\text{ mA}$	2.1	2.4		
$V_{OL}$	Low-level output voltage	$V_{DD} = \text{min to max}$ ,	$I_{OL} = -100\text{ }\mu\text{A}$			0.2	V
		$V_{DD} = 3\text{ V}$	$I_{OL} = 12\text{ mA}$			0.8	
			$I_{OL} = 6\text{ mA}$			0.55	
$I_{OH}$	High-level output current	$V_{DD} = 3\text{ V}$ ,	$V_O = 1\text{ V}$	-28			mA
		$V_{DD} = 3.3\text{ V}$ ,	$V_O = 1.65\text{ V}$	-36			
		$V_{DD} = 3.6\text{ V}$ ,	$V_O = 3.135\text{ V}$	-14			
$I_{OL}$	Low-level output current	$V_{DD} = 3\text{ V}$ ,	$V_O = 1.95\text{ V}$	28			mA
		$V_{DD} = 3.3\text{ V}$ ,	$V_O = 1.65\text{ V}$	36			
		$V_{DD} = 3.6\text{ V}$ ,	$V_O = 0.4\text{ V}$	14			
<b><math>V_{DD} = 2.5\text{ V} \pm 0.2\text{ V}</math></b>							
$V_{OH}$	High-level output voltage	$V_{DD} = \text{min to max}$ ,	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{DD} - 0.2$			V
		$V_{DD} = 2.3\text{ V}$	$I_{OH} = -6\text{ mA}$	1.8			
$V_{OL}$	Low-level output voltage	$V_{DD} = \text{min to max}$ ,	$I_{OL} = 100\text{ }\mu\text{A}$			0.2	V
		$V_{DD} = 2.3\text{ V}$	$I_{OL} = 6\text{ mA}$			0.55	
$I_{OH}$	High-level output current	$V_{DD} = 2.3\text{ V}$ ,	$V_O = 1\text{ V}$	-15			mA
		$V_{DD} = 2.5\text{ V}$ ,	$V_O = 1.25\text{ V}$	-25			
		$V_{DD} = 2.7\text{ V}$ ,	$V_O = 2.375\text{ V}$	-10			
$I_{OL}$	Low-level output current	$V_{DD} = 2.3\text{ V}$ ,	$V_O = 1.2\text{ V}$	15			mA
		$V_{DD} = 2.5\text{ V}$ ,	$V_O = 1.25\text{ V}$	25			
		$V_{DD} = 2.7\text{ V}$ ,	$V_O = 0.3\text{ V}$	10			

 (1) All typical values are at respective nominal  $V_{DD}$ .

 (2) For  $I_{CC}$  over frequency, see [Figure 6](#).

## TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating junction temperature

		MIN	NOM	MAX	UNIT	
f <sub>clk</sub>	Clock frequency	V <sub>DD</sub> = 3 V to 3.6 V		0	200	MHz
		V <sub>DD</sub> = 2.3 V to 2.7 V		0	170	

## JITTER CHARACTERISTICS

Characterized using CDCVF2310 Performance EVM when V<sub>DD</sub>=3.3 V. Outputs not under test are terminated to 50 Ω.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>jitter</sub>	Additive phase jitter from input to output 1Y0	12 kHz to 5 MHz, f <sub>out</sub> = 30.72 MHz		52	fs rms
		12 kHz to 20 MHz, f <sub>out</sub> = 125 MHz		45	

## SWITCHING CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>V<sub>DD</sub> = 3.3 V ±0.3 V (see Figure 2)</b>						
t <sub>PLH</sub>	CLK to Yn	f = 0 MHz to 200 MHz For circuit load, see Figure 2.		1.3	3.3	ns
t <sub>PHL</sub>						
t <sub>sk(o)</sub>	Output skew (Ym to Yn) <sup>(1)</sup> (see Figure 4)				100	ps
t <sub>sk(p)</sub>	Pulse skew (see Figure 5)				570	ps
t <sub>sk(pp)</sub>	Part-to-part skew				500	ps
t <sub>r</sub>	Rise time (see Figure 3)	V <sub>O</sub> = 0.4 V to 2 V		0.7	2.2	V/ns
t <sub>f</sub>	Fall time (see Figure 3)	V <sub>O</sub> = 2 V to 0.4 V		0.7	2.2	V/ns
t <sub>su(en)</sub>	Enable setup time, G_high before CLK ↓			0.1		ns
t <sub>su(dis)</sub>	Disable setup time, G_low before CLK ↓			0.1		ns
t <sub>h(en)</sub>	Enable hold time, G_high after CLK ↓			0.4		ns
t <sub>h(dis)</sub>	Disable hold time, G_low after CLK ↓			0.4		ns
<b>V<sub>DD</sub> = 2.5 V ±0.2 V (see Figure 2)</b>						
t <sub>PLH</sub>	CLK to Yn	f = 0 MHz to 170 MHz For circuit load, see Figure 2.		1.5	4	ns
t <sub>PHL</sub>						
t <sub>sk(o)</sub>	Output skew (Ym to Yn) <sup>(1)</sup> (see Figure 4)				170	ps
t <sub>sk(p)</sub>	Pulse skew (see Figure 5)				680	ps
t <sub>sk(pp)</sub>	Part-to-part skew				600	ps
t <sub>r</sub>	Rise time (see Figure 3)	V <sub>O</sub> = 0.4 V to 1.7 V		0.5	1.4	V/ns
t <sub>f</sub>	Fall time (see Figure 3)	V <sub>O</sub> = 1.7 V to 0.4 V		0.5	1.4	V/ns
t <sub>su(en)</sub>	Enable setup time, G_high before CLK ↓			0.1		ns
t <sub>su(dis)</sub>	Disable setup time, G_low before CLK ↓			0.1		ns
t <sub>h(en)</sub>	Enable hold time, G_high after CLK ↓			0.4		ns
t <sub>h(dis)</sub>	Disable hold time, G_low after CLK ↓			0.4		ns

(1) The t<sub>sk(o)</sub> specification is only valid for equal loading of all outputs.

DETAILED DESCRIPTION

Output Enable Glitch Suppression Circuit

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer is enabled or disabled on the next full period of the input clock (negative edge triggered by the input clock) (see Figure 1).

The G input must fulfill the timing requirements ( $t_{su}$ ,  $t_h$ ) according to the *Switching Characteristics* table for predictable operation.

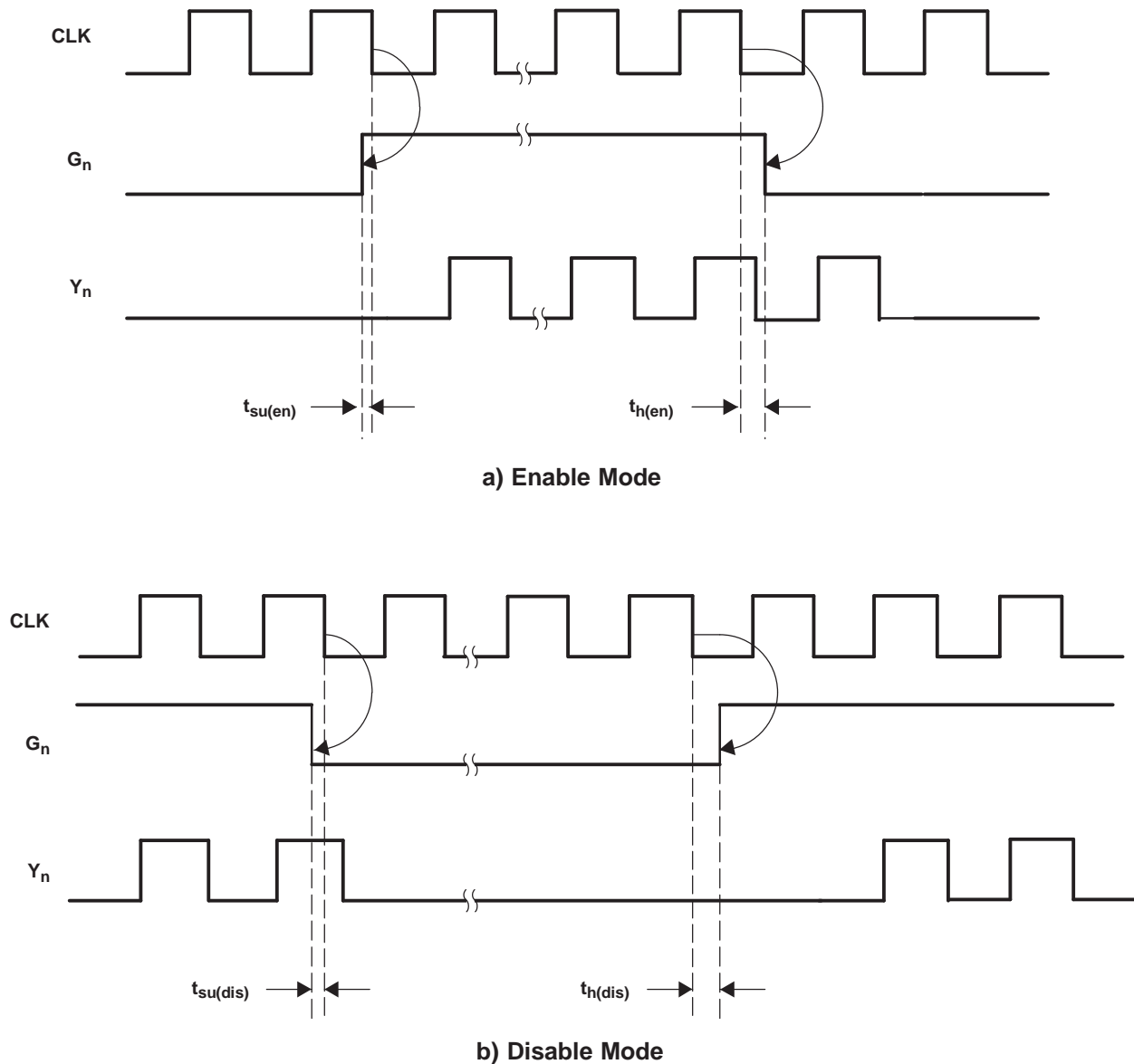
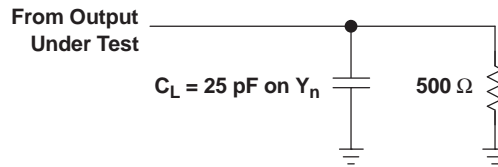


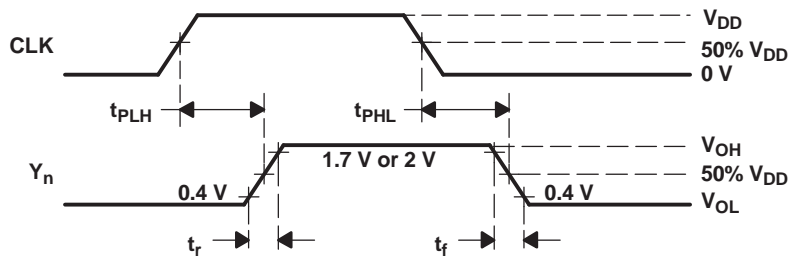
Figure 1. Enable and Disable Mode Relative to CLK↓

**PARAMETER MEASUREMENT INFORMATION**

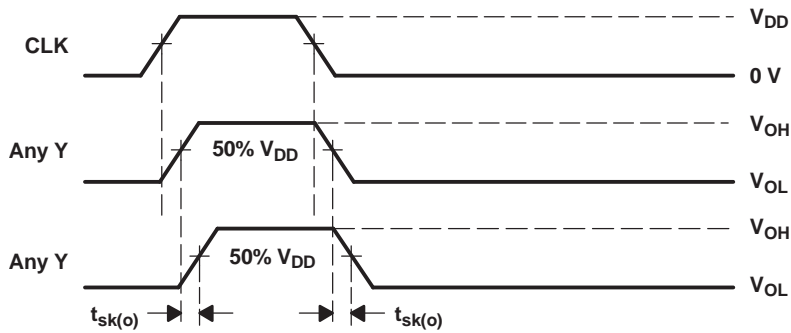


- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 200$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 1.2$  ns,  $t_f < 1.2$  ns.

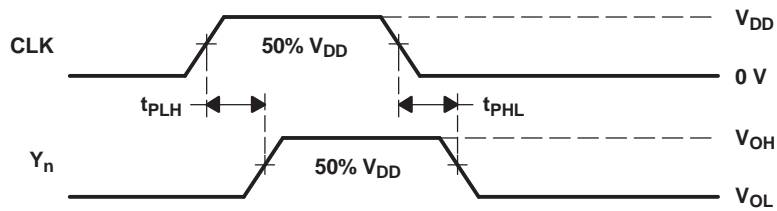
**Figure 2. Test Load Circuit**



**Figure 3. Voltage Waveforms Propagation Delay Times**



**Figure 4. Output Skew**



NOTE:  $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

**Figure 5. Pulse Skew**

PARAMETER MEASUREMENT INFORMATION (continued)

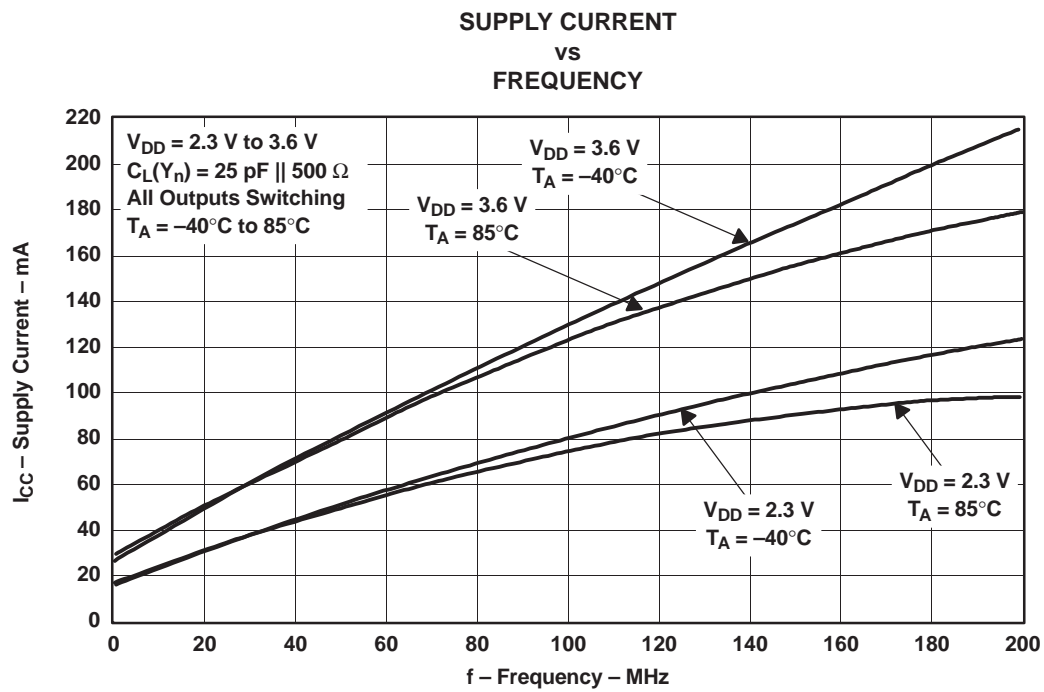


Figure 6.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCVF2310MPWEP	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	<a href="#">Samples</a>
CDCVF2310MPWREP	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	<a href="#">Samples</a>
V62/13603-01XE	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	<a href="#">Samples</a>
V62/13603-01XE-T	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CDCVF2310-EP :**

- Catalog: [CDCVF2310](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2310MPWREP	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

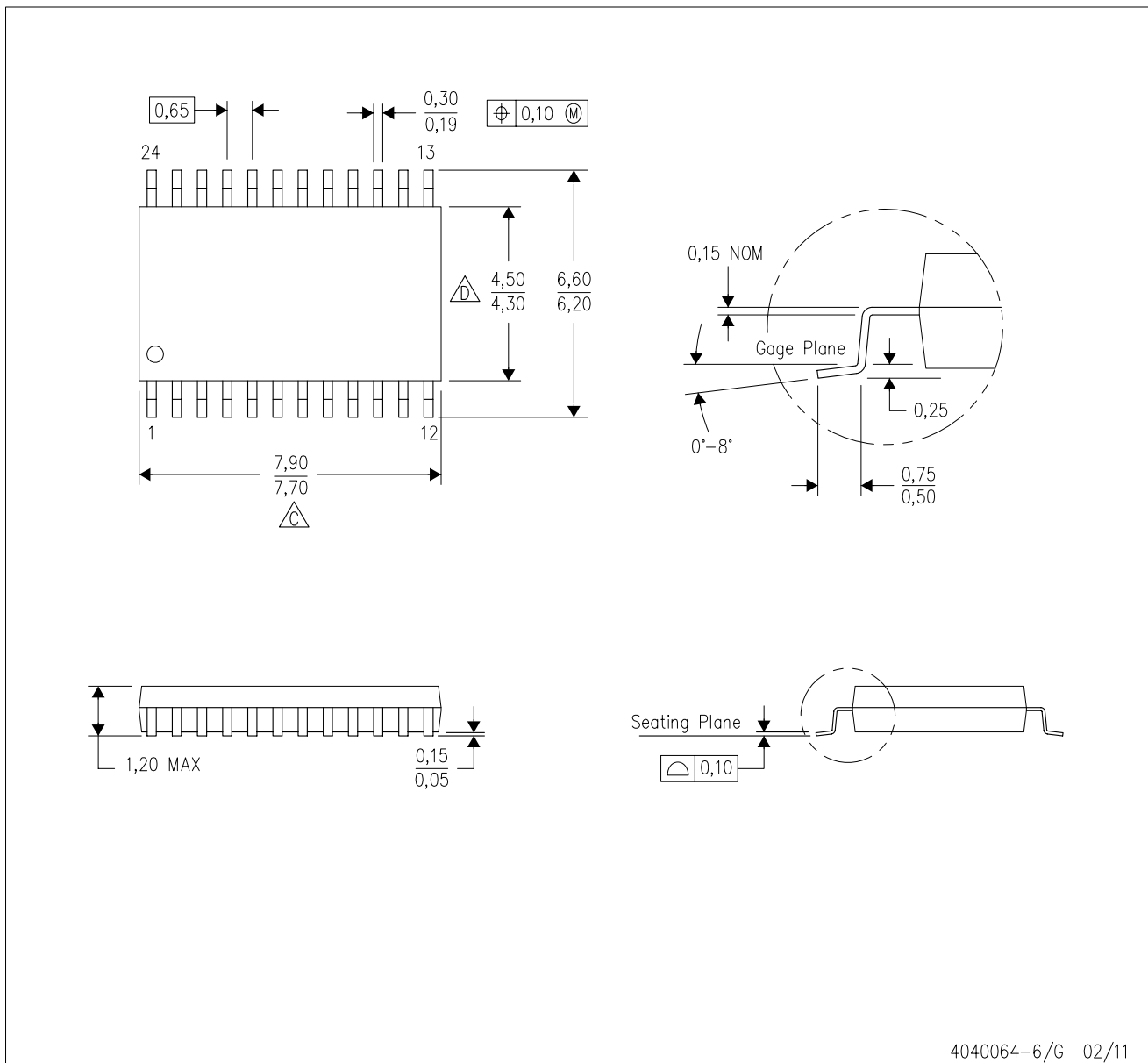




\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2310MPWREP	TSSOP	PW	24	2000	367.0	367.0	38.0

PW (R-PDSO-G24)

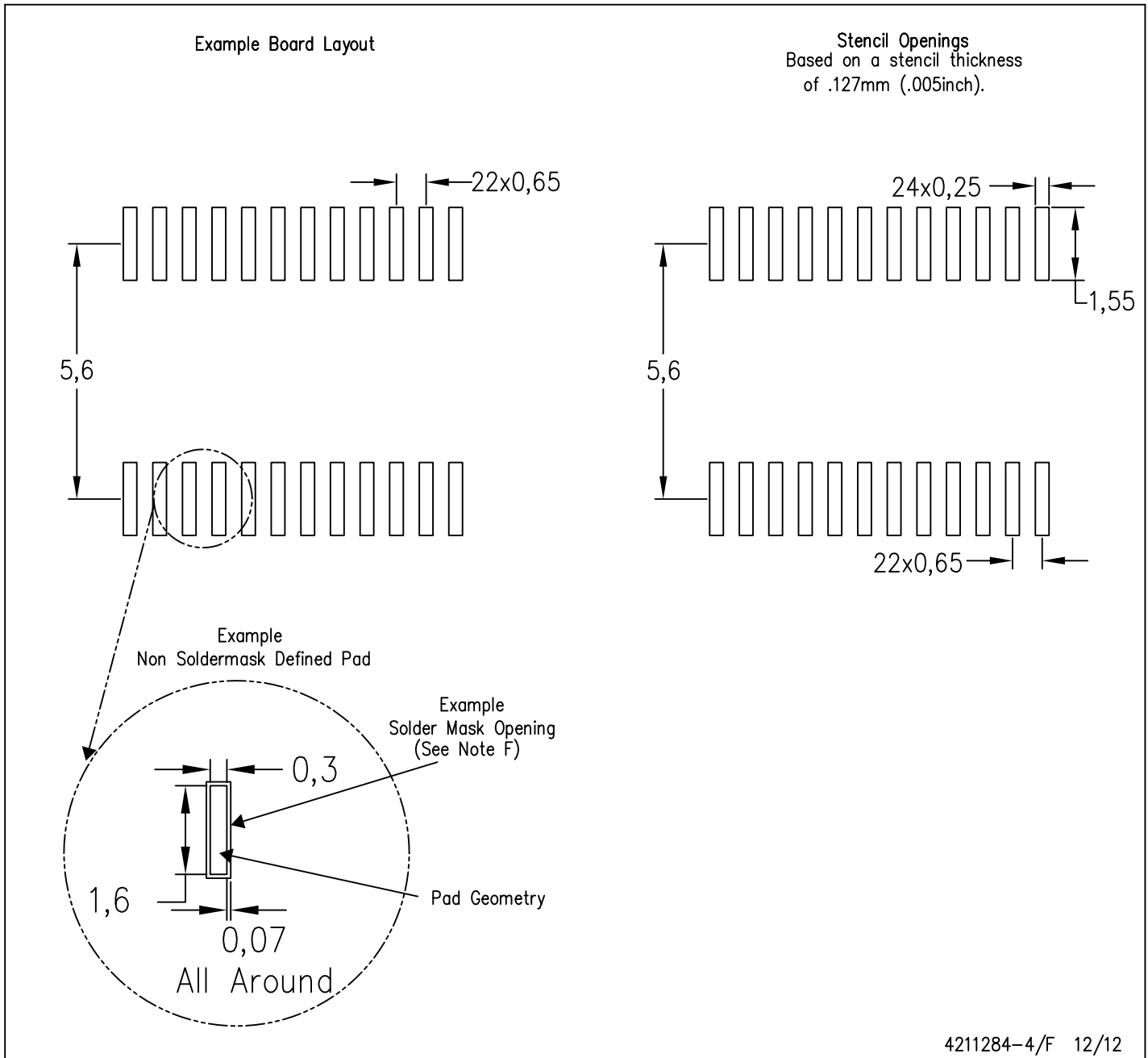
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)