CC1021 Single Chip Low Power RF Transceiver for Narrowband Systems

Not Recommended for New Designs NRND

1 Device Overview

1.1 Features

- True Single Chip UHF RF Transceiver
- Frequency Range 402 MHz to 470 MHz and 804 MHz to 960 MHz
- High Sensitivity
  - Up to –112 dBm for 38.4 kHz Receiver Channel Filter Bandwidth
  - Up to –106 dBm for 102.4 kHz Receiver Channel Filter Bandwidth
- Programmable Output Power
- Low Current Consumption
  - RX: 19.9 mA
- Low Supply Voltage
  - From 2.3 V to 3.6 V
- Very Few External Components Required
- Small Size
  - QFN 32 Package
- Pb-Free Package
- Digital RSSI and Carrier Sense Indicator
- Data Rate Up to 153.6 kBaud
- OOK, FSK, and GFSK Data Modulation
- Integrated Bit Synchronizer
- Image Rejection Mixer
- Programmable Frequency
- Automatic Frequency Control (AFC)
- Suitable for Frequency Hopping Systems
- Suited for Systems Targeting Compliance With EN 300 220, FCC CFR47 Part 15, ARIB STD-T96
- Development Kit Available
- Easy-to-Use Software for Generating the CC1021 Configuration Data
- Fully Compatible With CC1020 for Receiver Channel Filter Bandwidths of 38.4 kHz and Higher

1.2 Applications

- Low Power UHF Wireless Data Transmitters and Receivers With Channel Spacings of 50 kHz or Higher
- 433-, 868-, 915-, 960-MHz ISM/SRD Band Systems
- AMR – Automatic Meter Reading
- Wireless Alarm and Security Systems
- Home Automation
- Low Power Telemetry
- Automotive (RKE/TPMS)

1.3 Description

The CC1021 device is a true single-chip UHF transceiver designed for very low power and very low voltage wireless applications. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency bands at 433 MHz, 868 MHz, and 915 MHz, but can easily be programmed for multichannel operation at other frequencies in the 402- to 470-MHz and 804- to 960-MHz range.

The CC1021 device is especially suited for narrowband systems with channel spacing of 50 kHz and higher complying with EN 300 220, FCC CFR47 part 15, and ARIB STD-T96.

The CC1021 main operating parameters can be programmed through a serial bus, thus making CC1021 a very flexible and easy to use transceiver.

In a typical system, CC1021 will be used together with a microcontroller and a few external passive components.

Table 1-1. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CC1021	VQFNP (32)	7.00 mm × 7.00 mm

(1) For more information, see *Section 8*, *Mechanical Packaging and Orderable Information.*

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

1.4 Functional Block Diagram

Figure 1-1 shows the system block diagram of the CC1021 device.

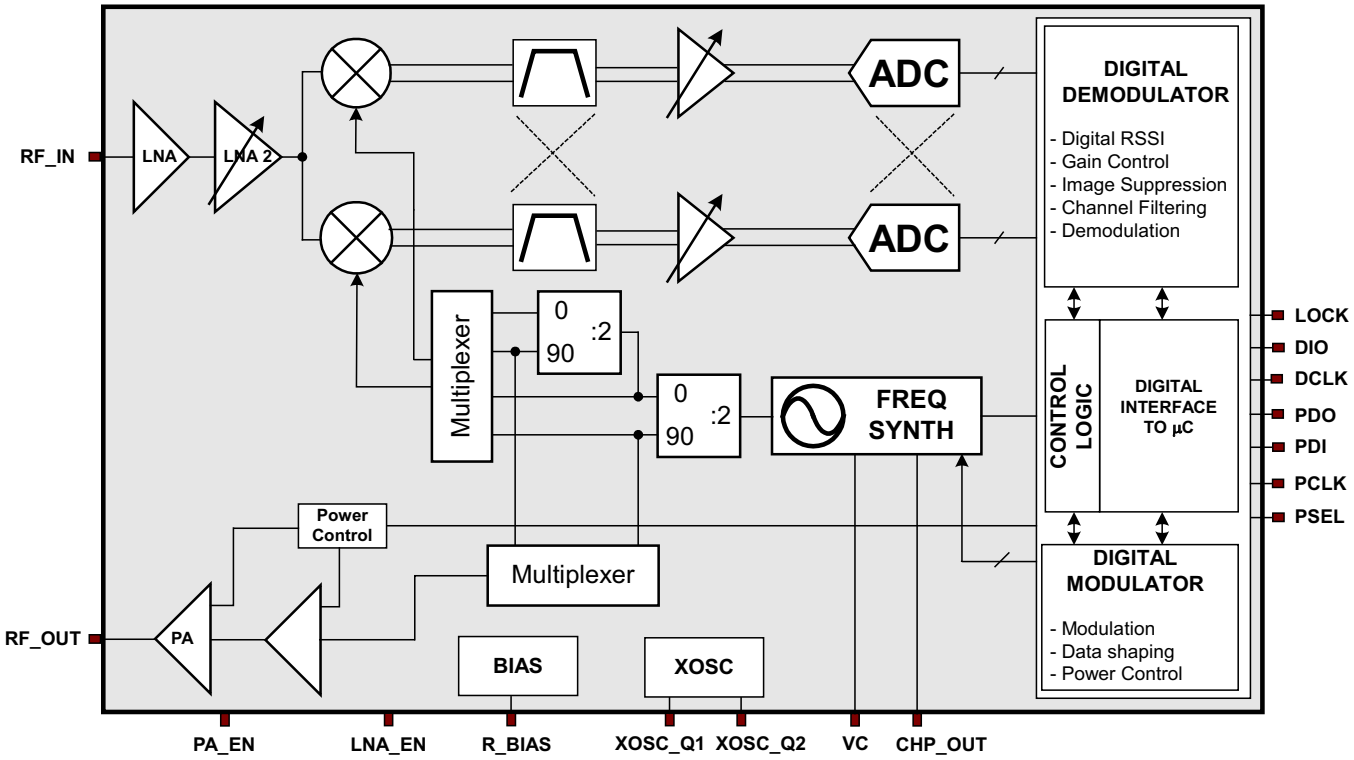

Figure 1-1. Functional Block Diagram

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2 Revision History

This data manual revision history highlights the changes made to the SWRS045C device-specific data manual to make it an SWRS045D revision.

Changes from Revision C (February 2010) to Revision D	Page
• Converted document to new TI standards.	1
• Added Thermal Resistance Characteristics for *VQFNP* Package.	15
• Changed Register table format to new TI standards.	60

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3 Terminal Configuration and Functions

3.1 Pin Diagram

Figure 3-1 shows pin names and locations for the CC1021 device.

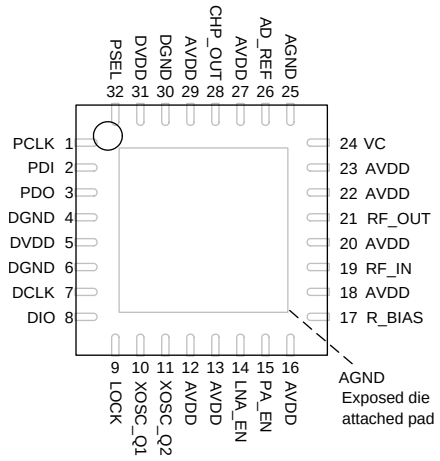

Figure 3-1. Package 7-mm × 7-mm VQFNP (Top View)

3.2 Pin Configuration

Table 3-1. Pin Attributes(1)(2)

PIN NO.	PIN NAME	TYPE	DESCRIPTION
—	AGND	Ground (analog)	Exposed die attached pad. Must be soldered to a solid ground plane as this is the ground connection for all analog modules. See *Section 6.3* for more details.
1	PCLK	Digital input	Programming clock for SPI configuration interface
2	PDI	Digital input	Programming data input for SPI configuration interface
3	PDO	Digital output	Programming data output for SPI configuration interface
4	DGND	Ground (digital)	Ground connection (0 V) for digital modules and digital I/O
5	DVDD	Power (digital)	Power supply (3 V typical) for digital modules and digital I/O
6	DGND	Ground (digital)	Ground connection (0 V) for digital modules (substrate)
7	DCLK	Digital output	Clock for data in both receive and transmit mode Can be used as receive data output in asynchronous mode
8	DIO	Digital input/output	Data input in transmit mode; data output in receive mode Can also be used to start power-up sequencing in receive
9	LOCK	Digital output	PLL Lock indicator, active low. Output is asserted (low) when PLL is in lock. The pin can also be used as a general digital output, or as receive data output in synchronous NRZ/Manchester mode
10	XOSC_Q1	Analog input	Crystal oscillator or external clock input
11	XOSC_Q2	Analog output	Crystal oscillator
12	AVDD	Power (analog)	Power supply (3 V typical) for crystal oscillator
13	AVDD	Power (analog)	Power supply (3 V typical) for the IF VGA
14	LNA_EN	Digital output	General digital output. Can be used for controlling an external LNA if higher sensitivity is needed.
15	PA_EN	Digital output	General digital output. Can be used for controlling an external PA if higher output power is needed.
16	AVDD	Power (analog)	Power supply (3 V typical) for global bias generator and IF anti-alias filter

(1) DCLK, DIO and LOCK are high-impedance (3-state) in power down (BIAS_PD = 1 in the MAIN register).
(2) The exposed die attached pad must be soldered to a solid ground plane as this is the main ground connection for the chip.

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Table 3-1. Pin Attributes[1][2] (continued)

PIN NO.	PIN NAME	TYPE	DESCRIPTION
17	R_BIAS	Analog output	Connection for external precision bias resistor (82 kΩ, ±1%)
18	AVDD	Power (analog)	Power supply (3 V typical) for LNA input stage
19	RF_IN	RF Input	RF signal input from antenna (external AC-coupling)
20	AVDD	Power (analog)	Power supply (3 V typical) for LNA
21	RF_OUT	RF output	RF signal output to antenna
22	AVDD	Power (analog)	Power supply (3 V typical) for LO buffers, mixers, prescaler, and first PA stage
23	AVDD	Power (analog)	Power supply (3 V typical) for VCO
24	VC	Analog input	VCO control voltage input from external loop filter
25	AGND	Ground (analog)	Ground connection (0 V) for analog modules (guard)
26	AD_REF	Power (analog)	3 V reference input for ADC
27	AVDD	Power (analog)	Power supply (3 V typical) for charge pump and phase detector
28	CHP_OUT	Analog output	PLL charge pump output to external loop filter
29	AVDD	Power (analog)	Power supply (3 V typical) for ADC
30	DGND	Ground (digital)	Ground connection (0 V) for digital modules (guard)
31	DVDD	Power (digital)	Power supply connection (3 V typical) for digital modules
32	PSEL	Digital input	Programming chip select, active low, for configuration interface. Internal pullup resistor.

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4 Specifications

4.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT	CONDITION
Supply voltage, VDD	–0.3	5	V	All supply pins must have the same voltage
Voltage on any pin	–0.3	VDD + 0.3, max 5.0	V	
Input RF level		10	dBm	
Package body temperature		260	°C	Norm: IPC/JEDEC J-STD-020(2)
Humidity non-condensing	5%	85%		
Storage temperature range, T_{stg}	–50	150	°C	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD_020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices”.

4.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge (ESD) performance:	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001(1)(2)	All pads except RF	±1	kV
			RF Pads	±0.4	kV
		Charged Device Model (CDM)		250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) According to JEDEC STD 22, method A114, Human Body Model

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT	CONDITION
RF Frequency Range	402		470	MHz	Programmable in < 300 Hz steps
	804		960	MHz	Programmable in < 600 Hz steps
Operating ambient temperature range	–40		85	°C	
Supply voltage	2.3	3.0	3.6	V	The same supply voltage should be used for digital (DVDD) and analog (AVDD) power.

4.4 RF Transmit

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER		MIN	TYP	MAX	UNIT	CONDITION
Transmit data rate		0.45		153.6	kBaud	Minimum data rate for OOK is 2.4 kBaud NRZ or Manchester encoding can be used. 153.6 kBaud equals 153.6 kbps using NRZ coding and 76.8 kbps using Manchester coding. See *Section 5.4.2* for details The data rate is programmable. See *Section 5.7* for details.
Binary FSK frequency separation	in 402 to 470 MHz range	0		108	kHz	108/216 kHz is the maximum specified separation at 1.84 MHz reference frequency. Larger separations can be achieved at higher reference frequencies.
	in 804 to 960 MHz range	0		216	kHz	

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RF Transmit *(continued)*

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER		MIN	TYP	MAX	UNIT	CONDITION
Output power	433 MHz		–20 to +10		dBm	Delivered to 50 Ω single-ended load. The output power is programmable and should not be programmed to exceed +10/+5 dBm at 433/868 MHz under any operating conditions. See *Section 5.11* for details.
	868 MHz		–20 to +5		dBm	
Output power tolerance	At 2.3 V, +85°C		–4		dB	At maximum output power
	At 3.6 V, –40°C		3		dB	
Harmonics, radiated CW	2nd harmonic, 433 MHz, +10 dBm		–50		dBc	Harmonics are measured as EIRP values according to EN 300 220. The antenna (SMAFF-433 and SMAFF-868 from R.W. Badland) plays a part in attenuating the harmonics.
	3rd harmonic, 433 MHz, +10 dBm		–50		dBc	
	2nd harmonic, 868 MHz, +5 dBm		–50		dBc	
	3rd harmonic, 868 MHz, +5 dBm		–50		dBc	
Adjacent channel power (GFSK)	433 MHz		–46		dBc	ACP is measured in a 100 kHz bandwidth at ±100 kHz offset. Modulation: 19.2 kBaud NRZ PN9 sequence, ±19.8 kHz frequency deviation.
	868 MHz		–42		dBc	
Occupied bandwidth (99.5%,GFSK)	433 MHz		60		kHz	Bandwidth for 99.5% of total average power. Modulation: 19.2 kBaud NRZ PN9 sequence, ±19.8 kHz frequency deviation.
	868 MHz		60		kHz	
Modulation bandwidth, 868 MHz	19.2 kBaud, ±9.9 kHz frequency deviation		48		kHz	Bandwidth where the power envelope of modulation equals –36 dBm. Spectrum analyzer RBW = 1 kHz.
	38.4 kBaud, ±19.8 kHz frequency deviation		106		kHz	
Spurious emission, radiated CW	47 to 74 MHz, 87.5 to 118 MHz, 174 to 230 MHz, 470 to 862 MHz			–54	dBm	At maximum output power, +10/+5 dBm at 433/868 MHz. To comply with EN 300 220, FCC CFR47 part 15 and ARIB STD-T96 an external (antenna) filter, as implemented in the application circuit in Figure 5-22, must be used and tailored to each individual design to reduce out-of-band spurious emission levels. Spurious emissions can be measured as EIRP values according to EN 300 220. The antenna (SMAFF-433 and SMAFF-868 from R.W. Badland) plays a part in attenuating the spurious emissions. If the output power is increased using an external PA, a filter must be used to attenuate spurs below 862 MHz when operating in the 868 MHz frequency band in Europe. Application Note Application Note *AN036 CC1020/1021 Reducing Spurious Emission* (SWRA057) presents and discusses a solution that reduces the TX mode spurious emission close to 862 MHz by increasing the REF_DIV from 1 to 7.
	9 kHz to 1 GHz			–36	dBm	
	1 to 4 GHz			–30	dBm	

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RF Transmit *(continued)*

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER		MIN	TYP	MAX	UNIT	CONDITION
Optimum load impedance	433 MHz		54 + j44		Ω	Transmit mode. For matching details see *Section 5.11*.
	868 MHz		15 + j24		Ω	
	915 MHz		20 + j35		Ω	

4.5 RF Receive

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER		MIN	TYP	MAX	UNIT	CONDITION
Receiver Sensitivity, 433 MHz, FSK	38.4 kHz channel filter BW (1)		–109		dBm	Sensitivity is measured with PN9 sequence at BER = 10^{-3} (1) 38.4 kHz receiver channel filter bandwidth: 4.8 kBaud, NRZ coded data, ±4.95 kHz frequency deviation. (2) 102.4 kHz receiver channel filter bandwidth: 19.2 kBaud, NRZ coded data, ±19.8 kHz frequency deviation. (3) 102.4 kHz receiver channel filter bandwidth: 38.4 kBaud, NRZ coded data, ±19.8 kHz frequency deviation. (4) 307.2 kHz receiver channel filter bandwidth: 153.6 kBaud, NRZ coded data, ±72 kHz frequency deviation. See Table 5-6 and Table 5-7 or typical sensitivity figures at other channel filter bandwidths.
	102.4 kHz channel filter BW (2)		–104		dBm	
	102.4 kHz channel filter BW (3)		–104		dBm	
	307.2 kHz channel filter BW (4)		–96		dBm	
Receiver Sensitivity, 868 MHz, FSK	38.4 kHz channel filter BW (1)		–108		dBm	
	102.4 kHz channel filter BW (2)		–103		dBm	
	102.4 kHz channel filter BW (3)		–103		dBm	
	307.2 kHz channel filter BW (4)		–94		dBm	
Receiver sensitivity, 433 MHz, OOK	9.6 kBaud		–103		dBm	Manchester coded data. See Table 5-14 for typical sensitivity figures at other data rates. Sensitivity is measured with PN9 sequence at BER = 10^{-3}
	153.6 kBaud		–81		dBm	
Receiver sensitivity, 868 MHz, OOK	9.6 kBaud		–104		dBm	
	153.6 kBaud		–87		dBm	
Saturation (maximum input level)	FSK and OOK		10		dBm	FSK: Manchester/NRZ coded data OOK: Manchester coded data BER = 10^{-3}
System noise bandwidth			38.4 to 307.2		kHz	The receiver channel filter 6 dB bandwidth is programmable from 38.4 kHz to 307.2 kHz. See *Section 5.9.2* for details.
Noise figure, cascaded	433 and 868 MHz		7		dB	NRZ coded data
Input IP3(1)	433 MHz, 102.4 kHz channel filter BW		–23		dBm	LNA2 maximum gain
			–18		dBm	LNA2 medium gain
			–16		dBm	LNA2 minimum gain
	868 MHz, 102.4 kHz channel filter BW		–18		dBm	LNA2 maximum gain
			–15		dBm	LNA2 medium gain
			–13		dBm	LNA2 minimum gain
Co-channel rejection, FSK and OOK	433 MHz and 868 MHz, 102.4 kHz channel filter BW		–11		dB	Wanted signal 3 dB above the sensitivity level, CW jammer at operating frequency, BER = 10^{-3}

(1) Two tone test (+10 MHz and +20 MHz)

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RF Receive *(continued)*

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER			MIN	TYP	MAX	UNIT	CONDITION
Adjacent channel rejection (ACR)	433 MHz, 102.4 kHz channel filter BW			32		dB	Measured at ±100 kHz offset. See Figure 5-13 through Figure 5-16. Wanted signal 3 dB above the sensitivity level, CW jammer at adjacent channel, BER = 10^{-3}.
	868 MHz, 102.4 kHz channel filter BW			30		dB	
Image channel rejection	433/868 MHz	No I/Q gain and phase calibration		25/25		dB	Wanted signal 3 dB above the sensitivity level, CW jammer at image frequency, BER = 10^{-3}. 102.4 kHz channel filter bandwidth. See Figure 5-13 through Figure 5-16. Image rejection after calibration will depend on temperature and supply voltage. Refer to *Section 5.9.6*.
		I/Q gain and phase calibrated		50/50		dB	
Selectivity (2)	433 MHz, 102.4 kHz channel filter BW	±200 kHz offset		45		dB	Wanted signal 3 dB above the sensitivity level. CW jammer is swept in 20 kHz steps within ±1 MHz from wanted channel. BER = 10^{-3}. Adjacent channel and image channel are excluded. See Figure 5-13 through Figure 5-16.
		±300 kHz offset		53		dB	
	868 MHz, 102.4 kHz channel filter BW	±200 kHz offset		45		dB	
		±300 kHz offset		50		dB	
Blocking / Desensitization (3)	433/868 MHz	±1 MHz		52/58		dB	Wanted signal 3 dB above the sensitivity level, CW jammer at ±1, 2, 5 and 10 MHz offset, BER = 10^{-3}. 102.4 kHz channel filter bandwidth. Complying with EN 300 220, class 2 receiver requirements.
		±2 MHz		56/64		dB	
		±5 MHz		58/64		dB	
		±10 MHz		64/66		dB	
Image frequency suppression	433/868 MHz	No I/Q gain and phase calibration		35/35		dB	Ratio between sensitivity for a signal at the image frequency to the sensitivity in the wanted channel. Image frequency is RF− 2 IF. BER = 10^{-3}. 102.4 kHz channel filter bandwidth.
		I/Q gain and phase calibrated		60/60		dB	
Spurious rejection			37			dB	Ratio between sensitivity for an unwanted frequency to the sensitivity in the wanted channel. The signal source is swept over all frequencies 100 MHz to 2 GHz. Signal level for BER = 10^{-3}. 102.4 kHz channel filter bandwidth.
LO leakage	433/868 MHz			< –80/–66		dBm	
VCO leakage				–64		dBm	VCO frequency resides between 1608 to 1880 MHz
Spurious emission, radiated CW	9 kHz to 1 GHz			< –60		dBm	Complying with EN 300 220, FCC CFR47 part 15 and ARIB STD-T96. Spurious emissions can be measured as EIRP values according to EN 300 220.
	1 to 4 GHz			< –60		dBm	
Input impedance	433 MHz			58 – j10		Ω	Receive mode. See *Section 5.11* for details.
	868 MHz			54 – j22		Ω	

(2) Close-in spurious response rejection.
(3) Out-of-band spurious response rejection.

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RF Receive *(continued)*

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER		MIN	TYP	MAX	UNIT	CONDITION
Matched input impedance, S11	433 MHz		–14		dB	Using application circuit matching network. See *Section 5.11* for details.
	868 MHz		–12		dB	
Matched input impedance	433 MHz		39 – j14		Ω	Using application circuit matching network. See *Section 5.11* for details.
	868 MHz		32 – j10		Ω	
Bit synchronization offset				8000	ppm	The maximum bit rate offset tolerated by the bit synchronization circuit for 6 dB degradation (synchronous modes only)
Data latency	NRZ mode		4		Baud	Time from clocking the data on the transmitter DIO pin until data is available on receiver DIO pin
	Manchester mode		8		Baud	

4.6 RSSI / Carrier Sense

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER			TYP	UNIT	CONDITION
RSSI dynamic range			55	dB	See *Section 5.9.5* for details.
RSSI accuracy			±3	dB	See *Section 5.9.5* for details.
RSSI linearity			±1	dB	
RSSI attach time	51.2 kHz channel filter BW		730	µs	Shorter RSSI attach times can be traded for lower RSSI accuracy. See *Section 5.9.5* for details. Shorter RSSI attach times can also be traded for reduced sensitivity and selectivity by increasing the receiver channel filter bandwidth.
	102.4 kHz channel filter BW		380	µs	
	307.2 kHz channel filter BW		140	µs	
Carrier sense programmable range			40	dB	Accuracy is as for RSSI
Carrier sense at ±100 kHz and ±200 kHz offset	102.4 kHz channel filter BW, 433 MHz	±100 kHz	–57	dBm	At carrier sense level –98 dBm, CW jammer at ±100 kHz and ±200 kHz offset. Carrier sense is measured by applying a signal at ±100 kHz and ±200 kHz offset and observe at which level carrier sense is indicated.
		±200 kHz	–44	dBm	
	102.4 kHz channel filter BW, 868 MHz	±100 kHz	–60	dBm	
		±200 kHz	–44	dBm	

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4.7 Intermediate Frequency (IF)

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER	TYP	UNIT	CONDITION
Intermediate frequency (IF)	307.2	kHz	See *Section 5.9.1* for details.
Digital channel filter bandwidth	38.4 to 307.2	kHz	The channel filter 6 dB bandwidth is programmable from 9.6 kHz to 307.2 kHz. See *Section 5.9.2* for details.
AFC resolution	1200	Hz	At 19.2 kBaud Given as Baud rate / 16. See *Section 5.9.13* for details.

4.8 Crystal Oscillator

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER		MIN	TYP	MAX	UNIT	CONDITION
Crystal Oscillator Frequency		4.9152	14.7456	19.6608	MHz	Recommended frequency is 14.7456 MHz. See *Section 5.16* for details.
Crystal operation			Parallel			C4 and C5 are loading capacitors. See *Section 5.16* for details.
Crystal load capacitance	4.9 to 6 MHz, 22 pF recommended	12	22	30	pF	
	6 to 8 MHz, 16 pF recommended	12	16	30	pF	
	8 to 19.6 MHz, 16 pF recommended	12	16	16	pF	
Crystal oscillator start-up time	4.9152 MHz, 12 pF load		1.55		ms	
	7.3728 MHz, 12 pF load		1		ms	
	9.8304 MHz, 12 pF load		0.9		ms	
	14.7456 MHz, 16 pF load		0.95		ms	
	17.2032 MHz, 12 pF load		0.6		ms	
	19.6608 MHz, 12 pF load		0.63		ms	
External clock signal drive, sine wave			300		mVpp	The external clock signal must be connected to XOSC_Q1 using a DC block (10 nF). Set XOSC_BYPASS = 0 in the INTERFACE register when using an external clock signal with low amplitude or a crystal.
External clock signal drive, full-swing digital external clock			0 – VDD		V	The external clock signal must be connected to XOSC_Q1. No DC block shall be used. Set XOSC_BYPASS = 1 in the INTERFACE register when using a full-swing digital external clock.

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4.9 Frequency Synthesizer

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER		TYP	UNIT	CONDITION
Phase noise, 402 to 470 MHz	At 12.5 kHz offset from carrier	–79	dBc/Hz	Unmodulated carrier Measured using loop filter components given in Table 6-2. The phase noise will be higher for larger PLL loop filter bandwidth.
	At 25 kHz offset from carrier	–80	dBc/Hz	
	At 50 kHz offset from carrier	–87	dBc/Hz	
	At 100 kHz offset from carrier	–100	dBc/Hz	
	At 1 MHz offset from carrier	–105	dBc/Hz	
Phase noise, 804 to 960 MHz	At 12.5 kHz offset from carrier	–73	dBc/Hz	Unmodulated carrier Measured using loop filter components given in Table 6-2. The phase noise will be higher for larger PLL loop filter bandwidth.
	At 25 kHz offset from carrier	–74	dBc/Hz	
	At 50 kHz offset from carrier	–81	dBc/Hz	
	At 100 kHz offset from carrier	–94	dBc/Hz	
	At 1 MHz offset from carrier	–111	dBc/Hz	
PLL loop filter bandwidth	Loop filter 2, up to 19.2 kBaud	15	kHz	After PLL and VCO calibration. The PLL loop bandwidth is programmable. See Table 5-12 for loop filter component values.
	Loop filter 3, up to 38.4 kBaud	30.5	kHz	
PLL lock time (RX / TX turn time)	Loop filter 2, up to 19.2 kBaud	140	µs	307.2 kHz frequency step to RF frequency within ±10 kHz, ±15 kHz, ±50 kHz settling accuracy for loop filter 2, 3 and 5 respectively. Depends on loop filter component values and PLL_BW register setting. See Table 5-13 for more details.
	Loop filter 3, up to 38.4 kBaud	75	µs	
	Loop filter 5, up to 153.6 kBaud	14	µs	
PLL turn-on time. From power down mode with crystal oscillator running.	Loop filter 2, up to 19.2 kBaud	1300	µs	Time from writing to registers to RF frequency within ±10 kHz, ±15 kHz, ±50 kHz settling accuracy for loop filter 2, 3 and 5 respectively. Depends on loop filter component values and PLL_BW register setting. See Table 5-12 for more details.
	Loop filter 3, up to 38.4 kBaud	1080	µs	
	Loop filter 5, up to 153.6 kBaud	700	µs	

4.10 Digital Inputs / Outputs

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Logic "0" input voltage	0		0.3 × VDD	V	
Logic "1" input voltage	0.7 × VDD		VDD	V	
Logic "0" output voltage	0		0.4	V	Output current –2.0 mA, 3.0 V supply voltage
Logic "1" output voltage	2.5		VDD	V	Output current 2.0 mA, 3.0 V supply voltage
Logic "0" input current	N/A		–1	µA	Input signal equals GND. PSEL has an internal pullup resistor and during configuration the current will be –350 mA.
Logic "1" input current	N/A		1	µA	Input signal equals VDD
DIO setup time	20			ns	TX mode, minimum time DIO must be ready before the positive edge of DCLK. Data should be set up on the negative edge of DCLK.

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Digital Inputs / Outputs *(continued)*

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER			MIN	TYP	MAX	UNIT	CONDITION
DIO hold time			10			ns	TX mode, minimum time DIO must be held after the positive edge of DCLK. Data should be set up on the negative edge of DCLK.
Serial interface (PCLK, PDI, PDO and PSEL) timing specification							See Table 5-1 for more details
Pin drive, LNA_EN, PA_EN	Source current	0 V on LNA_EN, PA_EN pins		0.90		mA	See Figure 5-32 for more details.
		0.5 V on LNA_EN, PA_EN pins		0.87		mA	
		1.0 V on LNA_EN, PA_EN pins		0.81		mA	
		1.5 V on LNA_EN, PA_EN pins		0.69		mA	
	Sink current	3.0 V on LNA_EN, PA_EN pins		0.93		mA	
		2.5 V on LNA_EN, PA_EN pins		0.92		mA	
		2.0 V on LNA_EN, PA_EN pins		0.89		mA	
		1.5 V on LNA_EN, PA_EN pins		0.79		mA	

4.11 Current Consumption

All measurements were performed using the two-layer PCB CC1020EMX reference design. See Figure 6-1. The electrical specifications given for 868 MHz are also applicable for 902 to 928 MHz. T_A = 25°C, AVDD = DVDD = 3.0 V, f_C = 14.7456 MHz if nothing else stated.

PARAMETER		MIN	TYP	MAX	UNIT	CONDITION
Power Down mode			0.2	1.8	µA	Oscillator core off
Current Consumption, receive mode 433 and 868 MHz			19.9		mA	
Current Consumption, transmit mode 433/868 MHz	P = –20 dBm		12.3/14.5		mA	The output power is delivered to a 50 Ω single-ended load. See *Section 5.10.2* for more details.
	P = –5 dBm		14.4/17.0		mA	
	P = 0 dBm		16.2/20.5		mA	
	P = +5 dBm		20.5/25.1		mA	
	P = +10 dBm (433 MHz only)		27.1		mA	
Current Consumption, crystal oscillator			77		µA	14.7456 MHz, 16 pF load crystal
Current Consumption, crystal oscillator and bias			500		µA	14.7456 MHz, 16 pF load crystal
Current Consumption, crystal oscillator, bias and synthesizer			7.5		mA	14.7456 MHz, 16 pF load crystal

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4.12 Thermal Resistance Characteristics for *VQFNP* Package

NAME	DESCRIPTION	°C/W(1) (2)
$R_{\theta JC(top)}$	Junction-to-case (top)	16.2
$R_{\theta JB}$	Junction-to-board	6.9
$R_{\theta JA}$	Junction-to-free air	30.7
Psi_{JT}	Junction-to-package top	0.2
Psi_{JB}	Junction-to-board	6.9
$R_{\theta JC(bottom)}$	Junction-to-case (bottom)	1.0

(1) °C/W = degrees Celsius per watt.

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70ºC is assumed.

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5 Detailed Description

5.1 Overview

A simplified block diagram of CC1021 is shown in Figure 5-1. Only signal pins are shown.

CC1021 features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA and LNA2) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signal is complex filtered and amplified, and then digitized by the ADCs. Automatic gain control, fine channel filtering, demodulation and bit synchronization is performed digitally. CC1021 outputs the digital demodulated data on the DIO pin. A synchronized data clock is available at the DCLK pin. RSSI is available in digital format and can be read via the serial interface. The RSSI also features a programmable carrier sense indicator.

In transmit mode, the synthesized RF frequency is fed directly to the power amplifier (PA). The RF output is frequency shift keyed (FSK) by the digital bit stream that is fed to the DIO pin. Optionally, a Gaussian filter can be used to obtain Gaussian FSK (GFSK).

The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase splitter for generating the LO_I and LO_Q signals to the down-conversion mixers in receive mode. The VCO operates in the frequency range 1.608 to 1.880 GHz. The CHP_OUT pin is the charge pump output and VC is the control node of the on-chip VCO. The external loop filter is placed between these pins. A crystal is to be connected between XOSC_Q1 and XOSC_Q2. A lock signal is available from the PLL.

The 4-wire SPI serial interface is used for configuration.

5.2 Functional Block Diagram

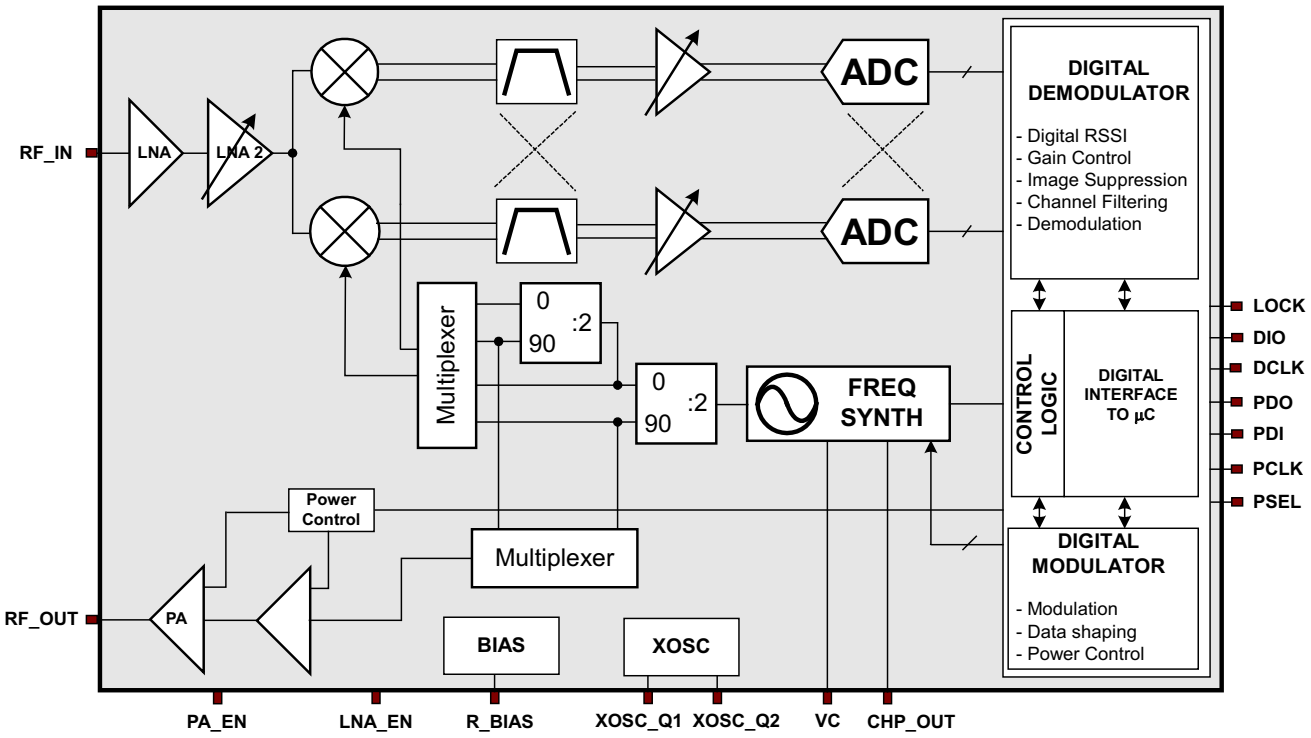

Figure 5-1. CC1021 Simplified Block Diagram

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5.3 Configuration Overview

CC1021 can be configured to achieve the optimum performance for different applications. Through the programmable configuration registers the following key parameters can be programmed:

- Receive / transmit mode
- RF output power
- Frequency synthesizer key parameters:
  - RF output frequency
  - FSK frequency separation
  - Crystal oscillator reference frequency
- Power-down / power-up mode
- Crystal oscillator power up or power down
- Data rate and data format (NRZ, Manchester coded or UART interface)
- Synthesizer lock indicator mode
- Digital RSSI and carrier sense
- FSK / GFSK / OOK modulation

5.3.1 Configuration Software

TI provides users of CC1021 with a software program, SmartRF Studio (Windows interface) that generates all necessary CC1021 configuration data based on the user's selections of various parameters. These hexadecimal numbers will then be the necessary input to the microcontroller for the configuration of CC1021. In addition, the program will provide the user with the component values needed for the input/output matching circuit, the PLL loop filter and the LC filter.

Figure 5-2 shows the user interface of the CC1021 configuration software.

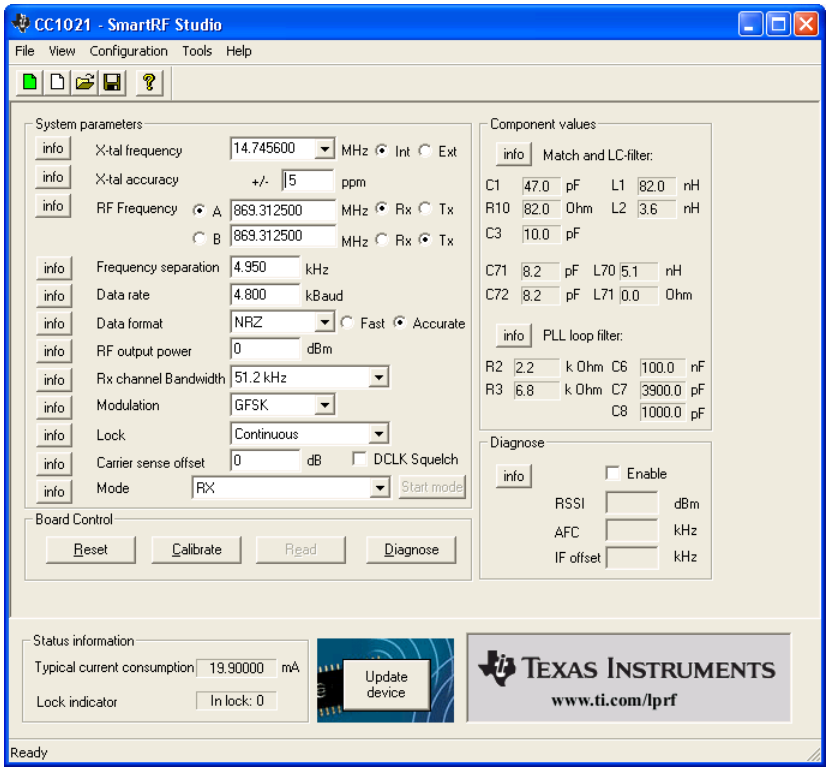

Figure 5-2. SmartRF™ Studio User Interface

NOTE

The CC1020/1070DK Development Kit with a fully assembled CC1020EMX Evaluation Module together with the CC1021 specific software should be used for evaluation of the CC1021 transceiver.

5.4 Microcontroller Interface

Used in a typical system, CC1021 will interface to a microcontroller. This microcontroller must be able to:

- Program CC1021 into different modes via the 4-wire serial configuration interface (PDI, PDO, PCLK and PSEL)
- Interface to the bi-directional synchronous data signal interface (DIO and DCLK)
- Optionally, the microcontroller can do data encoding / decoding
- Optionally, the microcontroller can monitor the LOCK pin for frequency lock status, carrier sense status or other status information.
- Optionally, the microcontroller can read back the digital RSSI value and other status information via the 4-wire serial interface.

5.4.1 Configuration Interface

The microcontroller interface is shown in Figure 5-3. The microcontroller uses 3 or 4 I/O pins for the configuration interface (PDI, PDO, PCLK and PSEL). PDO should be connected to a microcontroller input. PDI, PCLK and PSEL must be microcontroller outputs. One I/O pin can be saved if PDI and PDO are connected together and a bi-directional pin is used at the microcontroller.

The microcontroller pins connected to PDI, PDO and PCLK can be used for other purposes when the configuration interface is not used. PDI, PDO and PCLK are high impedance inputs as long as PSEL is not activated (active low).

PSEL has an internal pullup resistor and should be left open (tri-stated by the microcontroller) or set to a high level during power down mode in order to prevent a trickle current flowing in the pullup.

5.4.2 Signal Interface

A bi-directional pin is usually used for data (DIO) to be transmitted and data received. DCLK providing the data timing should be connected to a microcontroller input.

As an option, the data output in receive mode can be made available on a separate pin. See *Section 5.6* further details.

5.4.3 PLL Lock Signal

Optionally, one microcontroller pin can be used to monitor the LOCK signal. This signal is at low logic level when the PLL is in lock. It can also be used for carrier sense and to monitor other internal test signals.

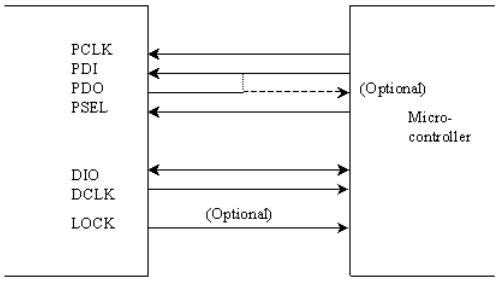

Figure 5-3. Microcontroller Interface

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5.5 4-wire Serial Configuration Interface

CC1021 is configured via a simple 4-wire SPI-compatible interface (PDI, PDO, PCLK and PSEL) where CC1021 is the slave. There are 8-bit configuration registers, each addressed by a 7-bit address. A Read/Write bit initiates a read or write operation. A full configuration of CC1021 requires sending 33 data frames of 16 bits each (7 address bits, R/W bit and 8 data bits). The time needed for a full configuration depends on the PCLK frequency. With a PCLK frequency of 10 MHz the full configuration is done in less than 53 ms. Setting the device in power down mode requires sending one frame only and will in this case take less than 2 ms. All registers are also readable.

During each write-cycle, 16 bits are sent on the PDI-line. The seven most significant bits of each data frame (A6:0) are the address-bits. A6 is the MSB (Most Significant Bit) of the address and is sent as the first bit. The next bit is the R/W bit (high for write, low for read). The 8 data-bits are then transferred (D7:0). During address and data transfer the PSEL (Program SELect) must be kept low. See Figure 5-4.

The timing for the programming is also shown in Figure 5-4 with reference to Table 5-1. The clocking of the data on PDI is done on the positive edge of PCLK. Data should be set up on the negative edge of PCLK by the microcontroller. When the last bit, D0, of the 8 data-bits has been loaded, the data word is loaded into the internal configuration register.

The configuration data will be retained during a programmed power down mode, but not when the power supply is turned off. The registers can be programmed in any order.

The configuration registers can also be read by the microcontroller via the same configuration interface. The seven address bits are sent first, then the R/W bit set low to initiate the data read-back. CC1021 then returns the data from the addressed register. PDO is used as the data output and must be configured as an input by the microcontroller. The PDO is set at the negative edge of PCLK and should be sampled at the positive edge. The read operation is illustrated in Figure 5-5.

PSEL must be set high between each read/write operation.

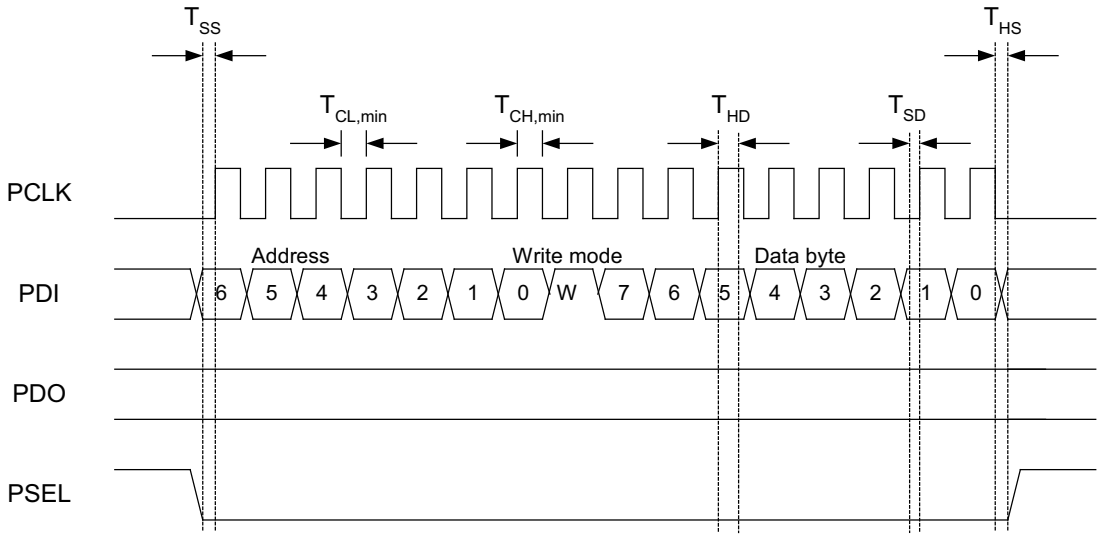

Figure 5-4. Configuration Registers Write Operation

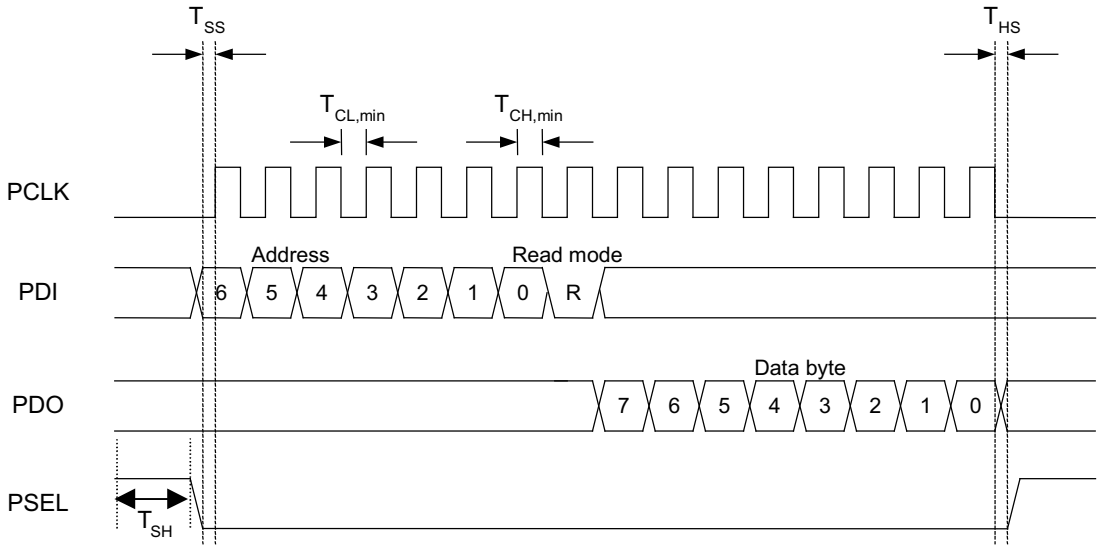

Figure 5-5. Configuration Registers Read Operation

Table 5-1. Serial Interface, Timing Specification(1)

PARAMETER		MIN	MAX	UNIT	CONDITIONS
F_{PCLK}	PCLK, clock frequency		10	MHz	
$T_{CL,min}$	PCLK low pulse duration	50		ns	The minimum time PCLK must be low.
$T_{CH,min}$	PCLK high pulse duration	50		ns	The minimum time PCLK must be high.
T_{SS}	PSEL setup time	25		ns	The minimum time PSEL must be low before positive edge of PCLK.
T_{HS}	PSEL hold time	25		ns	The minimum time PSEL must be held low after the negative edge of PCLK.
T_{SH}	PSEL high time	50		ns	The minimum time PSEL must be high.
T_{SD}	PDI setup time	25		ns	The minimum time data on PDI must be ready before the positive edge of PCLK.
T_{HD}	PDI hold time	25		ns	The minimum time data must be held at PDI, after the positive edge of PCLK.
T_{rise}	Rise time		100	ns	The maximum rise time for PCLK and PSEL
T_{fall}	Fall time		100	ns	The maximum fall time for PCLK and PSEL

(1) The setup and hold times refer to 50% of VDD. The rise and fall times refer to 10% / 90% of VDD. The maximum load that this table is valid for is 20 pF.

5.6 Signal Interface

The CC1021 can be used with NRZ (Non-Return-to-Zero) data or Manchester (also known as bi-phase-level) encoded data. CC1021 can also synchronize the data from the demodulator and provide the data clock at DCLK. The data format is controlled by the DATA_FORMAT[1:0] bits in the MODEM register.

CC1021 can be configured for three different data formats:

- Synchronous NRZ mode
- Transparent Asynchronous UART mode
- Synchronous Manchester encoded mode

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5.6.1 Synchronous NRZ Mode

In transmit mode CC1021 provides the data clock at DCLK and DIO is used as data input. Data is clocked into CC1021 at the rising edge of DCLK. The data is modulated at RF without encoding.

In receive mode CC1021 performs the synchronization and provides received data clock at DCLK and data at DIO. The data should be clocked into the interfacing circuit at the rising edge of DCLK. See Figure 5-6.

5.6.2 Transparent Asynchronous UART Mode

In transmit mode, DIO is used as data input. The data is modulated at RF without synchronization or encoding.

In receive mode, the raw data signal from the demodulator is sent to the output (DIO). No synchronization or decoding of the signal is done in CC1021 and should be done by the interfacing circuit.

If SEP_DI_DO = 0 in the INTERFACE register, the DIO pin is the data output in receive mode and data input in transmit mode. The DCLK pin is not active and can be set to a high or low level by DATA_FORMAT[0].

If SEP_DI_DO = 1 in the INTERFACE register, the DCLK pin is the data output in receive mode and the DIO pin is the data input in transmit mode. In TX mode the DCLK pin is not active and can be set to a high or low level by DATA_FORMAT[0]. See Figure 5-8.

5.6.3 Synchronous Manchester Encoded Mode

In transmit mode CC1021 provides the data clock at DCLK and DIO is used as data input. Data is clocked into CC1021 at the rising edge of DCLK and should be in NRZ format. The data is modulated at RF with Manchester code. The encoding is done by CC1021. In this mode the effective bit rate is half the baud rate due to the coding. As an example, 19.2 kBaud Manchester encoded data corresponds to 9.6 kbps.

In receive mode CC102 performs the synchronization and provides received data clock at DCLK and data at DIO. CC1021 performs the decoding and NRZ data is presented at DIO. The data should be clocked into the interfacing circuit at the rising edge of DCLK. See Figure 5-7.

In synchronous NRZ or Manchester mode the DCLK signal runs continuously both in RX and TX unless the DCLK signal is gated with the carrier sense signal or the PLL lock signal. Refer to *Section 5.18* for more details.

If SEP_DI_DO = 0 in the INTERFACE register, the DIO pin is the data output in receive mode and data input in transmit mode.

As an option, the data output can be made available at a separate pin. This is done by setting SEP_DI_DO = 1 in the INTERFACE register. Then, the LOCK pin will be used as data output in synchronous mode, overriding other use of the LOCK pin.

5.6.3.1 Manchester Encoding and Decoding

In the Synchronous Manchester encoded mode CC1021 uses Manchester coding when modulating the data. The CC1021 also performs the data decoding and synchronization. The Manchester code is based on transitions; a “0” is encoded as a low-to-high transition, a “1” is encoded as a high-to-low transition. See Figure 5-7.

The Manchester code ensures that the signal has a constant DC component, which is necessary in some FSK demodulators. Using this mode also ensures compatibility with CC400 and CC900 designs.

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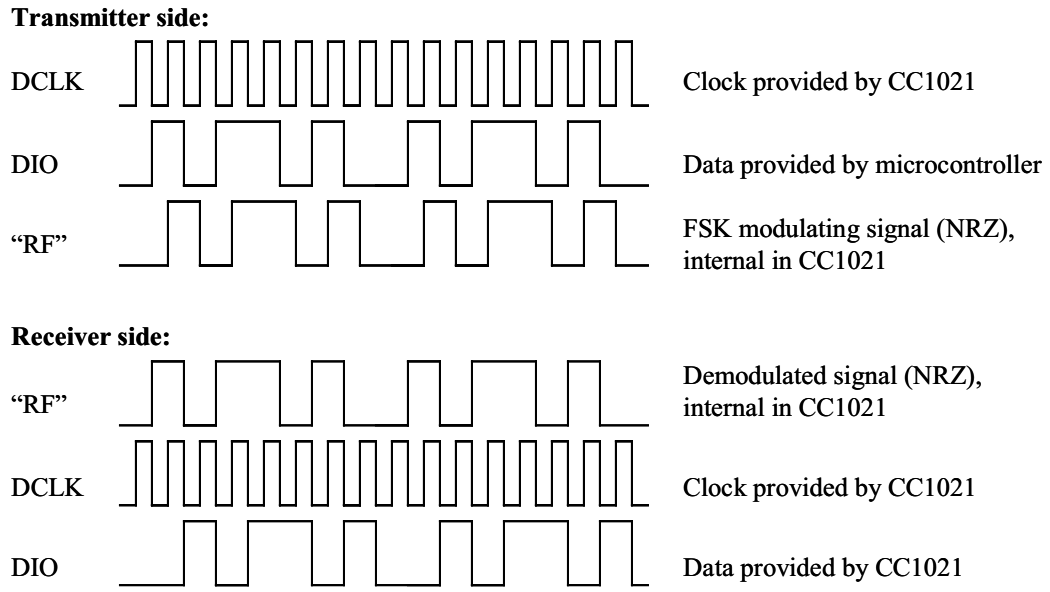

Figure 5-6. Synchronous NRZ Mode (SEP_DI_DO = 0)

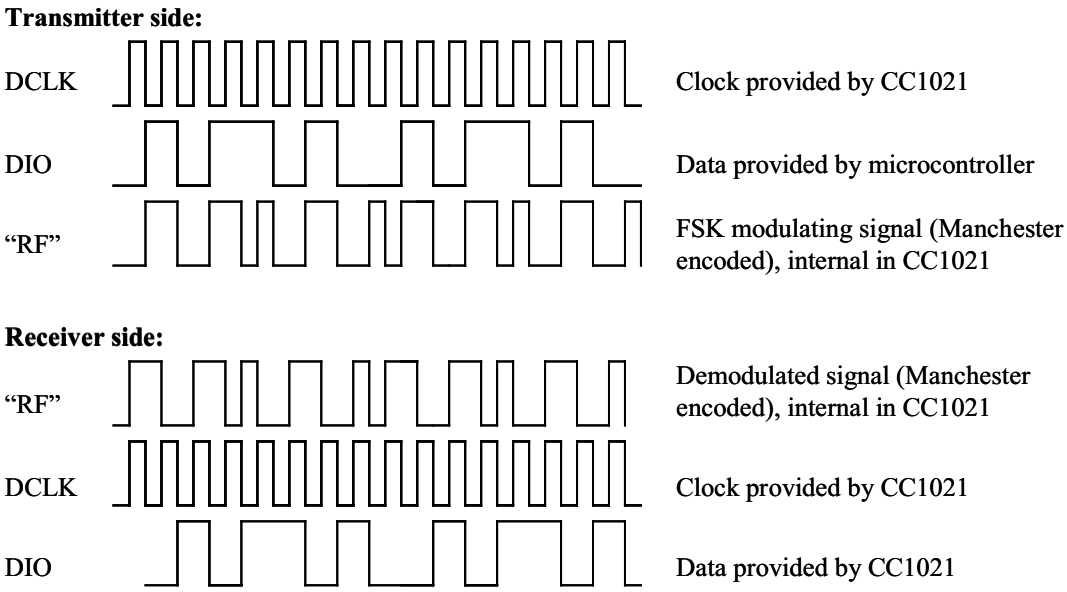

Figure 5-7. Synchronous Manchester Encoded Mode (SEP_DI_DO = 0)

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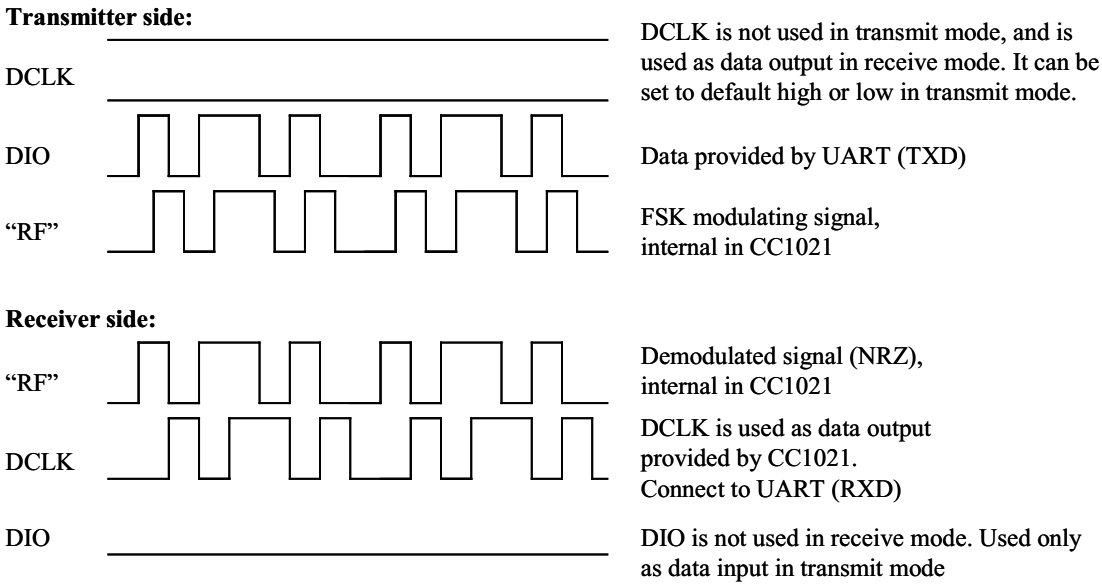

Figure 5-8. Transparent Asynchronous UART Mode (SEP_DI_DO = 1)

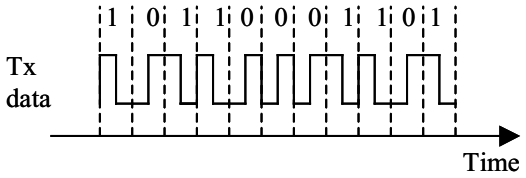

Figure 5-9. Manchester Encoding

5.7 Data Rate Programming

The data rate (baud rate) is programmable and depends on the crystal frequency and the programming of the CLOCK (CLOCK_A and CLOCK_B) registers.

The baud rate (B.R.) is given by Equation 1.

$$B.R. = \frac{f_{xosc}}{8 \times (REF_DIV + 1) \times DIV1 \times DIV2} \quad (1)$$

Where:

DIV1 and DIV2 are given by the value of MCLK_DIV1 and MCLK_DIV2.

Table 5-4 shows some possible data rates as a function of crystal frequency in synchronous mode. In asynchronous transparent UART mode any data rate up to 153.6 kBaud can be used.

Table 5-2. DIV2 for Different Settings of MCLK_DIV2

MCLK_DIV2[1:0]	DIV2
00	1
01	2
10	4
11	8

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Table 5-3. DIV1 for Different Settings of MCLK_DIV1

MCLK_DIV1[2:0]	DIV1
000	2.5
001	3
010	4
011	7.5
100	12.5
101	40
110	48
111	64

Table 5-4. Some Possible Data Rates Versus Crystal Frequency

DATA RATE [kBaud]	CRYSTAL FREQUENCY [MHz]						
	4.9152	7.3728	9.8304	12.288	14.7456	17.2032	19.6608
0.45		X			X		
0.5				X			
0.6	X	X	X	X	X	X	X
0.9		X			X		
1				X			
1.2	X	X	X	X	X	X	X
1.8		X			X		
2				X			
2.4	X	X	X	X	X	X	X
3.6		X			X		
4				X			
4.096			X				X
4.8	X	X	X	X	X	X	X
7.2		X			X		
8				X			
8.192			X				X
9.6	X	X	X	X	X	X	X
14.4		X			X		
16				X			
16.384			X				X
19.2	X	X	X	X	X	X	X
28.8		X			X		
32				X			
32.768			X				X
38.4	X	X	X	X	X	X	X
57.6		X			X		
64				X			
65.536							X
76.8	X	X	X	X	X	X	X
115.2		X			X		
128				X			
153.6		X		X	X	X	X

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5.8 Frequency Programming

Programming the frequency word in the configuration registers sets the operation frequency. There are two frequency words registers, termed FREQ_A and FREQ_B, which can be programmed to two different frequencies. One of the frequency words can be used for RX (local oscillator frequency) and the other for TX (transmitting carrier frequency) in order to be able to switch very fast between RX mode and TX mode. They can also be used for RX (or TX) at two different channels. The F_REG bit in the MAIN register selects frequency word A or B.

The frequency word is located in FREQ_2A:FREQ_1A:FREQ_0A and FREQ_2B:FREQ_1B:FREQ_0B for the FREQ_A and FREQ_B word respectively. The LSB of the FREQ_0 registers are used to enable dithering (see *Section 5.8.1*).

The PLL output frequency is given by Equation 2 in the frequency band 402 to 470 MHz, and by Equation 3 in the frequency band 804 to 960 MHz.

$$f_c = f_{ref} \times \left(\frac{3}{4} + \frac{FREQ + 0.5 \times DITHER}{32768} \right) \quad (2)$$

$$f_c = f_{ref} \times \left(\frac{3}{2} + \frac{FREQ + 0.5 \times DITHER}{16384} \right) \quad (3)$$

The BANDSELECT bit in the ANALOG register controls the frequency band used. BANDSELECT = 0 gives 402 to 470 MHz, and BANDSELECT = 1 gives 804 to 960 MHz.

The reference frequency is the crystal oscillator clock frequency divided by REF_DIV (3 bits in the CLOCK_A or CLOCK_B register), a number between 1 and 7, as shown in Equation 4.

$$f_{ref} = \frac{f_{xosc}}{REF_DIV + 1} \quad (4)$$

FSK frequency deviation is programmed in the DEVIATION register. The deviation programming is divided into a mantissa (TXDEV_M[3:0]) and an exponent (TXDEV_X[2:0]).

Generally REF_DIV should be as low as possible, but the requirements shown in Equation 5 must be met in the frequency band 402 to 470 MHz.

$$9.8304 \geq f_{ref} > \frac{f_c}{256} \text{ [MHz]} \quad (5)$$

The requirements shown in Equation 6 must be met in the frequency band 804 to 960 MHz.

$$9.8304 \geq f_{ref} > \frac{f_c}{512} \text{ [MHz]} \quad (6)$$

The PLL output frequency equations give the carrier frequency, f_c , in transmit mode (centre frequency). The two FSK modulation frequencies are given by Equation 7 and Equation 8.

$$f_0 = f_c - f_{dev} \quad (7)$$

$$f_1 = f_c + f_{dev} \quad (8)$$

Where:

f_{dev} is set by the DEVIATION register.

f_{dev} is set by the DEVIATION register shown in Equation 9 in the frequency band 402 to 470 MHz.

$$f_{dev} = f_{ref} \times TXDEV_M \times 2^{(TXDEV_X - 16)} \quad (9)$$

f_{dev} is set by the DEVIATION register shown in Equation 10 in the frequency band 804 to 960 MHz.

$$f_{dev} = f_{ref} \times TXDEV_M \times 2^{(TXDEV_X - 15)} \quad (10)$$

OOK (On-Off Keying) is used if TXDEV_M[3:0] = 0000.

The TX_SHAPING bit in the DEVIATION register controls Gaussian shaping of the modulation signal.

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In receive mode the frequency must be programmed to be the LO frequency. Low side LO injection is used, hence Equation 11.

$$f_{LO} = f_c - f_{IF} \quad (11)$$

Where:

f_{IF} is the IF frequency (ideally 307.2 kHz).

5.8.1 Dithering

Spurious signals will occur at certain frequencies depending on the division ratios in the PLL. To reduce the strength of these spurs, a common technique is to use a dithering signal in the control of the frequency dividers. Dithering is activated by setting the DITHER bit in the FREQ_0 registers. It is recommended to use the dithering in order to achieve the best possible performance.

5.9 Receiver

5.9.1 IF Frequency

The IF frequency is derived from the crystal frequency as shown in Equation 12.

$$f_{IF} = \frac{f_{xoscx}}{8 \times (ADC_DIV[2:0] + 1)} \quad (12)$$

Where:

ADC_DIV[2:0] is set in the MODEM register.

The analog filter succeeding the mixer is used for wideband and anti-alias filtering which is important for the blocking performance at 1 MHz and larger offsets. This filter is fixed and centered on the nominal IF frequency of 307.2 kHz. The bandwidth of the analog filter is about 160 kHz.

Using crystal frequencies which gives an IF frequency within 300 to 320 kHz means that the analog filter can be used (assuming low frequency deviations and low data rates).

Large offsets, however, from the nominal IF frequency will give an un-symmetric filtering (variation in group delay and different attenuation) of the signal, resulting in decreased sensitivity and selectivity. See Application Note *AN022 Crystal Frequency Selection* (SWRA070) for more details.

For IF frequencies other than 300 to 320 kHz and for high frequency deviation and high data rates (typically ≥ 76.8 kBaud) the analog filter must be bypassed by setting FILTER_BYPASS = 1 in the FILTER register. In this case the blocking performance at 1 MHz and larger offsets will be degraded.

The IF frequency is always the ADC clock frequency divided by 4. The ADC clock frequency should therefore be as close to 1.2288 MHz as possible.

5.9.2 Receiver Channel Filter Bandwidth

In order to meet different channel spacing requirements, the receiver channel filter bandwidth is programmable. It can be programmed from 38.4 to 307.2 kHz.

The minimum receiver channel filter bandwidth depends on data rate, frequency separation and crystal tolerance.

The signal bandwidth must be smaller than the available receiver channel filter bandwidth. The signal bandwidth (SBW) can be approximated by (Carson's rule) as shown in Equation 13.

$$SBW = 2 \times f_m + 2 \times \text{frequency deviation} \quad (13)$$

Where:

f_m is the modulating signal.

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In Manchester mode the maximum modulating signal occurs when transmitting a continuous sequence of 0s (or 1s). In NRZ mode the maximum modulating signal occurs when transmitting a 0-1-0 sequence. In both Manchester and NRZ mode $2 \times f_m$ is then equal to the programmed baud rate. The equation for SBW can then be rewritten as shown in Equation 14.

SBW = Baud rate + frequency separation (14)

Furthermore, the frequency offset of the transmitter and receiver must also be considered. Assuming equal frequency error in the transmitter and receiver (same type of crystal) the total frequency error is shown in Equation 15.

f_error = ±2 × XTAL_ppm × f_RF (15)

Where:

XTAL_ppm is the total accuracy of the crystal including initial tolerance, temperature drift, loading and ageing.

f_RF is the RF operating frequency.

The minimum receiver channel filter bandwidth (ChBW) can then be estimated as shown in Equation 16.

ChBW > SBW + 2 × f_error (16)

The DEC_DIV[2:0] bits in the FILTER register control the receiver channel filter bandwidth. The 6 dB bandwidth is given by Equation 17.

$$\text{ChBW} = \frac{307.2}{(\text{DEC_DIV} + 1)} \text{ [kHz]} \quad (17)$$

Where:

The IF frequency is set to 307.2 kHz.

Table 5-5 shows the available channel filter bandwidths.

There is a tradeoff between selectivity as well as sensitivity and accepted frequency tolerance. In applications where larger frequency drift is expected, the filter bandwidth can be increased, but with reduced adjacent channel rejection (ACR) and sensitivity.

Table 5-5. Channel Filter Bandwidth

FILTER BANDWIDTH [kHz]	FILTER.DEC_DIV[2:0] [decimal(binary)]
38.4	7 (111b)
43.9	6 (110b)
51.2	5 (101b)
61.4	4 (100b)
76.8	3 (011b)
102.4	2 (010b)
153.6	1 (001b)
307.2	0 (000b)

5.9.3 Demodulator, Bit Synchronizer and Data Decision

The block diagram for the demodulator, data slicer and bit synchronizer is shown in Figure 5-10. The built-in bit synchronizer synchronizes the internal clock to the incoming data and performs data decoding. The data decision is done using over-sampling and digital filtering of the incoming signal. This improves the reliability of the data transmission. Using the synchronous modes simplifies the data-decoding task substantially.

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The recommended preamble is a '010101…' bit pattern. The same bit pattern should also be used in Manchester mode, giving a '011001100110…'chip' pattern. This is necessary for the bit synchronizer to synchronize to the coding correctly.

The data slicer does the bit decision. Ideally the two received FSK frequencies are placed symmetrically around the IF frequency. However, if there is some frequency error between the transmitter and the receiver, the bit decision level should be adjusted accordingly. In CC1021 this is done automatically by measuring the two frequencies and use the average value as the decision level.

The digital data slicer in CC1021 uses an average value of the minimum and maximum frequency deviation detected as the comparison level. The RXDEV_X[1:0] and RXDEV_M[3:0] in the AFC_CONTROL register are used to set the expected deviation of the incoming signal. Once a shift in the received frequency larger than the expected deviation is detected, a bit transition is recorded and the average value to be used by the data slicer is calculated.

The minimum number of transitions required to calculate a slicing level is 3. That is, a 010 bit pattern (NRZ).

The actual number of bits used for the averaging can be increased for better data decision accuracy. This is controlled by the SETTLING[1:0] bits in the AFC_CONTROL register. If RX data is present in the channel when the RX chain is turned on, then the data slicing estimate will usually give correct results after 3 bit transitions. The data slicing accuracy will increase after this, depending on the SETTLING[1:0] bits. If the start of transmission occurs after the RX chain has turned on, the minimum number of bit transitions (or preamble bits) before correct data slicing will depend on the SETTLING[1:0] bits.

The automatic data slicer average value function can be disabled by setting SETTLING[1:0] = 00. In this case a symmetrical signal around the IF frequency is assumed.

The internally calculated average FSK frequency value gives a measure for the frequency offset of the receiver compared to the transmitter. This information can also be used for an automatic frequency control (AFC) as described in *Section 5.9.13*.

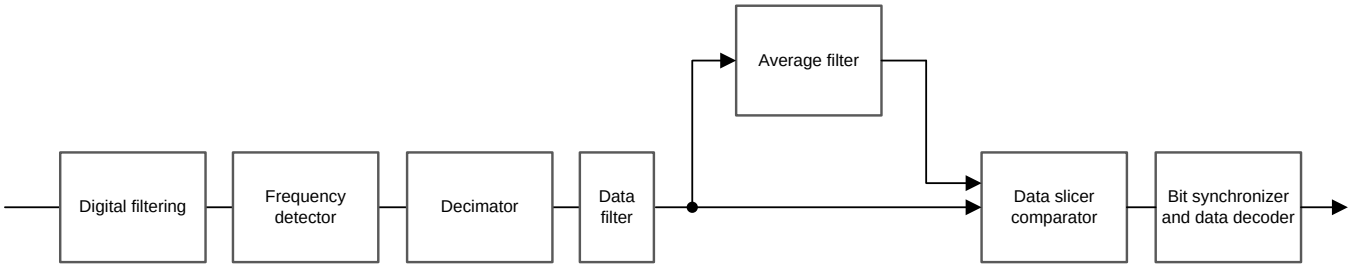

Figure 5-10. Demodulator Block Diagram

5.9.4 Receiver Sensitivity versus Data Rate and Frequency Separation

The receiver sensitivity depends on the channel filter bandwidth, data rate, data format, FSK frequency separation and the RF frequency. Typical figures for the receiver sensitivity (BER = 10^{-3}) are shown in Table 5-6 and Table 5-7 for FSK. For best performance, the frequency deviation should be at least half the baud rate in FSK mode.

The sensitivity is measured using the matching network shown in the application circuit in Figure 6-1, which includes an external T/R switch.

Refer to Application Note *AN029 CC1020/1021 Automatic Frequency Control (AFC)* (SWRA063) for plots of sensitivity versus frequency offset.

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Table 5-6. Typical Receiver Sensitivity as a Function of Data Rate at 433 MHz, FSK Modulation, BER = 10^{-3}, Pseudo-Random Data (PN9 Sequence)

DATA RATE [kBaud]	DEVIATION [kHz]	FILTER BW [kHz]	SENSITIVITY [dBm]		
			NRZ MODE	MANCHESTER MODE	UART MODE
4.8	±4.95	38.4	–109	–112	–109
19.2	±9.9	51.2	–107	–108	–107
19.2	±19.8	102.4	–104	–106	–104
38.4	±19.8	102.4	–104	–104	–104
76.8	±36.0	153.6	–101	–101	–101
153.6	±72.0	307.2	–96	–97	–96

Table 5-7. Typical Receiver Sensitivity as a Function of Data Rate at 868 MHz, FSK Modulation, BER = 10^{-3}, Pseudo-Random Data (PN9 Sequence)

DATA RATE [kBaud]	DEVIATION [kHz]	FILTER BW [kHz]	SENSITIVITY [dBm]		
			NRZ MODE	MANCHESTER MODE	UART MODE
4.8	±4.95	38.4	–108	–111	–108
19.2	±9.9	51.2	–107	–107	–107
19.2	±19.8	102.4	–103	–106	–103
38.4	±19.8	102.4	–103	–103	–103
76.8	±36.0	153.6	–99	–100	–99
153.6	±72.0	307.2	–94	–94	–94

5.9.5 RSSI

CC1021 has a built-in RSSI (Received Signal Strength Indicator) giving a digital value that can be read form the RSSI register. The RSSI reading must be offset and adjusted for VGA gain setting (VGA_SETTING[4:0] in the VGA3 register).

The digital RSSI value is ranging from 0 to 106 (7 bits).

The RSSI reading is a logarithmic measure of the average voltage amplitude after the digital filter in the digital part of the IF chain as shown in Equation 18.

$$RSSI = 4 \log_2 (\text{signal amplitude}) \quad (18)$$

The relative power is then given by RSSI × 1.5 dB in a logarithmic scale.

The number of samples used to calculate the average signal amplitude is controlled by AGC_AVG[1:0] in the VGA2 register. The RSSI update rate is given by Equation 19.

$$f_{RSSI} = \frac{f_{filter_clock}}{2^{AGC_AVG[1:0]+1}} \quad (19)$$

Where:

AGC_AVG[1:0] is set in the VGA2 register.

f_{filter_clock} = 2 × ChBW.

Maximum VGA gain is programmed by the VGA_SETTING[4:0] bits. The VGA gain is programmed in approximately 3 dB/LSB. The RSSI measurement can be referred to the power (absolute value) at the RF_IN pin by using Equation 20.

$$P = 1.5 \times RSSI - 3 \times VGA_SETTING - RSSI_Offset \text{ [dBm]} \quad (20)$$

The RSSI_Offset depends on the channel filter bandwidth used due to different VGA settings. Figure 5-11 and Figure 5-12 show typical plots of RSSI reading as a function of input power for different channel filter bandwidths. Refer to Application Note *AN030 CC1020/1021 Received Signal Strength Indicator* (SWRA062) for further details.

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Equation 21 can be used to calculate the power, P, in dBm from the RSSI readout values in Figure 5-11 and Figure 5-12.

$$P = 1.5 \times [RSSI - RSSI_ref] + P_ref \quad (21)$$

Where:

P is the output power in dBm for the current RSSI readout value.

RSSI_ref is the RSSI readout value taken from Figure 5-11 or Figure 5-12 for an input power level of P_ref.

NOTE

The RSSI readings in decimal value changes for different channel filter bandwidths.

The analog filter has a finite dynamic range and is the reason why the RSSI reading is saturated at lower channel filter bandwidths. Higher channel filter bandwidths are typically used for high frequency deviation and data rates. The analog filter bandwidth is about 160 kHz and is bypassed for high frequency deviation and data rates and is the reason why the RSSI reading is not saturated for 153.6 kHz and 307.2 kHz channel filter bandwidths in Figure 5-11 and Figure 5-12.

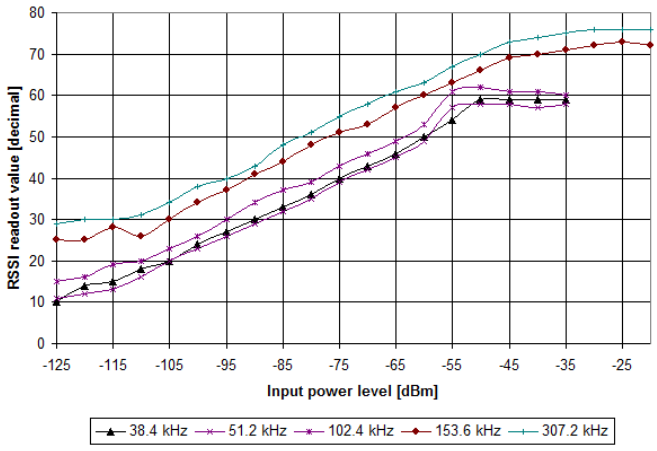

Figure 5-11. Typical RSSI Value vs Input Power for Different Channel Filter Bandwidths, 433 MHz

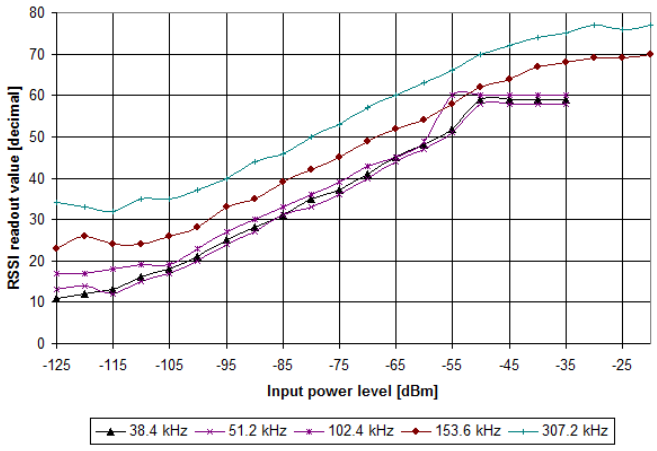

Figure 5-12. Typical RSSI Value vs Input Power for Different Channel Filter Bandwidths, 868 MHz

5.9.6 Image Rejection Calibration

For perfect image rejection, the phase and gain of the “I” and “Q” parts of the analog RX chain must be perfectly matched. To improve the image rejection, the “I” and “Q” phase and gain difference can be fine-tuned by adjusting the PHASE_COMP and GAIN_COMP registers. This allows compensation for process variations and other nonidealities. The calibration is done by injecting a signal at the image frequency, and adjusting the phase and gain difference for minimum RSSI value.

During image rejection calibration, an unmodulated carrier should be applied at the image frequency (614.4 kHz below the desired channel), No signal should be present in the desired channel. The signal level should be 50 to 60 dB above the sensitivity in the desired channel, but the optimum level will vary from application to application. Too large input level gives poor results due to limited linearity in the analog IF chain, while too low input level gives poor results due to the receiver noise floor.

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For best RSSI accuracy, use AGC_AVG(1:0] = 11 during image rejection calibration (RSSI value is averaged over 16 filter output samples). The RSSI register update rate then equals the receiver channel bandwidth (set in FILTER register) divided by 8, as the filter output rate is twice the receiver channel bandwidth. This gives the minimum waiting time between RSSI register reads (0.5 ms is used below). TI recommends the following image calibration procedure:

1. Define 3 variables: XP = 0, XG = 0 and DX = 64. Go to step 3.
2. Set DX = DX/2.
3. Write XG to GAIN_COMP register.

```
If XP + 2 × DX < 127, then
    write XP + 2 × DX to PHASE_COMP register
else
    write 127 to PHASE_COMP register.
```

4. Wait at least 3 ms. Measure signal strength Y4 as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
5. Write XP+DX to PHASE_COMP register.
6. Wait at least 3 ms. Measure signal strength Y3 as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
7. Write XP to PHASE_COMP register.
8. Wait at least 3 ms. Measure signal strength Y2 as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
9. Write XP-DX to PHASE_COMP register.
10. Wait at least 3 ms. Measure signal strength Y1 as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
11. Write XP – 2 × DX to PHASE_COMP register.
12. Wait at least 3 ms. Measure signal strength Y0 as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
13. Set AP = 2 × (Y0 – Y2 + Y4) – (Y1 + Y3).
14.

```
If AP > 0 then
    set DP = ROUND ( 7 × DX × (2 × (Y0 – Y4) + Y1 – Y3) / (10 × AP))
else
    if Y0 + Y1 > Y3 + Y4 then
          set DP = DX
       else
          set DP = –DX.
```

15.

```
If DP > DX then
    set DP = DX
else
    if DP < –DX then set DP = –DX.
```

16. Set XP = XP + DP.
17. Write XP to PHASE_COMP register.
18.

```
If XG + 2 × DX < 127 then
    write XG + 2 × DX to GAIN_COMP register
else
    write 127 to GAIN_COMP register.
```

19. Wait at least 3 ms. Measure signal strength Y4 as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
20. Write XG + DX to GAIN_COMP register.
21. Wait at least 3 ms. Measure signal strength Y3 as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
22. Write XG to GAIN_COMP register.
23. Wait at least 3 ms. Measure signal strength Y2 as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.

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24. Write XG – DX to GAIN_COMP register.
25. Wait at least 3 ms. Measure signal strength Y1 as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
26. Write XG – 2 × DX to GAIN_COMP register.
27. Wait at least 3 ms. Measure signal strength Y0 as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
28. Set AG = 2 × (Y0 – Y2 + Y4) – (Y1 + Y3).
29.
```
If AG > 0 then
    set DG = ROUND (7 × DX × (2 × (Y0 – Y4) + Y1 – Y3) / (10 × AG)
else
    if Y0 + Y1 > Y3 + Y4 then
        set DG = DX
    else
        set DG = –DX.
```
30.
```
If DG > DX then
    set DG = DX
else
    if DG < –DX then set DG = –DX
```
31. Set XG = XG + DG.
32. If DX > 1 then go to step 2.
33. Write XP to PHASE_COMP register and XG to GAIN_COMP register.

If repeated calibration gives varying results, try to change the input level or increase the number of RSSI reads N. A good starting point is N=8. As accuracy is more important in the last fine-calibration steps, it can be worthwhile to increase N for each loop iteration.

For high frequency deviation and high data rates (typically ≥ 76.8 kBaud) the analog filter succeeding the mixer must be bypassed by setting FILTER_BYPASS = 1 in the FILTER register. In this case the image rejection is degraded.

The image rejection is reduced for low supply voltages (typically < 2.5 V) when operating in the 402 to 470 MHz frequency range.

5.9.7 Blocking and Selectivity

Figure 5-13 shows the blocking/selectivity for 102.4 kHz channel filter bandwidth at 433 MHz and 19.2 kBaud data rate. Figure 5-14 shows the blocking/selectivity for 102.4 kHz channel filter bandwidth at 433 MHz and 38.4 kBaud data rate. Figure 5-15 shows the blocking/selectivity for 102.4 kHz channel filter bandwidth at 868 MHz and 19.2 kBaud data rate. Figure 5-16 shows the blocking/selectivity for 102.4 kHz channel filter bandwidth at 868 MHz and 38.4 kBaud data rate. The blocking rejection is the ratio between a blocker (interferer) and a wanted signal 3 dB above the sensitivity limit.

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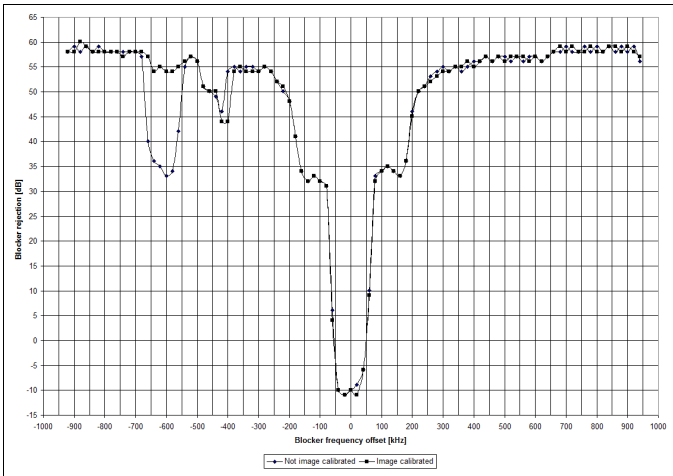

Figure 5-13. Typical Blocker Rejection. Carrier Frequency Set to 434.3072 MHz (102.4 kHz Channel Filter Bandwidth, 19.2 kBaud)

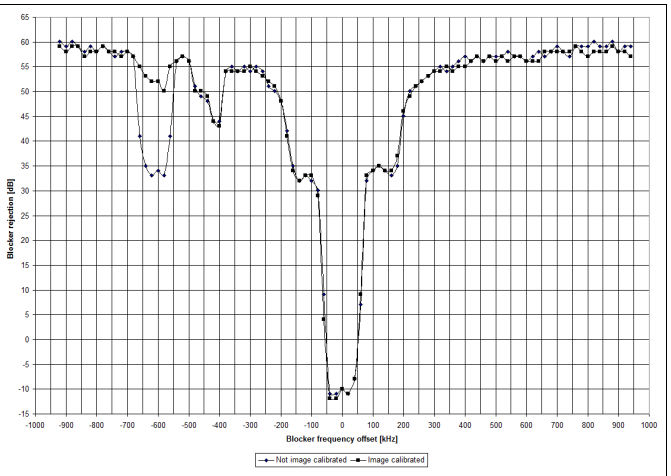

Figure 5-14. Typical Blocker Rejection. Carrier Frequency Set to 434.3072 MHz (102.4 kHz Channel Filter Bandwidth, 38.4 kBaud)

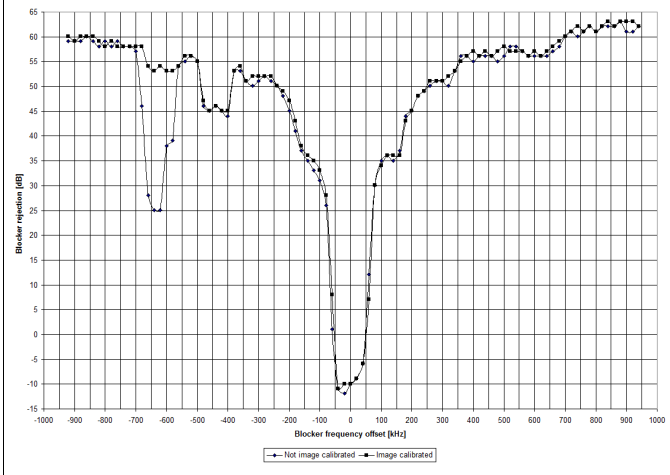

Figure 5-15. Typical Blocker Rejection. Carrier Frequency Set to 868.3072 MHz (102.4 kHz Channel Filter Bandwidth, 19.2 kBaud)

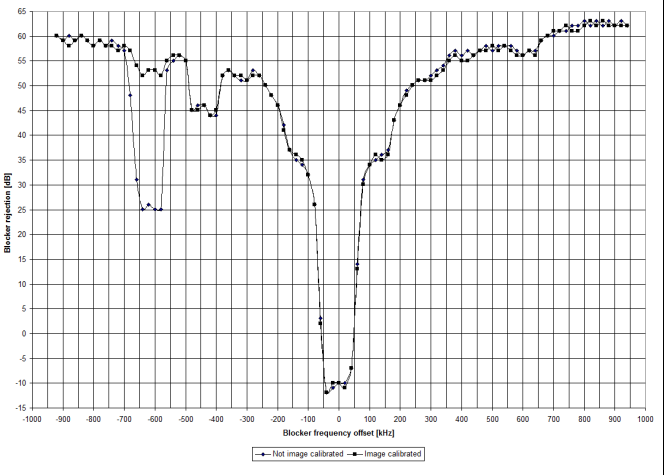

Figure 5-16. Typical Blocker Rejection. Carrier Frequency Set to 868.3072 MHz (102.4 kHz Channel Filter Bandwidth, 38.4 kBaud)

5.9.8 Linear IF Chain and AGC Settings

CC1021 is based on a linear IF chain where the signal amplification is done in an analog VGA (Variable Gain Amplifier). The gain is controlled by the digital part of the IF chain after the ADC (Analog to Digital Converter). The AGC (Automatic Gain Control) loop ensures that the ADC operates inside its dynamic range by using an analog/digital feedback loop.

The maximum VGA gain is programmed by the VGA_SETTING[4:0] in the VGA3 register. The VGA gain is programmed in approximately 3 dB/LSB. The VGA gain should be set so that the amplified thermal noise from the front-end balance the quantization noise from the ADC. Therefore the optimum maximum VGA gain setting will depend on the channel filter bandwidth.

A digital RSSI is used to measure the signal strength after the ADC. The CS_LEVEL[4:0] in the VGA4 register is used to set the nominal operating point of the gain control (and also the carrier sense level). Further explanation can be found in Figure 5-17.

The VGA gain will be changed according to a threshold set by the VGA_DOWN[2:0] in the VGA3 register and the VGA_UP[2:0] in the VGA4 register. Together, these two values specify the signal strength limits used by the AGC to adjust the VGA gain.

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To avoid unnecessary tripping of the VGA, an extra hysteresis and filtering of the RSSI samples can be added. The AGC_HYSTERESIS bit in the VGA2 register enables this.

The time dynamics of the loop can be altered by the VGA_BLANKING bit in the ANALOG register, and VGA_FREEZE[1:0] and VGA_WAIT[2:0] bits in the VGA1 register.

When VGA_BLANKING is activated, the VGA recovery time from DC offset spikes after a gain step is reduced.

VGA_FREEZE determines the time to hold bit synchronization, VGA and RSSI levels after one of these events occur:

- RX power-up
- The PLL has been out of lock
- Frequency register setting is switched between A and B

This feature is useful to avoid AGC operation during start-up transients and to ensure minimum dwell time using frequency hopping. This means that bit synchronization can be maintained from hop to hop.

VGA_WAIT determines the time to hold the present bit synchronization and RSSI levels after changing VGA gain. This feature is useful to avoid AGC operation during the settling of transients after a VGA gain change. Some transients are expected due to DC offsets in the VGA.

At the sensitivity limit, the VGA gain is set by VGA_SETTING. In order to optimize selectivity, this gain should not be set higher than necessary. The SmartRF Studio software gives the settings for VGA1 through VGA4 registers. For reference, the following method can be used to find the AGC settings:

1. Disable AGC and use maximum LNA2 gain by writing BFh to the VGA2 register. Set minimum VGA gain by writing to the VGA3 register with VGA_SETTING = 0.
2. Apply no RF input signal, and measure ADC noise floor by reading the RSSI register.
3. Apply no RF input signal, and write VGA3 register with increasing VGA_SETTING value until the RSSI register value is approximately 4 larger than the value read in step 2. This places the front-end noise floor around 6 dB above the ADC noise floor.
4. Apply an RF signal with strength equal the desired carrier sense threshold. The RF signal should preferably be modulated with correct Baud rate and deviation. Read the RSSI register value, subtract 8, and write to CS_LEVEL in the VGA4 register. Vary the RF signal level slightly and check that carrier sense indication (bit 3 in STATUS register) switches at the desired input level.
5. If desired, adjust the VGA_UP and VGA_DOWN settings according to the explanation in Figure 5-17.
6. Enable AGC and select LNA2 gain change level. Write 55h to VGA2 register if the resulting VGA_SETTING>10. Otherwise, write 45h to VGA2. Modify AGC_AVG in the above VGA2 value if faster carrier sense and AGC settling is desired.

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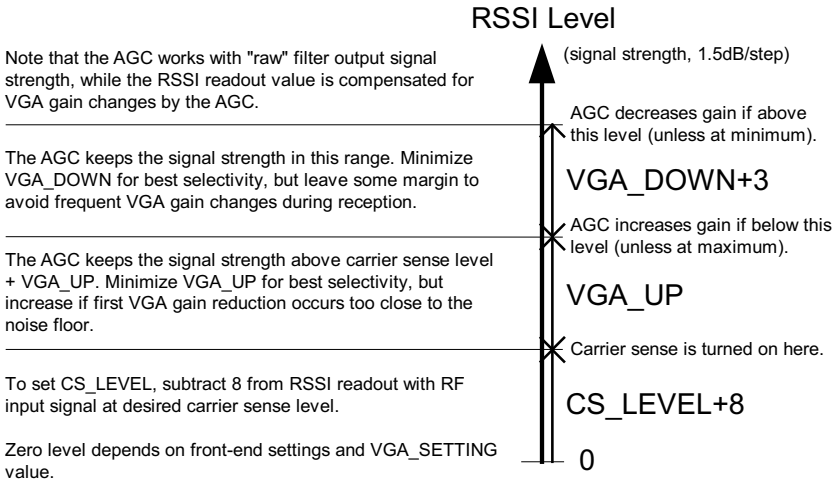

Figure 5-17. Relationship Between RSSI, Carrier Sense Level, and AGC Settings CS_LEVEL, VGA_UP and VGA_DOWN

5.9.9 AGC Settling

After turning on the RX chain, the following occurs:

A. The AGC waits 16-128 ADC_CLK (1.2288 MHz) periods, depending on the VGA_FREEZE setting in the VGA1 register, for settling in the analog parts.

B. The AGC waits 16-48 FILTER_CLK periods, depending on the VGA_WAIT setting in the VGA1 register, for settling in the analog parts and the digital channel filter.

C. The AGC calculates the RSSI value as the average magnitude over the next 2-16 FILTER_CLK periods, depending of the AGC_AVG setting in the VGA2 register.

D. If the RSSI value is higher than CS_LEVEL+8, then the carrier sense indicator is set (if CS_SET = 0). If the RSSI value is too high according to the CS_LEVEL, VGA_UP and VGA_DOWN settings, and the VGA gain is not already at minimum, then the VGA gain is reduced and the AGC continues from B).

E. If the RSSI value is too low according to the CS_LEVEL and VGA_UP settings, and the VGA gain is not already at maximum (given by VGA_SETTING), then the VGA gain is increased and the AGC continues from B).

Two to three VGA gain changes should be expected before the AGC has settled. Increasing AGC_AVG increases the settling time, but may be worthwhile if there is the time in the protocol, and for reducing false wake-up events when setting the carrier sense close to the noise floor.

The AGC settling time depends on the FILTER_CLK (= 2 × ChBW). Thus, there is a trade off between AGC settling time and receiver sensitivity because the AGC settling time can be reduced for data rates lower than 76.8 kBaud by using a wider receiver channel filter bandwidth (that is, larger ChBW).

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5.9.10 Preamble Length and Sync Word

The rules for choosing a good sync word are as follows:

1. The sync word should be significantly different from the preamble.
2. A large number of transitions is good for the bit synchronization or clock recovery. Equal bits reduce the number of transitions. The recommended sync word has at the most 3 equal bits in a row.
3. Autocorrelation. The sync word should not repeat itself, as this will increase the likelihood for errors.
4. In general the first bit of sync should be opposite of last bit in preamble, to achieve one more transition.

The recommended sync words for CC1021 are 2 bytes (D391), 3 bytes (D391DA) or 4 bytes (D391DA26) and are selected as the best compromise of the above criteria.

Using the register settings provided by the SmartRF Studio software, packet error rates (PER) less than 0.5% can be achieved when using 24 bits of preamble and a 16 bit sync word (D391). Using a preamble longer than 24 bits will improve the PER.

When performing the PER measurements described above the packet format consisted of 10 bytes of random data, 2 bytes CRC and 1 dummy byte in addition to the sync word and preamble at the start of each package.

For the test, 1000 packets were sent 10 times. The transmitter was put in power down between each packet. Any bit error in the packet, either in the sync word, in the data or in the CRC caused the packet to be counted as a failed packet.

5.9.11 Carrier Sense

The carrier sense signal is based on the RSSI value and a programmable threshold. The carrier sense function can be used to simplify the implementation of a CSMA (Carrier Sense Multiple Access) medium access protocol.

Carrier sense threshold level is programmed by CS_LEVEL[4:0] in the VGA4 register and VGA_SETTING[4:0] in the VGA3 register.

VGA_SETTING[4:0] sets the maximum gain in the VGA. This value must be set so that the ADC works with optimum dynamic range for a certain channel filter bandwidth. The detected signal strength (after the ADC) will therefore depend on this setting.

CS_LEVEL[4:0] sets the threshold for this specific VGA_SETTING[4:0] value. If the VGA_SETTING[4:0] is changed, the CS_LEVEL[4:0] must be changed accordingly to maintain the same absolute carrier sense threshold. See Figure 5-17 for an explanation of the relationship between RSSI, AGC and carrier sense settings.

The carrier sense signal can be read as the CARRIER_SENSE bit in the STATUS register.

The carrier sense signal can also be made available at the LOCK pin by setting LOCK_SELECT[3:0] = 0100 in the LOCK register.

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5.9.12 Automatic Power-Up Sequencing

CC1021 has a built-in automatic power-up sequencing state machine. By setting the CC1021 into this mode, the receiver can be powered-up automatically by a wake-up signal and will then check for a carrier signal (carrier sense). If carrier sense is not detected, it returns to power-down mode. A flow chart for automatic power-up sequencing is shown in Figure 5-18.

The automatic power-up sequencing mode is selected when PD_MODE[1:0] = 11 in the MAIN register. When the automatic power-up sequencing mode is selected, the functionality of the MAIN register is changed and used to control the sequencing.

By setting SEQ_PD = 1 in the MAIN register, CC1021 is set in power down mode. If SEQ_PSEL = 1 in the SEQUENCING register the automatic power-up sequence is initiated by a negative transition on the PSEL pin.

If SEQ_PSEL = 0 in the SEQUENCING register, then the automatic power-up sequence is initiated by a negative transition on the DIO pin (as long as SEP_DI_DO = 1 in the INTERFACE register).

Sequence timing is controlled through RX_WAIT[2:0] and CS_WAIT[3:0] in the SEQUENCING register.

VCO and PLL calibration can also be done automatically as a part of the sequence. This is controlled through SEQ_CAL[1:0] in the MAIN register. Calibration can be done every time, every 16th sequence, every 256th sequence, or never. See the register description for details. A description of when to do, and how the VCO and PLL self-calibration is done, is given in *Section 5.12.2*.

See also Application Note *AN070 CC1020 Automatic Power-Up Sequencing* (SWRA279).

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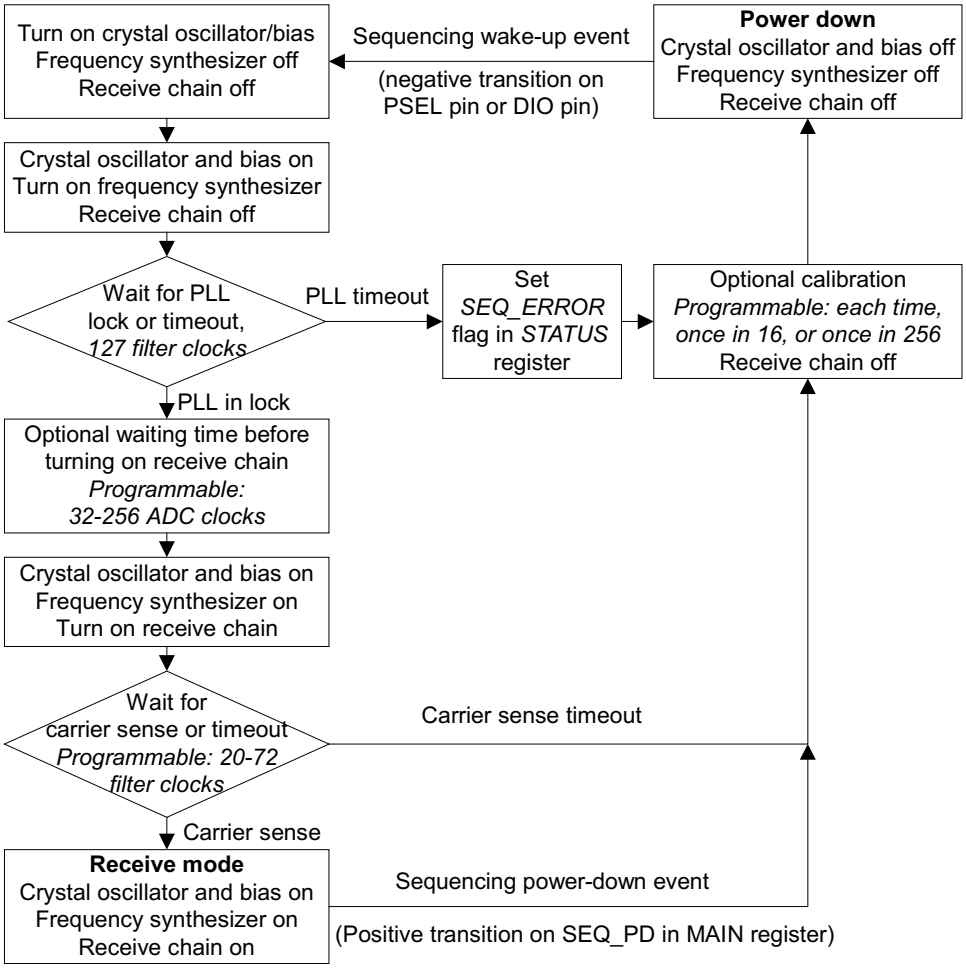

A. Filter clock (FILTER_CLK): $f_{filter_clock} = 2 \times ChBW$ where ChBW is defined in *Section 5.9.2*.

B. ADC clock (ADC_CLK): $f_{ADC} = \frac{f_{xoscx}}{2 \times (ADC_DIV[2:0] + 1)}$ where ADC_DIV[2:0] is set in the MODEM register.

Figure 5-18. Automatic Power-Up Sequencing Flow Chart

5.9.13 Automatic Frequency Control

CC1021 has a built-in feature called AFC (Automatic Frequency Control) that can be used to compensate for frequency drift.

The average frequency offset of the received signal (from the nominal IF frequency) can be read in the AFC register. The signed (2-complement) 8-bit value AFC[7:0] can be used to compensate for frequency offset between transmitter and receiver.

The frequency offset is given by Equation 22.

$$\Delta F = AFC \times \frac{\text{Baud rate}}{16} \tag{22}$$

The receiver can be calibrated against the transmitter by changing the operating frequency according to the measured offset. The new frequency must be calculated and written to the FREQ register by the microcontroller. The AFC can be used for an FSK/GFSK signal, but not for OOK. Application Note *AN029 CC1020/1021 Automatic Frequency Control (AFC)* (SWRA063) provides the procedure and equations necessary to implement AFC.

The AFC feature reduces the crystal accuracy requirement.

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5.9.14 Digital FM

It is possible to read back the instantaneous IF from the FM demodulator as a frequency offset from the nominal IF frequency. This digital value can be used to perform a pseudo analog FM demodulation.

The frequency offset can be read from the GAUSS_FILTER register and is a signed 8-bit value coded as 2-complement.

The instantaneous deviation is given by Equation 23.

$$F = GAUSS_FILTER \times \frac{\text{Baud rate}}{8} \tag{23}$$

The digital value should be read from the register and sent to a DAC and filtered in order to get an analog audio signal. The internal register value is updated at the MODEM_CLK rate. MODEM_CLK is available at the LOCK pin when LOCK_SELECT[3:0] = 1101 in the LOCK register, and can be used to synchronize the reading.

For audio (300 to 4000 Hz) the sampling rate should be higher than or equal to 8 kHz (Nyquist) and is determined by the MODEM_CLK. The MODEM_CLK, which is the sampling rate, equals 8 times the baud rate. That is, the minimum baud rate, which can be programmed, is 1 kBaud. However, the incoming data will be filtered in the digital domain and the 3-dB cut-off frequency is 0.6 times the programmed Baud rate. Thus, for audio the minimum programmed Baud rate should be approximately 7.2 kBaud.

The GAUSS_FILTER resolution decreases with increasing baud rate. A accumulate and dump filter can be implemented in the uC to improve the resolution.

NOTE

Each GAUSS_FILTER reading should be synchronized to the MODEM_CLK. As an example, accumulating four readings and dividing the total by 4 will improve the resolution by 2 bits.

Furthermore, to fully utilize the GAUSS_FILTER dynamic range the frequency deviation must be 16 times the programmed baud rate.

5.10 Transmitter

5.10.1 FSK Modulation Formats

The data modulator can modulate FSK, which is a two level FSK (Frequency Shift Keying), or GFSK, which is a Gaussian filtered FSK with BT = 0.5. The purpose of the GFSK is to make a more bandwidth efficient system. The modulation and the Gaussian filtering are done internally in the chip. The TX_SHAPING bit in the DEVIATION register enables the GFSK.

Figure 5-19 shows a typical eye diagram for 153.6 kBaud data rate at 868 MHz operation.

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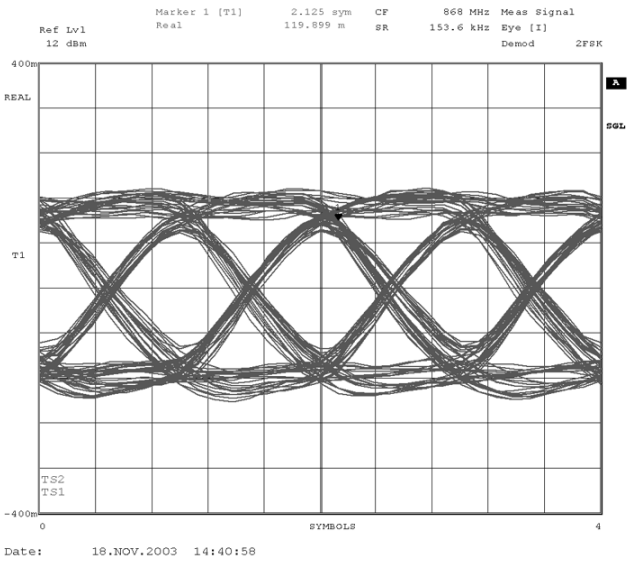

Figure 5-19. GFSK Eye Diagram. 153.6 kBaud, NRZ, ±79.2 kHz Frequency Deviation.

5.10.2 Output Power Programming

The RF output power from the device is programmable by the 8-bit PA_POWER register. Figure 5-20 and Figure 5-21 show the output power and total current consumption as a function of the PA_POWER register setting. It is more efficient in terms of current consumption to use either the lower or upper 4-bits in the register to control the power, as shown in Figure 5-20 and Figure 5-21. However, the output power can be controlled in finer steps using all the available bits in the PA_POWER register.

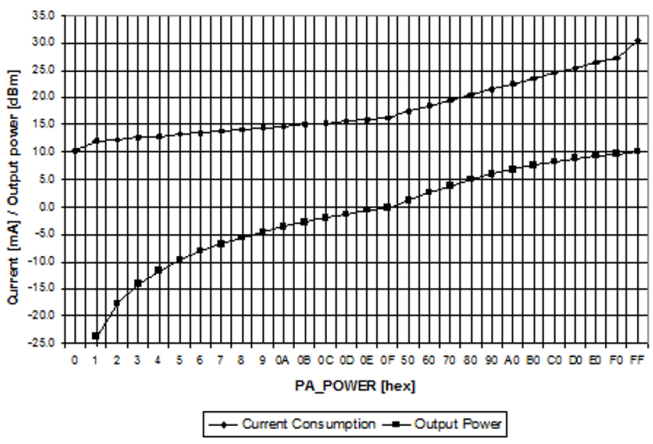

Figure 5-20. Typical Output Power and Current Consumption, 433 MHz

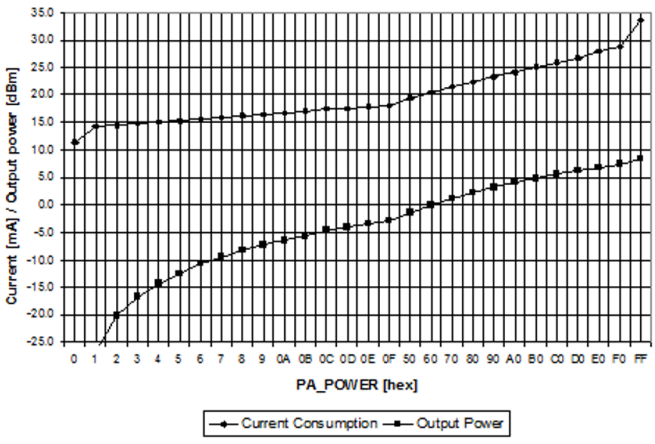

Figure 5-21. Typical Output Power and Current Consumption, 868 MHz

5.10.3 TX Data Latency

The transmitter will add a delay due to the synchronization of the data with DCLK and further clocking into the modulator. The user should therefore add a delay equivalent to at least 2 bits after the data payload has been transmitted before switching off the PA (that is, before stopping the transmission).

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5.10.4 Reducing Spurious Emission and Modulation Bandwidth

Modulation bandwidth and spurious emission are normally measured with the PA continuously on and a repeated test sequence.

In cases where the modulation bandwidth and spurious emission are measured with the CC1021 switching from power down mode to TX mode, a PA ramping sequence could be used to minimize modulation bandwidth and spurious emission.

PA ramping should then be used both when switching the PA on and off. A linear PA ramping sequence can be used where register PA_POWER is changed from 00h to 0Fh and then from 50h to the register setting that gives the desired output power (for example, F0h for +10 dBm output power at 433 MHz operation). The longer the time per PA ramping step the better, but setting the total PA ramping time equal to 2 bit periods is a good compromise between performance and PA ramping time.

5.11 Input and Output Matching and Filtering

When designing the impedance matching network for the CC1021 the circuit must be matched correctly at the harmonic frequencies as well as at the fundamental tone. A recommended matching network is shown in Figure 5-22. Component values for various frequencies are given in Table 5-8. Component values for other frequencies can be found using the SmartRF Studio software.

As can be seen from Figure 5-22 and Table 5-8, the 433 MHz network utilizes a T-type filter, while the 868/915 MHz network has a π-type filter topology.

It is important to remember that the physical layout and the components used contribute significantly to the reflection coefficient, especially at the higher harmonics. For this reason, the frequency response of the matching network should be measured and compared to the response of the TI reference design. Refer to Figure 5-24 and Table 5-9 as well as Figure 5-25 and Table 5-10.

The use of an external T/R switch reduces current consumption in TX for high output power levels and improves the sensitivity in RX. A recommended application circuit is available from the TI web site (CC1020EMX). The external T/R switch can be omitted in certain applications, but performance will then be degraded.

The match can also be tuned by a shunt capacitor array at the PA output (RF_OUT). The capacitance can be set in 0.4 pF steps and used either in RX mode or TX mode. The RX_MATCH[3:0] and TX_MATCH[3:0] bits in the MATCH register control the capacitor array.

Table 5-8. Component Values for the Matching Network Described in Figure 5-22

ITEM	433 MHz	868 MHz	915 MHz
C1	10 pF, 5%, NP0, 0402	47 pF, 5%, NP0, 0402	47 pF, 5%, NP0, 0402
C3	5.6 pF, 5%, NP0, 0402	10 pF, 5%, NP0, 0402	10 pF, 5%, NP0, 0402
C60	220 pF, 5%, NP0, 0402	220 pF, 5%, NP0, 0402	220 pF, 5%, NP0, 0402
C71	DNM(1)	8.2 pF 5%, NP0, 0402	8.2 pF 5%, NP0, 0402
C72	4.7 pF, 5%, NP0, 0402	8.2 pF 5%, NP0, 0402	8.2 pF 5%, NP0, 0402
L1	33 nH, 5%, 0402	82 nH, 5%, 0402	82 nH, 5%, 0402
L2	22 nH, 5%, 0402	3.6 nH, 5%, 0402	3.6 nH, 5%, 0402
L70	47 nH, 5%, 0402	5.1 nH, 5%, 0402	5.1 nH, 5%, 0402
L71	39 nH, 5%, 0402	0 Ω resistor, 0402	0 Ω resistor, 0402
R10	82 Ω, 5%, 0402	82 Ω, 5%, 0402	82 Ω, 5%, 0402

(1) DNM = Do Not Mount

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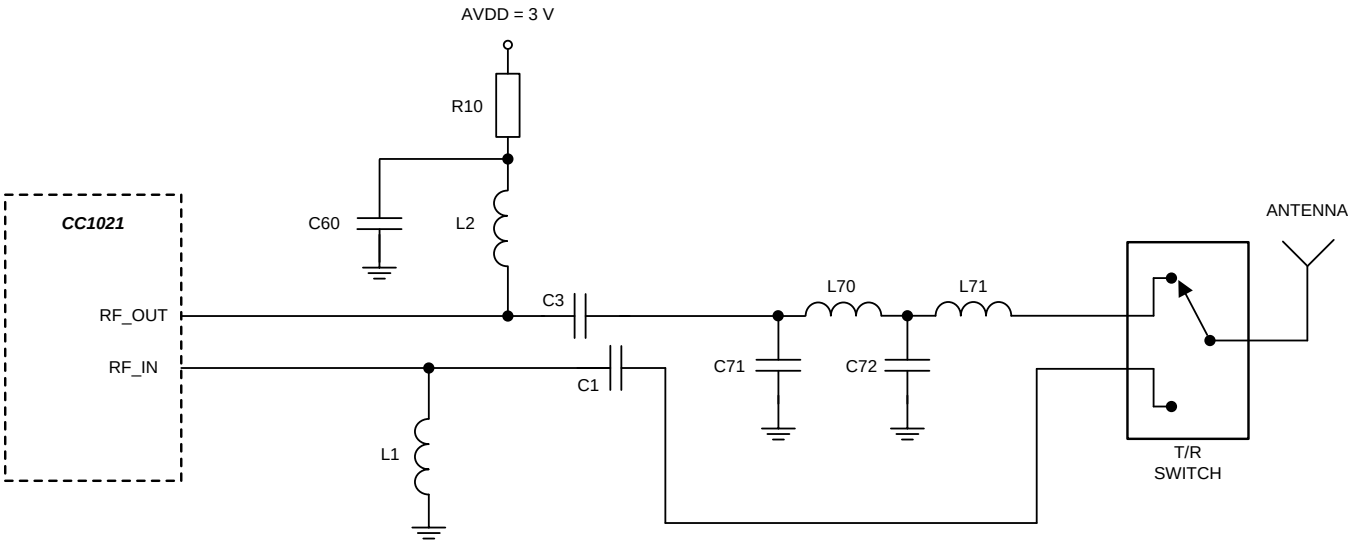

Figure 5-22. Input and Output Matching Network

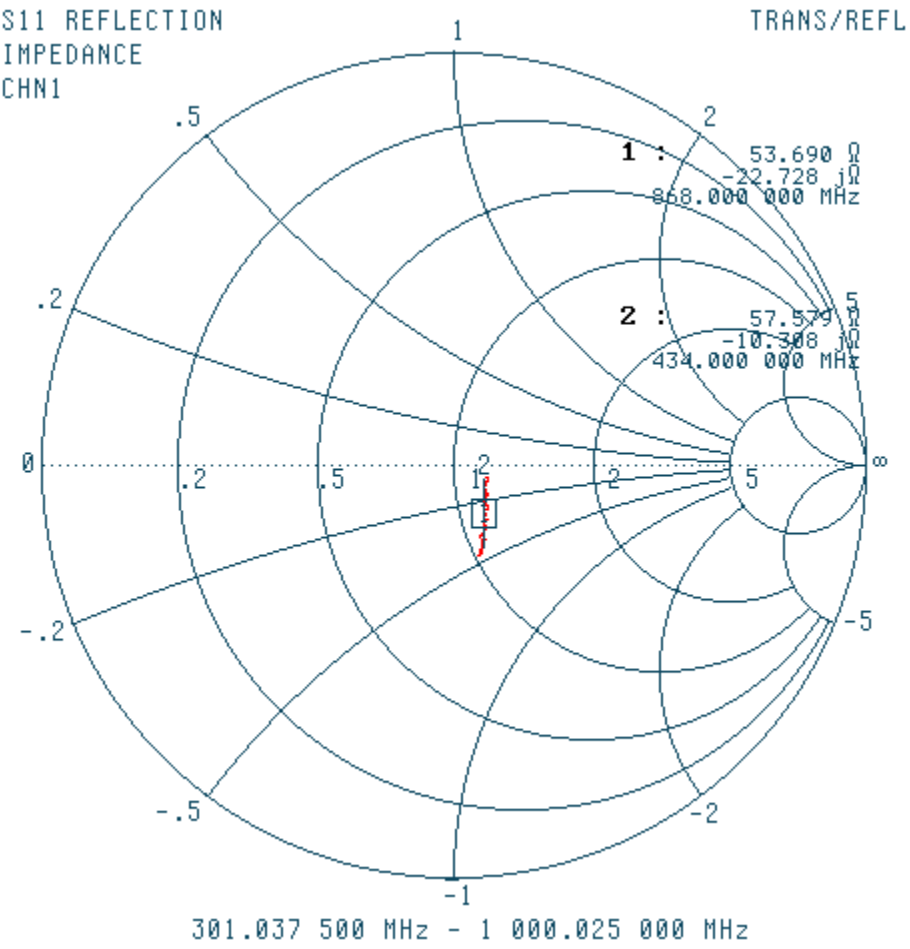

Figure 5-23. Typical LNA Input Impedance, 200 to 1000 MHz

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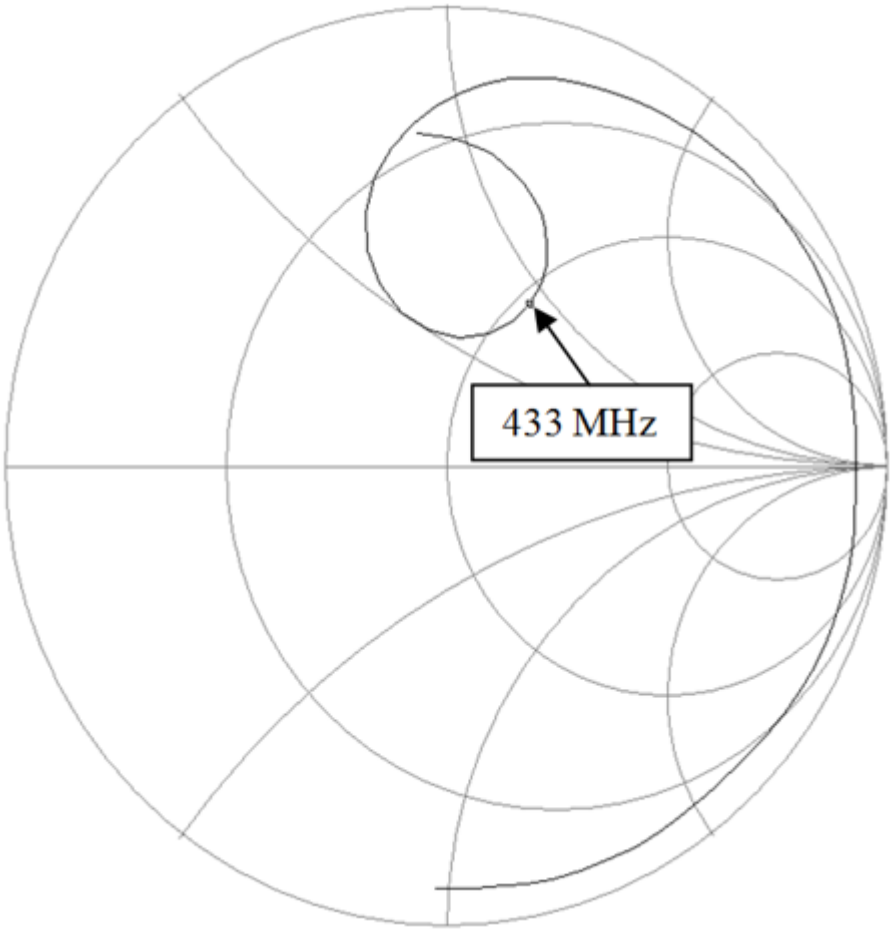

Figure 5-24. Typical Optimum PA Load Impedance, 433 MHz. The frequency is swept from 300 MHz to 2500 MHz. Values are listed in Table 5-9

Table 5-9. Impedances at the First 5 Harmonics (433 MHz Matching Network)

FREQUENCY (MHz)	REAL (Ohms)	IMAGINARY (Ohms)
433	54	44
866	20	173
1299	288	–563
1732	14	–123
2165	5	–66

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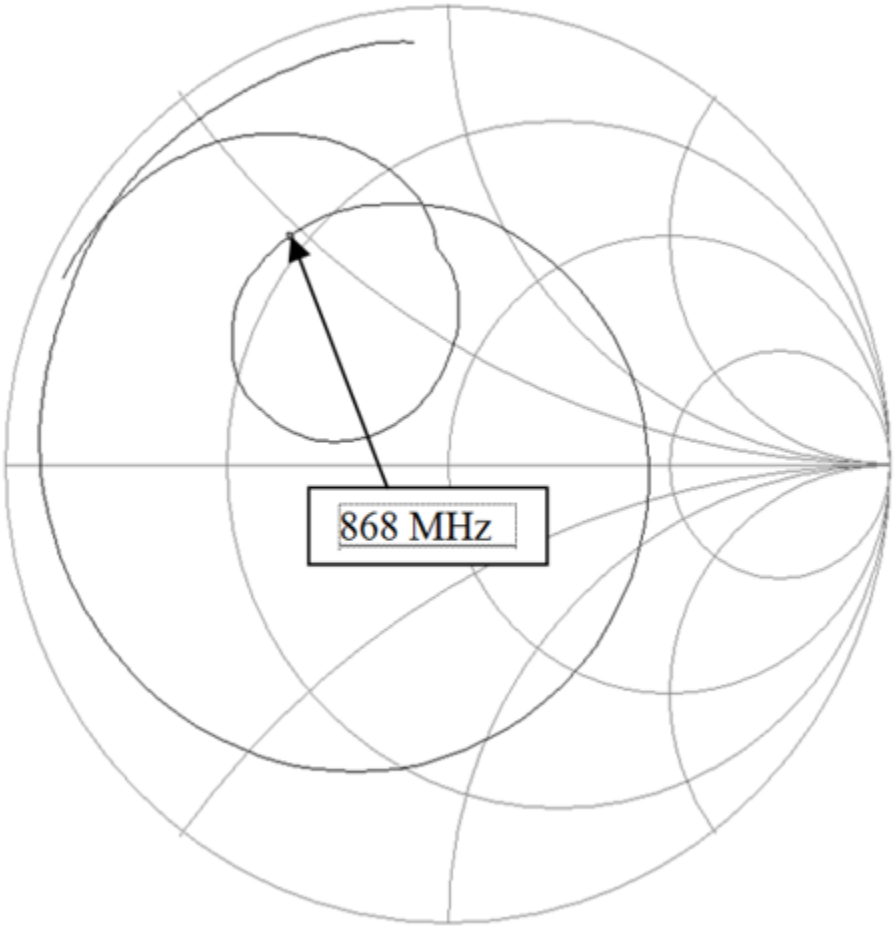

Figure 5-25. Typical Optimum PA Load Impedance, 868/915 MHz. The frequency is swept from 300 MHz to 2800 MHz. Values are listed in Table 5-10

Table 5-10. Impedances at the First 3 Harmonics (868/915 MHz Matching Network)

FREQUENCY (MHz)	REAL (Ohms)	IMAGINARY (Ohms)
868	15	24
915	20	35
1736	1.5	18
1830	1.7	22
2604	3.2	44
2745	3.6	45

5.12 Frequency Synthesizer

5.12.1 VCO, Charge Pump, and PLL Loop Filter

The VCO is completely integrated and operates in the 1608 to 1880 MHz range. A frequency divider is used to get a frequency in the UHF range (402 to 470 and 804 to 960 MHz). The BANDSELECT bit in the ANALOG register selects the frequency band.

The VCO frequency is given by Equation 24.

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$$f_{VCO} = f_{ref} \times \left(3 + \frac{FREQ + 0.5 \times DITHER}{8192}\right) \quad (24)$$

The VCO frequency is divided by 2 and by 4 to generate frequencies in the two bands, respectively.

The VCO sensitivity (sometimes referred to as VCO gain) varies over frequency and operating conditions. Typically the VCO sensitivity varies between 12 and 36 MHz/V. For calculations the geometrical mean at 21 MHz/V can be used. The PLL calibration (explained below) measures the actual VCO sensitivity and adjusts the charge pump current accordingly to achieve correct PLL loop gain and bandwidth (higher charge pump current when VCO sensitivity is lower).

Equation 25 through Equation 29 can be used for calculating PLL loop filter component values, see Figure 6-1, for a desired PLL loop bandwidth, BW.

$$C7 = 3037\left(\frac{f_{ref}}{BW^2}\right) - 7\ [pF] \quad (25)$$

$$R2 = 7126\left(\frac{BW}{f_{ref}}\right)\ [k\Omega] \quad (26)$$

$$C6 = 80.75\left(\frac{f_{ref}}{BW^2}\right)\ [nF] \quad (27)$$

$$R3 = 21823\left(\frac{BW}{f_{ref}}\right)\ [k\Omega] \quad (28)$$

$$C8 = 839\left(\frac{f_{ref}}{BW^2}\right) - 6\ [pF] \quad (29)$$

Define a minimum PLL loop bandwidth as shown in Equation 30.

$$BW_{min} = \sqrt{80.75 \times \frac{f_{ref}}{220}} \quad (30)$$

If BW_{min} > Baud rate/3 then set BW = BW_{min} and if BW_{min} < Baud rate/3 then set BW = Baud rate/3 in Equation 25 through Equation 29.

There is one special case when using the recommended 14.7456 MHz crystal:

If the data rate is 4.8 kBaud or below the following loop filter components are recommended:

C6 = 100 nF
C7 = 3900 pF
C8 = 1000 pF
R2 = 2.2 kΩ
R3 = 6.8 kΩ

After calibration, the PLL bandwidth is set by the PLL_BW register in combination with the external loop filter components calculated above. The PLL_BW can be found from Equation 31.

$$PLL_BW = 174 + 16\log_2\left(\frac{f_{ref}}{7.126}\right) \quad (31)$$

Where:

f_{ref} is the reference frequency (in MHz).

The PLL loop filter bandwidth increases with increasing PLL_BW setting.

After calibration, the applied charge pump current (CHP_CURRENT[3:0]) can be read in the STATUS1 register. The charge pump current is approximately given by Equation 32.

$$I_{CHP} = 16 \times 2^{CHP_CURRENT/4}\ [\mu A] \quad (32)$$

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The combined charge pump and phase detector gain (in A/rad) is given by the charge pump current divided by 2π.

The PLL bandwidth will limit the maximum modulation frequency and hence, data rate.

5.12.2 VCO and PLL Self-Calibration

To compensate for supply voltage, temperature and process variations, the VCO and PLL must be calibrated. The calibration is performed automatically and sets the maximum VCO tuning range and optimum charge pump current for PLL stability. After setting up the device at the operating frequency, the self-calibration can be initiated by setting the CAL_START bit in the CALIBRATE register. The calibration result is stored internally in the chip, and is valid as long as power is not turned off. If large supply voltage drops (typically more than 0.25 V) or temperature variations (typically more than 40°C) occur after calibration, a new calibration should be performed.

The nominal VCO control voltage is set by the CAL_ITERATE[2:0] bits in the CALIBRATE register.

The CAL_COMPLETE bit in the STATUS register indicates that calibration has finished. The calibration wait time (CAL_WAIT) is programmable and is proportional to the internal PLL reference frequency. The highest possible reference frequency should be used to get the minimum calibration time. It is recommended to use CAL_WAIT[1:0] = 11 in order to get the most accurate loop bandwidth.

Table 5-11. Typical Calibration Times

CALIBRATION TIME [MS]	REFERENCE FREQUENCY [MHz]		
CAL_WAIT	1.8432	7.3728	9.8304
0	49 ms	12 ms	10 ms
1	60 ms	15 ms	11 ms
10	71 ms	18 ms	13 ms
11	109 ms	27 ms	20 ms

The CAL_COMPLETE bit can also be monitored at the LOCK pin, configured by LOCK_SELECT[3:0] = 0101, and used as an interrupt input to the microcontroller.

To check that the PLL is in lock the user should monitor the LOCK_CONTINUOUS bit in the STATUS register. The LOCK_CONTINUOUS bit can also be monitored at the LOCK pin, configured by LOCK_SELECT[3:0] = 0010.

There are separate calibration values for the two frequency registers. However, dual calibration is possible if all of the following conditions apply:

- The two frequencies A and B differ by less than 1 MHz.
- Reference frequencies are equal (REF_DIV_A[2:0] = REF_DIV_B[2:0] in the CLOCK_A/CLOCK_B registers).
- VCO currents are equal (VCO_CURRENT_A[3:0] = VCO_CURRENT_B[3:0] in the VCO register).

The CAL_DUAL bit in the CALIBRATE register controls dual or separate calibration.

The single calibration algorithm (CAL_DUAL=0) using separate calibration for RX and TX frequency is illustrated in Figure 5-26. The same algorithm is applicable for dual calibration if CAL_DUAL=1. Refer to Application Note *AN023 CC1020 MCU Interfacing* (SWRA069), which includes example source code for single calibration.

TI recommends that single calibration be used for more robust operation.

There is a finite possibility that the PLL self-calibration will fail. The calibration routine in the source code should include a loop so that the PLL is re-calibrated until PLL lock is achieved if the PLL does not lock the first time. Refer to *CC1021 Errata Note 002*, available in the CC1021 product folder.

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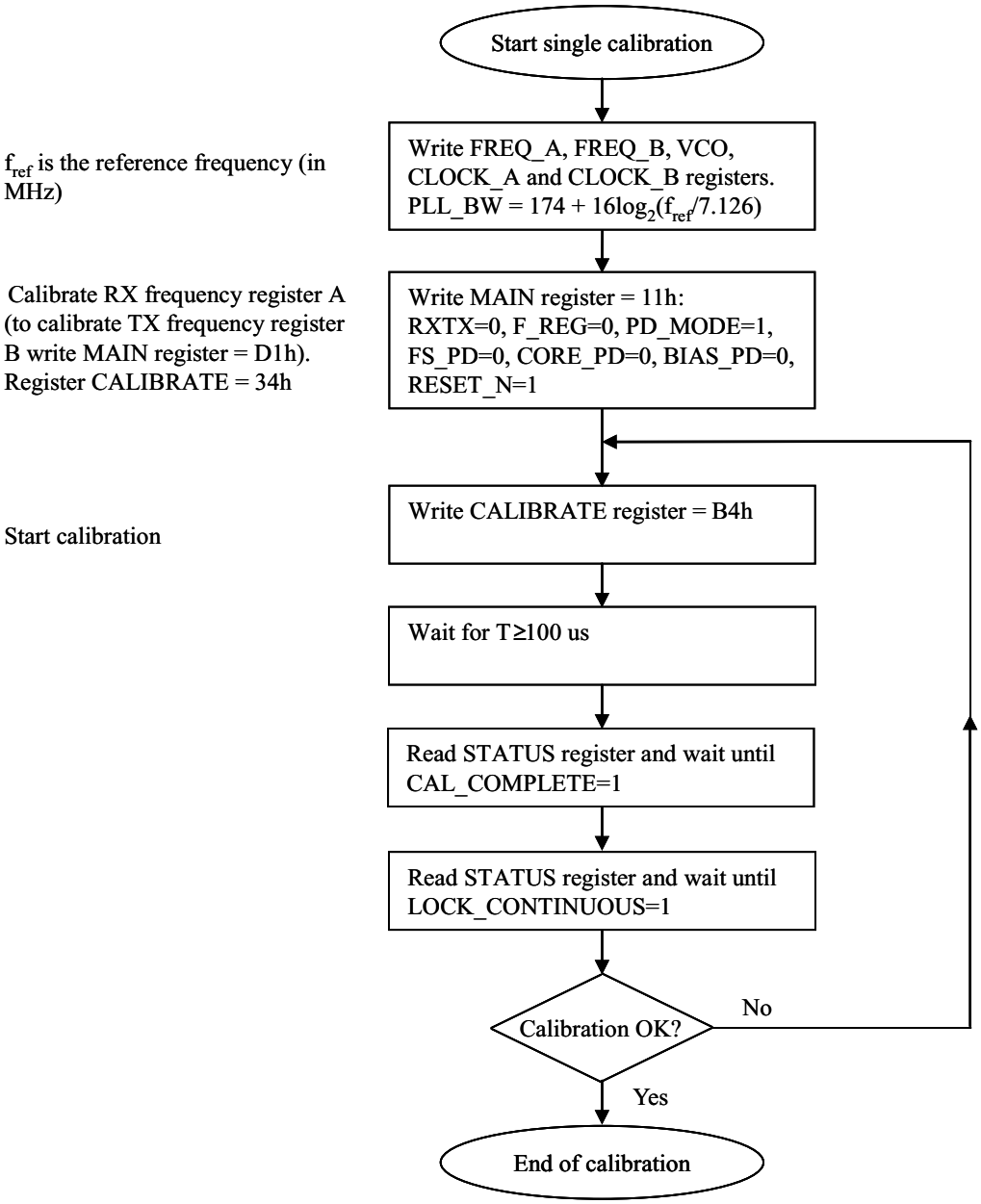

Figure 5-26. Single Calibration Algorithm for RX and TX

5.12.3 PLL Turn-on Time versus Loop Filter Bandwidth

If calibration has been performed the PLL turn-on time is the time needed for the PLL to lock to the desired frequency when going from power down mode (with the crystal oscillator running) to TX or RX mode. The PLL turn-on time depends on the PLL loop filter bandwidth. Table 5-12 gives the PLL turn-on time for different PLL loop filter bandwidths.

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Table 5-12. Typical PLL Turn-On Time to Within Specified Accuracy for Different Loop Filter Bandwidths

LOOP FILTER NO.	C6 [nF]	C7 [pF]	C8 [pF]	R2 [kΩ]	R3 [kΩ]	PLL TURN-ON TIME [µs]	COMMENT
1	56	2200	560	3.3	10	1400	Up to 9.6 kBaud data rate ±5 kHz settling accuracy
2	15	560	150	5.6	18	1300	Up to 19.2 kBaud data rate ±10 kHz settling accuracy
3	3.9	120	33	12	39	1080	Up to 38.4 kBaud data rate ±15 kHz settling accuracy
4	1.0	27	3.3	27	82	950	Up to 76.8 kBaud data rate ±20 kHz settling accuracy
5	0.2	1.5	—	47	150	700	Up to 153.6 kBaud data rate ±50 kHz settling accuracy

5.12.4 PLL Lock Time versus Loop Filter Bandwidth

If calibration has been performed the PLL lock time is the time needed for the PLL to lock to the desired frequency when going from RX to TX mode or vice versa. The PLL lock time depends on the PLL loop filter bandwidth. Table 5-13 gives the PLL lock time for different PLL loop filter bandwidths.

Table 5-13. Typical PLL Lock Time to Within Specified Accuracy for Different Loop Filter Bandwidths(1)

LOOP FILTER NO.	C6 [nF]	C7 [pF]	C8 [pF]	R2 [kΩ]	R3 [kΩ]	PLL LOCK TIME [µs]			COMMENT
						1	2	3	
1	56	2200	560	3.3	10	400	140 (50 kHz)	490	Up to 9.6 kBaud data rate ±5 kHz settling accuracy
2	15	560	150	5.6	18	140	70 (100 kHz)	230	Up to 19.2 kBaud data rate ±10 kHz settling accuracy
3	3.9	120	33	12	39	75	50 (150 kHz)	180	Up to 38.4 kBaud data rate ±15 kHz settling accuracy
4	1.0	27	3.3	27	82	30	15 (200 kHz)	55	Up to 76.8 kBaud data rate ±20 kHz settling accuracy
5	0.2	1.5	—	47	150	14	14 (500 kHz)	28	Up to 153.6 kBaud data rate ±50 kHz settling accuracy

(1) 1) 307.2 kHz step,
2) step as given in brackets,
3) 1 MHz step

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5.13 VCO and LNA Current Control

The VCO current is programmable and should be set according to operating frequency, RX/TX mode and output power. Recommended settings for the VCO_CURRENT bits in the VCO register are shown in Table 5-16 and also given by SmartRF Studio. The VCO current for frequency FREQ_A and FREQ_B can be programmed independently.

The bias currents for the LNA, mixer and the LO and PA buffers are also programmable. The FRONTEND and the BUFF_CURRENT registers control these currents.

5.14 Power Management

CC1021 offers great flexibility for power management in order to meet strict power consumption requirements in battery-operated applications. Power down mode is controlled through the MAIN register. There are separate bits to control the RX part, the TX part, the frequency synthesizer and the crystal oscillator in the MAIN register. This individual control can be used to optimize for lowest possible current consumption in each application. Figure 5-27 shows a typical power-on and initializing sequence for minimum power consumption.

Figure 5-28 shows a typical sequence for activating RX and TX mode from power down mode for minimum power consumption.

NOTE

PSEL should be tri-stated or set to a high level during power down mode in order to prevent a trickle current from flowing in the internal pullup resistor.

Application Note *AN023 CC1020 MCU Interfacing* (SWRA069) is also applicable for the CC1021 device and includes example source code.

TI recommends resetting the CC1021 (by clearing the RESET_N bit in the MAIN register) when the chip is powered up initially. All registers that need to be configured should then be programmed (those which differ from their default values). Registers can be programmed freely in any order. The CC1021 should then be calibrated in both RX and TX mode. After this is completed, the CC1021 is ready for use. See the detailed procedure flowcharts in Figure 5-26 through Figure 5-28.

NOTE

The CC1020 sub-routines are equally applicable for the CC1021.

With reference to Application Note *AN023 CC1020 MCU Interfacing* (SWRA069), TI recommends the following sequence:

After power up:

1. ResetCC1020
2. Initialize
3. WakeUpCC1020ToRX
4. Calibrate
5. WakeUpCC1020ToTX
6. Calibrate

After calibration is completed, enter TX mode (SetupCC1020TX), RX mode (SetupCC1020RX) or power down mode (SetupCC1020PD).

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From power-down mode to RX:

1. WakeUpCC1020ToRX
2. SetupCC1020RX

From power-down mode to TX:

1. WakeUpCC1020ToTX
2. SetupCC1020TX

Switching from RX to TX mode:

1. SetupCC1020TX

Switching from TX to RX mode:

1. SetupCC1020RX

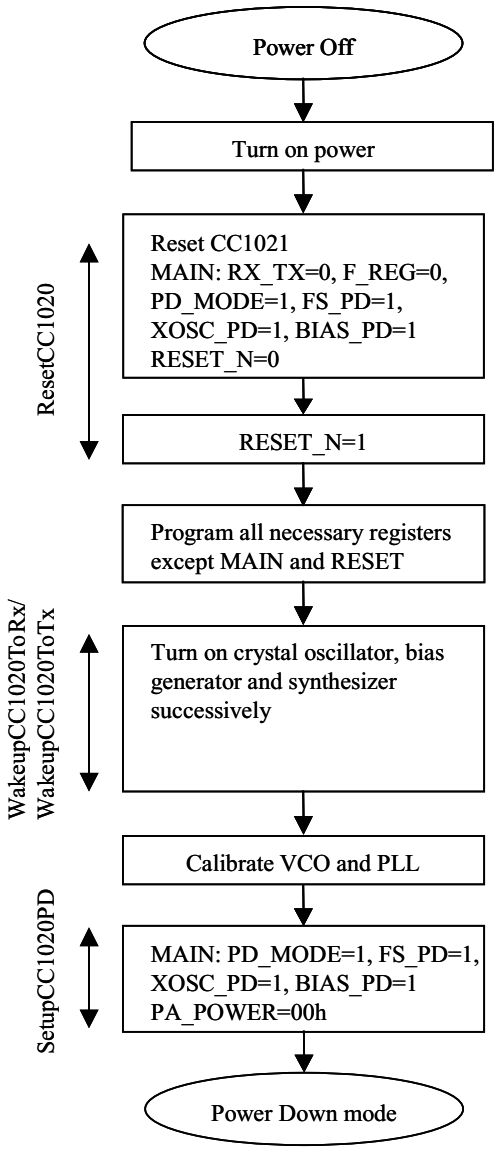

Figure 5-27. Initializing Sequence

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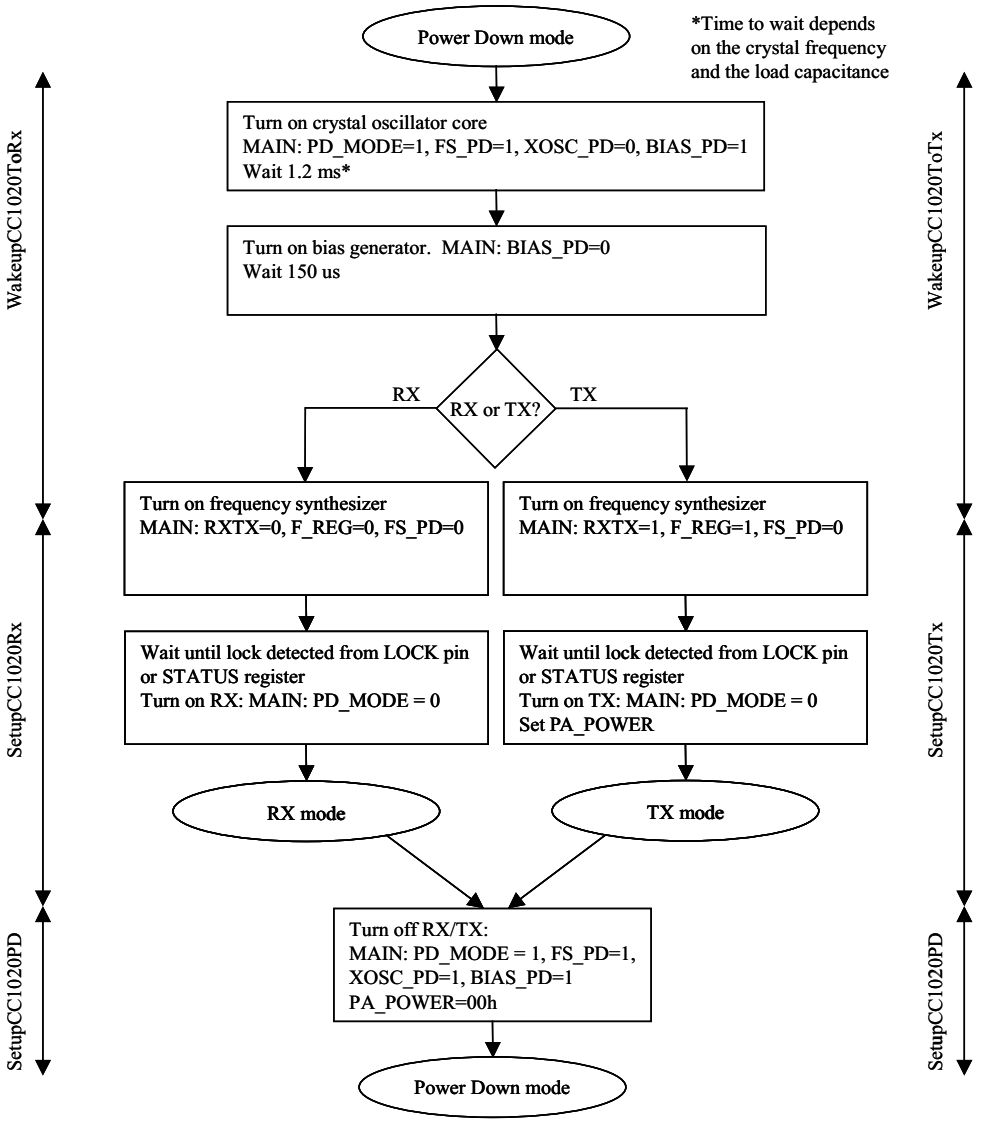

Figure 5-28. Sequence for Activating RX or TX Mode

5.15 On-Off Keying (OOK)

The data modulator can also provide OOK (On-Off Keying) modulation. OOK is an ASK (Amplitude Shift Keying) modulation using 100% modulation depth. OOK modulation is enabled in RX and in TX by setting TXDEV_M[3:0] = 0000 in the DEVIATION register. An OOK eye diagram is shown in Figure 5-29.

The data demodulator can also perform OOK demodulation. The demodulation is done by comparing the signal level with the "carrier sense" level (programmed as CS_LEVEL in the VGA4 register). The signal is then decimated and filtered in the data filter. Data decision and bit synchronization are as for FSK reception.

In this mode AGC_AVG in the VGA2 register must be set to 3. The channel bandwidth must be 4 times the Baud rate for data rates up to 9.6 kBaud. For the highest data rates the channel bandwidth must be 2 times the Baud rate (see Table 5-14). Manchester coding must always be used for OOK.

NOTE

The automatic frequency control (AFC) cannot be used when receiving OOK, as it requires a frequency shift.

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The AGC has a certain time-constant determined by FILTER_CLK, which depends on the IF filter bandwidth. There is a lower limit on FILTER_CLK and hence the AGC time constant. For low data rates the minimum time constant is too fast and the AGC will increase the gain when a "0" is received and decrease the gain when a "1" is received. For this reason, the minimum data rate in OOK is 9.6 kBaud.

Typical figures for the receiver sensitivity (BER = 10^{-3}) are shown in Table 5-14 for OOK.

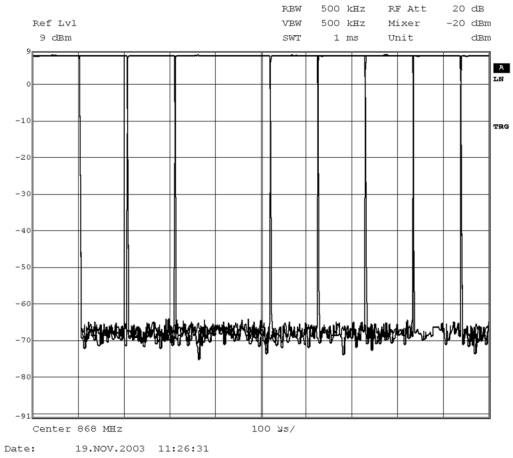

Figure 5-29. OOK Eye Diagram, 9.6 kBaud

Table 5-14. Typical Receiver Sensitivity as a Function of Data Rate at 433 and 868 MHz, OOK Modulation, BER = 10^{-3}, Pseudo-random Data (PN9 Sequence)

DATA RATE [kBaud]	FILTER BW [kHz]	SENSITIVITY [dBm]	
		433 MHz MANCHESTER MODE	868 MHz MANCHESTER MODE
9.6	38.4	–103	–104
19.2	51.2	–102	–101
38.4	102.4	–95	–97
76.8	153.6	–92	–94
153.6	307.2	–81	–87

5.16 Crystal Oscillator

The recommended crystal frequency is 14.7456 MHz, but any crystal frequency in the range 4 to 20 MHz can be used. Using a crystal frequency different from 14.7456 MHz might in some applications give degraded performance. Refer to Application Note *AN022 Crystal Frequency Selection* (SWRA070) for more details on the use of other crystal frequencies than 14.7456 MHz. The crystal frequency is used as reference for the data rate (as well as other internal functions) and in the 4 to 20 MHz range the frequencies 4.9152, 7.3728, 9.8304, 12.2880, 14.7456, 17.2032, 19.6608 MHz will give accurate data rates as shown in Table 5-4 and an IF frequency of 307.2 kHz. The crystal frequency will influence the programming of the CLOCK_A, CLOCK_B and MODEM registers.

An external clock signal or the internal crystal oscillator can be used as main frequency reference. An external clock signal should be connected to XOSC_Q1, while XOSC_Q2 should be left open. The XOSC_BYPASS bit in the INTERFACE register should be set to '1' when an external digital rail-to-rail clock signal is used. No DC block should be used then. A sine with smaller amplitude can also be used. A DC blocking capacitor must then be used (10 nF) and the XOSC_BYPASS bit in the INTERFACE register should be set to '0'. For input signal amplitude, see *Section 4.8*.

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Using the internal crystal oscillator, the crystal must be connected between the XOSC_Q1 and XOSC_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C4 and C5) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L , specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_4} + \frac{1}{C_5}} + C_{parasitic} \quad (33)$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 8 pF. A trimming capacitor may be placed across C5 for initial tuning if necessary.

The crystal oscillator circuit is shown in Figure 5-30. Typical component values for different values of C_L are given in Table 5-15.

The crystal oscillator is amplitude regulated. This means that a high current is required to initiate the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 600 mVpp amplitude. This ensures a fast start-up, keeps the drive level to a minimum and makes the oscillator insensitive to ESR variations. As long as the recommended load capacitance values are used, the ESR is not critical.

The initial tolerance, temperature drift, aging and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application. By specifying the total expected frequency accuracy in SmartRF Studio together with data rate and frequency separation, the software will estimate the total bandwidth and compare to the available receiver channel filter bandwidth. The software will report any contradictions and a more accurate crystal will be recommended if required.

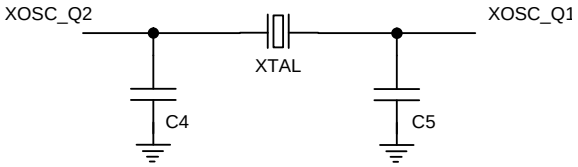

Figure 5-30. Crystal Oscillator Circuit

Table 5-15. Crystal Oscillator Component Values

ITEM	C_L = 12 pF	C_L = 16 pF	C_L = 22 pF
C4	6.8 pF	15 pF	27 pF
C5	6.8 pF	15 pF	27 pF

5.17 Built-in Test Pattern Generator

The CC1021 has a built-in test pattern generator that generates a PN9 pseudo random sequence. The PN9_ENABLE bit in the MODEM register enables the PN9 generator. A transition on the DIO pin is required after enabling the PN9 pseudo random sequence.

The PN9 pseudo random sequence is defined by the polynomial x9 + x5 + 1.

The PN9 sequence is 'XOR'ed with the DIO signal in both TX and RX mode as shown in Figure 5-31. Hence, by transmitting only zeros (DIO = 0), the BER (Bit Error Rate) can be tested by counting the number of received ones.

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NOTE

The nine first received bits should be discarded in this case. Also, one bit error will generate three received bit errors.

Transmitting only ones (DIO = 1), the BER can be tested by counting the number of received zeroes.

The PN9 generator can also be used for transmission of 'real-life' data when measuring narrowband ACP (Adjacent Channel Power), modulation bandwidth or occupied bandwidth.

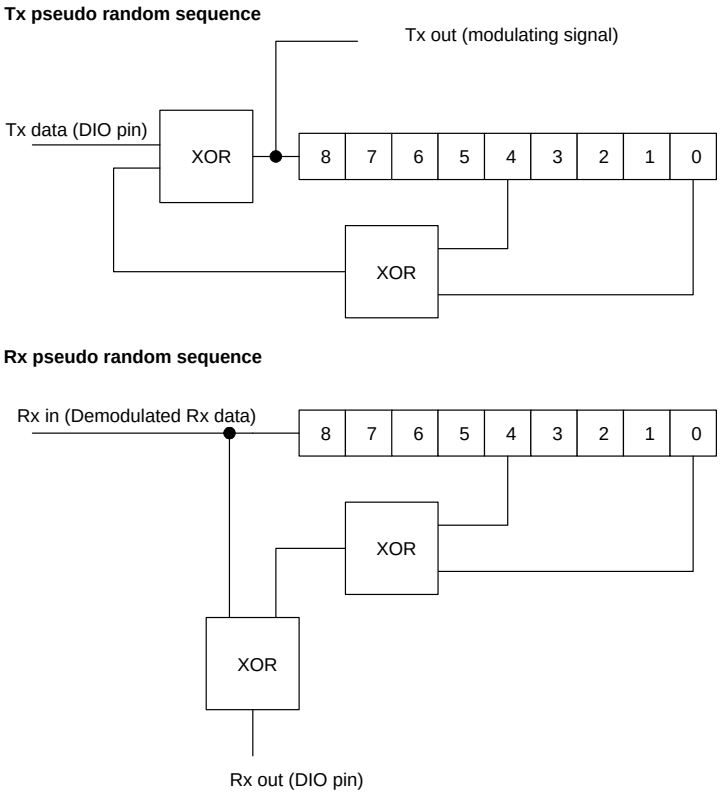

Figure 5-31. PN9 Pseudo Random Sequence Generator in TX and RX Mode

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5.18 Interrupt on Pin DCLK

5.18.1 Interrupt Upon PLL Lock

In synchronous mode the DCLK pin on CC1021 can be used to give an interrupt signal to wake the microcontroller when the PLL is locked.

PD_MODE[1:0] in the MAIN register should be set to 01. If DCLK_LOCK in the INTERFACE register is set to 1 the DCLK signal is always logic high if the PLL is not in lock. When the PLL locks to the desired frequency the DCLK signal changes to logic 0. When this interrupt has been detected write PD_MODE[1:0] = 00. This will enable the DCLK signal.

This function can be used to wait for the PLL to be locked before the PA is ramped up in transmit mode. In receive mode, it can be used to wait until the PLL is locked before searching for preamble.

5.18.2 Interrupt Upon Received Signal Carrier Sense

In synchronous mode the DCLK pin on CC1021 can also be used to give an interrupt signal to the microcontroller when the RSSI level exceeds a certain threshold (carrier sense threshold). This function can be used to wake or interrupt the microcontroller when a strong signal is received.

Gating the DCLK signal with the carrier sense signal makes the interrupt signal.

This function should only be used in receive mode and is enabled by setting DCLK_CS = 1 in the INTERFACE register.

The DCLK signal is always logic high unless carrier sense is indicated. When carrier sense is indicated the DCLK starts running. When gating the DCLK signal with the carrier sense signal at least 2 dummy bits should be added after the data payload in TX mode. The reason being that the carrier sense signal is generated earlier in the receive chain (that is, before the demodulator), causing it to be updated 2 bits before the corresponding data is available on the DIO pin.

In transmit mode DCLK_CS must be set to 0. Refer to *CC1021 Errata Note 001*, located in the CC1021 product folder.

5.19 PA_EN and LNA_EN Digital Output Pins

5.19.1 Interfacing an External LNA or PA

CC1021 has two digital output pins, PA_EN and LNA_EN, which can be used to control an external LNA or PA. The functionality of these pins are controlled through the INTERFACE register. The outputs can also be used as general digital output control signals.

EXT_PA_POL and EXT_LNA_POL control the active polarity of the signals.

EXT_PA and EXT_LNA control the function of the pins. If EXT_PA = 1, then the PA_EN pin will be activated when the internal PA is turned on. Otherwise, the EXT_PA_POL bit controls the PA_EN pin directly. If EXT_LNA = 1, then the LNA_EN pin will be activated when the internal LNA is turned on. Otherwise, the EXT_LNA_POL bit controls the LNA_EN pin directly.

These two pins can therefore also be used as two general control signals, *Section 5.19.2*. In the TI reference design, LNA_EN and PA_EN are used to control the external T/R switch.

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5.19.2 General Purpose Output Control Pins

The two digital output pins, PA_EN and LNA_EN, can be used as two general control signals by setting EXT_PA = 0 and EXT_LNA = 0. The output value is then set directly by the value written to EXT_PA_POL and EXT_LNA_POL.

The LOCK pin can also be used as a general-purpose output pin. The LOCK pin is controlled by LOCK_SELECT[3:0] in the LOCK register. The LOCK pin is low when LOCK_SELECT[3:0] = 0000, and high when LOCK_SELECT[3:0] = 0001.

These features can be used to save I/O pins on the microcontroller when the other functions associated with these pins are not used.

5.19.3 PA_EN and LNA_EN Pin Drive

Figure 5-32 shows the PA_EN and LNA_EN pin drive currents. The sink and source currents have opposite signs but absolute values are used in Figure 5-32.

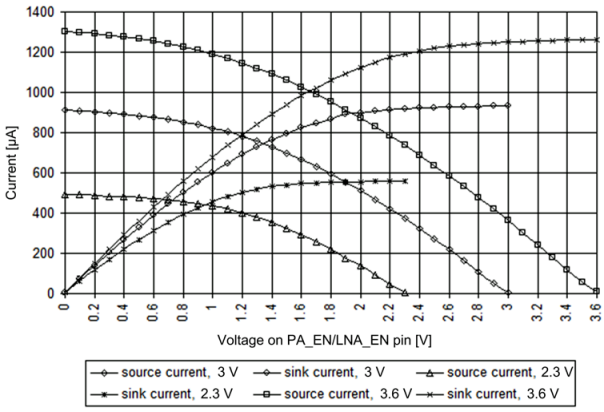

Figure 5-32. PA_EN and LNA_EN Pin Drive

5.20 System Considerations and Guidelines

5.20.1 SRD Regulations

International regulations and national laws regulate the use of radio receivers and transmitters. SRDs (Short Range Devices) for license free operation are allowed to operate in the 433 and 868 to 870 MHz bands in most European countries. In the United States, such devices operate in the 260 to 470 and 902 to 928 MHz bands. A summary of the most important aspects of these regulations can be found in Application Note *AN001 SRD Regulations for License Free Transceiver Operation* (SWRA090).

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5.20.2 Narrowband Systems

CC1021 is recommended for narrowband applications with channel spacing of 50 kHz and higher complying with FCC CFR47 part 15 and EN 300 220.

CC1020 is recommended in narrowband applications with channel spacing of 12.5 or 25 kHz complying with ARIB STD T-67 and EN 300 220.

CC1020 and CC1021 are fully compatible for channel spacings of 50 kHz and higher (receiver channel filter bandwidths of 38.4 kHz and higher).

Due to on-chip complex filtering, the image frequency is removed. An on-chip calibration circuit is used to get the best possible image rejection. A narrowband preselector filter is not necessary to achieve image rejection.

A unique feature in CC1021 is the very fine frequency resolution. This can be used for temperature compensation of the crystal if the temperature drift curve is known and a temperature sensor is included in the system. Even initial adjustment can be performed using the frequency programmability. This eliminates the need for an expensive TCXO and trimming in some applications. For more details refer to Application Note *AN027 Temperature Compensation by Indirect Method* (SWRA065).

In less demanding applications, a crystal with low temperature drift and low aging could be used without further compensation. A trimmer capacitor in the crystal oscillator circuit (in parallel with C5) could be used to set the initial frequency accurately.

The frequency offset between a transmitter and receiver is measured in the CC1021 and can be read back from the AFC register. The measured frequency offset can be used to calibrate the receiver frequency using the transmitter as the reference. For more details refer to Application Note *AN029 CC1020/1021 Automatic Frequency Control (AFC)* (SWRA063).

CC1021 also has the possibility to use Gaussian shaped FSK (GFSK). This spectrum-shaping feature improves adjacent channel power (ACP) and occupied bandwidth. In ‘true’ FSK systems with abrupt frequency shifting, the spectrum is inherently broad. By making the frequency shift ‘softer’, the spectrum can be made significantly narrower. Thus, higher data rates can be transmitted in the same bandwidth using GFSK.

5.20.3 Low Cost Systems

As the CC1021 provide true narrowband multi-channel performance without any external filters, a very low cost high performance system can be achieved. The oscillator crystal can then be a low cost crystal with 50 ppm frequency tolerance using the on-chip frequency tuning possibilities.

5.20.4 Battery Operated Systems

In low power applications, the power down mode should be used when CC1021 is not being active. Depending on the start-up time requirement, the oscillator core can be powered during power down. See *Section 5.14* for information on how effective power management can be implemented.

5.20.5 High Reliability Systems

Using a SAW filter as a preselector will improve the communication reliability in harsh environments by reducing the probability of blocking. The receiver sensitivity and the output power will be reduced due to the filter insertion loss. By inserting the filter in the RX path only, together with an external RX/TX switch, only the receiver sensitivity is reduced and output power is remained. The PA_EN and LNA_EN pin can be configured to control an external LNA, RX/TX switch or power amplifier. This is controlled by the INTERFACE register.

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5.20.6 Frequency Hopping Spread Spectrum Systems (FHSS)

Due to the very fast locking properties of the PLL, the CC1021 is also very suitable for frequency hopping systems. Hop rates of 1 to 100 hops/s are commonly used depending on the bit rate and the amount of data to be sent during each transmission. The two frequency registers (FREQ_A and FREQ_B) are designed such that the 'next' frequency can be programmed while the 'present' frequency is used. The switching between the two frequencies is done through the MAIN register. Several features have been included to do the hopping without a need to re-synchronize the receiver. For more details refer to Application Note *AN014 Frequency Hopping Systems* (SWRA077).

In order to implement a frequency hopping system with CC1021 do the following:

1. Set the desired frequency, calibrate and store the following register settings in non-volatile memory:

   STATUS1[3:0]: CHP_CURRENT[3:0]
   STATUS2[4:0]: VCO_ARRAY[4:0]
   STATUS3[5:0]:VCO_CAL_CURRENT[5:0]

2. Repeat the calibration for each desired frequency. VCO_CAL_CURRENT[5:0] is not dependent on the RF frequency and the same value can be used for all frequencies. When performing frequency hopping, write the stored values to the corresponding TEST1, TEST2 and TEST3 registers, and enable override:

   TEST1[3:0]: CHP_CO[3:0]
   TEST2[4:0]: VCO_AO[4:0]
   TEST2[5]: VCO_OVERRIDE
   TEST2[6]: CHP_OVERRIDE
   TEST3[5:0]:VCO_CO[5:0]
   TEST3[6]:VCO_CAL_OVERRIDE

3. CHP_CO[3:0] is the register setting read from CHP_CURRENT[3:0], VCO_AO[4:0] is the register setting read from VCO_ARRAY[4:0] and VCO_CO[5:0] is the register setting read from VCO_CAL_CURRENT[5:0].
4. Assume channel 1 defined by register FREQ_A is currently being used and that CC1021 should operate on channel 2 next (to change channel simply write to register MAIN[6]). The channel 2 frequency can be set by register FREQ_B which can be written to while operating on channel 1. The calibration data must be written to the TEST1-3 registers after switching to the next frequency. That is, when hopping to a new channel write to register MAIN[6] first and the test registers next. The PA should be switched off between each hop and the PLL should be checked for lock before switching the PA back on after a hop has been performed.

NOTE

The override bits VCO_OVERRIDE, CHP_OVERRIDE and VCO_CAL_OVERRIDE must be disabled when performing a re-calibration.

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5.21 Antenna Considerations

CC1021 can be used together with various types of antennas. The most common antennas for short-range communication are monopole, helical and loop antennas.

Monopole antennas are resonant antennas with a length corresponding to one quarter of the electrical wavelength ($\frac{\lambda}{4}$). They are very easy to design and can be implemented simply as a “piece of wire” or even integrated onto the PCB.

Non-resonant monopole antennas shorter than $\frac{\lambda}{4}$ can also be used, but at the expense of range. In size and cost critical applications such an antenna may very well be integrated onto the PCB.

Helical antennas can be thought of as a combination of a monopole and a loop antenna. They are a good compromise in size critical applications. But helical antennas tend to be more difficult to optimize than the simple monopole.

Loop antennas are easy to integrate into the PCB, but are less effective due to difficult impedance matching because of their very low radiation resistance.

For low-power applications, the $\frac{\lambda}{4}$ monopole antenna is recommended due to its simplicity as well as providing the best range.

The length of the $\frac{\lambda}{4}$ monopole antenna is given by:

$$L = \frac{7125}{f} \quad (34)$$

Where:

f is in MHz, giving the length in cm.

An antenna for 868 MHz should be 8.2 cm, and 16.4 cm for 433 MHz.

The antenna should be connected as close as possible to the IC. If the antenna is located away from the input pin the antenna should be matched to the feeding transmission line (50 Ω).

For a more thorough background on antennas, please refer to Application Note *AN003 SRD Antennas* (SWRA088).

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5.22 Configuration Registers

The configuration of CC1021 is done by programming the 8-bit configuration registers. The configuration data based on selected system parameters are most easily found by using the SmartRF Studio software. Complete descriptions of the registers are given in the *Section 5.22.1* section. After a RESET is programmed, all the registers have default values. The TEST registers also get default values after a RESET, and should not be altered by the user.

TI recommends using the register settings found using the SmartRF Studio software. These are the register settings that TI specifies across temperature, voltage and process. Check the TI web site for regularly updates to the SmartRF Studio software.

Table 5-16. CC1021 Register Overview

ADDRESS	ACRONYM	REGISTER NAME
00h	MAIN	Main control register
01h	INTERFACE	Interface control register
02h	RESET	Digital module reset register
03h	SEQUENCING	Automatic power-up sequencing control register
04h	FREQ_2A	Frequency register 2A
05h	FREQ_1A	Frequency register 1A
06h	FREQ_0A	Frequency register 0A
07h	CLOCK_A	Clock generation register A
08h	FREQ_2B	Frequency register 2B
09h	FREQ_1B	Frequency register 1B
0Ah	FREQ_0B	Frequency register 0B
0Bh	CLOCK_B	Clock generation register B
0Ch	VCO	VCO current control register
0Dh	MODEM	Modem control register
0Eh	DEVIATION	TX frequency deviation register
0Fh	AFC_CONTROL	RX AFC control register
10h	FILTER	Channel filter / RSSI control register
11h	VGA1	VGA control register 1
12h	VGA2	VGA control register 2
13h	VGA3	VGA control register 3
14h	VGA4	VGA control register 4
15h	LOCK	Lock control register
16h	FRONTEND	Front end bias current control register
17h	ANALOG	Analog modules control register
18h	BUFF_SWING	LO buffer and prescaler swing control register
19h	BUFF_CURRENT	LO buffer and prescaler bias current control register
1Ah	PLL_BW	PLL loop bandwidth / charge pump current control register
1Bh	CALIBRATE	PLL calibration control register
1Ch	PA_POWER	Power amplifier output power register
1Dh	MATCH	Match capacitor array control register, for RX and TX impedance matching
1Eh	PHASE_COMP	Phase error compensation control register for LO I/Q
1Fh	GAIN_COMP	Gain error compensation control register for mixer I/Q
20h	POWERDOWN	Power-down control register
21h	TEST1	Test register for overriding PLL calibration
22h	TEST2	Test register for overriding PLL calibration
23h	TEST3	Test register for overriding PLL calibration
24h	TEST4	Test register for charge pump and IF chain testing

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Table 5-16. CC1021 Register Overview (continued)

ADDRESS	ACRONYM	REGISTER NAME
25h	TEST5	Test register for ADC testing
26h	TEST6	Test register for VGA testing
27h	TEST7	Test register for VGA testing
40h	STATUS	Status information register (PLL lock, RSSI, calibration ready, and so on)
41h	RESET_DONE	Status register for digital module reset
42h	RSSI	Received signal strength register
43h	AFC	Average received frequency deviation from IF (can be used for AFC)
44h	GAUSS_FILTER	Digital FM demodulator register
45h	STATUS1	Status of PLL calibration results and so on (test only)
46h	STATUS2	Status of PLL calibration results and so on (test only)
47h	STATUS3	Status of PLL calibration results and so on (test only)
48h	STATUS4	Status of ADC signals (test only)
49h	STATUS5	Status of channel filter “I” signal (test only)
4Ah	STATUS6	Status of channel filter “Q” signal (test only)
4Bh	STATUS7	Status of AGC (test only)

5.22.1 Memory

Table 5-17. MAIN Register (00h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
MAIN[7]	RXTX	—	—	RX/TX switch, 0: RX , 1: TX
MAIN[6]	F_REG	—	—	Selection of Frequency Register, 0: Register A, 1: Register B
MAIN[5:4]	PD_MODE[1:0]	—	—	Power down mode 0 (00): Receive Chain in power-down in TX, PA in power-down in RX 1 (01): Receive Chain and PA in power down in both TX and RX 2 (10): Individual modules can be put in power down by programming the POWERDOWN register 3 (11): Automatic power-up sequencing is activated (see Table 5-18)
MAIN[3]	FS_PD	—	H	Power Down of Frequency Synthesizer
MAIN[2]	XOSC_PD	—	H	Power Down of Crystal Oscillator Core
MAIN[1]	BIAS_PD	—	H	Power Down of BIAS (Global Current Generator) and Crystal Oscillator Buffer
MAIN[0]	RESET_N	—	L	Reset, active low. Writing RESET_N low will write default values to all other registers than MAIN. Bits in MAIN do not have a default value and will be written directly through the configuration interface. Must be set high to complete reset.

Table 5-18. MAIN Register (00h) When Using Automatic Power-up Sequencing (RXTX = 0, PD_MODE[1:0] =11)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
MAIN[7]	RXTX	—	—	Automatic power-up sequencing only works in RX (RXTX=0)
MAIN[6]	F_REG	—	—	Selection of Frequency Register, 0: Register A, 1: Register B
MAIN[5:4]	PD_MODE[1:0]	—	H	Set PD_MODE[1:0]=3 (11) to enable sequencing

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Table 5-18. MAIN Register (00h) When Using Automatic Power-up Sequencing (RXTX = 0, PD_MODE[1:0] =11) (continued)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
MAIN[3:2]	SEQ_CAL[1:0]	—	—	Controls PLL calibration before re-entering power down 0: Never perform PLL calibration as part of sequence 1: Always perform PLL calibration at end of sequence 2: Perform PLL calibration at end of every 16th sequence 3: Perform PLL calibration at end of every 256th sequence
MAIN[1]	SEQ_PD	—	↑	↑1: Put the chip in power down and wait for start of new power-up sequence
MAIN[0]	RESET_N	—	L	Reset, active low. Writing RESET_N low will write default values to all other registers than MAIN. Bits in MAIN do not have a default value and will be written directly through the configuration interface. Must be set high to complete reset.

Table 5-19. INTERFACE Register (01h)(1)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
INTERFACE[7]	XOSC_BYPASS	0	H	Bypass internal crystal oscillator, use external clock 0: Internal crystal oscillator is used, or external sine wave fed through a coupling capacitor 1: Internal crystal oscillator in power down, external clock with rail-to-rail swing is used
INTERFACE[6]	SEP_DI_DO	0	H	Use separate pin for RX data output 0: DIO is data output in RX and data input in TX. LOCK pin is available (Normal operation). 1: DIO is always input, and a separate pin is used for RX data output (synchronous mode: LOCK pin, asynchronous mode: DCLK pin). If SEP_DI_DO=1 and SEQ_PSEL=0 in SEQUENCING register then negative transitions on DIO is used to start power-up sequencing when PD_MODE=3 (power-up sequencing is enabled).
INTERFACE[5]	DCLK_LOCK	0	H	Gate DCLK signal with PLL lock signal in synchronous mode Only applies when PD_MODE = “01” 0: DCLK is always 1 1: DCLK is always 1 unless PLL is in lock
INTERFACE[4]	DCLK_CS	0	H	Gate DCLK signal with carrier sense indicator in synchronous mode Use when receive chain is active (in power up) Always set to 0 in TX mode. 0: DCLK is independent of carrier sense indicator. 1: DCLK is always 1 unless carrier sense is indicated
INTERFACE[3]	EXT_PA	0	H	Use PA_EN pin to control external PA 0: PA_EN pin always equals EXT_PA_POL bit 1: PA_EN pin is asserted when internal PA is turned on
INTERFACE[2]	EXT_LNA	0	H	Use LNA_EN pin to control external LNA 0: LNA_EN pin always equals EXT_LNA_POL bit 1: LNA_EN pin is asserted when internal LNA is turned on
INTERFACE[1]	EXT_PA_POL	0	H	Polarity of external PA control 0: PA_EN pin is “0” when activating external PA 1: PA_EN pin is “1” when activating external PA
INTERFACE[0]	EXT_LNA_POL	0	H	Polarity of external LNA control 0: LNA_EN pin is “0” when activating external LNA 1: LNA_EN pin is “1” when activating external LNA

(1) If TF_ENABLE=1 or TA_ENABLE=1 in TEST4 register, then INTERFACE[3:0] controls analog test module: INTERFACE[3] = TEST_PD, INTERFACE[2:0] = TEST_MODE[2:0]. Otherwise, TEST_PD=1 and TEST_MODE[2:0]=001.

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Table 5-20. RESET Register (02h)(1)(2)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
RESET[7]	ADC_RESET_N	0	L	Reset ADC control logic
RESET[6]	AGC_RESET_N	0	L	Reset AGC (VGA control) logic
RESET[5]	GAUSS_RESET_N	0	L	Reset Gaussian data filter
RESET[4]	AFC_RESET_N	0	L	Reset AFC / FSK decision level logic
RESET[3]	BITSYNC_RESET_N	0	L	Reset modulator, bit synchronization logic and PN9 PRBS generator
RESET[2]	SYNTH_RESET_N	0	L	Reset digital part of frequency synthesizer
RESET[1]	SEQ_RESET_N	0	L	Reset power-up sequencing logic
RESET[0]	CAL_LOCK_RESET_N	0	L	Reset calibration logic and lock detector

(1) For reset of CC1020 write RESET_N=0 in the MAIN register. The reset register should not be used during normal operation.
(2) Bits in the RESET register are self-clearing (will be set to 1 when the reset operation starts). Relevant digital clocks must be running for the resetting to complete. After writing to the RESET register, the user should verify that all reset operations have been completed, by reading the RESET_DONE status register (41h) until all bits equal 1.

Table 5-21. SEQUENCING Register (03h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
SEQUENCING[7]	SEQ_PSEL	1	H	Use PSEL pin to start sequencing 0: PSEL pin does not start sequencing. Negative transitions on DIO starts power-up sequencing if SEP_DI_DO=1. 1: Negative transitions on the PSEL pin will start power-up sequencing
SEQUENCING[6:4]	RX_WAIT[2:0]	0	—	Waiting time from PLL enters lock until RX power up 0: Wait for approx. 32 ADC_CLK periods (26 µs) 1: Wait for approx. 44 ADC_CLK periods (36 µs) 2: Wait for approx. 64 ADC_CLK periods (52 µs) 3: Wait for approx. 88 ADC_CLK periods (72 µs) 4: Wait for approx. 128 ADC_CLK periods (104 µs) 5: Wait for approx. 176 ADC_CLK periods (143 µs) 6: Wait for approx. 256 ADC_CLK periods (208 µs) 7: No additional waiting time before RX power up
SEQUENCING[3:0]	CS_WAIT[3:0]	10	—	Waiting time for carrier sense from RX power up 0: Wait 20 FILTER_CLK periods before power down 1: Wait 22 FILTER_CLK periods before power down 2: Wait 24 FILTER_CLK periods before power down 3: Wait 26 FILTER_CLK periods before power down 4: Wait 28 FILTER_CLK periods before power down 5: Wait 30 FILTER_CLK periods before power down 6: Wait 32 FILTER_CLK periods before power down 7: Wait 36 FILTER_CLK periods before power down 8: Wait 40 FILTER_CLK periods before power down 9: Wait 44 FILTER_CLK periods before power down 10: Wait 48 FILTER_CLK periods before power down 11: Wait 52 FILTER_CLK periods before power down 12: Wait 56 FILTER_CLK periods before power down 13: Wait 60 FILTER_CLK periods before power down 14: Wait 64 FILTER_CLK periods before power down 15: Wait 72 FILTER_CLK periods before power down

Table 5-22. FREQ_2A Register (04h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
FREQ_2A[7:0]	FREQ_A[22:15]	131	—	8 MSB of frequency control word A

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Table 5-23. FREQ_1A Register (05h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
FREQ_1A[7:0]	FREQ_1A[7:0]	177	—	Bit 15 to 8 of frequency control word A

Table 5-24. FREQ_0A Register (06h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
FREQ_0A[7:1]	FREQ_A[6:0]	124	—	7 LSB of frequency control word A
FREQ_0A[0]	DITHER_A	1	H	Enable dithering for frequency A

Table 5-25. CLOCK_A Register (07h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
CLOCK_A[7:5]	REF_DIV_A[2:0]	2	—	Reference frequency divisor (A): 0: Not supported 1: REF_CLK frequency = Crystal frequency / 2 … 7: REF_CLK frequency = Crystal frequency / 8 It is recommended to use the highest possible reference clock frequency that allows the desired Baud rate.
CLOCK_A[4:2]	MCLK_DIV1_A[2:0]	4	—	Modem clock divider 1 (A): 0: Divide by 2.5 1: Divide by 3 2: Divide by 4 3: Divide by 7.5 (2.5 × 3) 4: Divide by 12.5 (2.5 × 5) 5: Divide by 40 (2.5 × 16) 6: Divide by 48 (3 × 16) 7: Divide by 64 (4 × 16)
CLOCK_A[1:0]	MCLK_DIV2_A[1:0]	0	—	Modem clock divider 2 (A): 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 MODEM_CLK frequency is FREF frequency divided by the product of divider 1 and divider 2. Baud rate is MODEM_CLK frequency divided by 8.

Table 5-26. FREQ_2B Register (08h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
FREQ_2B[7:0]	FREQ_B[22:15]	131	—	8 MSB of frequency control word B

Table 5-27. FREQ_1B Register (09h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
FREQ_1B[7:0]	FREQ_B[14:7]	189	—	8 MSB of frequency control word B

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Table 5-28. FREQ_0B Register (0Ah)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
FREQ_0B[7:1]	FREQ_B[6:0]	124	—	7 LSB of frequency control word B
FREQ_0B[0]	DITHER_B	1	H	Enable dithering for frequency B

Table 5-29. CLOCK_B Register (0Bh)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
CLOCK_B[7:5]	REF_DIV_B[2:0]	2	—	Reference frequency divisor (B): 0: Not supported 1: REF_CLK frequency = Crystal frequency / 2 … 7: REF_CLK frequency = Crystal frequency / 8
CLOCK_B[4:2]	MCLK_DIV1_B[2:0]	4	—	Modem clock divider 1 (B): 0: Divide by 2.5 1: Divide by 3 2: Divide by 4 3: Divide by 7.5 (2.5 × 3) 4: Divide by 12.5 (2.5 × 5) 5: Divide by 40 (2.5 × 16) 6: Divide by 48 (3 × 16) 7: Divide by 64 (4 × 16)
CLOCK_B[1:0]	MCLK_DIV2_B[1:0]	0	—	Modem clock divider 2 (B): 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 MODEM_CLK frequency is FREF frequency divided by the product of divider 1 and divider 2. Baud rate is MODEM_CLK frequency divided by 8.

Table 5-30. VCO Register (0Ch)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
VCO[7:4]	VCO_CURRENT_A[3:0]	8	—	Control of current in VCO core for frequency A 0 : 1.4 mA current in VCO core 1 : 1.8 mA current in VCO core 2 : 2.1 mA current in VCO core 3 : 2.5 mA current in VCO core 4 : 2.8 mA current in VCO core 5 : 3.2 mA current in VCO core 6 : 3.5 mA current in VCO core 7 : 3.9 mA current in VCO core 8 : 4.2 mA current in VCO core 9 : 4.6 mA current in VCO core 10 : 4.9 mA current in VCO core 11 : 5.3 mA current in VCO core 12 : 5.6 mA current in VCO core 13 : 6.0 mA current in VCO core 14 : 6.4 mA current in VCO core 15 : 6.7 mA current in VCO core Recommended setting: VCO_CURRENT_A=4
VCO[3:0]	VCO_CURRENT_B[3:0]	8	—	Control of current in VCO core for frequency B The current steps are the same as for VCO_CURRENT_A Recommended setting: VCO_CURRENT_B=4

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Table 5-31. MODEM Register (0Dh)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
MODEM[7]	—	0	—	Reserved, write 0
MODEM[6:4]	ADC_DIV[2:0]	3	—	ADC clock divisor(1) 0: Not supported 1: ADC frequency = XOSC frequency / 4 2: ADC frequency = XOSC frequency / 6 3: ADC frequency = XOSC frequency / 8 4: ADC frequency = XOSC frequency / 10 5: ADC frequency = XOSC frequency / 12 6: ADC frequency = XOSC frequency / 14 7: ADC frequency = XOSC frequency / 16
MODEM[3]	—	0	—	Reserved, write 0
MODEM[2]	PN9_ENABLE	0	H	Enable scrambling of TX and RX with PN9 pseudo-random bit sequence 0: PN9 scrambling is disabled 1: PN9 scrambling is enabled ($x^9 + x^5 + 1$) The PN9 pseudo-random bit sequence can be used for BER testing by only transmitting zeros, and then counting the number of received ones.
MODEM[1:0]	DATA_FORMAT[1:0]	0	—	Modem data format 0 (00): NRZ operation 1 (01): Manchester operation 2 (10): Transparent asynchronous UART operation, set DCLK=0 3 (11): Transparent asynchronous UART operation, set DCLK=1

(1) The intermediate frequency should be as close to 307.2 kHz as possible. ADC clock frequency is always 4 times the intermediate frequency and should therefore be as close to 1.2288 MHz as possible.

Table 5-32. DEVIATION Register (0Eh)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
DEVIATION[7]	TX_SHAPING	1	H	Enable Gaussian shaping of transmitted data Recommended setting: TX_SHAPING=1
DEVIATION[6:4]	TXDEV_X[2:0]	6	—	Transmit frequency deviation exponent
DEVIATION [3:0]	TXDEV_M[3:0]	8	—	Transmit frequency deviation mantissa Deviation in 402 to 470 MHz band: $F_{REF} \times XDEV_M \times 2^{(TXDEV_X-16)}$ Deviation in 804 to 960 MHz band: $F_{REF} \times TXDEV_M \times 2^{(TXDEV_X-15)}$ On-off-keying (OOK) is used in RX/TX if TXDEV_M[3:0]=0 To find TXDEV_M given the deviation and TXDEV_X: $TXDEV_M = deviation \times 2^{(16-TXDEV_X)} / F_{REF}$ in 402 to 470 MHz band, $TXDEV_M = deviation \times 2^{(15-TXDEV_X)} / F_{REF}$ in 804 to 960 MHz band, Decrease TXDEV_X and try again if TXDEV_M < 8. Increase TXDEV_X and try again if TXDEV_M ≥ 16.

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Table 5-33. AFC_CONTROL Register (0Fh)(1)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
AFC_CONTROL[7:6]	SETTLING[1:0]	2	—	Controls AFC settling time versus accuracy 0: AFC off; zero average frequency is used in demodulator 1: Fastest settling; frequency averaged over 1 0/1 bit pair 2: Medium settling; frequency averaged over 2 0/1 bit pairs 3: Slowest settling; frequency averaged over 4 0/1 bit pairs Recommended setting: AFC_CONTROL=3 for higher accuracy unless it is essential to have the fastest settling time when transmission starts after RX is activated.
AFC_CONTROL[5:4]	RXDEV_X[1:0]	1	—	RX frequency deviation exponent
AFC_CONTROL[3:0]	RXDEV_M[3:0]	12	—	RX frequency deviation mantissa Expected RX deviation should be: Baud rate × RXDEV_M × $2^{(RXDEV_X-3)}$ / 3 To find RXDEV_M given the deviation and RXDEV_X: RXDEV_M = 3 × deviation × $2^{(3-RXDEV_X)}$ / Baud rate Decrease RXDEV_X and try again if RXDEV_M < 8. Increase RXDEV_X and try again if RXDEV_M ≥ 16.

(1) The RX frequency deviation should be close to half the TX frequency deviation for GFSK at 100 kBaud data rate and below. The RX frequency deviation should be close to the TX frequency deviation for FSK and for GFSK at 100 kBaud data rate and above.

Table 5-34. FILTER Register (10h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
FILTER[7]	FILTER_BYPASS	0	H	Bypass analog image rejection / anti-alias filter. Set to 1 for increased dynamic range at high Baud rates. Recommended setting: FILTER_BYPASS=0 below 76.8 kBaud, FILTER_BYPASS=1 for 76.8 kBaud and up.
FILTER[6:5]	DEC_SHIFT[1:0]	0	—	Number of extra bits to shift decimator input (may improve filter accuracy and lower power consumption). Recommended settings: DEC_SHIFT=0 when DEC_DIV ≤ 1 (receiver channel bandwidth ≥ 153.6 kHz), DEC_SHIFT=1 when DEC_DIV > 1 (receiver channel bandwidth < 153.6 kHz)
FILTER[4:3]	—	—	—	Reserved
FILTER[2:0]	DEC_DIV[2:0]	0	—	Decimation clock divisor 0: Decimation clock divisor = 1, 307.2 kHz channel filter BW. 1: Decimation clock divisor = 2, 153.6 kHz channel filter BW. … 6: Decimation clock divisor = 7, 43.9 kHz channel filter BW. 31: Decimation clock divisor = 8, 38.4 kHz channel filter BW. Channel filter bandwidth is 307.2 kHz divided by the decimation clock divisor.

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Table 5-35. VGA1 Register (11h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
VGA1[7:6]	CS_SET[1:0]	1	—	Sets the number of consecutive samples at or above carrier sense level before carrier sense is indicated (for example, on LOCK pin) 0: Set carrier sense after first sample at or above carrier sense level 1: Set carrier sense after second sample at or above carrier sense level 2: Set carrier sense after third sample at or above carrier sense level 3: Set carrier sense after fourth sample at or above carrier sense level Increasing CS_SET reduces the number of “false” carrier sense events due to noise at the expense of increased carrier sense response time.
VGA1[5]	CS_RESET	1	—	Sets the number of consecutive samples below carrier sense level before carrier sense indication (for example, on lock pin) is reset 0: Carrier sense is reset after first sample below carrier sense level 1: Carrier sense is reset after second sample below carrier sense level Recommended setting: CS_RESET=1 in order to reduce the chance of losing carrier sense due to noise.
VGA1[4:2]	VGA_WAIT[2:0]	1	—	Controls how long AGC, bit synchronization, AFC and RSSI levels are frozen after VGA gain is changed when frequency is changed between A and B or PLL has been out of lock or after RX power up 0: Freeze operation for 16 filter clocks, 8 / (filter BW) seconds 1: Freeze operation for 20 filter clocks, 10 / (filter BW) seconds 2: Freeze operation for 24 filter clocks, 12 / (filter BW) seconds 3: Freeze operation for 28 filter clocks, 14 / (filter BW) seconds 4: Freeze operation for 32 filter clocks, 16 / (filter BW) seconds 5: Freeze operation for 40 filter clocks, 20 / (filter BW) seconds 6: Freeze operation for 48 filter clocks, 24 / (filter BW) seconds 7: Freeze present levels unconditionally
VGA1[1:0]	VGA_FREEZE[1:0]	1	—	Controls the additional time AGC, bit synchronization, AFC and RSSI levels are frozen when frequency is changed between A and B or PLL has been out of lock or after RX power up 0: Freeze levels for approx. 16 ADC_CLK periods (13 µs) 1: Freeze levels for approx. 32 ADC_CLK periods (26 µs) 2: Freeze levels for approx. 64 ADC_CLK periods (52 µs) 3: Freeze levels for approx. 128 ADC_CLK periods (104 µs)

Table 5-36. VGA2 Register (12h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
VGA2[7]	LNA2_MIN	0	—	Minimum LNA2 setting used in VGA 0: Minimum LNA2 gain 1: Medium LNA2 gain Recommended setting: LNA2_MIN=0 for best selectivity.
VGA2[6]	LNA2_MAX	1	—	Maximum LNA2 setting used in VGA 0: Medium LNA2 gain 1: Maximum LNA2 gain Recommended setting: LNA2_MAX=1 for best sensitivity.

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Table 5-36. VGA2 Register (12h) (continued)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
VGA2[5:4]	LNA2_SETTING[1:0]	3	—	Selects at what VGA setting the LNA gain should be changed 0: Apply LNA2 change below min. VGA setting. 1: Apply LNA2 change at approx. 1/3 VGA setting (around VGA setting 10). 2: Apply LNA2 change at approx. 2/3 VGA setting (around VGA setting 19). 3: Apply LNA2 change above max. VGA setting. Recommended setting: LNA2_SETTING=0 if VGA_SETTING<10, LNA2_SETTING=1 otherwise. If LNA2_MIN=1 and LNA2_MAX=0, then the LNA2 setting is controlled by LNA2_SETTING: 0: Between medium and maximum LNA2 gain 1: Minimum LNA2 gain 2: Medium LNA2 gain 3: Maximum LNA2 gain
VGA2[3]	AGC_DISABLE	0	H	Disable AGC 0: AGC is enabled 1: AGC is disabled (VGA_SETTING determines VGA gain) Recommended setting: AGC_DISABLE=0 for good dynamic range.
VGA2[2]	AGC_HYSTERESIS	1	H	Enable AGC hysteresis 0: No hysteresis. Immediate gain change for smallest up/down step 1: Hysteresis enabled. Two samples in a row must indicate gain change for smallest up or down step Recommended setting: AGC_HYSTERESIS=1.
VGA2[1:0]	AGC_AVG[1:0]	1	—	Sets how many samples that are used to calculate average output magnitude for AGC/RSSI. 0: Magnitude is averaged over 2 filter output samples 1: Magnitude is averaged over 4 filter output samples 2: Magnitude is averaged over 8 filter output samples 3: Magnitude is averaged over 16 filter output samples Recommended setting: AGC_AVG=1. For best AGC/RSSI accuracy AGC_AVG=3. For automatic power-up sequencing, the AGC_AVG and CS_SET values must be chosen so that carrier sense is available in time to be detected before the chip re-enters power down.

Table 5-37. VGA3 Register (13h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
VGA3[7:5]	VGA_DOWN[2:0]	1	—	Decides how much the signal strength must be above CS_LEVEL+VGA_UP before VGA gain is decreased. 0: Gain is decreased 4.5 dB above CS_LEVEL+ VGA_UP 1: Gain is decreased 6 dB above CS_LEVEL+ VGA_UP … 6: Gain is decreased 13.5 dB above CS_LEVEL+ VGA_UP 7: Gain is decreased 15 dB above CS_LEVEL+ VGA_UP See Figure 5-17 for an explanation of the relationship between RSSI, AGC and carrier sense settings.
VGA3[4:0]	VGA_SETTING[4:0]	24	H	VGA setting to be used when receive chain is turned on This is also the maximum gain that the AGC is allowed to use. See Figure 5-17 for an explanation of the relationship between RSSI, AGC and carrier sense settings.

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Table 5-38. VGA4 Register (14h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
VGA4[7:5]	VGA_UP[2:0]	1	—	Decides the level where VGA gain is increased if it is not already at the maximum set by VGA_SETTING. 0: Gain is increased when signal is below CS_LEVEL 1: Gain is increased when signal is below CS_LEVEL+ 1.5 dB … 6: Gain is increased when signal is below CS_LEVEL+ 9 dB 7: Gain is increased when signal below CS_LEVEL+ 10.5 dB See Figure 5-17 for an explanation of the relationship between RSSI, AGC and carrier sense settings.
VGA4[4:0]	CS_LEVEL[4:0]	24	H	Reference level for Received Signal Strength Indication (carrier sense level) and AGC. See Figure 5-17 for an explanation of the relationship between RSSI, AGC and carrier sense settings.

Table 5-39. LOCK Register (15h)(1)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
LOCK[7:4]	LOCK_SELECT[3:0]	0	—	Selection of signals to LOCK pin 0: Set to 0 1: Set to 1 2: LOCK_CONTINUOUS (active low) 3: LOCK_INSTANT (active low) 4: CARRIER_SENSE (RSSI above threshold, active low) 5: CAL_COMPLETE (active low) 6: SEQ_ERROR (active low) 7: FXOSC 8: REF_CLK 9: FILTER_CLK 10: DEC_CLK 11: PRE_CLK 12: DS_CLK 13: MODEM_CLK 14: VCO_CAL_COMP 15: F_COMP
LOCK[3]	WINDOW_WIDTH	0	—	Selects lock window width 0: Lock window is 2 prescaler clock cycles wide 1: Lock window is 4 prescaler clock cycles wide Recommended setting: WINDOW_WIDTH=0.
LOCK[2]	LOCK_MODE	0	—	Selects lock detector mode 0: Counter restart mode 1: Up/Down counter mode Recommended setting: LOCK_MODE=0.
LOCK[1:0]	LOCK_ACCURACY[1:0]	0	—	Selects lock accuracy (counter threshold values) 0: Declare lock at counter value 127, out of lock at value 111 1: Declare lock at counter value 255, out of lock at value 239 2: Declare lock at counter value 511, out of lock at value 495 3: Declare lock at counter value 1023, out of lock at value 1007

(1) Set LOCK_SELECT=2 to use the LOCK pin as a lock indicator.

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Table 5-40. FRONTEND Register (16h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
FRONTEND[7:6]	LNAMIX_CURRENT[1:0]	2	—	Controls current in LNA, LNA2 and mixer Recommended setting: LNAMIX_CURRENT=1
FRONTEND[5:4]	LNA_CURRENT[1:0]	1	—	Controls current in the LNA Recommended setting: LNA_CURRENT=3. Can be lowered to save power at the expense of reduced sensitivity.
FRONTEND[3]	MIX_CURRENT	0	—	Controls current in the mixer Recommended setting: MIX_CURRENT=1 at 402 to 470 MHz, MIX_CURRENT=0 at 804 to 960 MHz.
FRONTEND[2]	LNA2_CURRENT	0	—	Controls current in LNA 2 Recommended settings: LNA2_CURRENT=0 at 402 to 470 MHz, LNA2_CURRENT=1 at 804 to 960 MHz.
FRONTEND[1]	SDC_CURRENT	0	—	Controls current in the single-to-diff. Converter Recommended settings: SDC_CURRENT=0 at 426 to 464 MHz, SDC_CURRENT=1 at 852 to 928 MHz.
FRONTEND[0]	LNAMIX_BIAS	1	—	Controls how front-end bias currents are generated 0: Constant current biasing 1: Constant Gm × R biasing (reduces gain variation) Recommended setting: LNAMIX_BIAS=0.

Table 5-41. ANALOG Register (17h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
ANALOG[7]	BANDSELECT	1	—	Frequency band selection 0: 402 to 470 MHz band 1: 804 to 960 MHz band
ANALOG[6]	LO_DC	1	—	Lower LO DC level to mixers 0: High LO DC level to mixers 1: Low LO DC level to mixers Recommended settings: LO_DC=1 for 402 to 470 MHz, LO_DC=0 for 804 to 960 MHz.
ANALOG[5]	VGA_BLANKING	1	H	Enable analog blanking switches in VGA when changing VGA gain. 0: Blanking switches are disabled 1: Blanking switches are turned on for approx. 0.8 µs when gain is changed (always on if AGC_DISABLE=1) Recommended setting: VGA_BLANKING=0.
ANALOG[4]	PD_LONG	0	H	Selects short or long reset delay in phase detector 0: Short reset delay 1: Long reset delay Recommended setting: PD_LONG=0.
ANALOG[3]	—	0	—	Reserved, write 0
ANALOG[2]	PA_BOOST	0	H	Boost PA bias current for higher output power Recommended setting: PA_BOOST=1.

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Table 5-41. ANALOG Register (17h) (continued)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
ANALOG[1:0]	DIV_BUFF_CURRENT[1:0]	3	—	Overall bias current adjustment for VCO divider and buffers 0: 4/6 of nominal VCO divider and buffer current 1: 4/5 of nominal VCO divider and buffer current 2: Nominal VCO divider and buffer current 3: 4/3 of nominal VCO divider and buffer current Recommended setting: DIV_BUFF_CURRENT=3

Table 5-42. BUFF_SWING Register (18h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
BUFF_SWING[7:6]	PRE_SWING[1:0]	3	—	Prescaler swing. 0: 2/3 of nominal swing 1: 1/2 of nominal swing 2: 4/3 of nominal swing 3: Nominal swing Recommended setting: PRE_SWING=0.
BUFF_SWING[5:3]	RX_SWING[2:0]	4	—	LO buffer swing, in RX (to mixers) 0: Smallest load resistance (smallest swing) … 7: Largest load resistance (largest swing) Recommended setting: RX_SWING=2.
BUFF_SWING[2:0]	TX_SWING[2:0]	1	—	LO buffer swing, in TX (to power amplifier driver) 0: Smallest load resistance (smallest swing) … 7: Largest load resistance (largest swing) Recommended settings: TX_SWING=4 for 402 to 470 MHz, TX_SWING=0 for 804 to 960 MHz.

Table 5-43. BUFF_CURRENT Register (19h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
BUFF_CURRENT[7:6]	PRE_CURRENT[1:0]	1	—	Prescaler current scaling 0: Nominal current 1: 2/3 of nominal current 2: 1/2 of nominal current 3: 2/5 of nominal current Recommended setting: PRE_CURRENT=0.
BUFF_CURRENT[5:3]	RX_CURRENT[2:0]	4	—	LO buffer current, in RX (to mixers) 0: Minimum buffer current … 7: Maximum buffer current Recommended setting: RX_CURRENT=4.
BUFF_CURRENT[2:0]	TX_CURRENT[2:0]	5	—	LO buffer current, in TX (to PA driver) 0: Minimum buffer current … 7: Maximum buffer current Recommended settings: TX_CURRENT=2 for 402 to 470 MHz, TX_CURRENT=5 for 804 to 960 MHz.

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Table 5-44. PLL_BW Register (1Ah)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
PLL_BW[7:0]	PLL_BW[7:0]	134	—	Charge pump current scaling/rounding factor. Used to calibrate charge pump current for the desired PLL loop bandwidth. The value is given by: PLL_BW = 174 + 16 $\log_2(f_{ref} / 7.126)$ where f_{ref} is the reference frequency in MHz.

Table 5-45. CALIBRATE Register (1Bh)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
CALIBRATE[7]	CAL_START	0	↑	↑ 1: Calibration started 0: Calibration inactive
CALIBRATE[6]	CAL_DUAL	0	H	Use calibration results for both frequency A and B 0: Store results in A or B defined by F_REG (MAIN[6]) 1: Store calibration results in both A and B
CALIBRATE[5:4]	CAL_WAIT[1:0]	0	—	Selects calibration wait time (affects accuracy) 0 (00): Calibration time is approx. 90000 F_REF periods 1 (01): Calibration time is approx. 110000 F_REF periods 2 (10): Calibration time is approx. 130000 F_REF periods 3 (11): Calibration time is approx. 200000 F_REF periods Recommended setting: CAL_WAIT=3 for best accuracy in calibrated PLL loop filter bandwidth.
CALIBRATE[3]	—	0	—	Reserved, write 0
CALIBRATE[2:0]	CAL_ITERATE[2:0]	5	—	Iteration start value for calibration DAC 0 (000): DAC start value 1, VC < 0.49 V after calibration 1 (001): DAC start value 2, VC < 0.66 V after calibration 2 (010): DAC start value 3, VC < 0.82 V after calibration 3 (011): DAC start value 4, VC < 0.99 V after calibration 4 (100): DAC start value 5, VC < 1.15 V after calibration 5 (101): DAC start value 6, VC < 1.32 V after calibration 6 (110): DAC start value 7, VC < 1.48 V after calibration 7 (111): DAC start value 8, VC < 1.65 V after calibration Recommended setting: CAL_ITERATE=4.

Table 5-46. PA_POWER Register (1Ch)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
PA_POWER[7:4]	PA_HIGH [3:0]	0	—	Controls output power in high-power array 0: High-power array is off 1: Minimum high-power array output power … 15: Maximum high-power array output power
PA_POWER[3:0]	PA_LOW[3:0]	15	—	Controls output power in low-power array 0: Low-power array is off 1: Minimum low-power array output power … 15: Maximum low-power array output power It is more efficient in terms of current consumption to use either the lower or upper 4-bits in the PA_POWER register to control the power.

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Table 5-47. MATCH Register (1Dh)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
MATCH[7:4]	RX_MATCH[3:0]	0	—	Selects matching capacitor array value for RX. Each step is approximately 0.4 pF.
MATCH[3:0]	TX_MATCH[3:0]	0	—	Selects matching capacitor array value for TX. Each step is approximately 0.4 pF.

Table 5-48. PHASE_COMP Register (1Eh)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
PHASE_COMP[7:0]	PHASE_COMP[7:0]	0	—	Signed compensation value for LO I/Q phase error. Used for image rejection calibration. –128: approx. –6.2° adjustment between I and Q phase –1: approx. –0.02° adjustment between I and Q phase 0: approx. +0.02° adjustment between I and Q phase 127: approx. +6.2° adjustment between I and Q phase

Table 5-49. GAIN_COMP Register (1Fh)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
GAIN_COMP[7:0]	GAIN_COMP[7:0]	0	—	Signed compensation value for mixer I/Q gain error. Used for image rejection calibration. –128: approx. –1.16 dB adjustment between I and Q gain –1: approx. –0.004 dB adjustment between I and Q gain 0: approx. +0.004 dB adjustment between I and Q gain 127: approx. +1.16 dB adjustment between I and Q gain

Table 5-50. POWERDOWN Register (20h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
POWERDOWN[7]	PA_PD	0	H	Sets PA in power down when PD_MODE[1:0]=2
POWERDOWN[6]	VCO_PD	0	H	Sets VCO in power down when PD_MODE[1:0]=2
POWERDOWN[5]	BUFF_PD	0	H	Sets VCO divider, LO buffers and prescaler in power-down when PD_MODE[1:0]=2
POWERDOWN[4]	CHP_PD	0	H	Sets charge pump in power down when PD_MODE[1:0]=2
POWERDOWN[3]	LNAMIX_PD	0	H	Sets LNA/mixer in power down when PD_MODE[1:0]=2
POWERDOWN[2]	VGA_PD	0	H	Sets VGA in power down when PD_MODE[1:0]=2
POWERDOWN[1]	FILTER_PD	0	H	Sets image filter in power down when PD_MODE[1:0]=2
POWERDOWN[0]	ADC_PD	0	H	Sets ADC in power down when PD_MODE[1:0]=2

Table 5-51. TEST1 Register (21h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
TEST1[7:4]	CAL_DAC_OPEN[3:0]	4	—	Calibration DAC override value, active when BREAK_LOOP=1
TEST1[3:0]	CHP_CO[3:0]	13	—	Charge pump current override value

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Table 5-52. TEST2 Register (22h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
TEST2[7]	BREAK_LOOP	0	H	0: PLL loop closed 1: PLL loop open
TEST2[6]	CHP_OVERRIDE	0	H	0: use calibrated value 1: use CHP_CO[3:0] value
TEST2[5]	VCO_OVERRIDE	0	H	0: use calibrated value 1: use VCO_AO[4:0] value
TEST2[4:0]	VCO_AO[4:0]	16	—	VCO_ARRAY override value

Table 5-53. TEST3 Register (23h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
TEST3[7]	VCO_CAL_MANUAL	0	H	Enables “manual” VCO calibration (test only)
TEST3[6]	VCO_CAL_OVERRIDE	0	H	Override VCO current calibration 0: Use calibrated value 1: Use VCO_CO[5:0] value VCO_CAL_OVERRIDE controls VCO_CAL_CLK if VCO_CAL_MANUAL=1. Negative transitions are then used to sample VCO_CAL_COMP.
TEST3[5:0]	VCO_CO[5:0]	6	—	VCO_CAL_CURRENT override value

Table 5-54. TEST4 Register (24h, for Test Only)(1)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
TEST4[7]	CHP_DISABLE	0	H	Disable normal charge pump operation
TEST4[6]	CHP_TEST_UP	0	H	Force charge pump to output “up” current
TEST4[5]	CHP_TEST_DN	0	H	Force charge pump to output “down” current
TEST4[4:3]	TM_IQ[1:0]	0	—	Value of differential I and Q outputs from mixer when TM_ENABLE=1 0: I output negative, Q output negative 1: I output negative, Q output positive 2: I output positive, Q output negative 3: I output positive, Q output positive
TEST4[2]	TM_ENABLE	0	H	Enable DC control of mixer output (for testing)
TEST4[1]	TF_ENABLE	0	H	Connect analog test module to filter inputs
TEST4[0]	TA_ENABLE	0	H	Connect analog test module to ADC inputs

(1) If TF_ENABLE=1 or TA_ENABLE=1 in TEST4 register, then INTERFACE[3:0] controls analog test module: INTERFACE[3] = TEST_PD, INTERFACE[2:0] = TEST_MODE[2:0]. Otherwise, TEST_PD=1 and TEST_MODE[2]=1.

Table 5-55. TEST5 Register (25h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
TEST5[7]	F_COMP_ENABLE	0	H	Enable frequency comparator output F_COMP from phase detector
TEST5[6]	SET_DITHER_CLOCK	1	H	Enable dithering of delta-sigma clock
TEST5[5]	ADC_TEST_OUT	0	H	Outputs ADC samples on LOCK and DIO, while ADC_CLK is output on DCLK
TEST5[4]	CHOP_DISABLE	0	H	Disable chopping in ADC integrators
TEST5[3]	SHAPING_DISABLE	0	H	Disable ADC feedback mismatch shaping
TEST5[2]	VCM_ROT_DISABLE	0	H	Disable rotation for VCM mismatch shaping

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Table 5-55. TEST5 Register (25h, for Test Only) (continued)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
TEST5[1:0]	ADC_ROTATE[1:0]	0	—	Control ADC input rotation 0: Rotate in 00 01 10 11 sequence 1: Rotate in 00 10 11 01 sequence 2: Always use 00 position 3: Rotate in 00 10 00 10 sequence

Table 5-56. TEST6 Register (26h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
TEST6[7:4]	—	0	—	Reserved, write 0
TEST6[3]	VGA_OVERRIDE	0	—	Override VGA settings
TEST6[2]	AC1O	0	—	Override value to first AC coupler in VGA 0: Approx. 0 dB gain 1: Approx. –12 dB gain
TEST6[1:0]	AC2O[1:0]	0	—	Override value to second AC coupler in VGA 0: Approx. 0 dB gain 1: Approx. –3 dB gain 2: Approx. –12 dB gain 3: Approx. –15 dB gain

Table 5-57. TEST7 Register (27h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
TEST7[7:6]	—	0	—	Reserved, write 0
TEST7[5:4]	VGA1O[1:0]	0	—	Override value to VGA stage 1
TEST7[3:2]	VGA2O[1:0]	0	—	Override value to VGA stage 2
TEST7[1:0]	VGA3O[1:0]	0	—	Override value to VGA stage 3

Table 5-58. STATUS Register (40h, Read Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
STATUS[7]	CAL_COMPLETE	—	H	Set to 0 when PLL calibration starts, and set to 1 when calibration has finished
STATUS[6]	SEQ_ERROR	—	H	Set to 1 when PLL failed to lock during automatic power-up sequencing
STATUS[5]	LOCK_INSTANT	—	H	Instantaneous PLL lock indicator
STATUS[4]	LOCK_CONTINUOUS	—	H	PLL lock indicator, as defined by LOCK_ACCURACY. Set to 1 when PLL is in lock
STATUS[3]	CARRIER_SENSE	—	H	Carrier sense when RSSI is above CS_LEVEL
STATUS[2]	LOCK	—	H	Logical level on LOCK pin
STATUS[1]	DCLK	—	H	Logical level on DCLK pin
STATUS[0]	DIO	—	H	Logical level on DIO pin

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Table 5-59. RESET_DONE Register (41h, Read Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
RESET_DONE[7]	ADC_RESET_DONE	—	H	Reset of ADC control logic done
RESET_DONE[6]	AGC_RESET_DONE	—	H	Reset of AGC (VGA control) logic done
RESET_DONE[5]	GAUSS_RESET_DONE	—	H	Reset of Gaussian data filter done
RESET_DONE[4]	AFC_RESET_DONE	—	H	Reset of AFC / FSK decision level logic done
RESET_DONE[3]	BITSYNC_RESET_DONE	—	H	Reset of modulator, bit synchronization logic and PN9 PRBS generator done
RESET_DONE[2]	SYNTH_RESET_DONE	—	H	Reset digital part of frequency synthesizer done
RESET_DONE[1]	SEQ_RESET_DONE	—	H	Reset of power-up sequencing logic done
RESET_DONE[0]	CAL_LOCK_RESET_DONE	—	H	Reset of calibration logic and lock detector done

Table 5-60. RSSI Register (42h, Read Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
RSSI[7]	—	—	—	Not in use, will read 0
RSSI[6:0]	RSSI[6:0]	—	—	Received signal strength indicator. The relative power is given by RSSI × 1.5 dB in a logarithmic scale. The VGA gain set by VGA_SETTING must be taken into account. See *Section 5.9.5* for more details.

Table 5-61. AFC Register (43h, Read Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
AFC[7:0]	AFC[7:0]	—	—	Average received frequency deviation from IF. This 8-bit 2-complement signed value equals the demodulator decision level and can be used for AFC. The average frequency offset from the IF frequency is ΔF = Baud rate × AFC / 16

Table 5-62. GAUSS_FILTER Register (44h)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
GAUSS_FILTER[7:0]	GAUSS_FILTER[7:0]	—	—	Readout of instantaneous IF frequency offset from nominal IF. Signed 8-bit value. ΔF = Baud rate × GAUSS_FILTER / 8

Table 5-63. STATUS1 Register (45h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
STATUS1[7:4]	CAL_DAC[3:0]	—	—	Status vector defining applied Calibration DAC value
STATUS1[3:0]	CHP_CURRENT[3:0]	—	—	Status vector defining applied CHP_CURRENT value

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Table 5-64. STATUS2 Register (46h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
STATUS2[7:5]	CC1020_VERSION[2:0]	—	—	CC1021 version code: 0 : Pre-production version 1: First production version 2 through 7: Reserved for future use
STATUS2[4:0]	VCO_ARRAY[4:0]	—	—	Status vector defining applied VCO_ARRAY value

Table 5-65. STATUS3 Register (47h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
STATUS3[7]	F_COMP	—	—	Frequency comparator output from phase detector
STATUS3[6]	VCO_CAL_COMP	—	—	Readout of VCO current calibration comparator. Equals 1 if current defined by VCO_CURRENT_A/B is larger than the VCO core current
STATUS3[5:0]	VCO_CAL_CURRENT[5:0]	—	—	Status vector defining applied VCO_CAL_CURRENT value

Table 5-66. STATUS4 Register (48h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
STATUS4[7:6]	ADC_MIX[1:0]	—	—	Readout of mixer input to ADC
STATUS4[5:3]	ADC_I[2:0]	—	—	Readout of ADC “I” output
STATUS4[2:0]	ADC_Q[2:0]	—	—	Readout of ADC “Q” output

Table 5-67. STATUS5 Register (49h, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
STATUS5[7:0]	FILTER_I[7:0]	—	—	Upper bits of “I” output from channel filter

Table 5-68. STATUS6 Register (4Ah, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
STATUS6[7:0]	FILTER_Q[7:0]	—	—	Upper bits of “Q” output from channel filter

Table 5-69. STATUS7 Register (4Bh, for Test Only)

REGISTER	NAME	DEFAULT VALUE	ACTIVE	DESCRIPTION
STATUS7[7:5]	—	—	—	Not in use, will read 0
STATUS7[4:0]	VGA_GAIN_OFFSET[4:0]	—	—	Readout of offset between VGA_SETTING and actual VGA gain set by AGC

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6 Applications, Implementation, and Layout

NOTE

Information in *Section 6* is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

Very few external components are required for the operation of CC1021. The recommended application circuit is shown in Figure 6-1. The external components are described in Table 6-1 and values are given in Table 6-2.

6.1.1 Typical Application

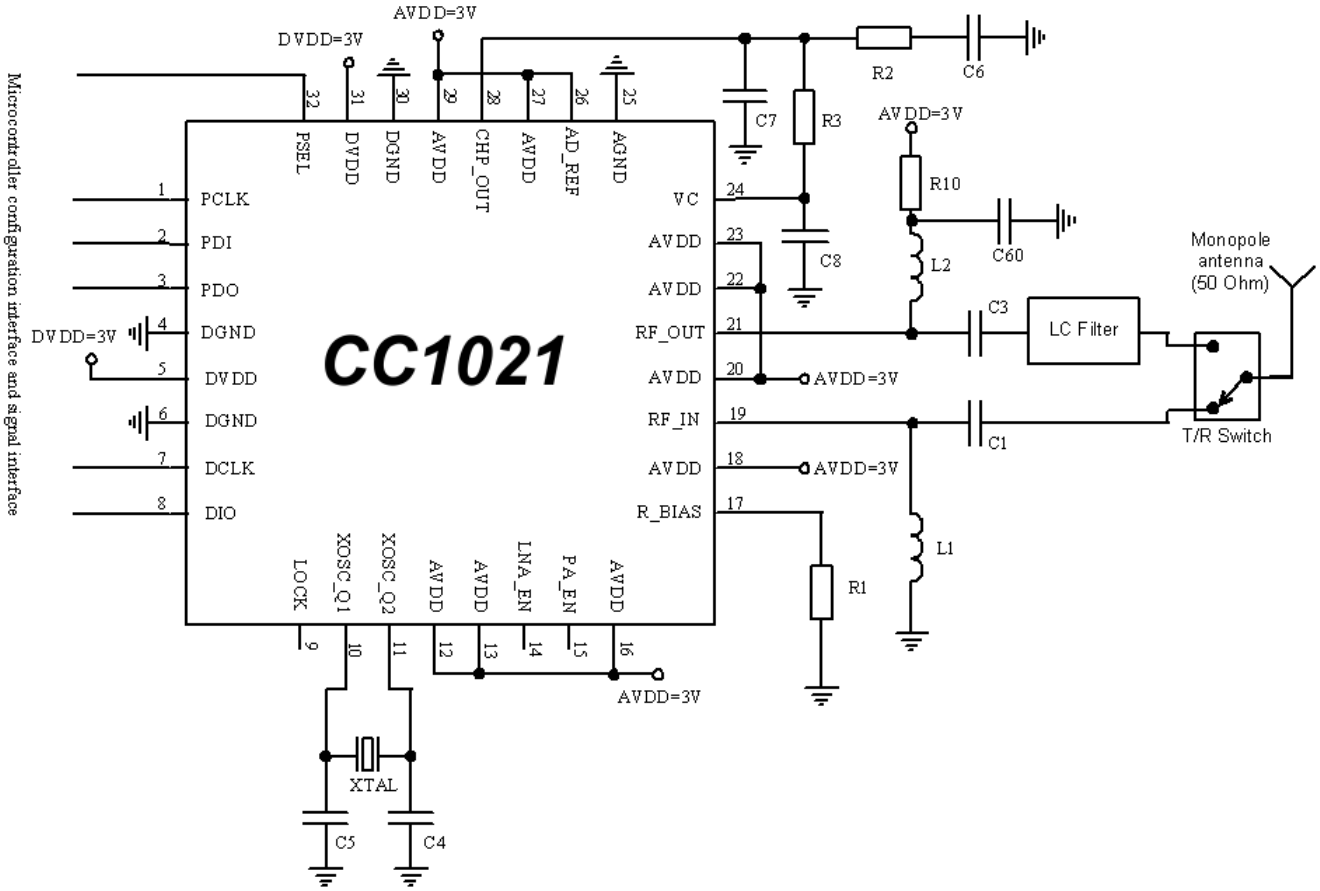

Figure 6-1. Typical Application and Test Circuit (Power Supply Decoupling Not Shown)

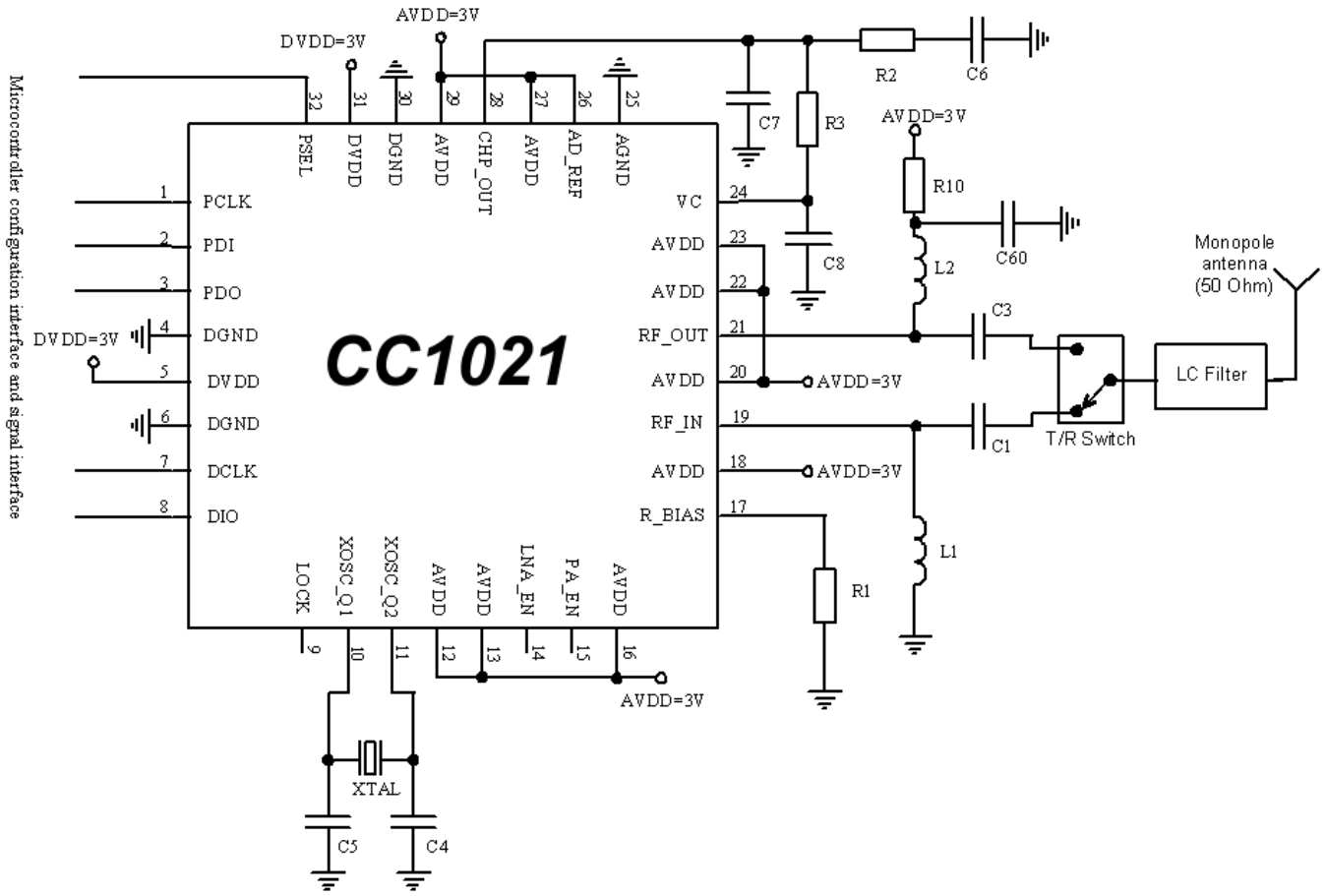

Figure 6-2. Alternative Application Circuit (Power Supply Decoupling Not Shown)

Table 6-1. Overview of External Components (Excluding Supply Decoupling Capacitors)

REF	DESCRIPTION
C1	LNA input match and DC block, see *Section 5.11*
C3	PA output match and DC block, see *Section 5.11*
C4	Crystal load capacitor, see *Section 5.16*
C5	Crystal load capacitor, see *Section 5.16*
C6	PLL loop filter capacitor
C7	PLL loop filter capacitor (may be omitted for highest loop bandwidth)
C8	PLL loop filter capacitor (may be omitted for highest loop bandwidth)
C60	Decoupling capacitor
L1	LNA match and DC bias (ground), see *Section 5.11*
L2	PA match and DC bias (supply voltage), see *Section 5.11*
R1	Precision resistor for current reference generator
R2	PLL loop filter resistor
R3	PLL loop filter resistor
R10	PA output match, see *Section 5.11*
XTAL	Crystal, see *Section 5.16*

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Table 6-2. Bill of Materials for the Application Circuit in Figure 6-1 (1)(2)

ITEM	433 MHz	868 MHz	915 MHz
C1 (3)	10 pF, 5%, NP0, 0402	47 pF, 5%, NP0, 0402	47 pF, 5%, NP0, 0402
C3 (3)	5.6 pF, 5%, NP0, 0402	10 pF, 5%, NP0, 0402	10 pF, 5%, NP0, 0402
C4	22 pF, 5%, NP0, 0402	22 pF, 5%, NP0, 0402	22 pF, 5%, NP0, 0402
C5	12 pF, 5%, NP0, 0402	12 pF, 5%, NP0, 0402	12 pF, 5%, NP0, 0402
C6	3.9 nF, 10%, X7R, 0603	3.9 nF, 10%, X7R, 0603	3.9 nF, 10%, X7R, 0603
C7	120 pF, 10%, X7R, 0402	120 pF, 10%, X7R, 0402	120 pF, 10%, X7R, 0402
C8	33 pF, 10%, X7R, 0402	33 pF, 10%, X7R, 0402	33 pF, 10%, X7R, 0402
C60	220 pF, 5%, NP0, 0402	220 pF, 5%, NP0, 0402	220 pF, 5%, NP0, 0402
L1 (3)	33 nH, 5%, 0402	82 nH, 5%, 0402	82 nH, 5%, 0402
L2 (3)	22 nH, 5%, 0402	3.6 nH, 5%, 0402	3.6 nH, 5%, 0402
R1	82 kΩ, 1%, 0402	82 kΩ, 1%, 0402	82 kΩ, 1%, 0402
R2	12 kΩ, 5%, 0402	12 kΩ, 5%, 0402	12 kΩ, 5%, 0402
R3	39 kΩ, 5%, 0402	39 kΩ, 5%, 0402	39 kΩ, 5%, 0402
R10	82 Ω, 5%, 0402	82 Ω, 5%, 0402	82 Ω, 5%, 0402
XTAL	14.7456 MHz crystal, 16 pF load	14.7456 MHz crystal, 16 pF load	14.7456 MHz crystal, 16 pF load

(1) The PLL loop filter is optimized for 38.4 kBaud data rate.
(2) The PLL loop filter component values in Table 6-2 (R2, R3, C6-C8) are optimized for 38.4 kBaud data rate. The SmartRF Studio software provides component values for other data rates using the equations in *Section 5.12.1*.
(3) Items shaded vary for different frequencies.

In the CC1020EMX reference design, which is also applicable for CC1021, LQG15HS series inductors from Murata have been used. The switch is SW-456 from M/A-COM.

The LC filter in Figure 6-1 is inserted in the TX path only. The filter will reduce the emission of harmonics and the spurious emissions in the TX path. An alternative is to insert the LC filter between the antenna and the T/R switch as shown in Figure 6-2.

The filter will reduce the emission of harmonics and the spurious emissions in the TX path as well as increase the receiver selectivity. The sensitivity will be slightly reduced due to the insertion loss of the LC filter.

6.2 Design Requirements

6.2.1 Input / Output Matching

L1 and C1 is the input match for the receiver. L1 is also a DC choke for biasing. L2 and C3 are used to match the transmitter to 50 Ω. Internal circuitry makes it possible to connect the input and output together and match the CC1021 to 50 Ω in both RX and TX mode. However, it is recommended to use an external T/R switch for optimum performance. See *Section 5.11* for details. Component values for the matching network are easily found using the SmartRF™ Studio software.

6.2.2 Bias Resistor

The precision bias resistor R1 is used to set an accurate bias current.

6.2.3 PLL Loop Filter

The loop filter consists of two resistors (R2 and R3) and three capacitors (C6 through C8). C7 and C8 may be omitted in applications where high loop bandwidth is desired. The values shown in Table 6-2 are optimized for 38.4 kBaud data rate. Component values for other data rates are easily found using the SmartRF Studio software.

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6.2.4 Crystal

An external crystal with two loading capacitors (C4 and C5) is used for the crystal oscillator. See *Section 5.16* for details.

6.2.5 Additional Filtering

Additional external components (for example, RF LC or SAW filter) may be used in order to improve the performance in specific applications. See *Section 5.11* for further information.

6.2.6 Power Supply Decoupling and Filtering

Power supply decoupling and filtering must be used (not shown in the application circuit). The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the optimum performance for narrowband applications. TI provides a reference design that should be followed very closely.

6.3 PCB Layout Guidelines

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and must be connected to the bottom ground plane with several vias. In the TI reference designs we have placed 9 vias inside the exposed die attached pad. These vias should be “tented” (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

Do not place a via underneath CC1021 at “pin #1 corner” as this pin is internally connected to the exposed die attached pad, which is the main ground connection for the chip.

Each decoupling capacitor should be placed as close as possible to the supply pin it is supposed to decouple. Each decoupling capacitor should be connected to the power line (or power plane) by separate vias. The best routing is from the power line (or power plane) to the decoupling capacitor and then to the CC1021 supply pin. Supply power filtering is very important, especially for pins 23, 22, 20 and 18.

Each decoupling capacitor ground pad should be connected to the ground plane using a separate via. Direct connections between neighboring power pins will increase noise coupling and should be avoided unless absolutely necessary.

The external components should ideally be as small as possible and surface mount devices are highly recommended.

Precaution should be used when placing the microcontroller in order to avoid noise interfering with the RF circuitry.

The recommended CC1021 PCB layout is the same as for the CC1020. A CC1020/1070DK Development Kit with a fully assembled CC1020EMX Evaluation Module is available. It is strongly advised that this reference layout is followed very closely in order to get the best performance. The layout Gerber files are available from the CC1020EMX product folder.

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7 Device and Documentation Support

7.1 Device Support

7.1.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *CC1021* is in production; therefore no prefix is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RUZ*).

For orderable part numbers of *CC1021* devices in the *RUZ* package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

7.2 Documentation Support

The following documents describe the *CC1021* device. Copies of these documents are available on the Internet at www.ti.com.

1. *AN022 Crystal Frequency Selection* (SWRA070)
2. *AN029 CC1020/1021 Automatic Frequency Control (AFC)* (SWRA063)
3. *AN030 CC1020/1021 Received Signal Strength Indicator* (SWRA062)
4. *AN070 CC1020 Automatic Power-Up Sequencing* (SWRA279)
5. *CC1020EMX Reference Design* (CC1020EMX)
6. *AN023 CC1020 MCU Interfacing* (SWRA069)
7. *CC1021 Errata Note 002*, located in the CC1021 product folder.
8. SmartRF Studio
9. *CC1021 Errata Note 001*, located in the CC1021 product folder.
10. *AN001 SRD Regulations for License Free Transceiver Operation* (SWRA090).
11. *AN027 Temperature Compensation by Indirect Method* (SWRA065).
12. *AN014 Frequency Hopping Systems* (SWRA077)
13. *AN003 SRD Antennas* (SWRA088).

7.2.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.3 Trademarks

SmartRF, E2E are trademarks of Texas Instruments.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1021-RTB1	ACTIVE	VQFNP	RUZ	32	52	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1021	Samples
CC1021-RTR1	ACTIVE	VQFNP	RUZ	32	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1021	Samples
CC1021RSS	ACTIVE	VQFNP	RUZ	32	52	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1021	Samples
CC1021RSSR	ACTIVE	VQFNP	RUZ	32	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1021	Samples
CC1021RUZ	ACTIVE	VQFNP	RUZ	32	52	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1021	Samples
CC1021RUZR	ACTIVE	VQFNP	RUZ	32	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1021	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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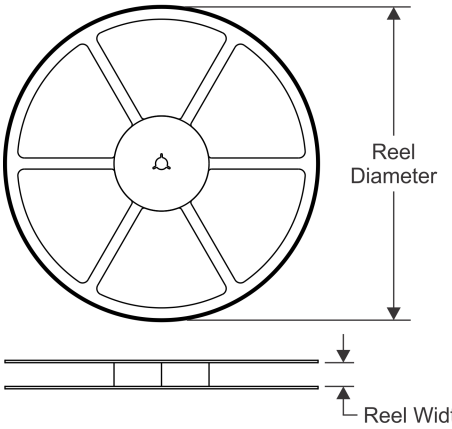
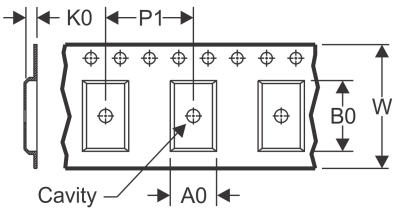
TAPE AND REEL INFORMATION

REEL DIMENSIONS

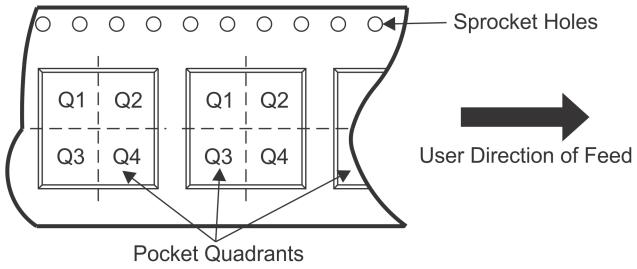


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

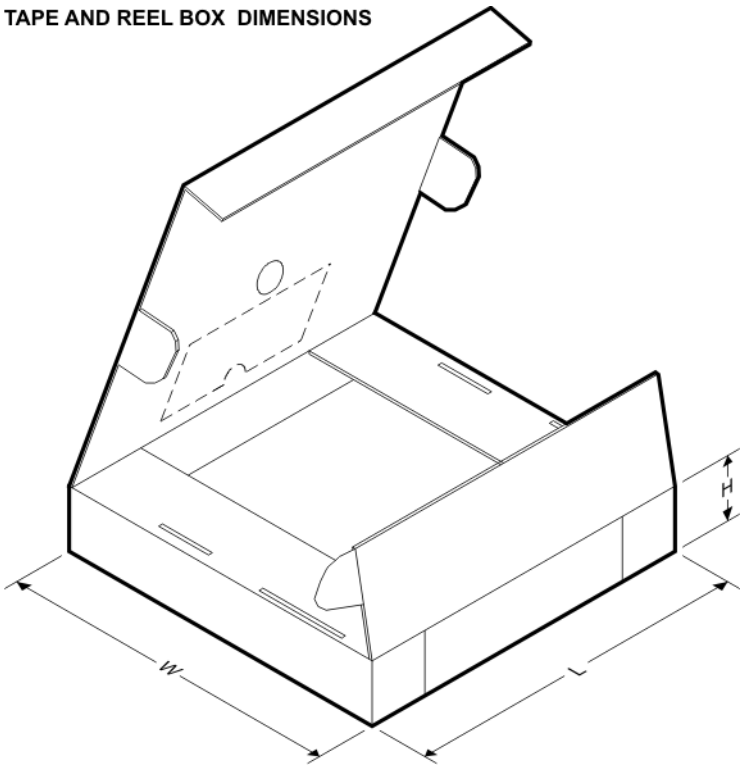
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1021RUZR	VQFNP	RUZ	32	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1021RUZR	VQFNP	RUZ	32	2500	336.6	336.6	28.6

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