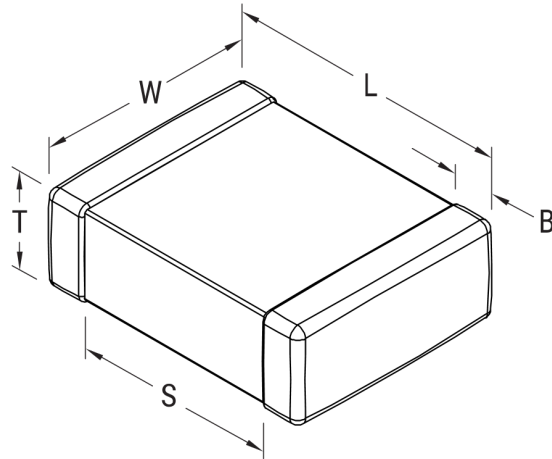


C1210C101JGGACTU

Aliases (C1210C101JGGAC7800)

SMD Comm COG HV, Ceramic, 100 pF, 5%, 2000 VDC, COG, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 1210



Click [here](#) for the 3D model.

Dimensions

Chip Size	1210
L	3.2mm +/-0.2mm
W	2.5mm +/-0.2mm
T	1.7mm +/-0.20mm
S	1.5mm MIN
B	0.5mm +/-0.25mm

Packaging Specifications

Packaging	T&R, 180mm, Plastic Tape
Packaging Quantity	2000

General Information

Series	SMD Comm COG HV
Style	SMD Chip
Description	SMD, MLCC, Ultra-Stable, Low Loss, Class I
Features	Ultra-Stable, Low Loss, Class I
RoHS	Yes
Termination	Tin
Marking	false
AEC-Q200	No
Typical Component Weight	70 mg
Shelf Life	78 Weeks
MSL	1

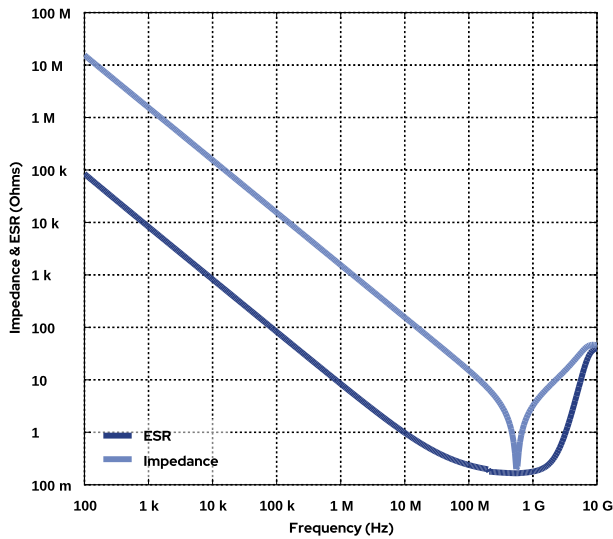
Specifications

Capacitance	100 pF
Measurement Condition	1 MHz 1.0Vrms
Capacitance Tolerance	5%
Voltage DC	2000 VDC
Dielectric Withstanding Voltage	2400 VDC
Temperature Range	-55/+125°C
Temperature Coefficient	COG
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	30 ppm/C, 1MegaHz 1.0Vrms
Dissipation Factor	0.1% 1 MHz 1.0Vrms
Aging Rate	0% Loss/Decade Hour
Insulation Resistance	100 GOhms

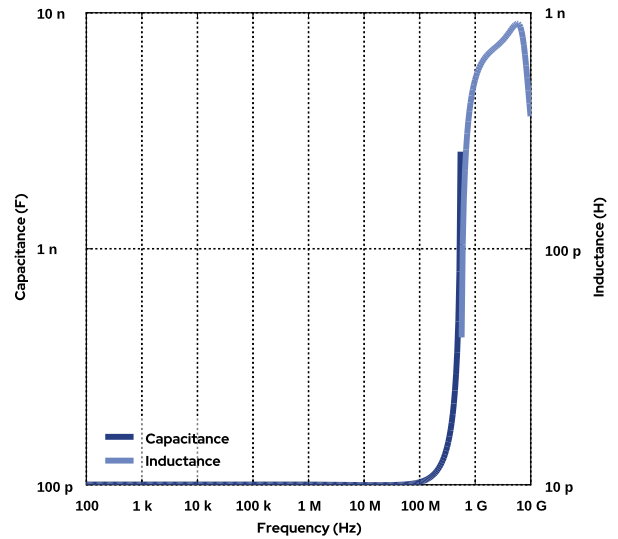
Simulations

For the complete simulation environment please visit [K-SIM](#).

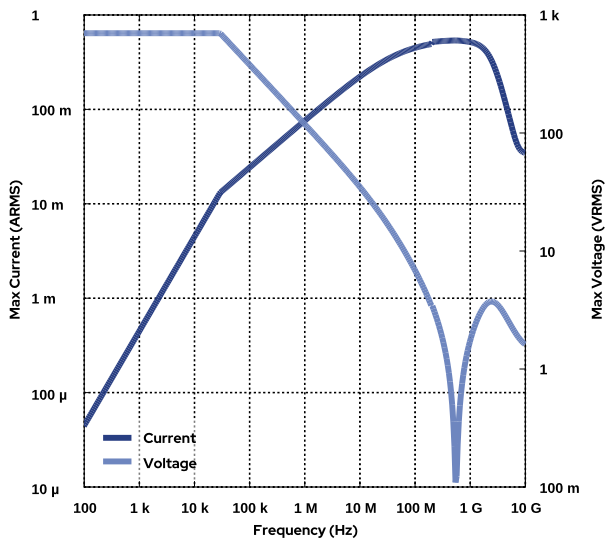
Impedance and ESR



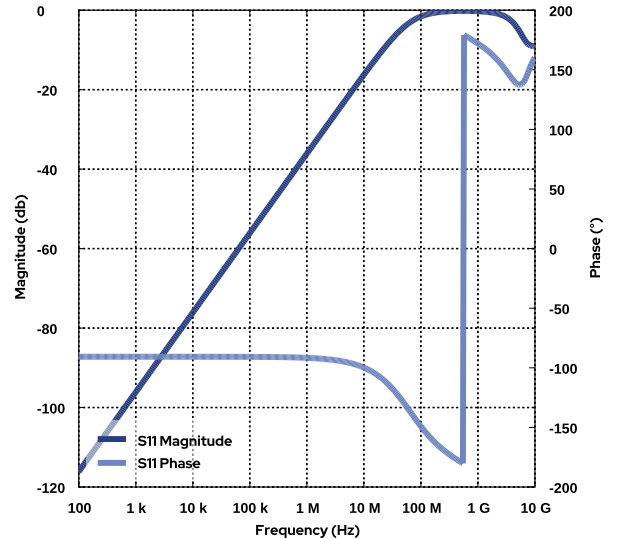
Capacitance and Inductance



Current and Voltage



S11



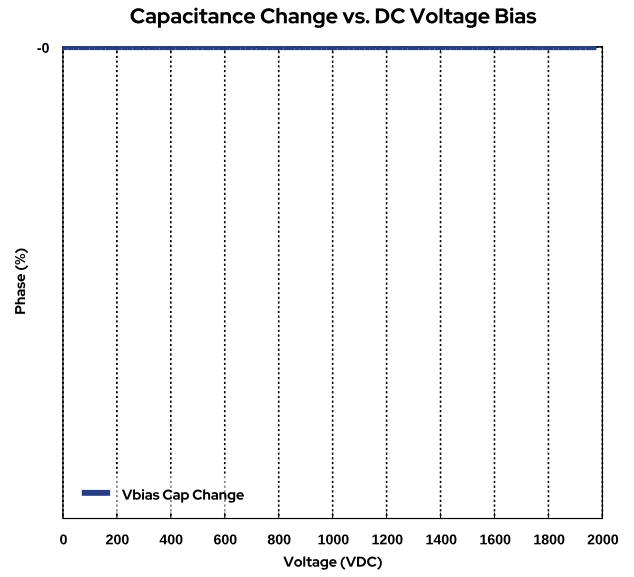
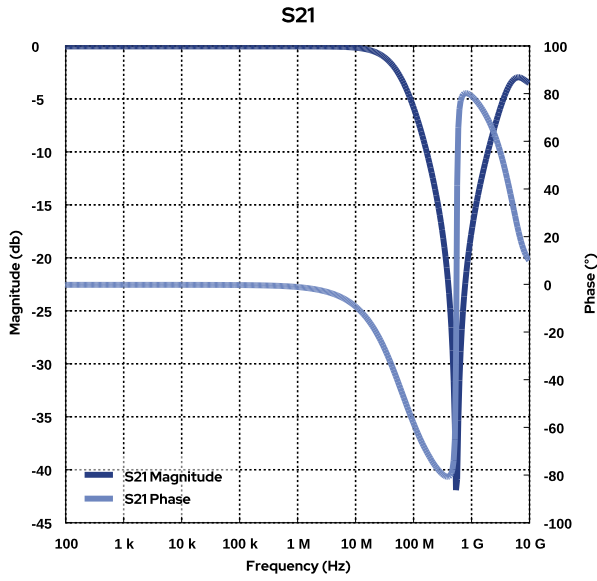


a YAGEO company

C1210C101JGGACTU

Aliases (C1210C101JGGAC7800)

SMD Comm COG HV, Ceramic, 100 pF, 5%, 2000 VDC, COG, SMD, MLCC, Ultra-Stable, Low Loss, Class I, 1210



These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.
- The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.