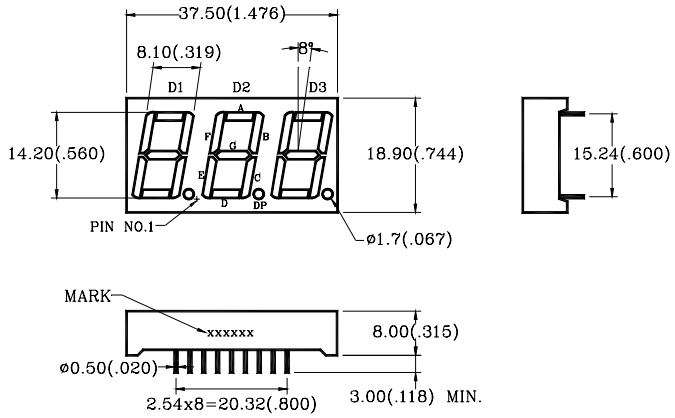
Features :

1. 0.56 inch (14.20mm) Digit Height.
2. Wide supply voltage operation.
3. Serial data input.
4. Constant current drivers.
5. Continuous brightness control.
6. Solid state reliability-long operation life.
7. No load signal required
8. Optional external data enable and reset
9. 34 outputs,20mA sink capability
10. TTL compatible.

Description :

1. The BT-M512RD-DR1 is a 14.2mm (0.56") numeric display modules, and a built-in M5450 MOS integrated circuits.
2. The integrated circuit contains serial data Input, 35 bits shift register. 34 LED driver output and a brightness control.
3. This device use green LED chips, which are made from GaP on GaP substrate.
4. This product has a black face and white segments.
5. The MOS integrated circuits are produced with N-channel silicon gate technology.
6. This product doesn't contain restriction substance, comply ROHS standard.

Package Dimensions :



Notes:
1. All dimensions are in millimeters(inches).
2. Tolerance is ±0.25mm(.01")unless otherwise specified.
3. Specifications are subject to change without notice.

Pin Connection:

Pin NO.	Description	Pin NO.	Description
1	VSS	10	Bit 31 Output
2	V_{LED}	11	Bit 32 Output
3	V_{LED}	12	Bit 33 Output
4	Bit 25 Output	13	Bit 34 Output
5	Bit 26 Output	14	Data Enable
6	Bit 27 Output	15	Data Input
7	Bit 28 Output	16	Clock Input
8	Bit 29 Output	17	V_{DD}
9	Bit 30 Output	18	BRT. Control

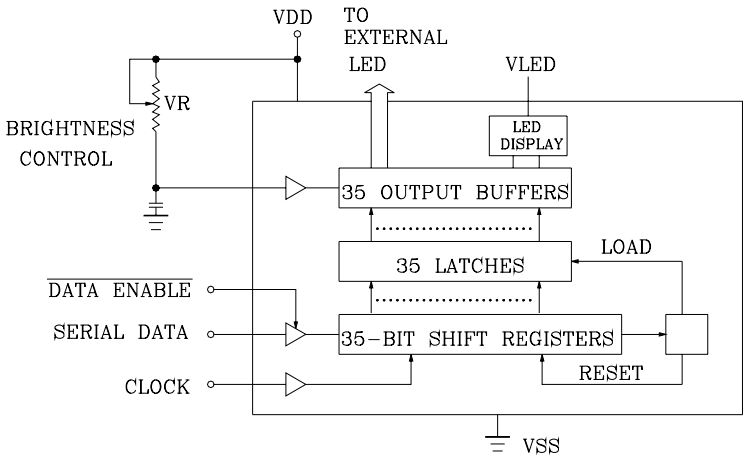
Note: Pin NO. 2 & 3 are internally connect.

Table I Serial Data Input Sequence

Bit	Digit	Segment	Bit	Digit	Segment
1	1	A	18	3	B
2	1	B	19	3	C
3	1	C	20	3	D
4	1	D	21	3	E
5	1	E	22	3	F
6	1	F	23	3	G
7	1	G	24	3	DP
8	1	DP	25		Pin 4
9	2	A	26		Pin 5
10	2	B	27		Pin 6
11	2	C	28		Pin 7
12	2	D	29		Pin 8
13	2	E	30		Pin 9
14	2	F	31		Pin 10
15	2	G	32		Pin 11
16	2	DP	33		Pin 12
17	3	A	34		Pin 13

Pad Name	Type	Description
V_{DD}	Power	Power
V_{SS}	Ground	Ground
Reset	Input	Reset Signal Input,(Normally LO; Active HI)
B.C.	Input	DC Current Input For LED Brightness Control
CLK	Input	Clock Input
Data IN	Input	Serial Data Input
ENB	Input	Data Input Enables, (Normally LO; Active LO)
Out 1~Out 35	Output	Nmos Output Drivers

Block Diagram



● Functional Description

1.Data is transferred serially via 2 signals : clock and serial data. Data transfer without the added inconvenience of an external load signal is accomplished by using a format of a leading “1” followed by the allowed 35 data bits. These 35 data bits are latched after the 36th clock has been transferred. This scheme provides non-multiplexed, direct drive to the led display. characters currently displayed(thus, data output) changes only if the serial data bits differ from those previously transferred.

2.Display brightness is determined by control of the output current for led displays. this control function can be achieved by varying the current flowing into B.C. terminal. a simple way is to set an external variable resistor illustrated in the block diagram. Typically, the output current is 36 times greater that current into B.C. terminal.

3. Figure 1 shows the input data format. A leading “1” is followed by 35 bits of data. After the 36th had been transferred, a load signal is generated synchronously with the clock high state. This loads the 35 bits of data into the latches. A reset signal is generated consecutively with the clock low which clears all shift registers for the next set of data. All shift registers are static master-slave, with no clear for the master portion of the first register, allowing continuous operation.There must be a complete of 36 clocks or the shift registers will not clear.

4. When the chip first powers on an internal power on reset signal is generated which resets all shift registers and all latches. The start bit and the first clock return the chip to its normal operation.

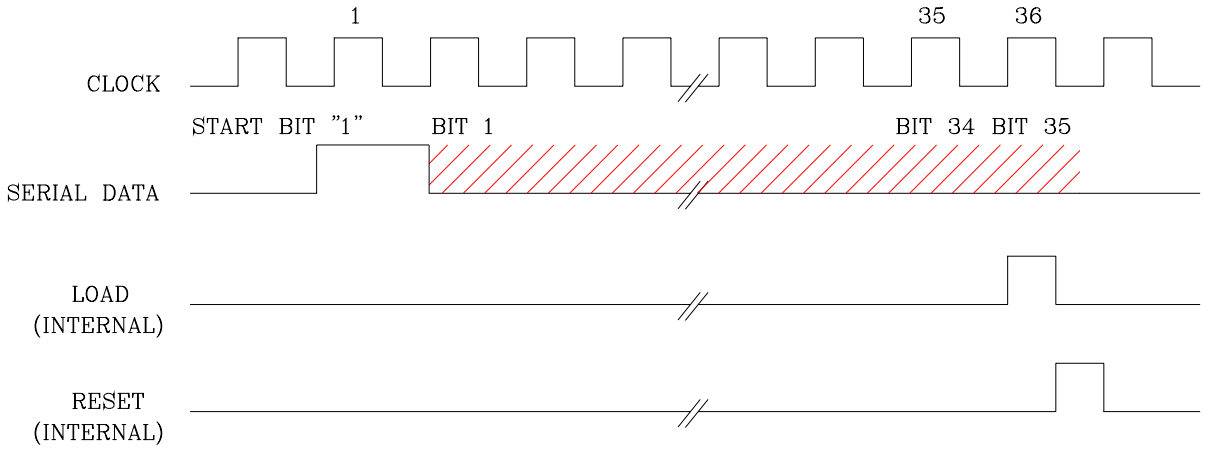
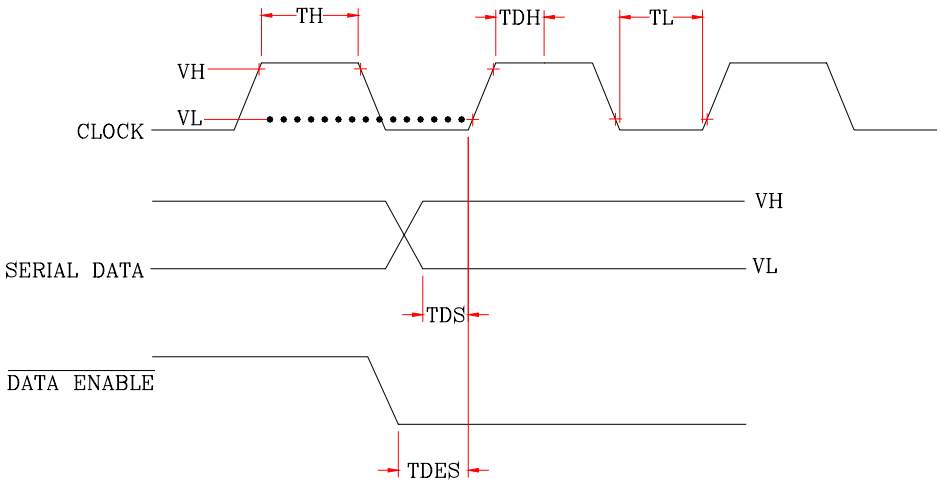


FIG.1 INPUT DATA FORMAT

● Absolute Maximum Ratings, Ta=25℃ (Unless Otherwise Specified)

Characteristics	Symbol	Rating	Unit
Supply Voltage	VDD	+3.5~+10	V
LED Supply Voltage	V_{LED}	2.4~3.0	V
Clock Frequency	Fosc	0~500K	H_Z
Input Voltage	V_{IN}	-0.3~VDD+0.3	V
Input B.C. Current	I_{BC}	550	μA
Output Sustaining Voltage	V_{DS}	12	V
Out Continuous Current	IOUT	20	mA

● Timing Chart & Timing Conditions



VDD=+5V, Ta=25℃, Unless Otherwise Specified					
Item	**Description**	**Min**	**Typ**	**Max**	**Unit**
TH	Clock Input High Time	950	-	-	nS
TL	Clock Input Low Time	950	-	-	nS
TDS	Serial Data Set-up Time	300	-	-	nS
TDH	Serial Data Hold Time	300	-	-	nS
TDES	Data Enable Set-up Time	100	-	-	nS

● Absolute Maximum Ratings(Ta=25℃)

Parameter	Symbol	Rating	Unit
Power Dissipation Per Segment	Pd	80	mW
Forward Current Per Segment	I_F	30	mA
Peak Forward Current Per Segment	I_{FP} (Duty 1/10, 1KHZ)	150	mA
Reverse Voltage Per Segment	V_R	5	V
Operating Temperature	Topr	-40℃~80℃	-
Storage Temperature	Tstg	-40℃~85℃	-
Soldering Temperature (1/16" From Body)	Tsol	260℃ For 5 Seconds	-

● Electrical And Optical Characteristics(Ta=25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage Per Segment	Vf	I_F=10mA	-	2.1	2.5	V
Luminous Intensity Per Segment	Iv	I_F=10mA	-	3.0	-	mcd
Reverse Current Per Segment	I_R	V_R=5V	-	-	100	μA
Peak Wave Length	λp	I_F=10mA	-	568	-	nm
Dominant Wave Length	λd	I_F=10mA	569	-	574	nm
Spectral Line Half-width	Δλ	I_F=10mA	-	30	-	nm

● Typical Electro-Optical Characteristics Curves

(25℃ Ambient Temperature Unless Otherwise Noted)

Fig.1 Relative Radiant Intensity VS. Wavelength

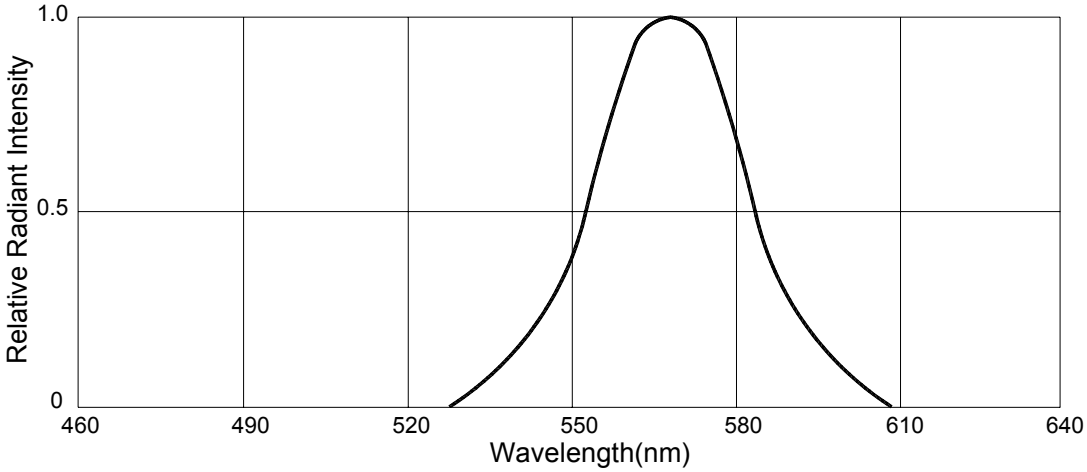


Fig.2 Forward Current VS. Forward Voltage

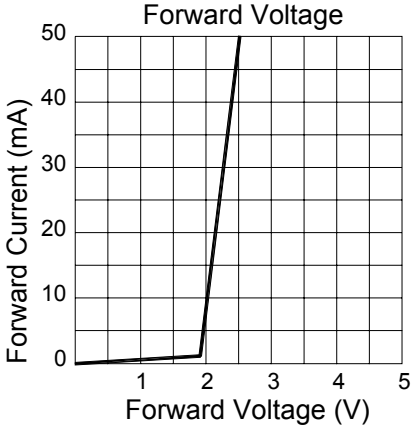


Fig.3 Relative Luminous Intensity VS. Ambient Temperature

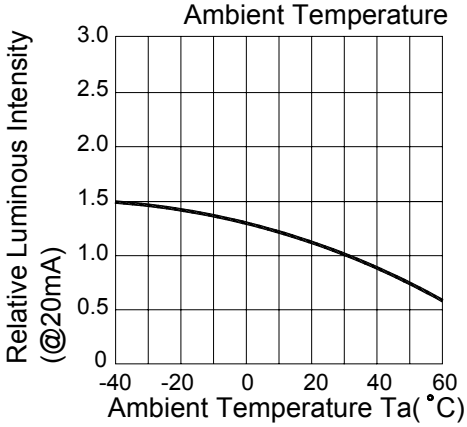


Fig.4 Relative Luminous Intensity VS. Forward Current

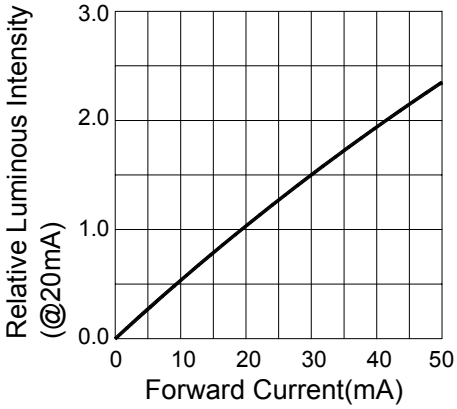


Fig.5 Forward Current Derating Curve VS. Ambient Temperature