

n-Channel Power MOSFET

OptiMOS™
BSB008NE2LX

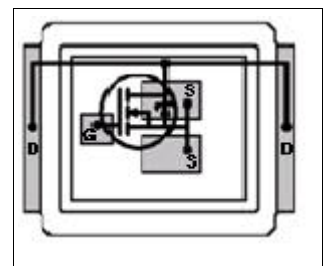
Data Sheet

1.3, 2011-09-16
Preliminary

Industrial & Multimarket

1 Description

OptiMOS™25V products are class leading power MOSFETs for highest power density and energy efficient solutions. Ultra low gate and output charges together with lowest on state resistance in small footprint packages make OptiMOS™ 25V the best choice for the demanding requirements of voltage regulator solutions in Servers, Datacom and Telecom applications. Super fast switching Control FETs together with low EMI Sync FETs provide solutions that are easy to design in. OptiMOS™ products are available in high performance packages to tackle your most challenging applications giving full flexibility in optimizing space, efficiency and cost. OptiMOS™ products are designed to meet and exceed the energy efficiency and power density requirements of the sharpened next generation voltage regulation standards in computing applications.



Features

- Optimized for e-fuse and OR-ing application
- 100% avalanche tested
- Ultra low $R_{DS(on)}$ in CanPAK-MX footprint
- Qualified according to JEDEC¹⁾ for target applications
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Double.sided cooling
- Compatible with DirectFET® package MX footprint and outline
- 100% Rg Tested
- Low profile (<0.7 mm)

Applications

- On board power for server
- Power managment for high performance computing
- Synchronous rectification
- High power density point of load converters



Table 1 Key Performance Parameters

Parameter	Value	Unit	Related Links
V_{DS}	25	V	IFX OptiMOS webpage IFX OptiMOS product brief IFX OptiMOS spice models IFX Design tools
$R_{DS(on),max}$	0.8	mΩ	
I_D	180	A	
Q_{OSS}	74	nC	
$Q_{g,typ}$	240		

Type	Package	Marking
BSB008NE2LX	MG-WDSON-2	04E2

1) J-STD20 and JESD22

2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	180	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$
		-	-	165		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$
		-	-	46		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=45\text{ K/W}$
Pulsed drain current ¹⁾	$I_{D,pulse}$	-	-	400		$T_C=25\text{ °C}$
Avalanche current, single pulse ²⁾	I_{AS}	-	-	40		
Avalanche energy, single pulse	E_{AS}	-	-	600	mJ	$I_D=40\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	
Power dissipation	P_{tot}	-	-	89	W	$T_C=25\text{ °C}$
		-	-	2.8		$T_A=25\text{ °C}, R_{thJA}=45\text{ K/W}$
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	
IEC climatic category; DIN IEC 68-1		55	150	56	Ncm	

1) See figure 3 for more detailed information

2) See figure 13 for more detailed information

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	1.0	-	°K/W	bottom
		-	-	1.4		top
Device on PCB	R_{thJA}	-	-	45		6 cm ² cooling area ¹⁾

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70μ, thick) copper area for drain connection. PCB is vertical in still air.

4 Electrical characteristics

Electrical characteristics, at $T_J=25\text{ °C}$, unless otherwise specified.

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2		$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	10	μA	$V_{DS}=25\text{ V}$, $V_{GS}=0\text{ V}$, $T_J=25\text{ °C}$
		-	10	100		$V_{DS}=25\text{ V}$, $V_{GS}=0\text{ V}$, $T_J=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.75	1.0	$\text{m}\Omega$	$V_{GS}=4.5\text{ V}$, $I_D=25\text{ A}$
		-	0.6	0.8		$V_{GS}=10\text{ V}$, $I_D=30\text{ A}$
Gate resistance	R_G	-	0.5	-	Ω	
Transconductance	g_{fs}	120	240	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=30\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	12000	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=12\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	3800	-		
Reverse transfer capacitance	C_{rss}	-	3300	-		
Turn-on delay time	$t_{d(on)}$	-	12.6	-	ns	$V_{DD}=12\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_G=1.6\text{ }\Omega$
Rise time	t_r	-	47.2	-		
Turn-off delay time	$t_{d(off)}$	-	75	-		
Fall time	t_f	-	32.4	-		

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition	
		Min.	Typ.	Max.			
Gate to source charge	Q_{gs}	-	27	-	nC	$V_{DD}=12\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$	
Gate charge at threshold	$Q_{g(th)}$	-	19	-			
Gate to drain charge	Q_{gd}	-	73	-			
Switching charge	Q_{sw}	-	81	-			
Gate charge total	Q_g	-	146	8.1			
Gate plateau voltage	$V_{plateau}$	-	2.2	-	V		
Gate charge total	Q_g	-	258	-	nC	$V_{DD}=12\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	88	-			$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge	Q_{oss}	-	74	-			$V_{DD}=12\text{ V}$, $V_{GS}=0\text{ V}$

1) See figure 16 for gate charge parameter definition

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_s	-	-	89	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{s,pulse}$	-	-	400		
Diode forward voltage	V_{SD}	-	0.78	-	V	$V_{GS}=0\text{ V}$, $I_F=30\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery charge	Q_{rr}	-	20	-	nC	$V_R=15\text{ V}$, $I_F=I_s$, $di_F/dt=400\text{ A}/\mu\text{s}$

5 Electrical characteristics diagrams

Table 8

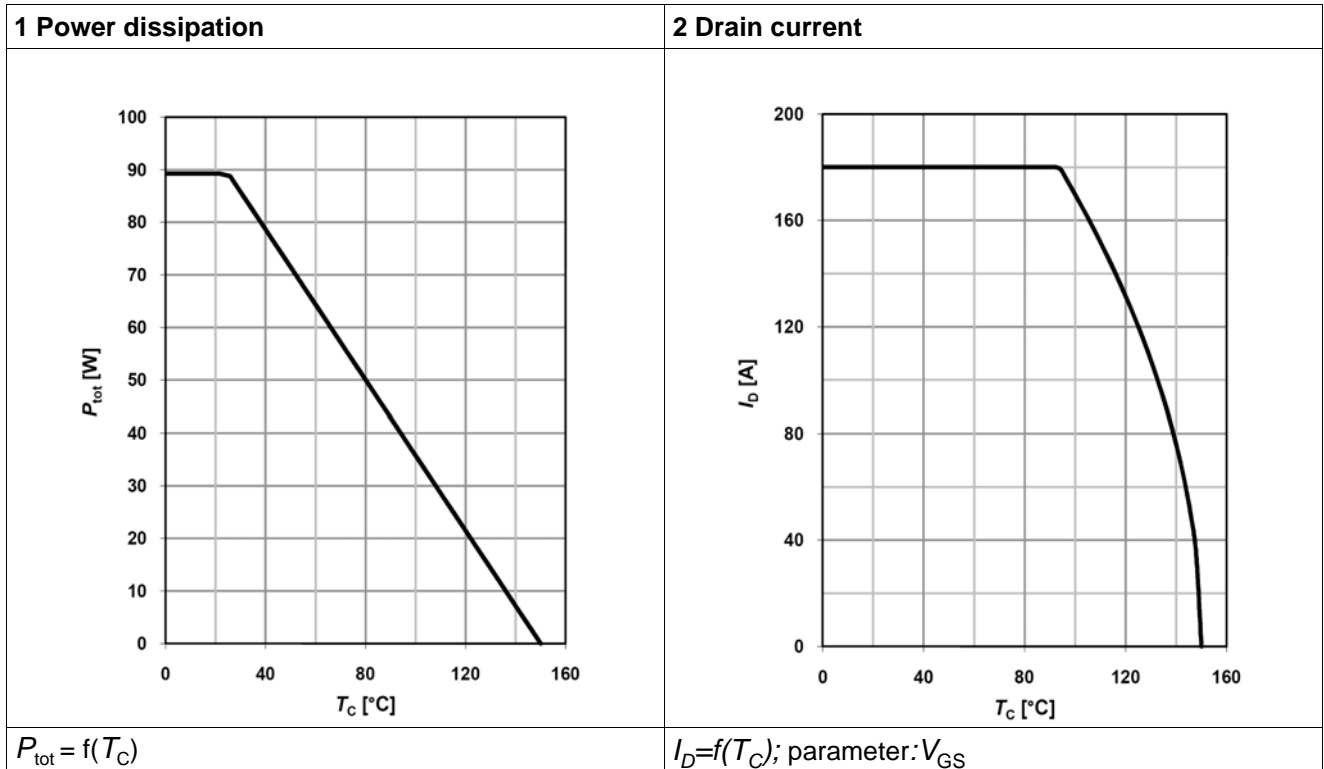


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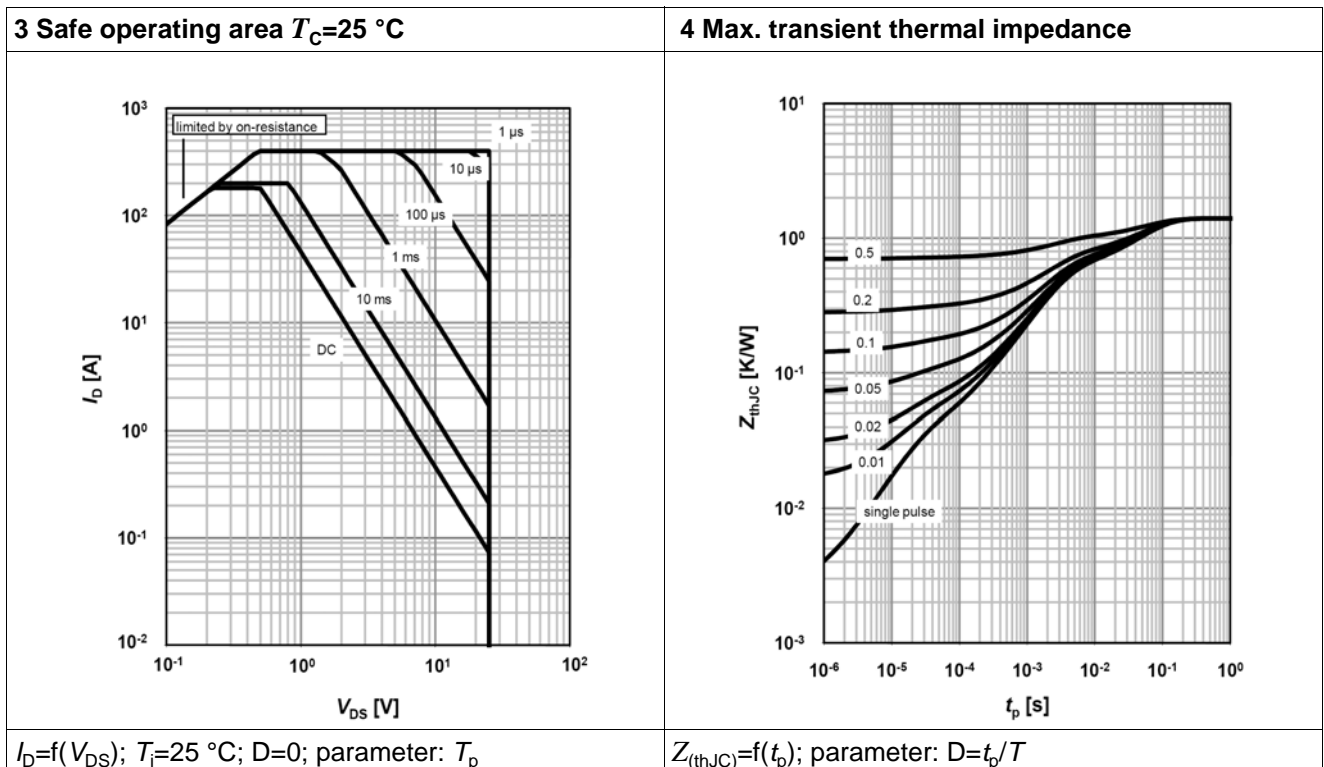


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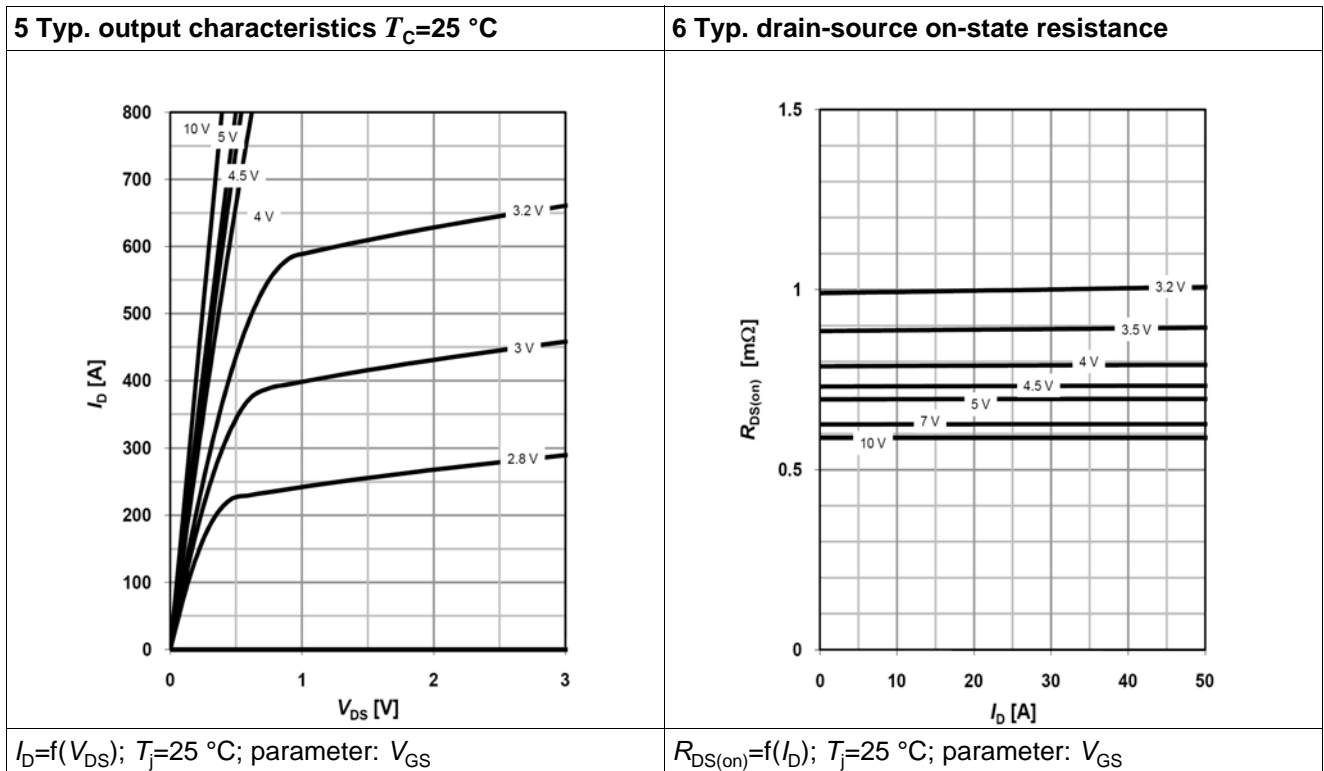


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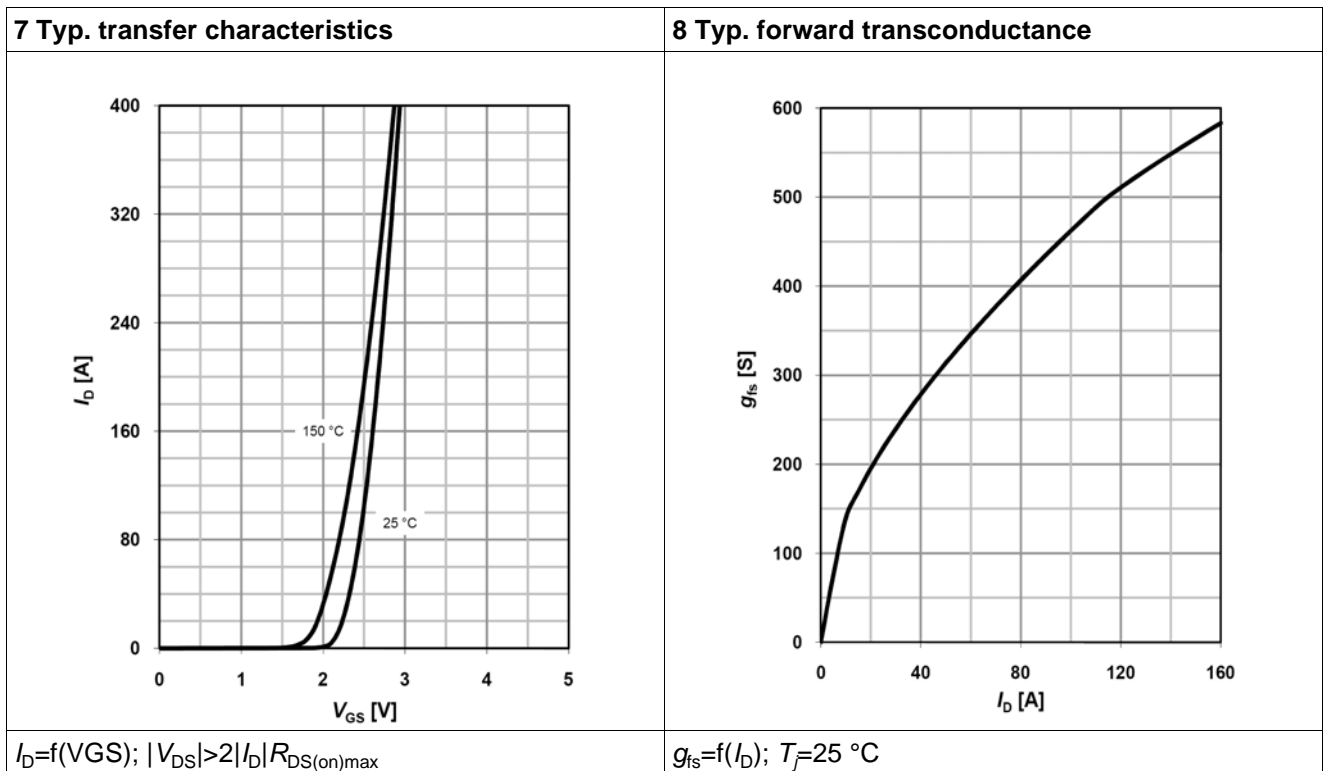


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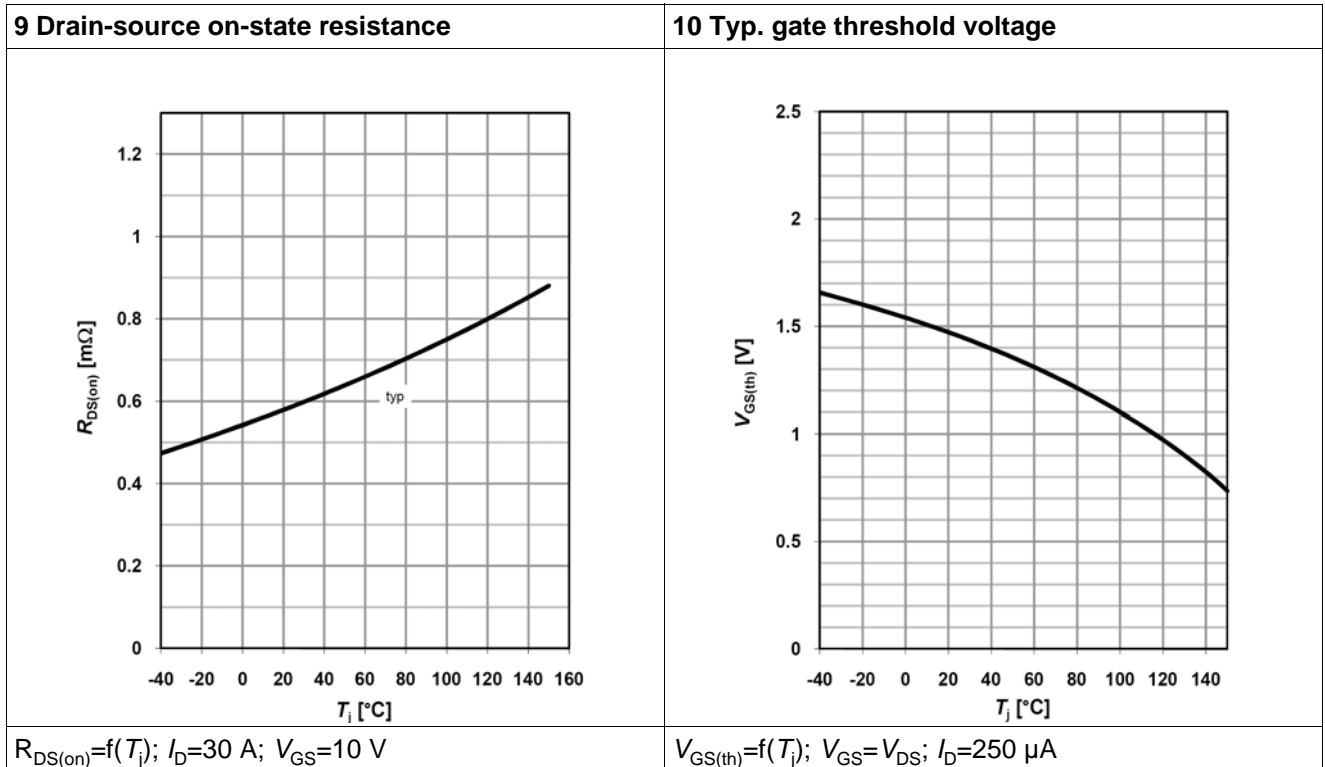


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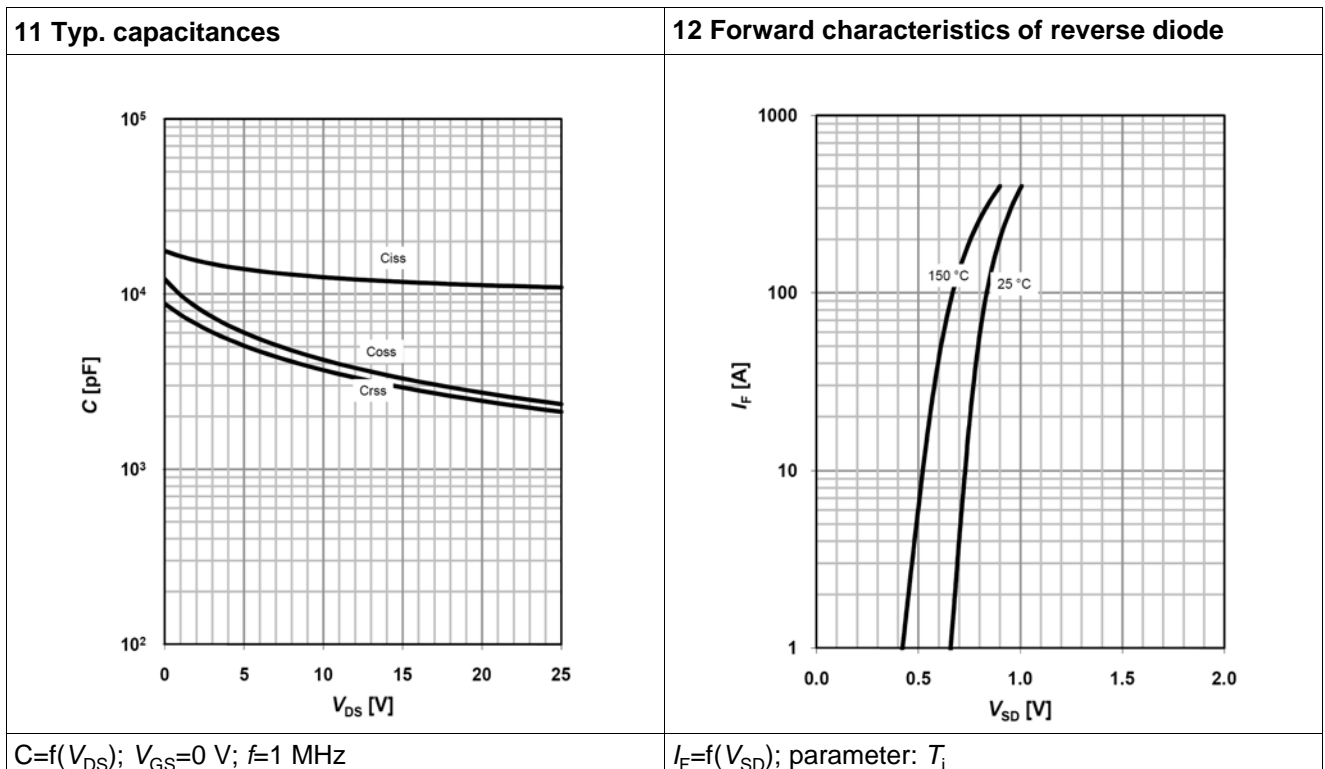


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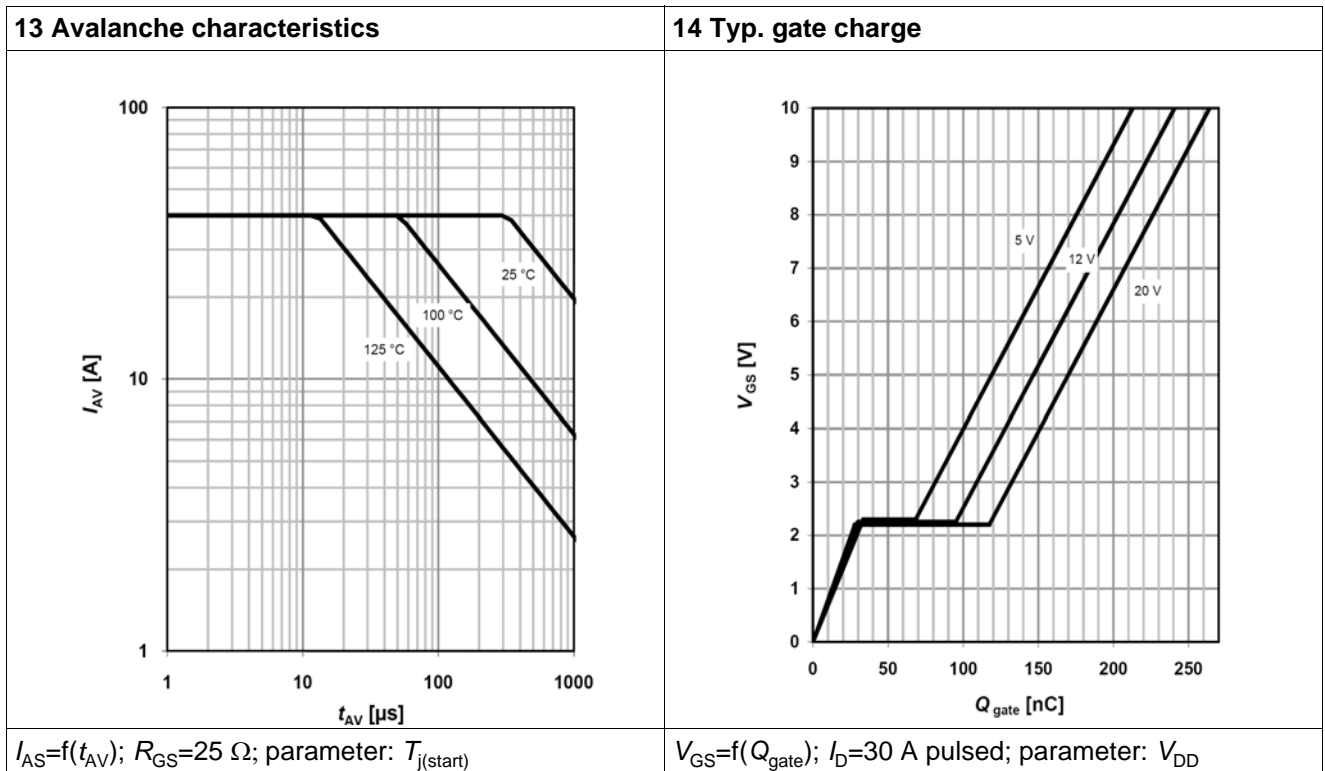
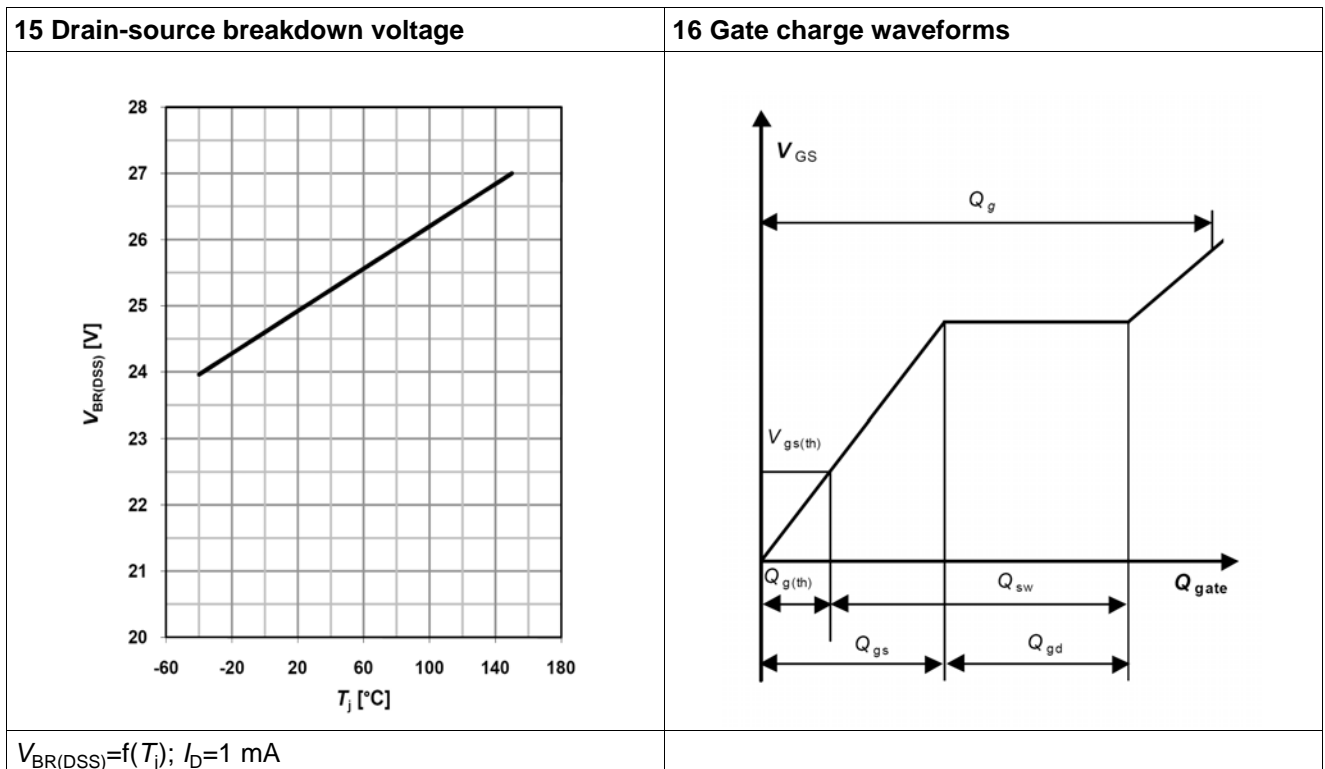


Table 15



6 Package outlines

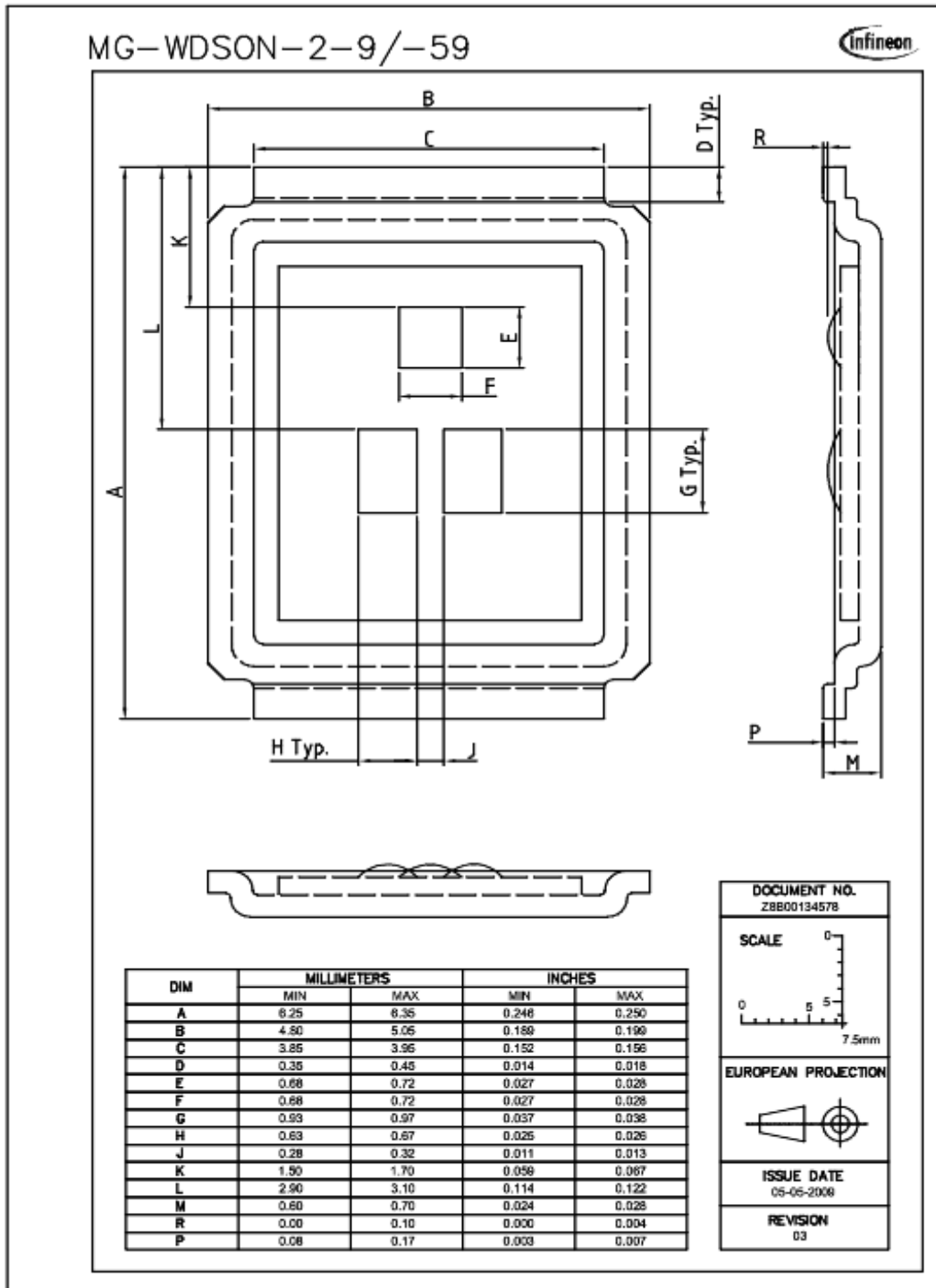


Figure 1 Outlines MG-WDSO_N-2, dimensions in mm/inches

7 Package outlines

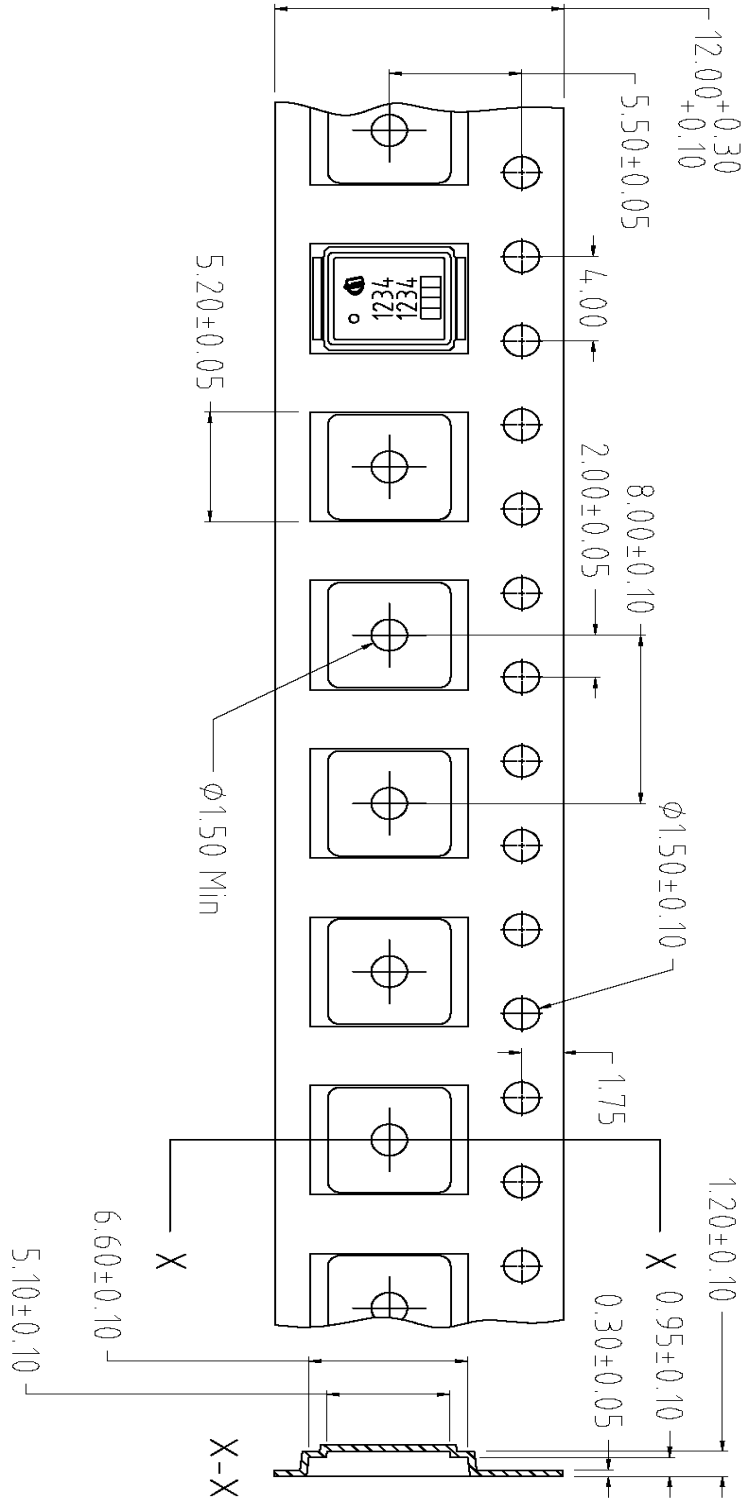


Figure 2 Outlines MG-WDSO-2, dimensions in mm/inches

8 Package outlines

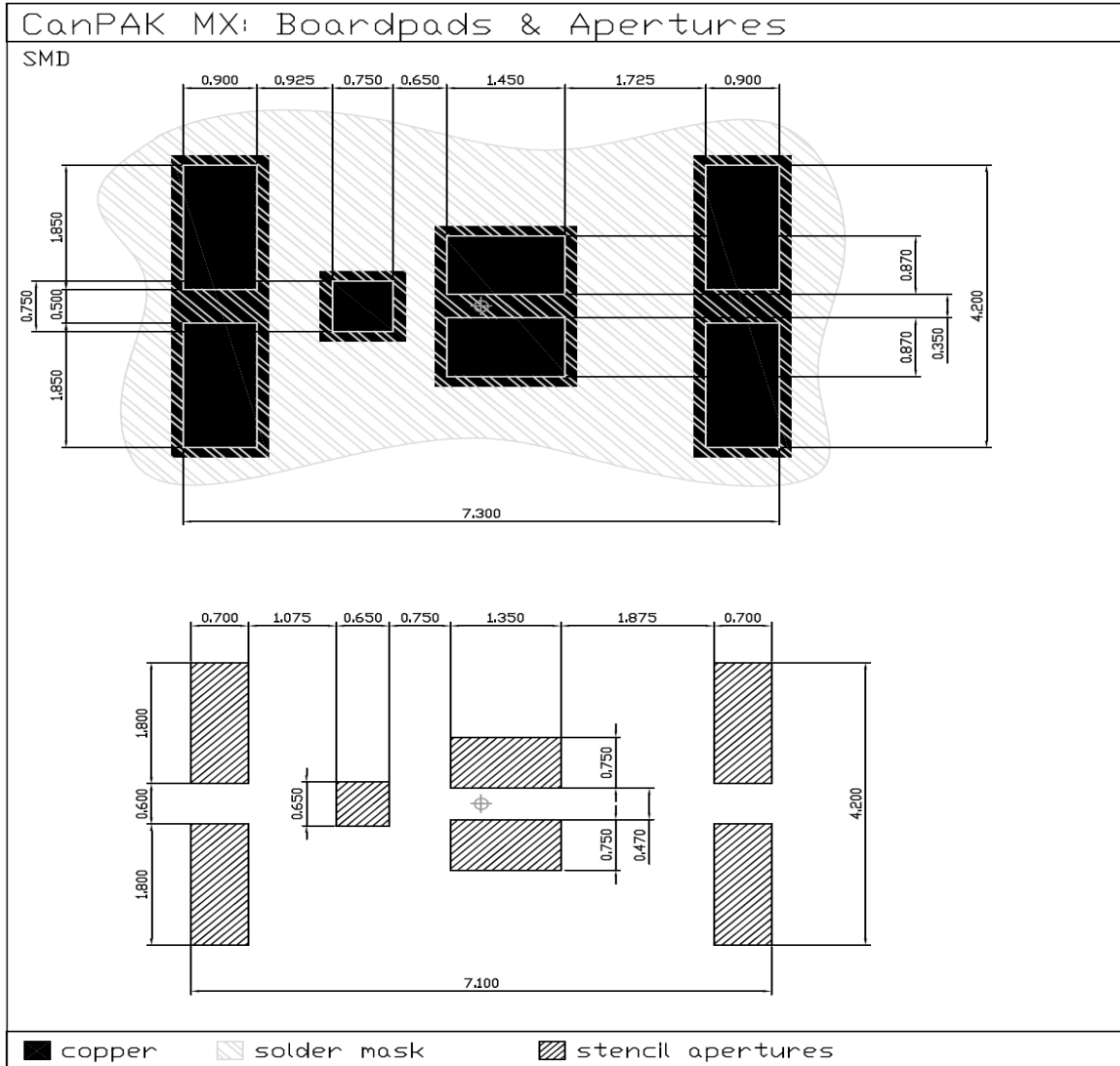
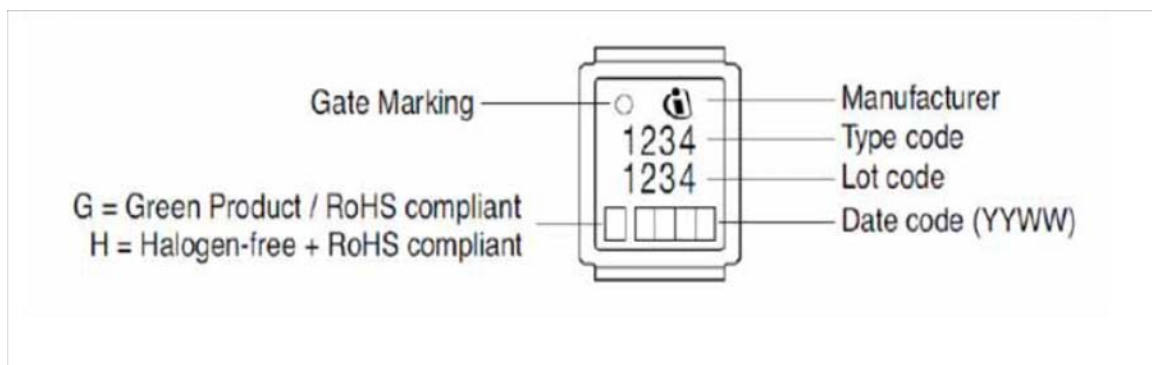


Figure 3 Outlines MG-WDSO-2, dimensions in mm/inches

9 Marking Layout



9 Revision History

Revision History: 2011-09-16, 1.3

Previous Revision:

Revision	Subjects (major changes since last revision)
0.2	Release of Target data sheet
1.0	Release of Preliminary data sheet
1.1	DirectFET Disclaimer expired
1.2	Inserting Marking Layout

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