Power Management ICs for Automotive Body Control

Voltage Detector ICs with Watchdog Timer

BD37A19FVM,BD37A41FVM,BD87A28FVM,BD87A29FVM BD87A34FVM,BD87A41FVM,BD99A41F

No.10039EAT12

●Description

The BD37A19FVM, BD37A41FVM, BD87A28FVM, BD87A29FVM, BD87A34FVM, BD87A41FVM and BD99A41F are watchdog timer reset ICs. It delivers a high precision detection voltage of ±1.5% and a super-low current consumption of 5 μA (Typ.). It can be used in a wide range of electronic devices to monitor power supply voltages and in system operation to prevent runaway operation.

●Features

1) High precision detection voltage: ±1.5%, ±2.5% (Ta = −40℃ to 105℃)
2) Super-low current consumption: 5 μA (Typ.)
3) Built-in watchdog timer
4) Reset delay time can be set with the CT pin's external capacitance.
5) Watchdog timer monitor time and reset time can be set with the CTW pin's external capacitance.
6) Output circuit type: N-channel open drain
7) Package: MSOP8 (BD37A□□FVM, BD87A□□FVM) / SOP8 (BD99A41F)

●Applications

All devices using microcontrollers or DSP, including vehicle equipment, displays, servers, DVD players, and telephone systems.

●Product line

INH logic	H: Active		L: Active
Model	BD37A□□FVM	BD99A41F	BD87A□□FVM
Detection voltage	1.9 V/4.1V	4.1 V	2.8V/2.9V/3.4 V/4.1V

●**Absolute maximum ratings** (Ta = 25℃)

Parameter	Symbol	Ratings	Unit
Power supply voltage	VDD	−0.3 to 10	V
CT pin voltage	VCT	−0.3 to VDD + 0.3	V
CTW pin voltage	VCTW	−0.3 to VDD + 0.3	V
RESET pin voltage	VRESET	−0.3 to VDD + 0.3	V
INH pin voltage	VINH	−0.3 to VDD + 0.3	V
CLK pin voltage	VCLK	−0.3 to VDD + 0.3	V
Power dissipation	Pd	470*1	mW
		550*2	
Operating ambient temperature	Topr	−40 to + 105	℃
Storage temperature	Tstg	−55 to + 125	℃
Maximum junction temperature	Tjmax	125	℃

*1 MSOP8 : Reduced by 4.70 mW/℃ over 25℃, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).
*2 SOP8 : Reduced by 5.50 mW/℃ over 25℃, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

●**Recommended operating ranges** (Ta = −40℃ to 105℃)

Parameter	Symbol	Min.	Max.	Unit
RESET power supply voltage	VDD RESET	1.0	10	V
WDT power supply voltage	VDD WDT	2.5	10	V

●**Electrical characteristics** (Unless otherwise specified, Ta = −40℃ to 105℃, VDD = 5 V)

Parameter		Symbol	Limits			Unit	Conditions
			Min.	Typ.	Max.		
[Overall]							
Total supply current 1 (during WDT operation)		IDD1	—	5	14	μA	INH : WDT ON Logic Input CTW = 0.1 μF
Total supply current 2 (when WDT stopped)		IDD2	—	5	14	μA	INH : WDT OFF Logic Input
Output leak current		Ileak	—	—	1	μA	VDD = VDS = 10 V
Output current capacity		IOL	0.7	—	—	mA	VDD = 1.2 V, VDS = 0.5 V
[RESET]							
Detection voltage 1	1.9V Detect	VDET1	1.871	1.900	1.929	V	Ta = 25℃
	2.8V Detect	VDET1	2.758	2.800	2.842	V	Ta = 25℃
	2.9V Detect	VDET1	2.886	2.930	2.974	V	Ta = 25℃
	3.4V Detect	VDET1	3.349	3.400	3.451	V	Ta = 25℃
	4.1V Detect	VDET1	4.039	4.100	4.162	V	Ta = 25℃
Detection voltage 2	1.9V Detect	VDET2	1.852	1.900	1.948	V	Ta = −40 to 105℃
	2.8V Detect	VDET2	2.730	2.800	2.870	V	Ta = −40 to 105℃
	2.9V Detect	VDET2	2.857	2.930	3.003	V	Ta = −40 to 105℃
	3.4V Detect	VDET2	3.315	3.400	3.485	V	Ta = −40 to 105℃
	4.1V Detect	VDET2	4.007	4.100	4.202	V	Ta = −40 to 105℃
Hysteresis width	1.9V Detect	Vrhys	VDET × 0.03	VDET × 0.13	VDET × 0.19	V	Ta = −40 to 105℃
	2.8V Detect	Vrhys	VDET × 0.018	VDET × 0.045	VDET × 0.060	V	Ta = −40 to 105℃
	2.9V Detect	Vrhys	VDET × 0.02	VDET × 0.05	VDET × 0.06	V	Ta = −40 to 105℃
	3.4V Detect	Vrhys	VDET × 0.02	VDET × 0.05	VDET × 0.07	V	Ta = −40 to 105℃
	4.1V Detect	Vrhys	VDET × 0.018	VDET × 0.035	VDET × 0.050	V	Ta = −40 to 105℃
RESET transmission delay time: low → high		TPLH	3.9	6.9	10.1	ms	CT = 0.001 μF*1 When VDD = VDET ±0.5 V
Delay circuit resistance		Rrst	5.8	10.0	14.5	MΩ	VCT = GND
Delay pin threshold voltage		VCTH	VDD × 0.3	VDD × 0.45	VDD × 0.6	V	RL = 470 KΩ
Delay pin output current		ICT	150	—	—	μA	VDD = 1.50 V, VCT = 0.5 V
Min. operating voltage		VOPL	1.0	—	—	V	VOL ≤ 0.4 V, RL = 470 KΩ
[WDT]							
WDT monitor time		TwH	7.0	10.0	20.0	ms	CTW = 0.01 μF*2
WDT reset time		TwL	2.4	3.3	7.0	ms	CTW = 0.01 μF*3
Clock input pulse width		TWCLK	500	—	—	ns	
CLK high threshold voltage		VCLKH	VDD × 0.8	—	VDD	V	
CLK low threshold voltage		VCLKL	0	—	VDD × 0.3	V	
CLK high threshold voltage		VINHH	VDD × 0.8	—	VDD	V	
CLK low threshold voltage		VINHL	0	—	VDD × 0.3	V	
CTW charge current		ICTWC	0.25	0.50	0.75	μA	VCTW = 0.2 V
CTW discharge current		ICTWO	0.75	1.50	2.00	μA	VCTW = 0.8 V

*1 TPLH can be varied by changing the CT capacitance value.
TPLH (s) ≈ 0.69 × Rrst (MΩ) × CT (μF) Rrst = 10 MΩ (Typ.)
*2 TwH can be varied by changing the CT capacitance value.
TwH (s) ≈ (0.5 × CTW (μF))/ICTWC (μA) ICTWC = 0.5 μA (Typ.)
*3 TwL can be varied by changing the CTW capacitance value.
TwL (s) ≈ (0.5 × CTW (μF))/ICTWO (μA) ICTWO = 1.5 μA (Typ.)
○ Note: This IC is not designed to be radiation-resistant.

●**Reference data** (Unless otherwise specified, Ta = 25℃) : 4.1V Detection

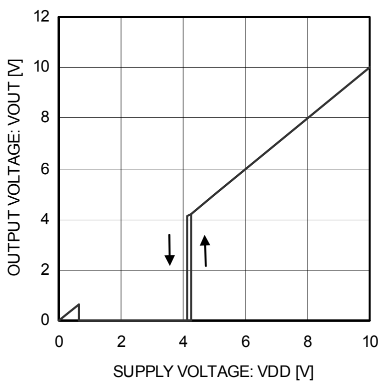


Fig.1 Detection Voltage

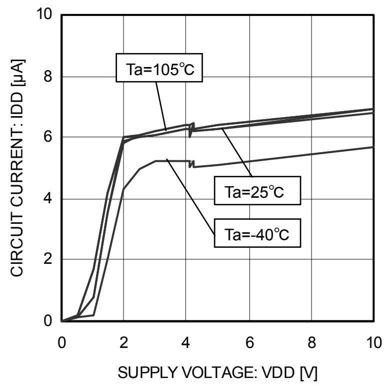


Fig.2 Total Supply Current

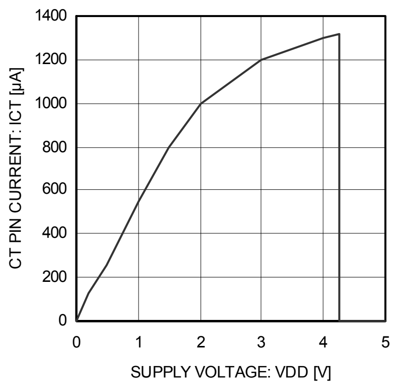


Fig.3 Delay Pin Current vs Power Supply Voltage

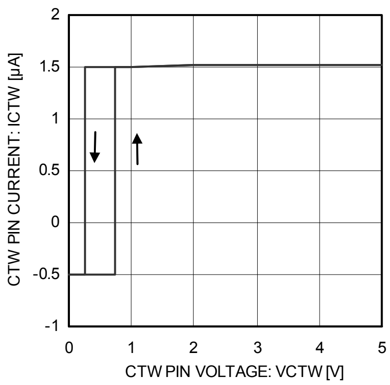


Fig.4 CTW Charge Discharge Current

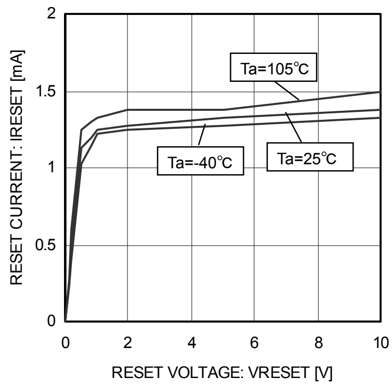


Fig.5 Output Current

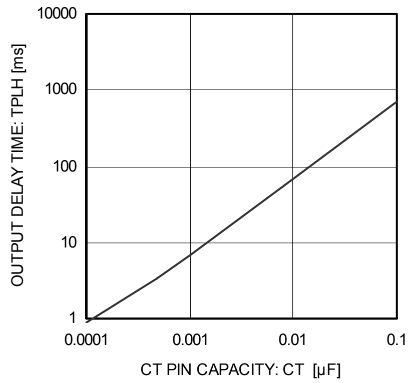


Fig.6 RESET Transmission Delay Time vs Capacitance

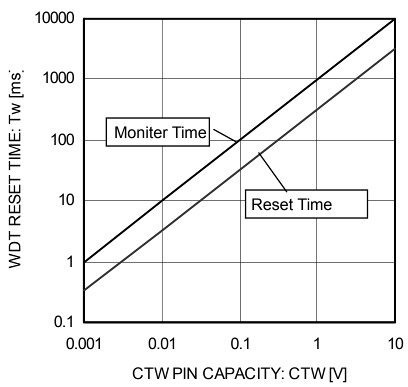


Fig.7 WDT Time vs Capacitance

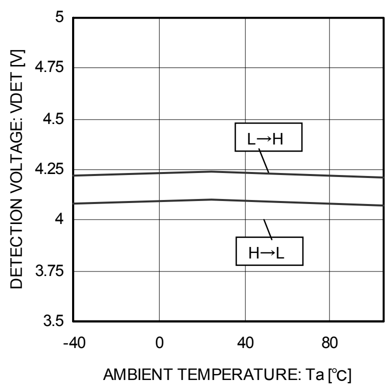


Fig.8 Detection Voltage vs Temperature

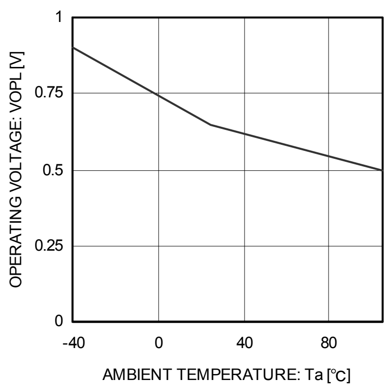


Fig.9 Operating Marginal Voltage vs Temperature

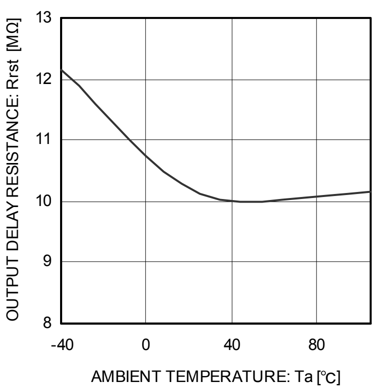


Fig.10 CT Pin Circuit Resistance vs Temperature

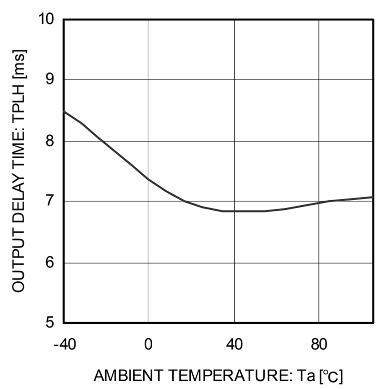


Fig.11 RESET Transmission Delay Time vs Temperature

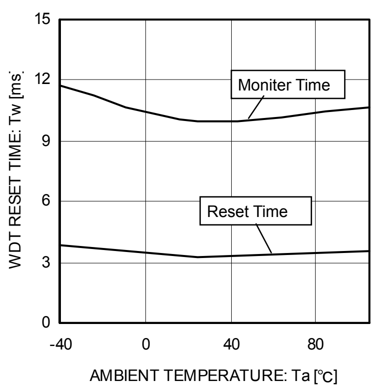
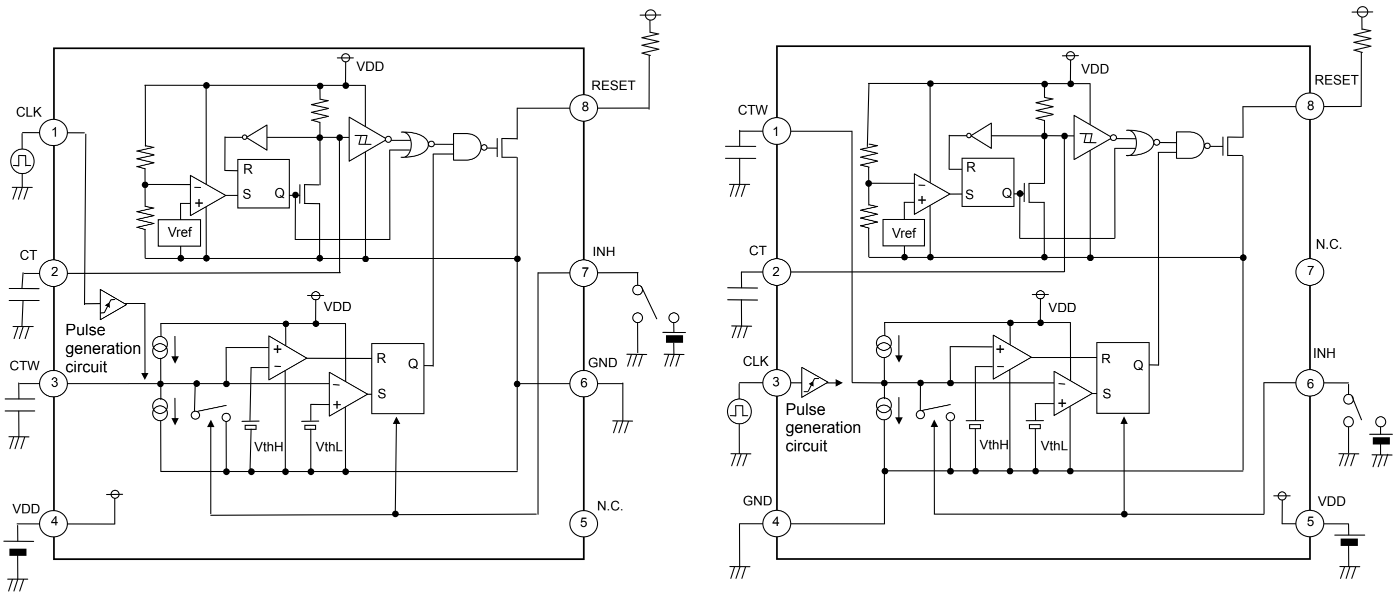


Fig.12 WDT Time vs Temperature

●Block diagram

BD37A□□FVM　　　　BD87A□□FVM / BD99A41F



CT pin capacitor: 470 pF to 3.3 μF
CTW pin capacitor: 0.001 μF to 10 μF

Fig.13

●Pin assignments

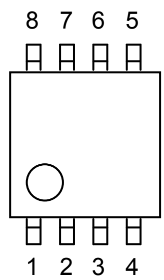


Fig.14

BD37A□□FVM

No.	Pin name	Function
1	CLK	Clock input from microcontroller
2	CT	Reset delay time setting capacitor connection pin
3	CTW	WDT time setting capacitor connection pin
4	VDD	Power supply pin
5	N.C.	NC pin
6	GND	GND pin
7	INH	WDT on/off setting pin INH=H/L:WDT=ON/OFF
8	RESET	Reset output pin

BD87A□□FVM / BD99A41F

No.	Pin name	Function
1	CTW	WDT time setting capacitor connection pin
2	CT	Reset delay time setting capacitor connection pin
3	CLK	Clock input from microcontroller
4	GND	GND pin
5	VDD	Power supply pin
6	INH	WDT on/off setting pin INH=H/L:WDT=OFF/ON(BD87A□□FVM) INH=H/L:WDT=ON/OFF(BD99A41F)
7	N.C.	NC pin
8	RESET	Reset output pin

●I/O Circuit diagram

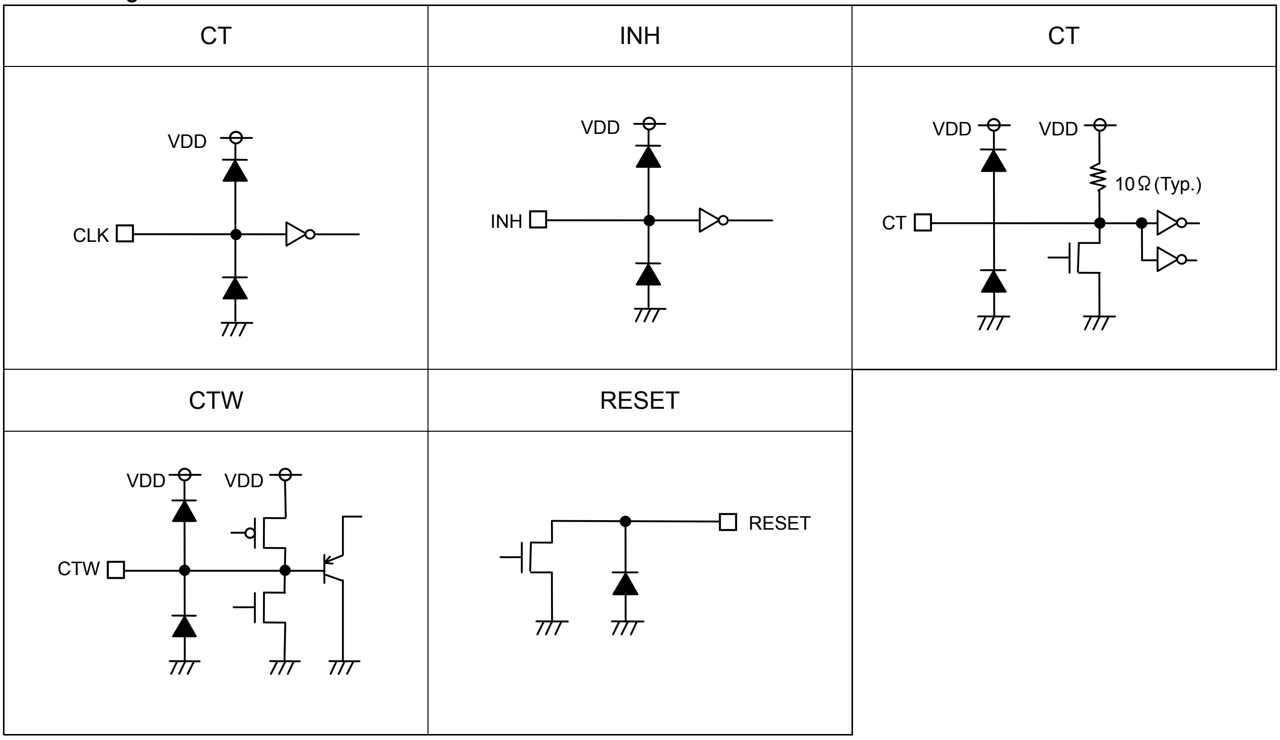


Fig.15

●Timing chart

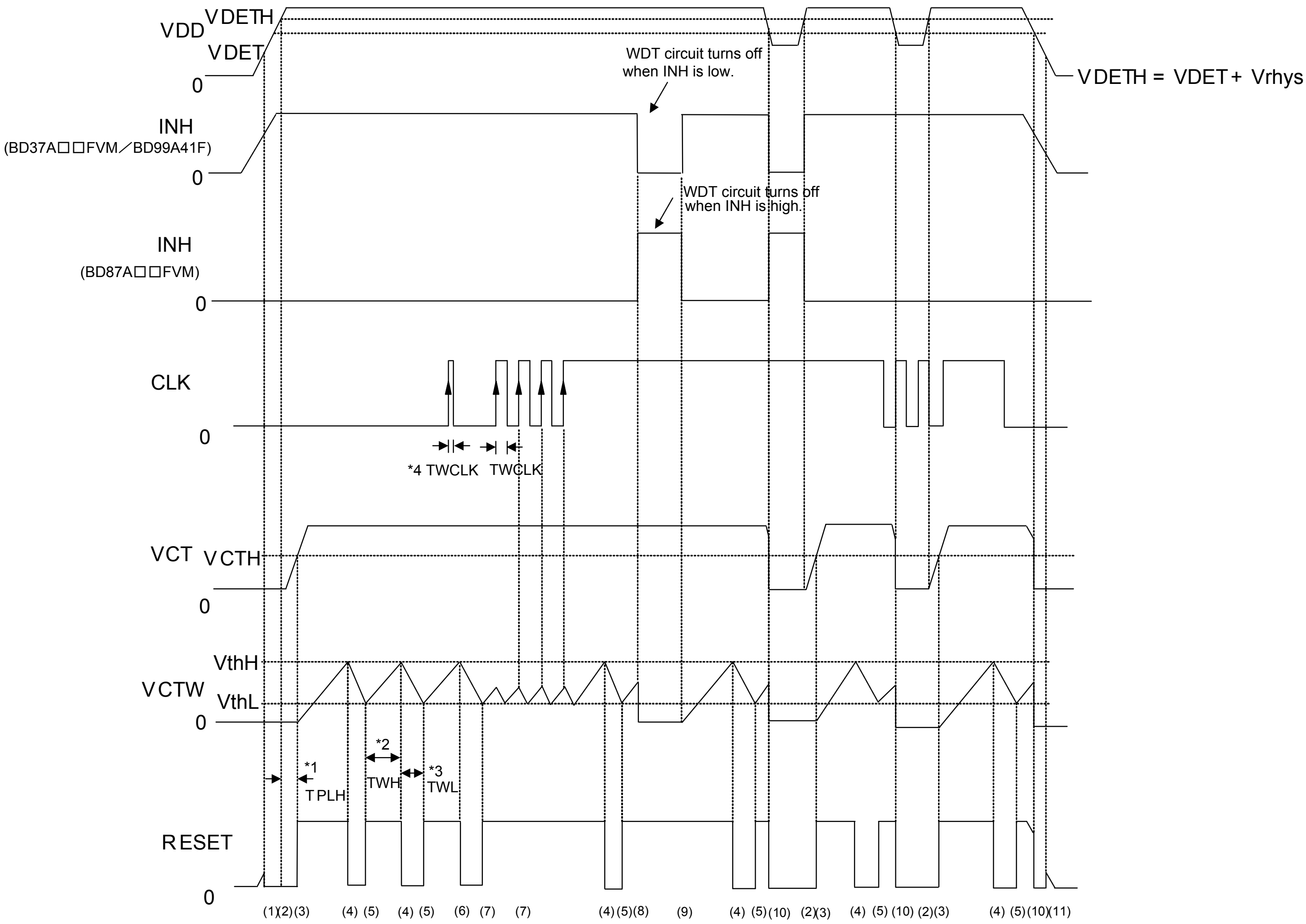


Fig.16

●Explanation

1) The RESET pin voltage (RESET) switches to low when the power supply voltage (VDD) falls to 0.8 V.

2) The external capacitor connected to the CT pin begins to charge when VDD rises above the reset detection voltage (VDETH). The RESET signal stays low until VDD reaches the VDETH voltage and switches to high when VDD reaches or exceeds the VDETH voltage. The RESET transmission delay time TPLH allowed to elapse before RESET switches from low to high is given by the following equation:
$$TPLH\ (s) \approx 0.69 \times Rrst \times CT\ (\mu F) \cdot\cdot\ [1]$$
Rrst denotes the IC's built-in resistance and is designed to be 10 MΩ (Typ.). CT denotes the external capacitor connected to the CT pin.

3) The external capacitor connected to the CTW pin begins to charge when RESET rises, triggering the watchdog timer.

4) The CTW pin state switches from charge to discharge when the CTW pin voltage (VCTW) reaches VthH, and RESET switches from high to low. The watchdog timer monitor time TWH is given by the following equation:
$$TWH\ (s) \approx (0.5 \times CTW\ (\mu F))/(ICTWC) \cdot\cdot\ [2]$$
ICTWC denotes the CTW charge current and is designed to be 0.50 μA (Typ.). CTW denotes the external capacitor connected to the CTW pin.

5) The CTW pin state switches from charge to discharge when VCTW reaches VthL, and RESET switches from low to high. The watchdog timer reset time TWL is given by the following equation:
$$TWL\ (s) \approx (0.5 \times CTW\ (\mu F))/(ICTWO) \cdot\cdot\ [3]$$
ICTWO denotes the CTW discharge current and is designed to be 1.50 μA (Typ.).

6) The CTW pin state may not switch from charge to discharge when the CLK input pulse width TWCLK is short. Use a TWCLK input pulse width of at least 500 ns.
$$TWCLK \geq 500\ ns\ (Min.)$$

7) When a pulse (positive edge trigger) of at least 500 ns is input to the CLK pin while the CTW pin is charging, the CTW state switches from charge to discharge. Once it discharges to VthL, it will charge again.

8) Watchdog timer operation is forced off when the INH pin switches to low:BD37A□□FVM (Switches to high: BD87A□□FVM, BD97A41F). At that time, only the watchdog timer is turned off. Reset detection is performed normally.

9) The watchdog timer function turns on when the INH pin switches to high. The external capacitor connected to the CTW pin begins to charge at that time.

10) RESET switches from high to low when VDD falls to the RESET detection voltage (VDET) or lower.

11) When VDD falls to 0 V, the RESET signal stays low until VDD reaches 0.8 V.

●Heat reduction curve

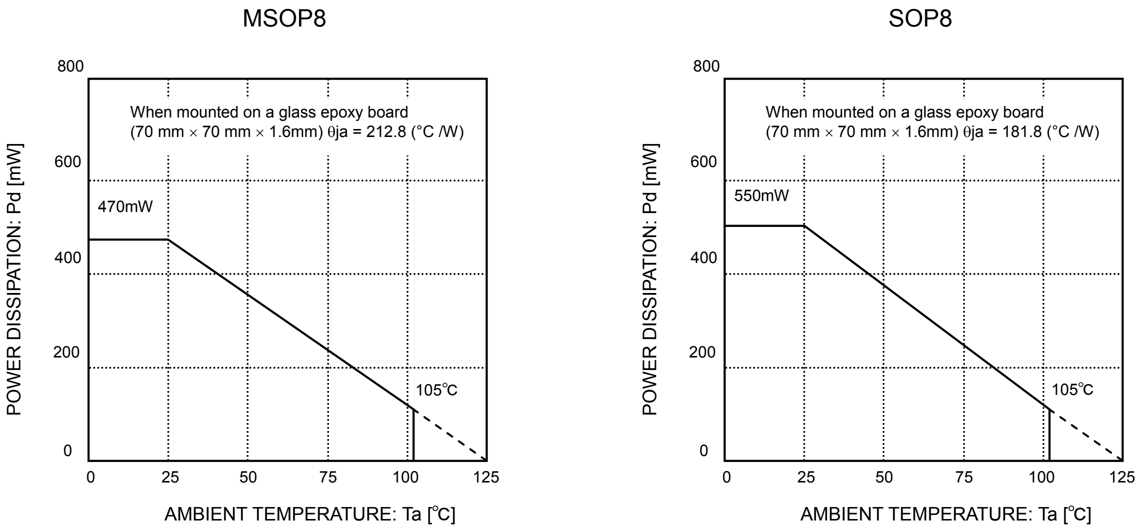


Fig.17

●External settings for pins and precautions

1) Connect a capacitor (0.001 µF to 1,000 µF) between the VDD and GND pins when the power line impedance is high. Use of the IC when the power line impedance is high may result in oscillation.

2) External capacitance
A capacitor must be connected to the CTW pin. When using a large capacitor such as 1 µF, the INH pin must allow a CTW discharge time of at least 2 ms. The power-on reset time is given by equation [1] on page 5. The WDT time is given by equations [2] and [3] on page 5, 6. The setting times are proportional to the capacitance value from the equations, so the maximum and minimum setting times can be calculated from the electrical characteristics according to the capacitance. Note however that the electrical characteristics do not include the external capacitor's temperature characteristics.

●Notes for use

1) Absolute maximum ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) GND voltage
The potential of GND pin must be minimum potential in all operating conditions.

3) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

5) Actions in strong electromagnetic field
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

7) Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

○When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

○When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

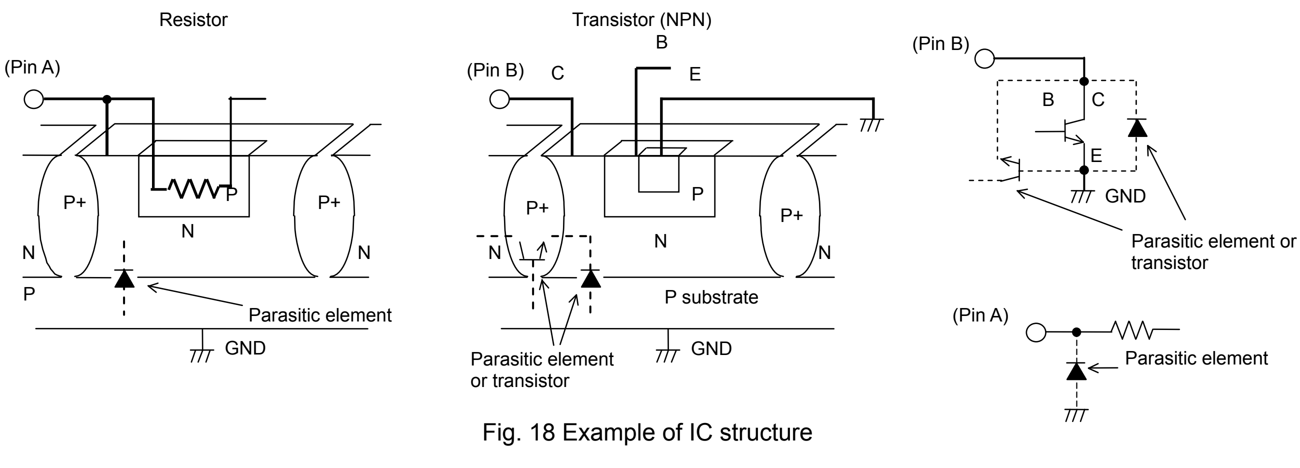


Fig. 18 Example of IC structure

8) Ground Wiring Pattern
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

9) Applications or inspection processes with modes where the potentials of the VDD pin and other pins may be reversed from their normal states may cause damage to the IC's internal circuitry or elements. Use an output pin capacitance of 1000 μF or lower in case VDD is shorted with the GND pin while the external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VDD or bypass diodes between Vcc and each pin.

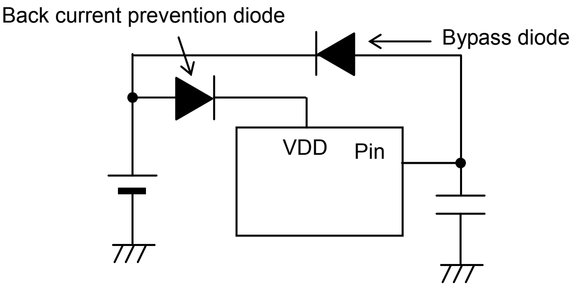


Fig.19

10) When VDD falls below the operating marginal voltage, output will be open. When output is being pulled up to input, output will be equivalent to VDD.

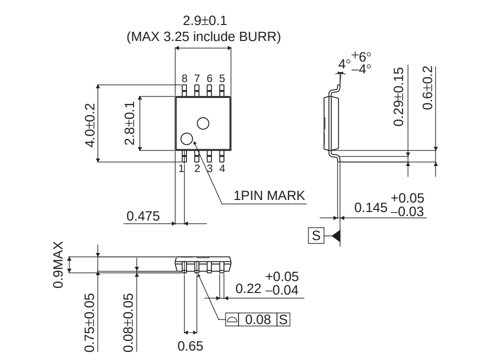
11) Input pin
The CLK and INH pins comprise inverter gates and should not be left open. (These pins should be either pulled up or down.) Input to the CLK pin is detected using a positive edge trigger and does not affect the CLK signal duty. Input the trigger to the CLK pin within the TWH time.

● Ordering part number

B	D		3	7	A	1	9		F	V	M	-	T	R

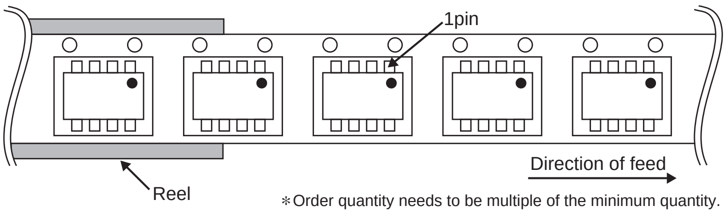
Part No.	Part No.	Package	Packaging and forming specification
BD	37A19, 37A41, 87A28, 87A29, 87A34, 87A41 99A41	FVM : MSOP8 F : SOP8	TR: Embossed tape and reel (MSOP8) E2: Embossed tape and reel (SOP8)

MSOP8



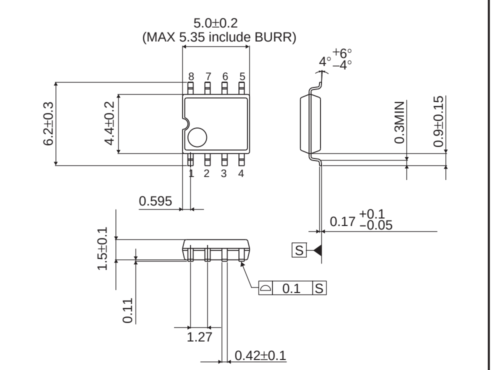
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



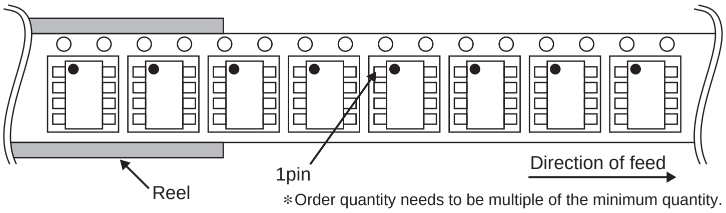
*Order quantity needs to be multiple of the minimum quantity.

SOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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