Am29LV800D

Data Sheet

For new designs, S29AL008D supersedes Am29LV800D and is the factory-recommended migration path. Please refer to the S29AL008D Data Sheet for specifications and ordering information.

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with “Am” and “MBM”. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

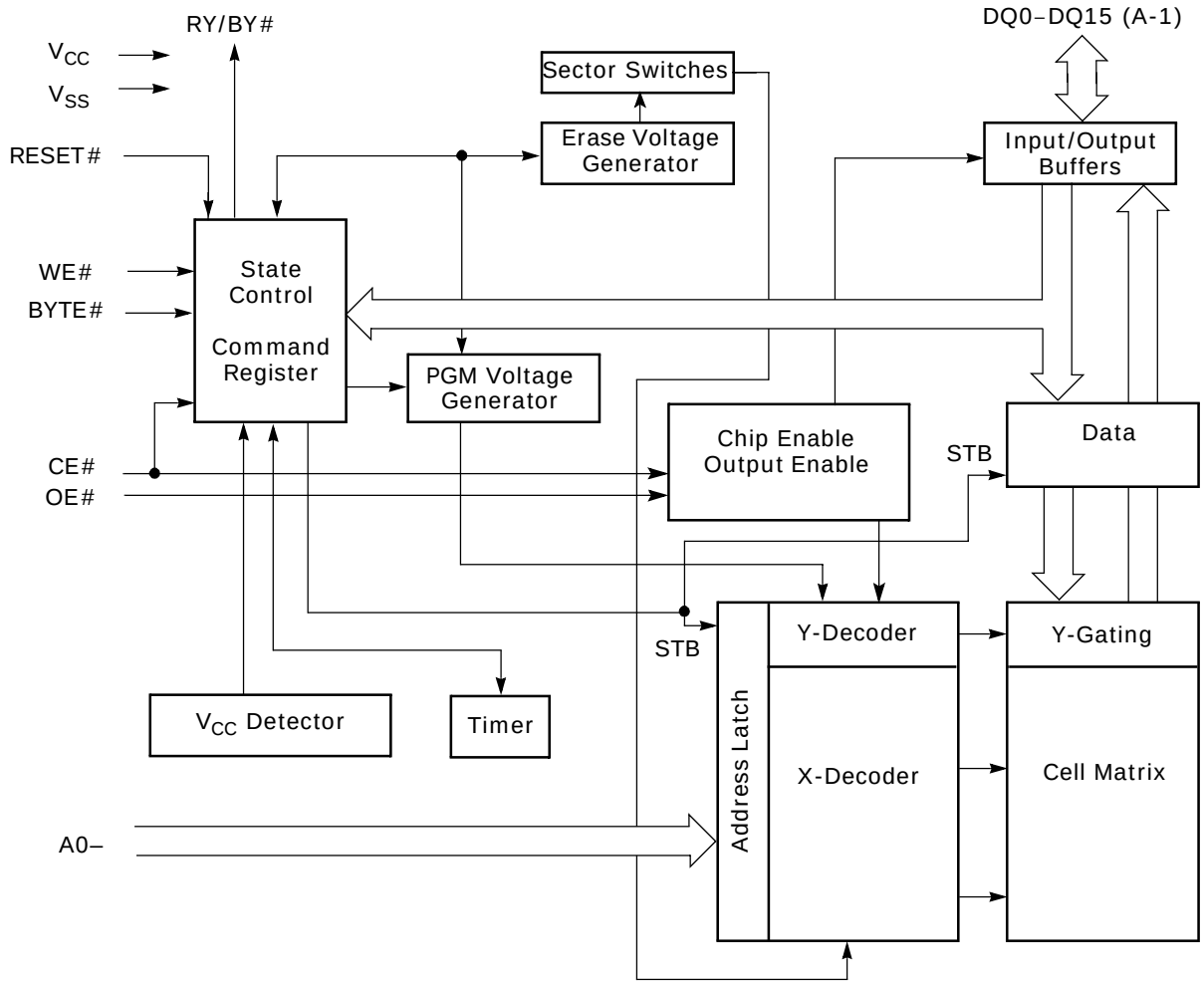
Publication Number **Am29LV800D_00** Revision **A** Amendment **4** Issue Date **January 21, 2005**

Product Selector Guide

Family Part Number		Am29LV800D		
Speed Options	Full Voltage Range: V_{CC} = 2.7–3.6 V	-70	-90	-120
Max access time, ns (t_{ACC})		70	90	120
Max CE# access time, ns (t_{CE})		70	90	120
Max OE# access time, ns (t_{OE})		30	35	50

Note: See "AC Characteristics" for full specifications.

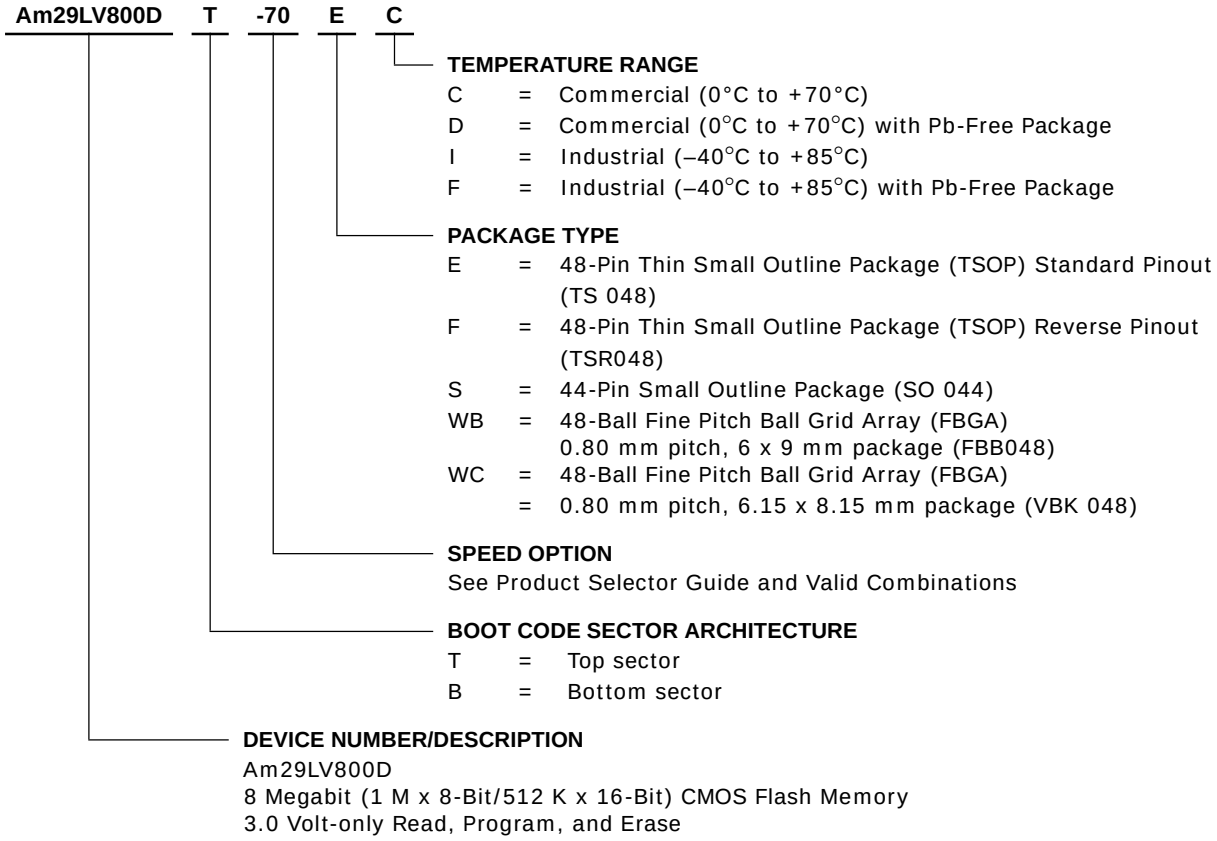
Block Diagram



Ordering Information

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations for TSOP and SO Packages	
AM29LV800DT-70, AM29LV800DB-70	EC, EI, ED, EF, FC, FD, FF, FI, SC, SD, SF, SI
AM29LV800DT-90, AM29LV800DB-90	EC, EI, ED,EF,FD, FF,FC, FI,SD, SFSC, SI
AM29LV800DT-120, AM29LV800DB-120	

Valid Combinations for FBGA Packages			
Order Number		**Package Marking**	
AM29LV800DT-70, AM29LV800DB-70	WBC WBI WBD WBF WCC WCI WCD WCF	L800DT70V, L800DB70V	C, I, D,F
AM29LV800DT-90, AM29LV800DB-90	WCC WCI WCD WCF WBC WBI WBD WBF	L800DT90V, L800DB90V	
AM29LV800DT-120, AM29LV800DB-120	WBC WBI WBD WBF	L800DT12V, L800DB12V	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29LV800D Device Bus Operations

Operation	CE#	OE #	WE #	RESET #	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
							BYTE # = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	
Standby	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

1. Addresses are A18:A0 in word mode (BYTE# = V_{IH}), A18:A-1 in byte mode (BYTE# = V_{IL}).
2. The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection/Unprotection" section.

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to Figure 1 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 1 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Am29LV800DT Top Boot Block Sector Addresses

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
									(x8) Address Range	(x16) Address Range
SA0	0	0	0	0	X	X	X	64/32	00000h–0FFFFh	00000h–07FFFh
SA1	0	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA2	0	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA3	0	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA4	0	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA5	0	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA6	0	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA7	0	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh
SA8	1	0	0	0	X	X	X	64/32	80000h–8FFFFh	40000h–47FFFh
SA9	1	0	0	1	X	X	X	64/32	90000h–9FFFFh	48000h–4FFFFh
SA10	1	0	1	0	X	X	X	64/32	A0000h–AFFFFh	50000h–57FFFh
SA11	1	0	1	1	X	X	X	64/32	B0000h–BFFFFh	58000h–5FFFFh
SA12	1	1	0	0	X	X	X	64/32	C0000h–CFFFFh	60000h–67FFFh
SA13	1	1	0	1	X	X	X	64/32	D0000h–DFFFFh	68000h–6FFFFh
SA14	1	1	1	0	X	X	X	64/32	E0000h–EFFFFh	70000h–77FFFh
SA15	1	1	1	1	0	X	X	32/16	F0000h–F7FFFh	78000h–7BFFFh
SA16	1	1	1	1	1	0	0	8/4	F8000h–F9FFFh	7C000h–7CFFFh
SA17	1	1	1	1	1	0	1	8/4	FA000h–FBFFFh	7D000h–7DFFFh
SA18	1	1	1	1	1	1	X	16/8	FC000h–FFFFFh	7E000h–7FFFFh

Table 3. Am29LV800DB Bottom Boot Block Sector Addresses

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
									(x8) Address Range	(x16) Address Range
SA0	0	0	0	0	0	0	X	16/8	00000h–03FFFh	00000h–01FFFh
SA1	0	0	0	0	0	1	0	8/4	04000h–05FFFh	02000h–02FFFh
SA2	0	0	0	0	0	1	1	8/4	06000h–07FFFh	03000h–03FFFh
SA3	0	0	0	0	1	X	X	32/16	08000h–0FFFFh	04000h–07FFFh
SA4	0	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA5	0	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA6	0	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA7	0	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA8	0	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA9	0	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA10	0	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh
SA11	1	0	0	0	X	X	X	64/32	80000h–8FFFFh	40000h–47FFFh
SA12	1	0	0	1	X	X	X	64/32	90000h–9FFFFh	48000h–4FFFFh
SA13	1	0	1	0	X	X	X	64/32	A0000h–AFFFFh	50000h–57FFFh
SA14	1	0	1	1	X	X	X	64/32	B0000h–BFFFFh	58000h–5FFFFh
SA15	1	1	0	0	X	X	X	64/32	C0000h–CFFFFh	60000h–67FFFh
SA16	1	1	0	1	X	X	X	64/32	D0000h–DFFFFh	68000h–6FFFFh
SA17	1	1	1	0	X	X	X	64/32	E0000h–EFFFFh	70000h–77FFFh
SA18	1	1	1	1	X	X	X	64/32	F0000h–FFFFFh	78000h–7FFFFh

Note for Tables 2 and 3: Address range is A18:A-1 in byte mode and A18:A0 in word mode. See "Word/Byte Configuration" section.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 4. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Tables 2 and 3). Table 4 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 5. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 4. Am29LV800D Autoselect Codes (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A18 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: AMD		L	L	H	X	X	V_{ID}	X	L	X	L	L	X	01h
Device ID: Am29LV800B (Top Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	DAh
	Byte	L	L	H									X	DAh
Device ID: Am29LV800B (Bottom Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	5Bh
	Byte	L	L	H									X	5Bh
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	01h (protected)
													X	00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

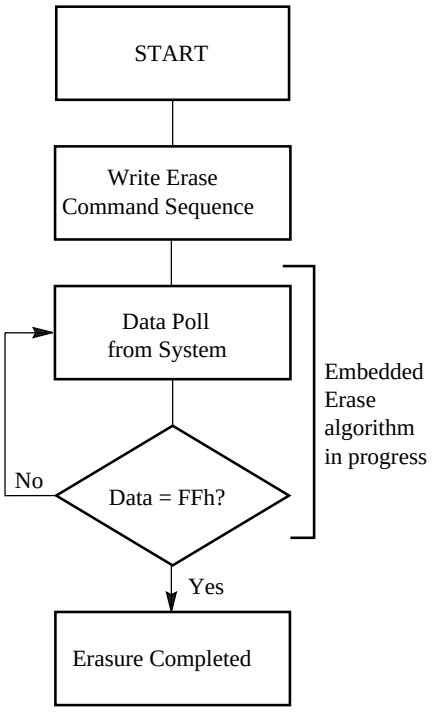
Sector Protection/unprotection can be implemented via two methods.

The primary method requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 1 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0 volt-only AMD flash devices. Publication number 20536 contains further details; contact an AMD representative to request a copy.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 1 shows the algo-



Notes:
1. See Table 5 for erase command sequence.
2. See "DQ3: Sector Erase Timer" for more information.

Figure 1. Erase Operation

Table 5. Am29LV800D Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2-5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	01				
		Byte		AAA		555		AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	90	X01	22DA				
		Byte		AAA		555		AAA		X02	DA				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	555	90	X01	225B				
		Byte		AAA		555		AAA		X02	5B				
	Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
											XX01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 10)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)			2	XXX	90	XXX	00								

Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 12)		1	XXX	B0										
Erase Resume (Note 13)		1	XXX	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A18–A12 uniquely select any sector.

Notes:

1. See Table 1 for description of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operations.
4. Data bits DQ15–DQ8 are don't cares for unlock and command cycles.
5. Address bits A18–A11 are don't cares for unlock and command cycles, unless PA or SA required.
6. No unlock or command cycles required when reading array data.
7. The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).
8. The fourth cycle of the autoselect command sequence is a read cycle.
9. The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.
10. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
11. The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.
12. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
13. The Erase Resume command is valid only during the Erase Suspend mode.

Write Operation Status

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 6 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1";

Table 6. Write Operation Status

Operation		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +85°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#, and
RESET# (Note 2) . . . . . –0.5 V to +12.5 V

All other pins (Note 1). . . . . –0.5 V to V_{CC}+0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 2. Maximum DC voltage on input or I/O pins is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 3.
2. Minimum DC input voltage on pins A9, OE#, and RESET# is –0.5 V. During voltage transitions, A9, OE#, and RESET# may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 2. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied.

Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . .0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . .–40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range . . . . +3.0 V to +3.6 V

V_{CC} for full voltage range . . . . . +2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed

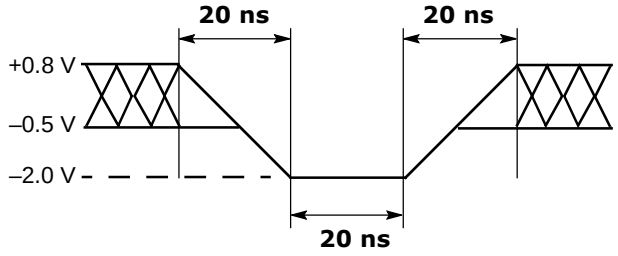


Figure 2. Maximum Negative Overshoot Waveform

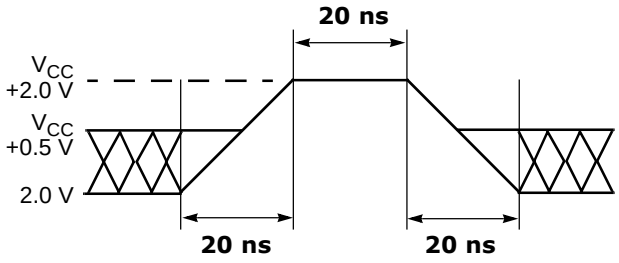


Figure 3. Maximum Positive Overshoot Waveform

DC Characteristics

CMOS Compatible

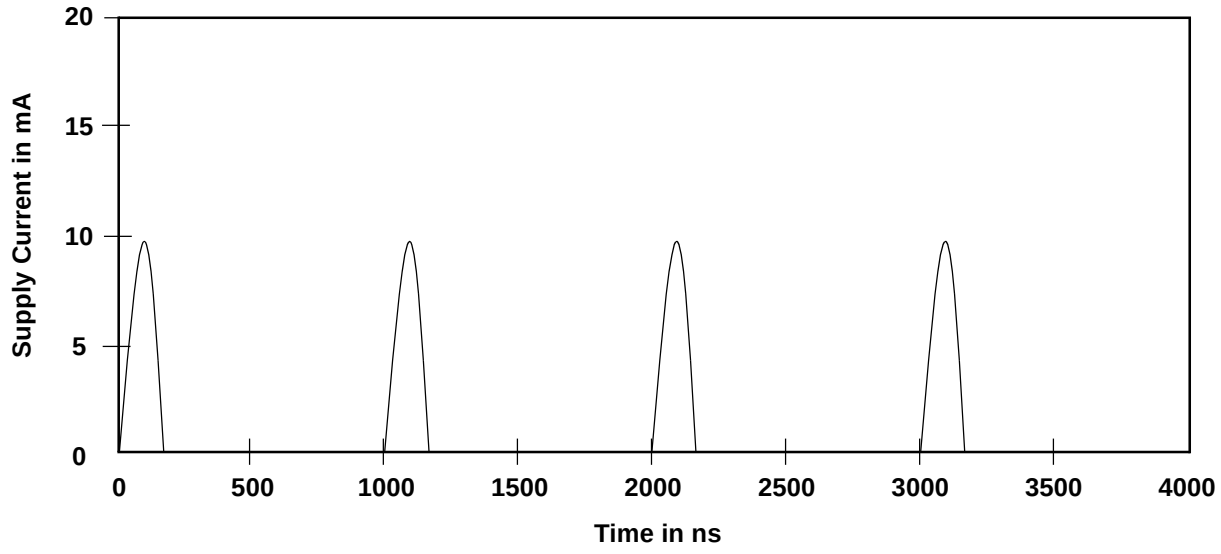
Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	V_{CC} = $V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		7	15	mA
			1 MHz		2	4	
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		7	15	
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3, 5)	CE# = V_{IL}, OE# = V_{IH}			15	30	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET# = V_{CC}±0.3 V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	V_{IH} = V_{CC} ± 0.3 V; V_{IL} = V_{SS} ± 0.3 V			0.2	5	µA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, V_{CC} = $V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, V_{CC} = $V_{CC\ min}$		0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = $V_{CC\ min}$		V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)			2.3		2.5	V

Notes:

1. The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 3.0 V.
2. Maximum I_{CC} specifications are tested with V_{CC} = V_{CCmax}.
3. I_{CC} active while Embedded Erase or Embedded Program is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.
5. Not 100% tested.

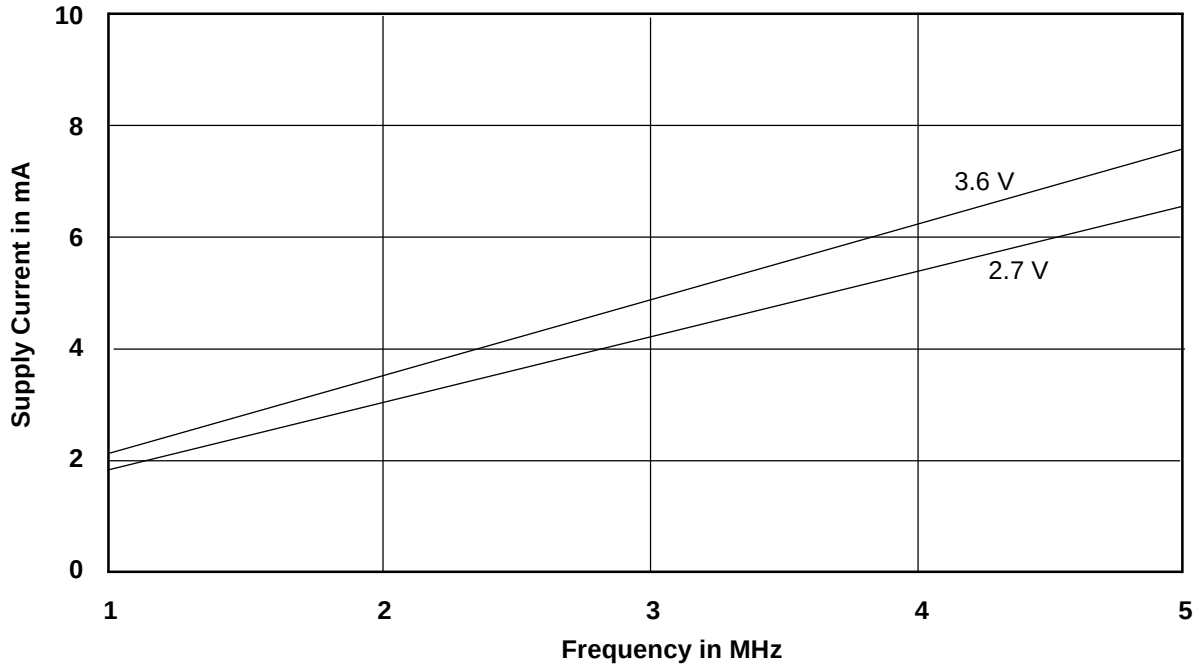
DC Characteristics (Continued)

Zero Power Flash



Note: Addresses are switching at 1 MHz

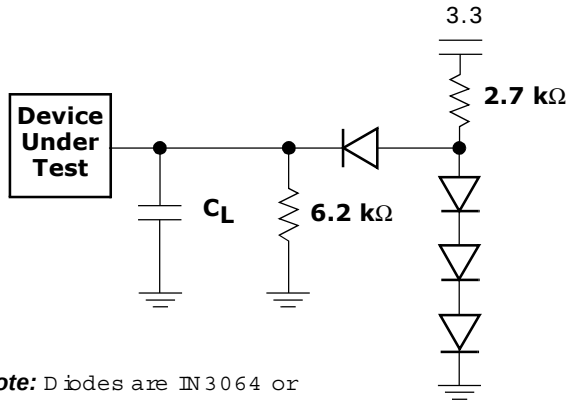
Figure 1. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: T = 25 °C

Figure 1. Typical I_{CC1} vs. Frequency

Test Conditions



Note: Diodes are IN3064 or

Figure 1. Test Setup

Table 7. Test Specifications

Test Condition	-70	-90, -120	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

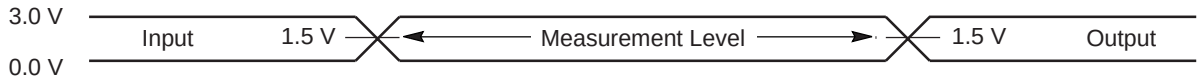


Figure 1. Input Waveforms and Measurement Levels

AC Characteristics

Read Operations

Parameter		Description		Test Setup		Speed Options			Unit
JEDEC	Std					-70	-90	-120	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	25	30	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0			ns

Notes:
1. Not 100% tested.
2. See Figure 1 and Table 7 for test specifications.

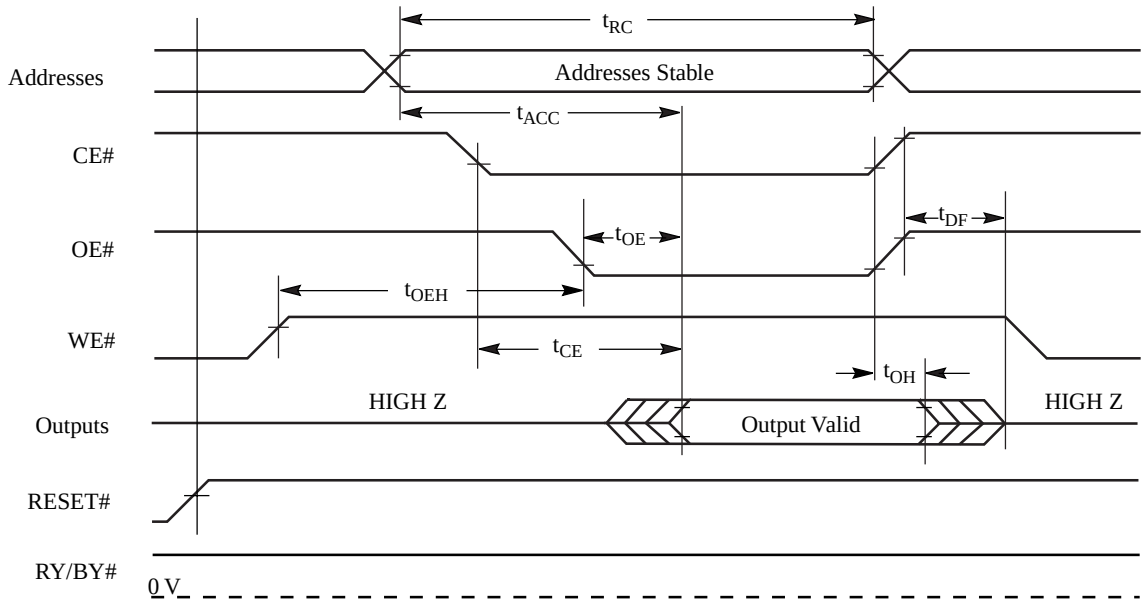


Figure 1. Read Operations Timings

AC Characteristics

Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note: Not 100% tested.

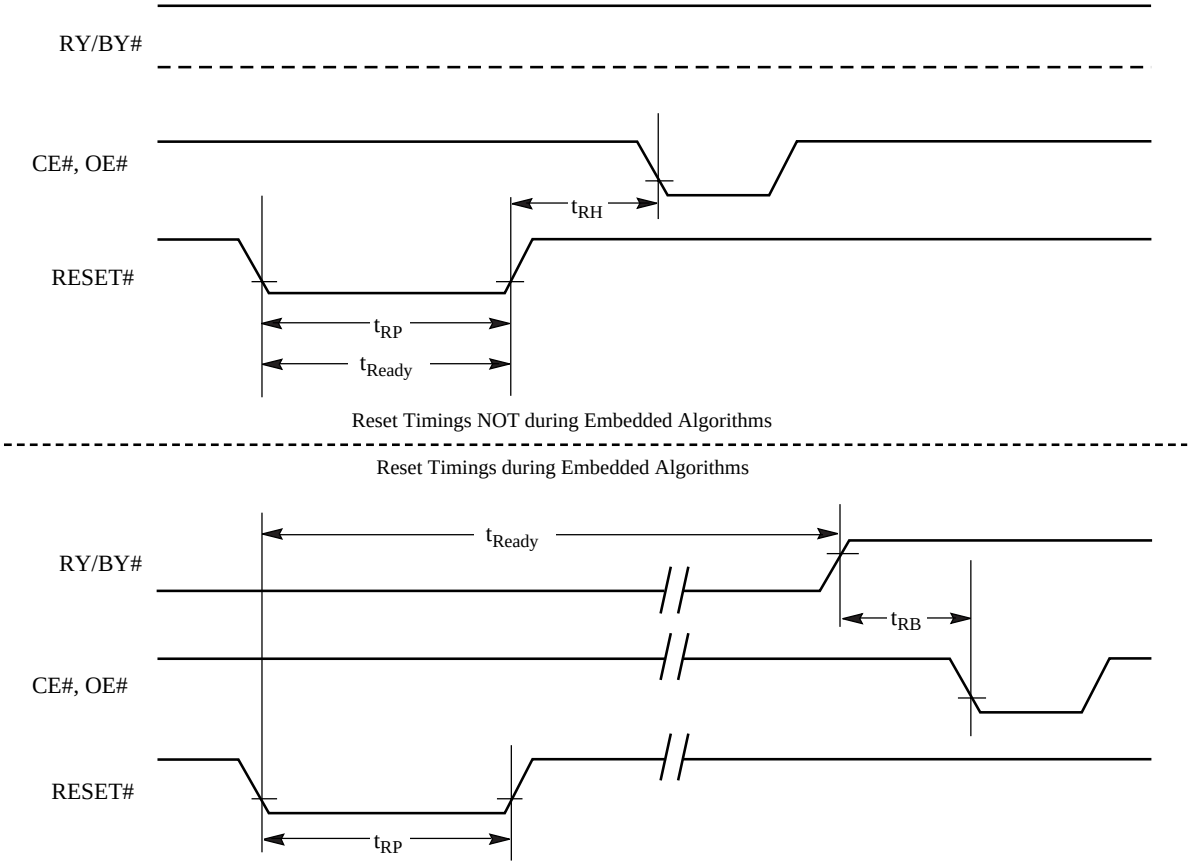


Figure 1. RESET# Timings

AC Characteristics

Word/Byte Configuration (BYTE#)

Parameter		Description		Speed Options			Unit
JEDEC	Std			-70	-90	-120	
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max	5			ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	25	30	30	ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	70	90	120	ns

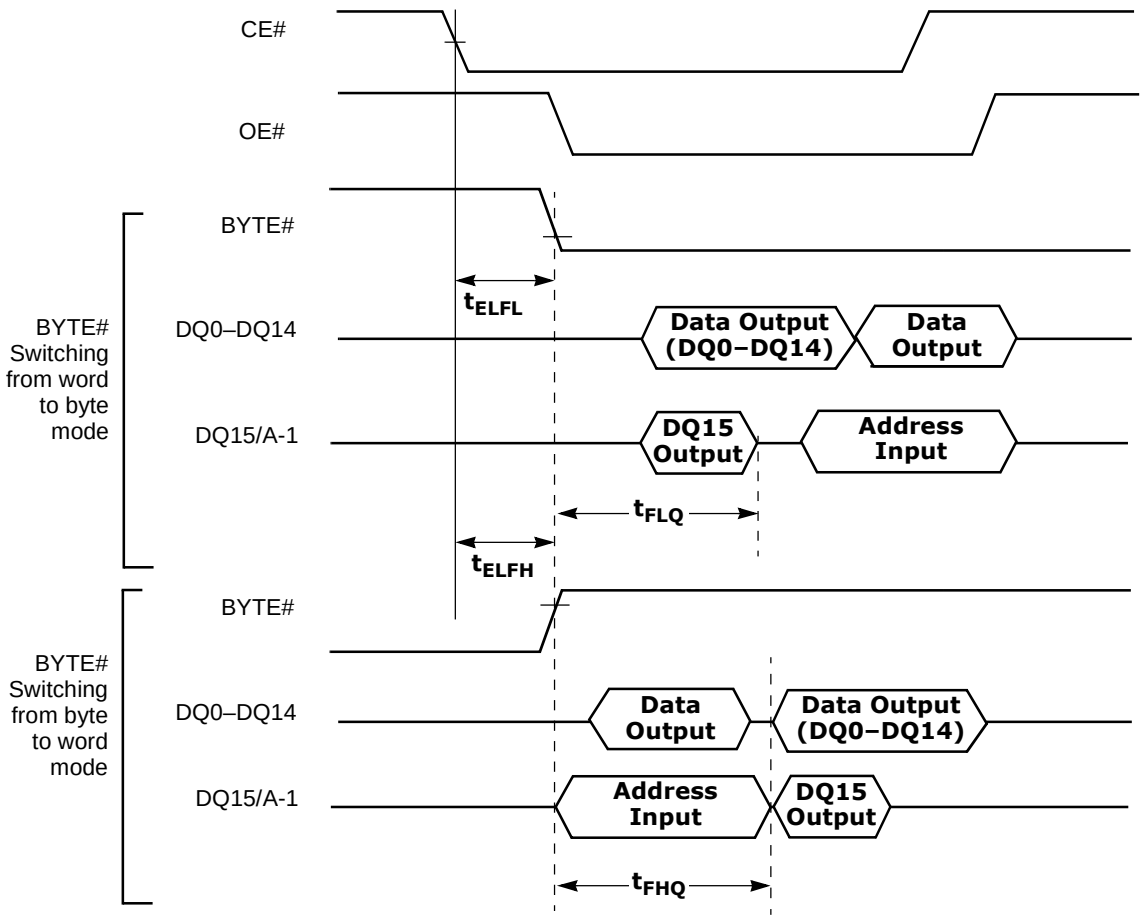
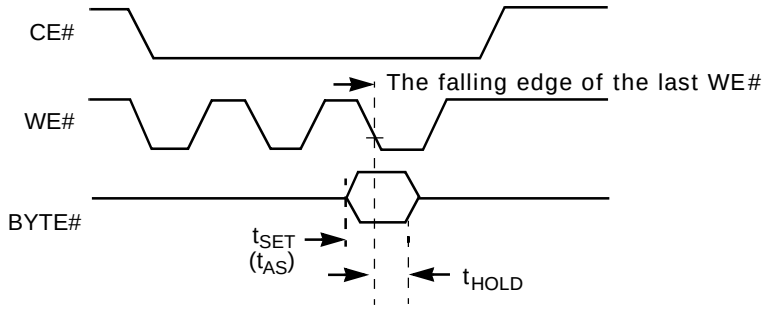


Figure 1. BYTE# Timings for Read Operations



Note: *Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.*

Figure 1. BYTE# Timings for Write Operations

AC Characteristics

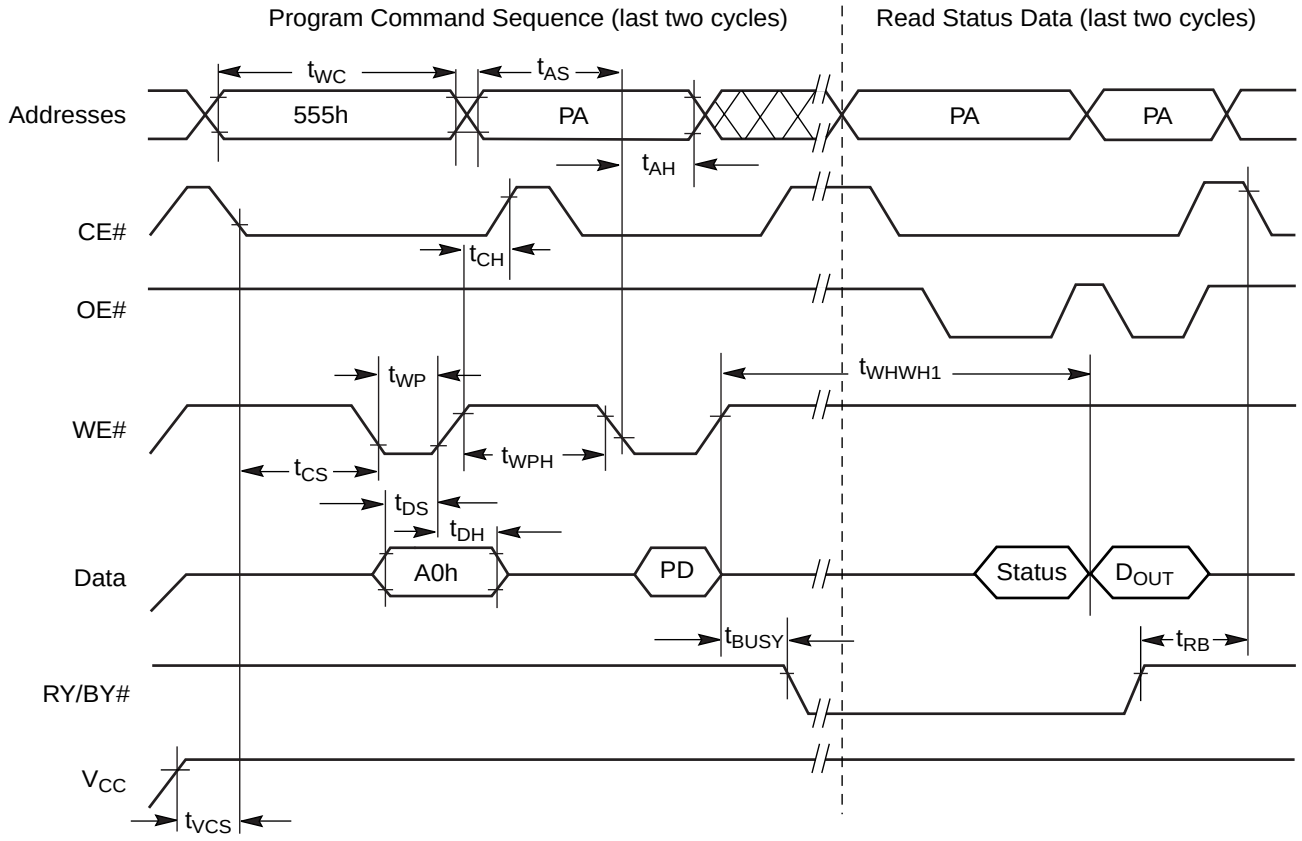
Erase/Program Operations

Parameter		Description			Speed Options			Unit
JEDEC	Std				-70	-90	-120	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0			ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0			ns
	t_{OES}	Output Enable Setup Time		Min	0			ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0			ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	8			µs
			Word	Typ	16			
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	1			sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50			µs
	t_{RB}	Recovery Time from RY/BY#		Min	0			ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Min	90			ns

Notes:

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

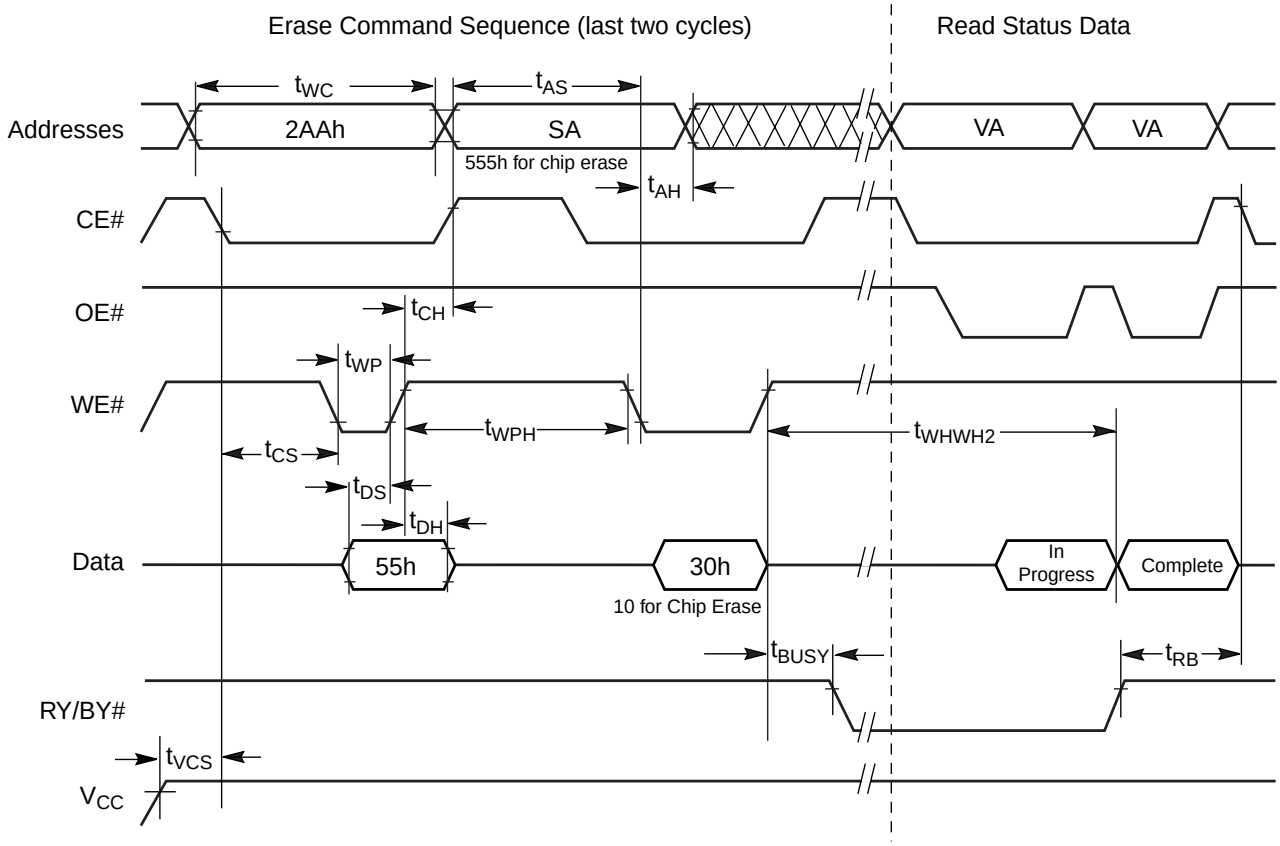
AC Characteristics



Notes:
1. PA = program address, PD = program data, D_{OUT} is the true data at the program address.
2. Illustration shows device in word mode.

Figure 1. Program Operation Timings

AC Characteristics

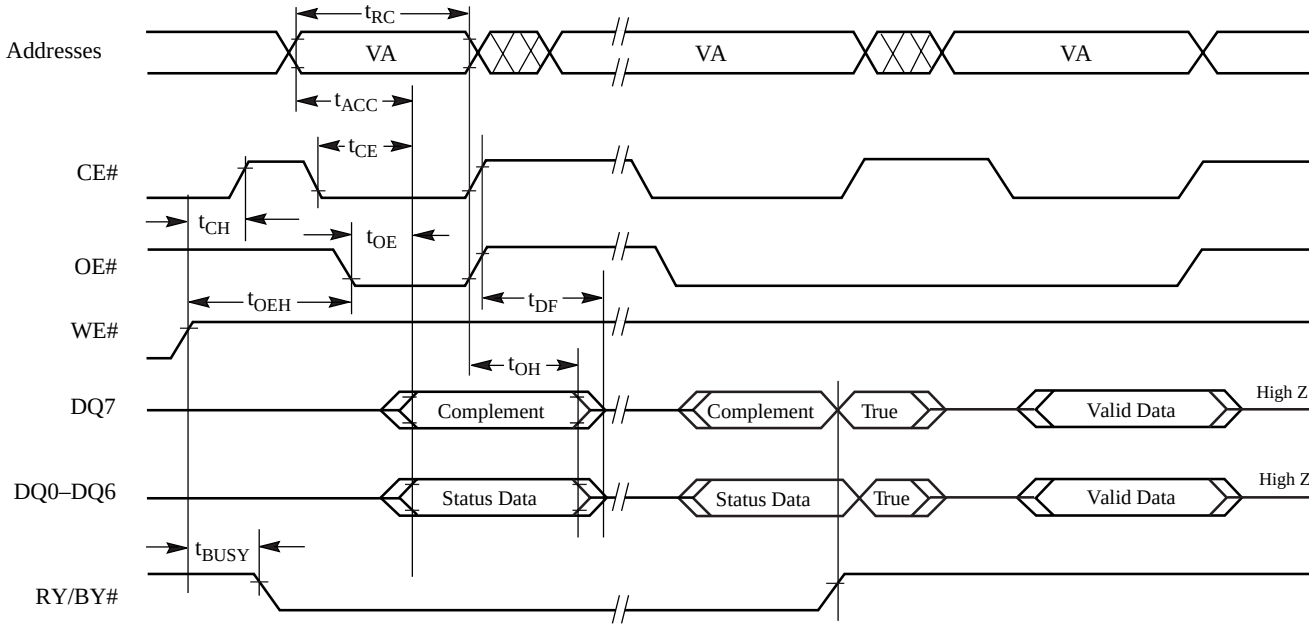


Notes:

1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").
2. Illustration shows device in word mode.

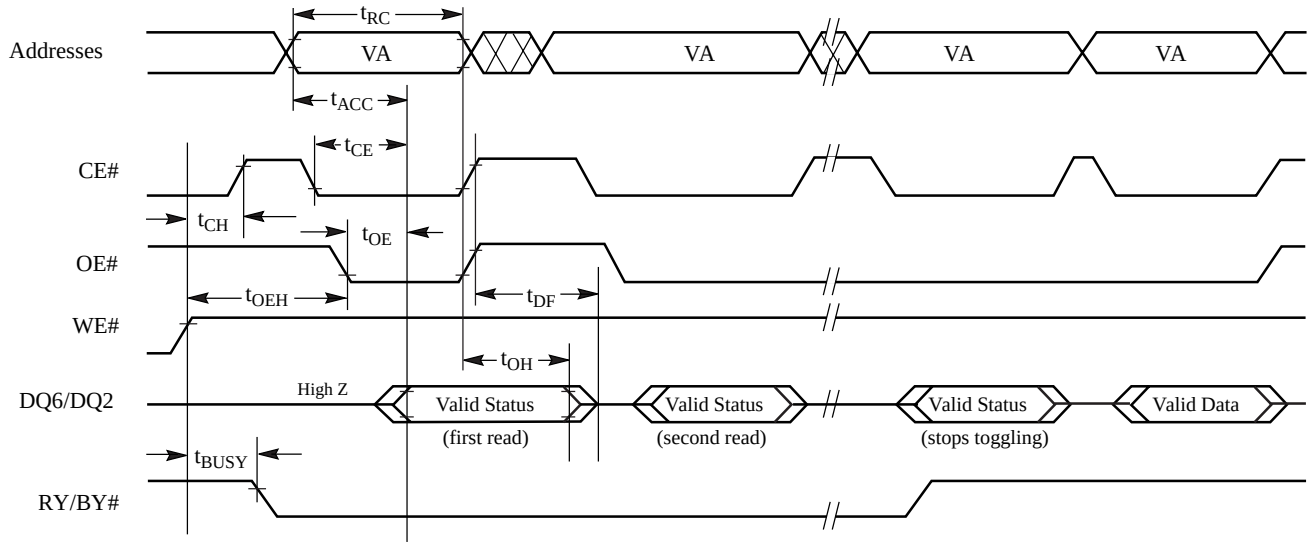
Figure 1. Chip/Sector Erase Operation Timings

AC Characteristics



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

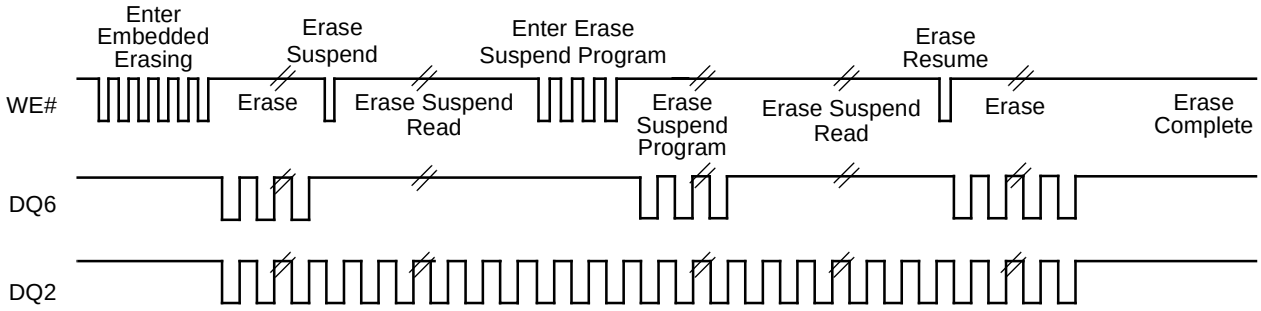
Figure 1. Data# Polling Timings (During Embedded Algorithms)



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 1. Toggle Bit Timings (During Embedded Algorithms)

AC Characteristics



Note: *The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

Figure 1. DQ2 vs. DQ6

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note: Not 100% tested.

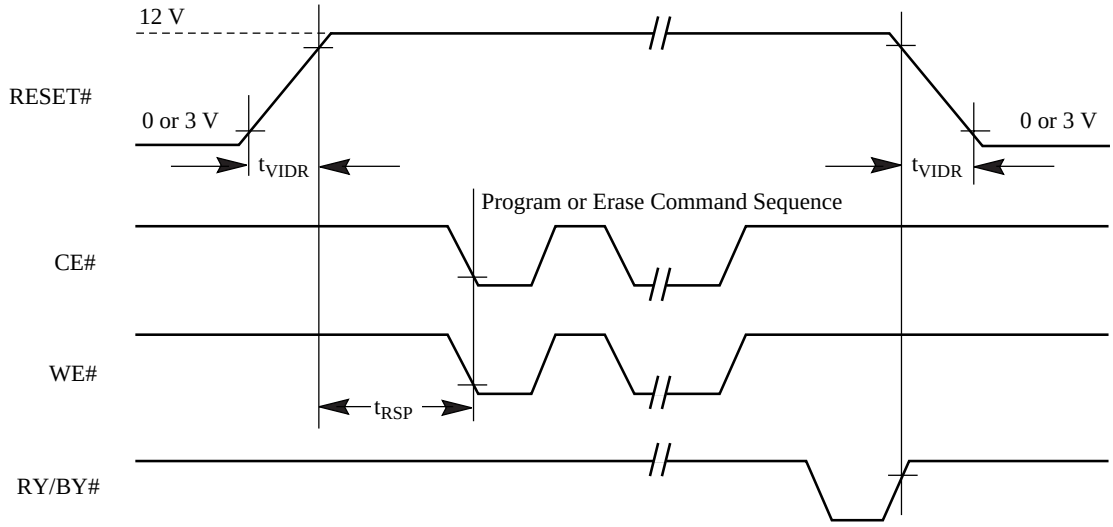
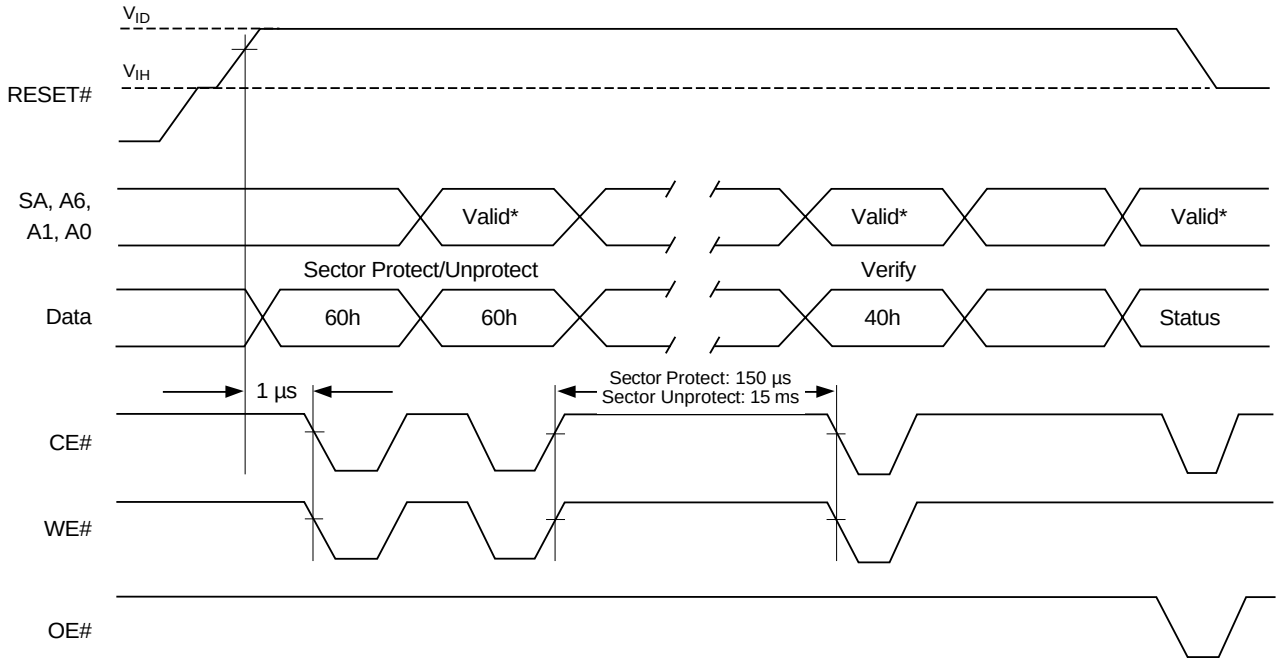


Figure 1. Temporary Sector Unprotect Timing Diagram

AC Characteristics



* *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 1. Sector Protect/Unprotect Timing Diagram

AC Characteristics

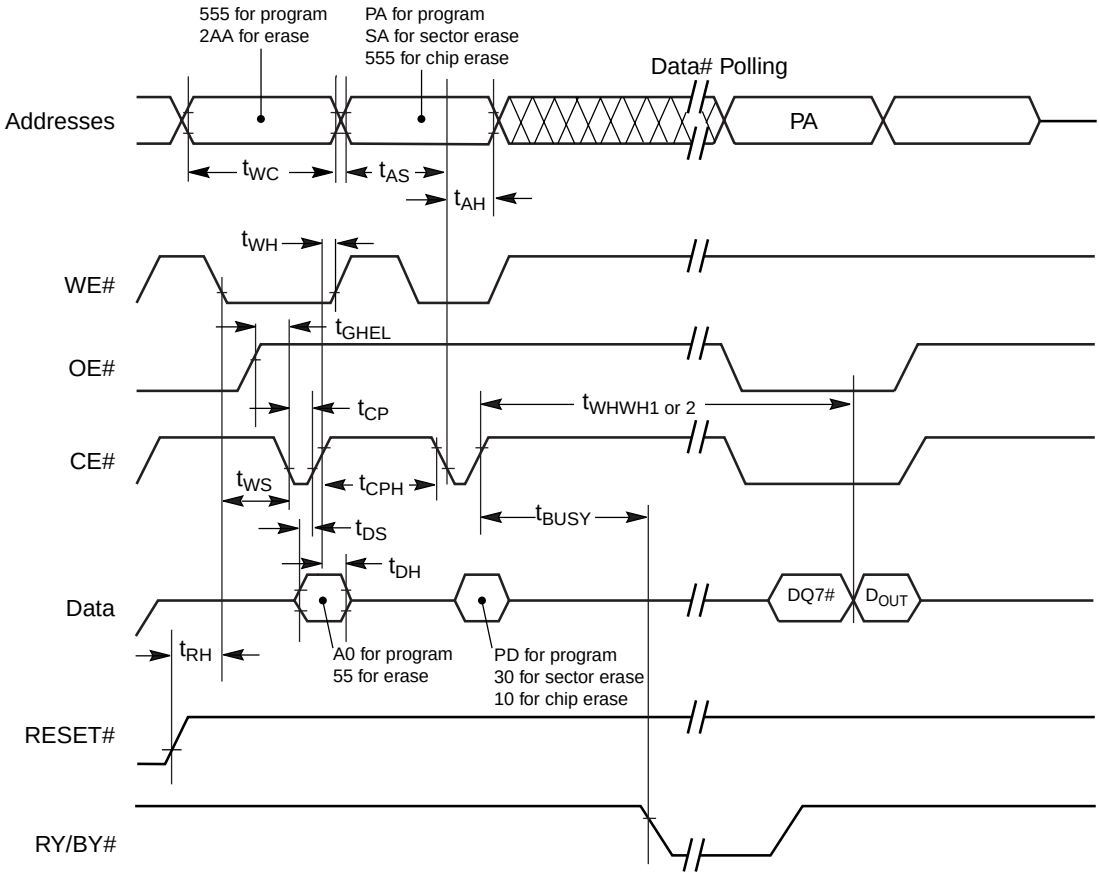
Alternate CE# Controlled Erase/Program Operations

Parameter		Description			Speed Options			Unit
JEDEC	Std				-70	-90	-120	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0			ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0			ns
	t_{OES}	Output Enable Setup Time		Min	0			ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0			ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0			ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0			ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35	35	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	8			µs
			Word	Typ	16			
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	1			sec

Notes:

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

AC Characteristics



Notes:

1. PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.
2. Figure indicates the last two bus cycles of command sequence.
3. Word mode address used as an example.

Figure 1. Alternate CE# Controlled Write Operation Timings

Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		1	10	s	Excludes 00h programming prior to erasure
Chip Erase Time		14		s	
Byte Programming Time		8	300	µs	Excludes system level overhead (Note 5)
Word Programming Time		16	360	µs	
Chip Programming Time (Note 3)	Byte Mode	8.4	25	s	
	Word Mode	5.8	17	s	

Notes:

1. Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.
2. Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 5 for further information on command definitions.
6. The device has a guaranteed minimum erase and program cycle endurance of 1,000,000 cycles.

Latchup Characteristics

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

TSOP and SO Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

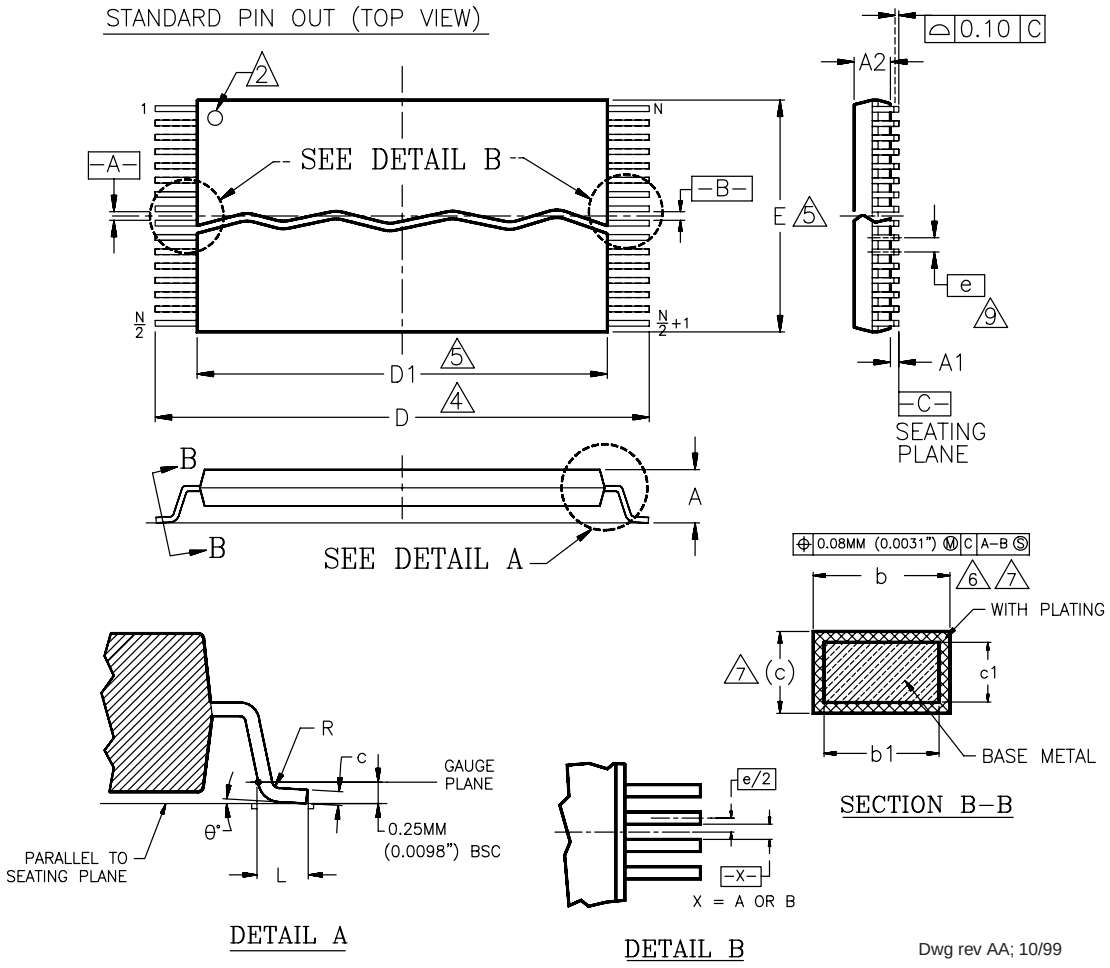
1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz.

Data Retention

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

Physical Dimensions*

TS 048—48-Pin Standard TSOP



Package	TS 048		
Jedec	MO–142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

* For reference only. BSC is an ANSI standard for Basic Space Centering.