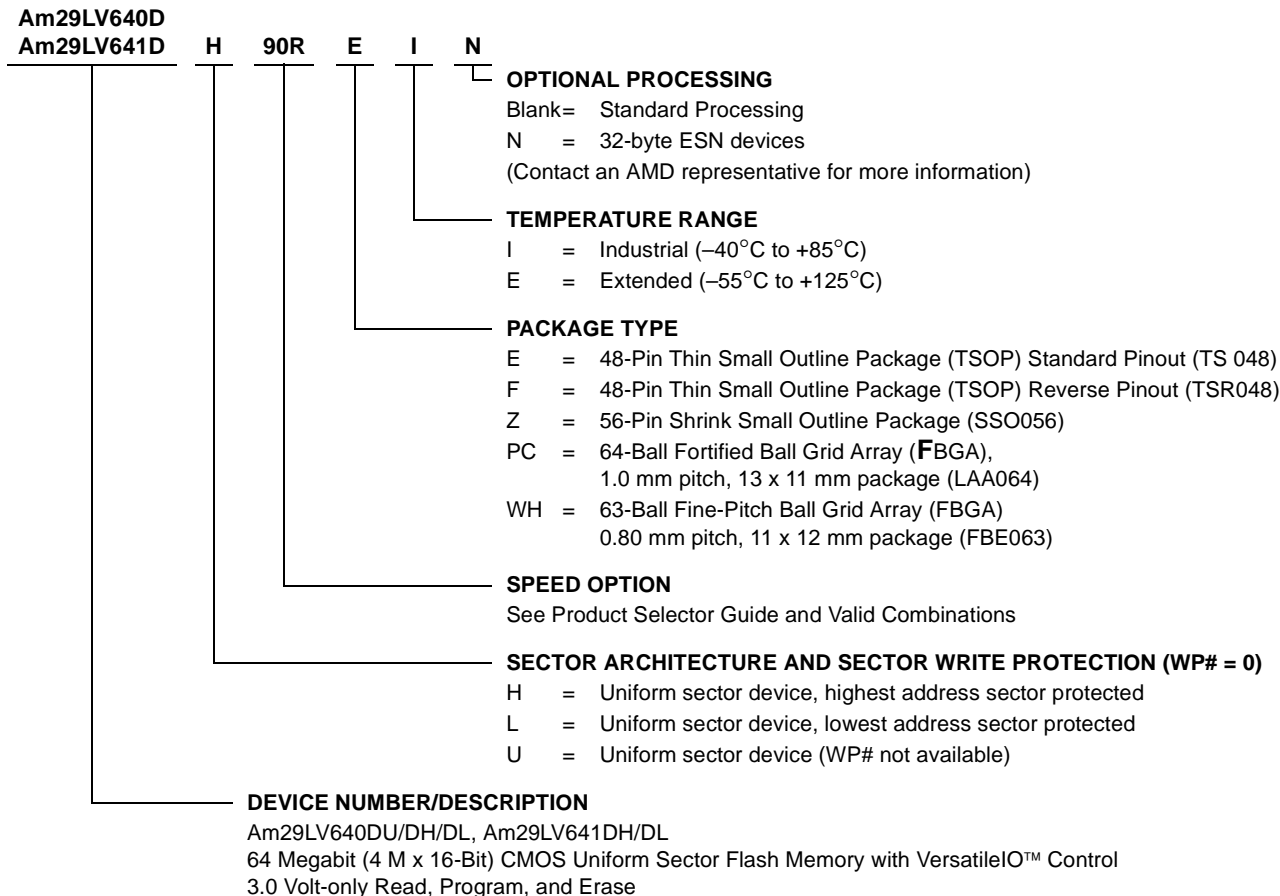


ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations for TSOP and SSOP Packages		Speed/V _{IO} Range
AM29LV640DH90R, AM29LV640DL90R	ZI	90ns, V _{IO} = 3.0 V – 5.0 V
AM29LV640DH101R, AM29LV640DL101R		100 ns, V _{IO} = 1.8 V – 2.9 V
AM29LV641DH90R, AM29LV641DL90R	EI, FI	90 ns V _{IO} = 3.0 V – 5.0 V
AM29LV641DH101R, AM29LV641DL101R		100 ns V _{IO} = 1.8 V – 2.9 V
AM29LV640DH120R, AM29LV640DL120R	ZI, ZE	120 ns, V _{IO} = 3.0 V – 5.0 V
AM29LV640DH121R, AM29LV640DL121R		120 ns, V _{IO} = 1.8 V – 2.9 V
AM29LV641DH120R, AM29LV641DL120R	EI, FI, EE, FE	120 ns, V _{IO} = 3.0 V – 5.0 V
AM29LV641DH121R, AM29LV641DL121R		120 ns V _{IO} = 1.8 V – 2.9 V
Note: LV640/641DH & DL have WP#, but no RY/BY#. U designator in base part number replaced by H or L.		

Valid Combinations for BGA Packages			Speed/ V _{IO} Range
Order Number	Package Marking		
AM29LV640DU90R	PCI	L640DU90N	I 90 ns, V _{IO} = 3.0 V – 5.0 V
	WHI	L640DU90R	
AM29LV640DU101R	PCI	L640DU01N	I 100 ns, V _{IO} = 1.8 V – 2.9 V
	WHI	L640DU01R	
AM29LV640DU120R	PCI, PCE	L640DU12N	I, E 120 ns, V _{IO} = 3.0 V – 5.0 V
	WHI, WHE	L640DU12R	
AM29LV640DU121R	PCI, PCE	L640DU21N	I, E 120 ns, V _{IO} = 1.8 V – 2.9 V
	WHI, WHE	L640DU21R	
Note: LV640DU has RY/BY#, but no WP#.			

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the

register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#	ACC	Addresses (Note 2)	DQ0– DQ15
Read	L	L	H	H	X	X	A _{IN}	D _{OUT}
Write (Program/Erase)	L	H	L	H	(Note 3)	X	A _{IN}	(Note 4)
Accelerated Program	L	H	L	H	(Note 3)	V _{HH}	A _{IN}	(Note 4)
Standby	V _{CC} ± 0.3 V	X	X	V _{CC} ± 0.3 V	X	H	X	High-Z
Output Disable	L	H	H	H	X	X	X	High-Z
Reset	X	X	X	L	X	X	X	High-Z
Sector Group Protect (Note 2)	L	H	L	V _{ID}	H	X	SA, A6 = L, A1 = H, A0 = L	(Note 4)
Sector Group Unprotect (Note 2)	L	H	L	V _{ID}	H	X	SA, A6 = H, A1 = H, A0 = L	(Note 4)
Temporary Sector Group Unprotect	X	X	X	V _{ID}	H	X	A _{IN}	(Note 4)

Legend: L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 8.5–12.5 V, V_{HH} = 11.5–12.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

- Addresses are A21:A0. Sector addresses are A21:A15.
- The sector protect and sector unprotect functions may also be implemented via programming equipment. See the “Sector Group Protection and Unprotection” section.
- If WP# = V_{IL}, the first or last sector remains protected. If WP# = V_{IH}, the first or last sector will be protected or unprotected as determined by the method described in “Sector Group Protection and Unprotection”. All sectors are unprotected when shipped from the factory (The SecSi Sector may be factory protected depending on version ordered.)
- D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 2).

VersatileIO™ (V_{IO}) Control

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on CE# and DQ I/Os to the same voltage level that is asserted on V_{IO}. V_{IO} is available in two configurations (1.8–2.9 V and 3.0–5.0 V) for operation in various system environments.

For example, a V_{IO} of 4.5–5.0 volts allows for I/O at the 5 volt level, driving and receiving signals to and from other 5 V devices on the same data bus.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid

data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See “Requirements for Reading Array Data” for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 13 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL} , and OE# to V_{IH} .

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The “Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address space that each sector occupies.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput during system production.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the ACC pin returns the device to normal operation. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autose-

lect Command Sequence sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH} .) If CE# and RESET# are held at V_{IH} , but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for $t_{ACC} + 30$ ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP} , the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3$ V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is com-

pleted within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH} .

Refer to the AC Characteristics tables for RESET# parameters and to Figure 14 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH} , output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Address Table

Sector	A21	A20	A19	A18	A17	A16	A15	16-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	000000–007FFF
SA1	0	0	0	0	0	0	1	008000–00FFFF
SA2	0	0	0	0	0	1	0	010000–017FFF
SA3	0	0	0	0	0	1	1	018000–01FFFF
SA4	0	0	0	0	1	0	0	020000–027FFF
SA5	0	0	0	0	1	0	1	028000–02FFFF
SA6	0	0	0	0	1	1	0	030000–037FFF
SA7	0	0	0	0	1	1	1	038000–03FFFF
SA8	0	0	0	1	0	0	0	040000–047FFF
SA9	0	0	0	1	0	0	1	048000–04FFFF
SA10	0	0	0	1	0	1	0	050000–057FFF
SA11	0	0	0	1	0	1	1	058000–05FFFF
SA12	0	0	0	1	1	0	0	060000–067FFF
SA13	0	0	0	1	1	0	1	068000–06FFFF
SA14	0	0	0	1	1	1	0	070000–077FFF
SA15	0	0	0	1	1	1	1	078000–07FFFF
SA16	0	0	1	0	0	0	0	080000–087FFF
SA17	0	0	1	0	0	0	1	088000–08FFFF
SA18	0	0	1	0	0	1	0	090000–097FFF
SA19	0	0	1	0	0	1	1	098000–09FFFF
SA20	0	0	1	0	1	0	0	0A0000–0A7FFF
SA21	0	0	1	0	1	0	1	0A8000–0AFFFF
SA22	0	0	1	0	1	1	0	0B0000–0B7FFF
SA23	0	0	1	0	1	1	1	0B8000–0BFFFF
SA24	0	0	1	1	0	0	0	0C0000–0C7FFF
SA25	0	0	1	1	0	0	1	0C8000–0CFFFF

Table 2. Sector Address Table (Continued)

Sector	A21	A20	A19	A18	A17	A16	A15	16-bit Address Range (in hexadecimal)
SA26	0	0	1	1	0	1	0	0D0000–0D7FFF
SA27	0	0	1	1	0	1	1	0D8000–0DFFFF
SA28	0	0	1	1	1	0	0	0E0000–0E7FFF
SA29	0	0	1	1	1	0	1	0E8000–0EFFFF
SA30	0	0	1	1	1	1	0	0F0000–0F7FFF
SA31	0	0	1	1	1	1	1	0F8000–0FFFFF
SA32	0	1	0	0	0	0	0	100000–107FFF
SA33	0	1	0	0	0	0	1	108000–10FFFF
SA34	0	1	0	0	0	1	0	110000–117FFF
SA35	0	1	0	0	0	1	1	118000–11FFFF
SA36	0	1	0	0	1	0	0	120000–127FFF
SA37	0	1	0	0	1	0	1	128000–12FFFF
SA38	0	1	0	0	1	1	0	130000–137FFF
SA39	0	1	0	0	1	1	1	138000–13FFFF
SA40	0	1	0	1	0	0	0	140000–147FFF
SA41	0	1	0	1	0	0	1	148000–14FFFF
SA42	0	1	0	1	0	1	0	150000–157FFF
SA43	0	1	0	1	0	1	1	158000–15FFFF
SA44	0	1	0	1	1	0	0	160000–167FFF
SA45	0	1	0	1	1	0	1	168000–16FFFF
SA46	0	1	0	1	1	1	0	170000–177FFF
SA47	0	1	0	1	1	1	1	178000–17FFFF
SA48	0	1	1	0	0	0	0	180000–187FFF
SA49	0	1	1	0	0	0	1	188000–18FFFF
SA50	0	1	1	0	0	1	0	190000–197FFF
SA51	0	1	1	0	0	1	1	198000–19FFFF
SA52	0	1	1	0	1	0	0	1A0000–1A7FFF
SA53	0	1	1	0	1	0	1	1A8000–1AFFFF
SA54	0	1	1	0	1	1	0	1B0000–1B7FFF
SA55	0	1	1	0	1	1	1	1B8000–1BFFFF
SA56	0	1	1	1	0	0	0	1C0000–1C7FFF
SA57	0	1	1	1	0	0	1	1C8000–1CFFFF
SA58	0	1	1	1	0	1	0	1D0000–1D7FFF
SA59	0	1	1	1	0	1	1	1D8000–1DFFFF
SA60	0	1	1	1	1	0	0	1E0000–1E7FFF