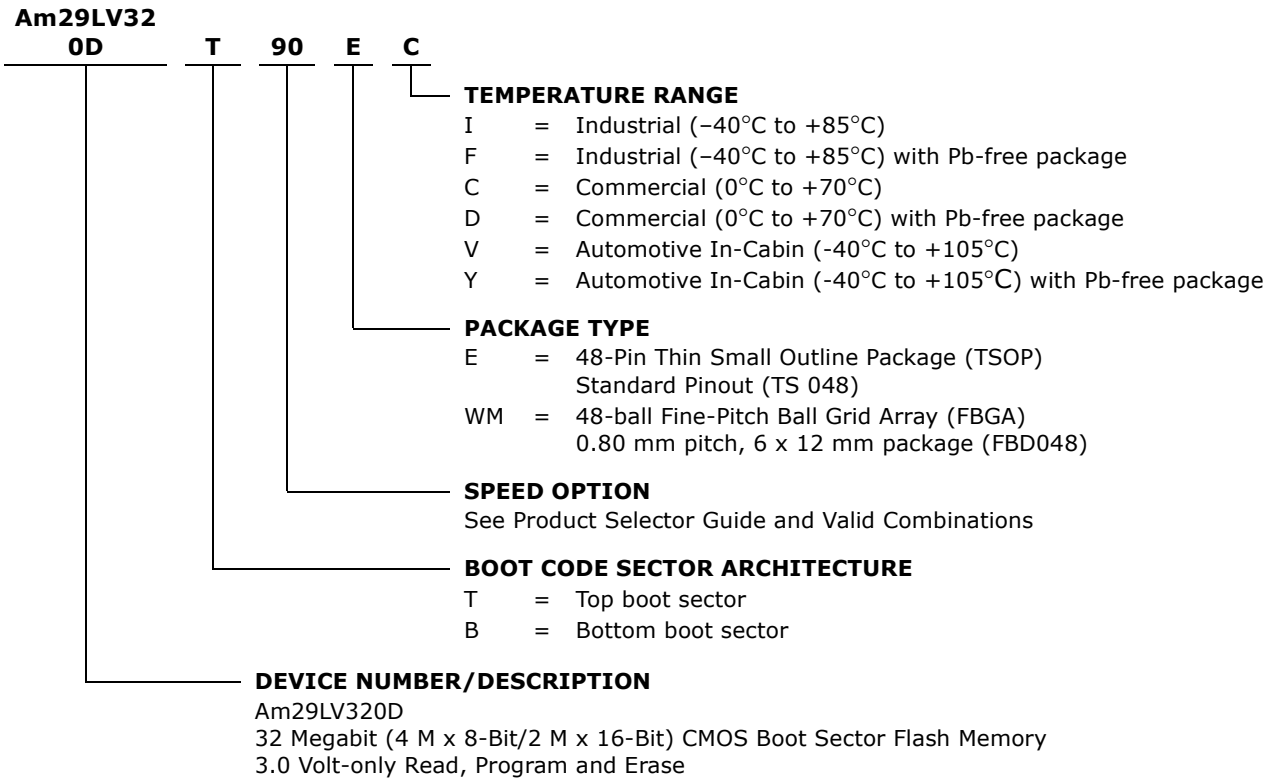
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations for TSOP Packages		Speed (Ns)	V_{CC} Range
AM29LV320DT90R, AM29LV320DB90R	EC, EI, ED, EF	90	3.0– 3.6V
Am29LV320DT90, Am29LV320DB90		90	2.7– 3.6V
AM29LV320DT120, AM29LV320DB120		120	2.7– 3.6V
Am29LV320DT120 Am29LV320DB120	EV, EY	120	2.7 – 3,6V

Valid Combinations for FBGA Packages			
Order Number		Package Marking	
AM29LV320DT90, AM29LV320DB90	WMC,WMI, WMD, WMF	L320DT90V, L320DB90V	C, I, D, F
AM29LV320DT120, AM29LV320DB120		L320DT12V, L320DB12V	
Am29LV320DT120 Am29LV320DB120	WNV	L320DT12V L320DB12V	V, Y

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29LV320D Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	Addresses (Note 2)	DQ0–DQ7	DQ8–DQ15	
								BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	(Note 3)	A_{IN}	(Note 4)	(Note 4)	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 4)	(Note 4)	
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	L/H	SA, A6 = L, A1 = H, A0 = L	(Note 4)	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	(Note 3)	SA, A6 = H, A1 = H, A0 = L	(Note 4)	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	(Note 3)	A_{IN}	(Note 4)	(Note 4)	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 11.5–12.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are A20:A0 in word mode (BYTE# = V_{IH}), A20:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See "Sector/Sector Block Protection and Unprotection" on page 17.*
3. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection" on page 17. If WP#/ACC = V_{HH}, all sectors are unprotected.*
4. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protection algorithm.*

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ0–DQ15 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Requirements for Reading Array Data" on page 11 for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 14, on page 38 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to "Word/Byte Configuration" on page 11 for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The "Word/Byte Configuration" on page 11 section contains details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2, on page 13 through Table 5, on page 16 indicate the address space that each sector occupies. A "sector address" is the address bits required to uniquely select a sector.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" on page 38 section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" on page 16 and "Autoselect Command Sequence" on page 25 sections for more information.

I_{CC6} and I_{CC7} in the DC Characteristics table represent the current specifications for read-while-program and read-while-erase, respectively.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3 V, the device is in the standby mode, but the standby current is greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the "DC Characteristics" on page 35 table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current is greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 15, on page 39 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Top Boot Sector Addresses (Am29LV320DT) (Sheet 1 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA0	000000xxx	64/32	000000h–00FFFFh	000000h–07FFFh
SA1	000001xxx	64/32	010000h–01FFFFh	008000h–0FFFFh
SA2	000010xxx	64/32	020000h–02FFFFh	010000h–17FFFh
SA3	000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh
SA4	000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh
SA5	000101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh
SA6	000110xxx	64/32	060000h–06FFFFh	030000h–037FFFh
SA7	000111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh
SA8	001000xxx	64/32	080000h–08FFFFh	040000h–047FFFh
SA9	001001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh
SA10	001010xxx	64/32	0A0000h–0AFFFFh	050000h–057FFFh
SA11	001011xxx	64/32	0B0000h–0BFFFFh	058000h–05FFFFh
SA12	001100xxx	64/32	0C0000h–0CFFFFh	060000h–067FFFh
SA13	001101xxx	64/32	0D0000h–0DFFFFh	068000h–06FFFFh
SA14	001110xxx	64/32	0E0000h–0EFFFFh	070000h–077FFFh
SA15	001111xxx	64/32	0F0000h–0FFFFFh	078000h–07FFFFh
SA16	010000xxx	64/32	100000h–10FFFFh	080000h–087FFFh
SA17	010001xxx	64/32	110000h–11FFFFh	088000h–08FFFFh
SA18	010010xxx	64/32	120000h–12FFFFh	090000h–097FFFh

Table 2. Top Boot Sector Addresses (Am29LV320DT) (Sheet 2 of 2)

Sector	Sector Address A20–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA19	010011xxx	64/32	130000h–13FFFFh	098000h–09FFFFh
SA20	010100xxx	64/32	140000h–14FFFFh	0A0000h–0A7FFFh
SA21	010101xxx	64/32	150000h–15FFFFh	0A8000h–0AFFFFh
SA22	010110xxx	64/32	160000h–16FFFFh	0B0000h–0B7FFFh
SA23	010111xxx	64/32	170000h–17FFFFh	0B8000h–0BFFFFh
SA24	011000xxx	64/32	180000h–18FFFFh	0C0000h–0C7FFFh
SA25	011001xxx	64/32	190000h–19FFFFh	0C8000h–0CFFFFh
SA26	011010xxx	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh
SA27	011011xxx	64/32	1B0000h–1BFFFFh	0D8000h–0DFFFFh
SA28	011100xxx	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh
SA29	011101xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh
SA30	011110xxx	64/32	1E0000h–1EFFFFh	0F0000h–0F7FFFh
SA31	011111xxx	64/32	1F0000h–1FFFFFh	0F8000h–0FFFFFh
SA32	100000xxx	64/32	200000h–20FFFFh	100000h–107FFFh
SA33	100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
SA34	100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
SA35	100011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
SA36	100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA37	100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA38	100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA39	100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA40	101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA41	101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA42	101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA43	101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA44	101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA45	101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA46	101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA47	101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA48	110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA49	110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA50	110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA51	110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA52	110100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA53	110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA54	110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA55	110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA56	111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA57	111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA58	111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA59	111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA60	111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA61	111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA62	111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA63	111111000	8/4	3F0000h–3F1FFFh	1F8000h–1F8FFFh
SA64	111111001	8/4	3F2000h–3F3FFFh	1F9000h–1F9FFFh
SA65	111111010	8/4	3F4000h–3F5FFFh	1FA000h–1FAFFFh
SA66	111111011	8/4	3F6000h–3F7FFFh	1FB000h–1FBFFFh
SA67	111111100	8/4	3F8000h–3F9FFFh	1FC000h–1FCFFFh
SA68	111111101	8/4	3FA000h–3FBFFFh	1FD000h–1FDFFFh
SA69	111111110	8/4	3FC000h–3FDFFFh	1FE000h–1FEFFFh
SA70	111111111	8/4	3FE000h–3FFFFFh	1FF000h–1FFFFFh

Note: *The address range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).*

Table 3. Top Boot SecSi™ Sector Addresses

Sector Address A20–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
111111xxx	64/32	3F0000h–3FFFFFh	1F8000h–1FFFFFh