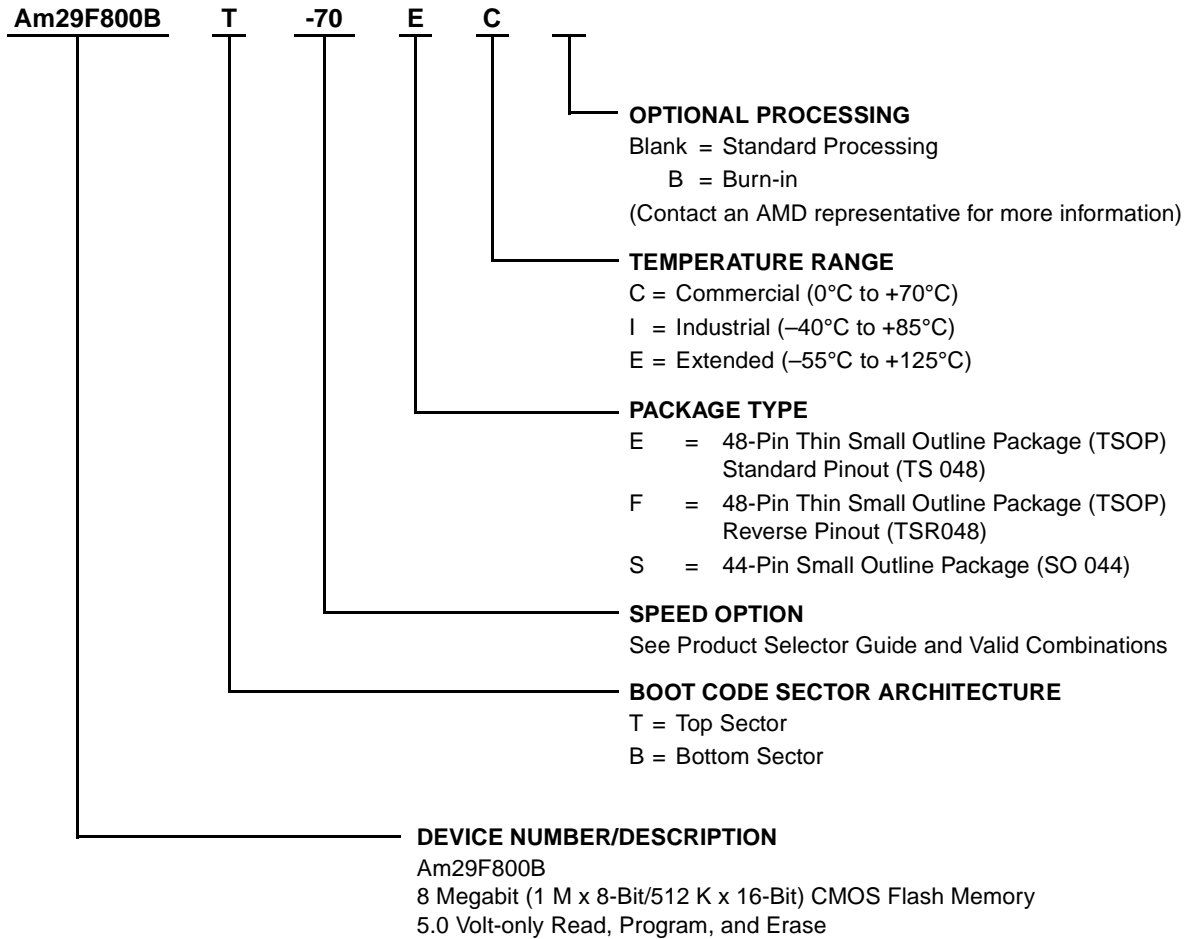


ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations	
Am29F800BT-55, Am29F800BB-55	EC, EI, FC, FI, SC, SI
Am29F800BT-70, Am29F800BB-70	EC, EI, EE, FC, FI, FE, SC, SI, SE
Am29F800BT-90, Am29F800BB-90	
Am29F800BT-120, Am29F800BB-120	
Am29F800BT-150, Am29F800BB-150	

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of

the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29F800B Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	A0–A18	DQ0–DQ7	DQ8–DQ15	
							BYTE# = V _{IH}	BYTE# = V _{IL}
Read	L	L	H	H	A _{IN}	D _{OUT}	D _{OUT}	High-Z
Write	L	H	L	H	A _{IN}	D _{IN}	D _{IN}	High-Z
CMOS Standby	V _{CC} ± 0.5 V	X	X	V _{CC} ± 0.5 V	X	High-Z	High-Z	High-Z
TTL Standby	H	X	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Hardware Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Temporary Sector Unprotect (See Note)	X	X	X	V _{ID}	A _{IN}	D _{IN}	D _{IN}	X

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out, A_{IN} = Address In

Note: See the sections on Sector Protection and Temporary Sector Unprotect for more information.

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that as-

sert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. See the "Command Definitions" section for details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the “Autoselect Mode” and “Autoselect Command Sequence” sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The “AC Characteristics” section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to “Write Operation Status” for more information, and to each AC Characteristics section for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when CE# and RESET# pins are both held at $V_{CC} \pm 0.5$ V. (Note that this is a more restricted voltage range than V_{IH} .) The device enters the TTL standby mode when CE# and RESET# pins are both held at V_{IH} . The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

The device also enters the standby mode when the RESET# pin is driven low. Refer to the next section, “RESET#: Hardware Reset Pin”.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In the DC Characteristics tables, I_{CC3} represents the standby current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin low for at least a period of t_{RP} the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{IL} , the device enters the TTL standby mode; if RESET# is held at $V_{SS} \pm 0.5$ V, the device enters the CMOS standby mode.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH} .

Refer to the AC Characteristics tables for RESET# parameters and timing diagram.

Output Disable Mode

When the OE# input is at V_{IH} , output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Am29F800BT Top Boot Block Sector Address Table

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
									(x16) Address Range	(x8) Address Range
SA0	0	0	0	0	X	X	X	64/32	00000h–07FFFh	00000h–0FFFFh
SA1	0	0	0	1	X	X	X	64/32	08000h–0FFFFh	10000h–1FFFFh
SA2	0	0	1	0	X	X	X	64/32	10000h–17FFFh	20000h–2FFFFh
SA3	0	0	1	1	X	X	X	64/32	18000h–1FFFFh	30000h–3FFFFh
SA4	0	1	0	0	X	X	X	64/32	20000h–27FFFh	40000h–4FFFFh
SA5	0	1	0	1	X	X	X	64/32	28000h–2FFFFh	50000h–5FFFFh
SA6	0	1	1	0	X	X	X	64/32	30000h–37FFFh	60000h–6FFFFh
SA7	0	1	1	1	X	X	X	64/32	38000h–3FFFFh	70000h–7FFFFh
SA8	1	0	0	0	X	X	X	64/32	40000h–47FFFh	80000h–8FFFFh
SA9	1	0	0	1	X	X	X	64/32	48000h–4FFFFh	90000h–9FFFFh
SA10	1	0	1	0	X	X	X	64/32	50000h–57FFFh	A0000h–AFFFFh
SA11	1	0	1	1	X	X	X	64/32	58000h–5FFFFh	B0000h–BFFFFh
SA12	1	1	0	0	X	X	X	64/32	60000h–67FFFh	C0000h–CFFFFh
SA13	1	1	0	1	X	X	X	64/32	68000h–6FFFFh	D0000h–DFFFFh
SA14	1	1	1	0	X	X	X	64/32	70000h–77FFFh	E0000h–EFFFFh
SA15	1	1	1	1	0	X	X	32/16	78000h–7BFFFh	F0000h–F7FFFh
SA16	1	1	1	1	1	0	0	8/4	7C000h–7CFFFh	F8000h–F9FFFh
SA17	1	1	1	1	1	0	1	8/4	7D000h–7DFFFh	FA000h–FBFFFh
SA18	1	1	1	1	1	1	X	16/8	7E000h–7FFFFh	FC000h–FFFFFh

Note:

Address range is A18:A-1 in byte mode and A18:A0 in word mode. See "Word/Byte Configuration" section for more information.