

AFE5816, AFE58JD16 16-Channel, Ultrasound, AFE with 90-mW/Channel Power, 0.95-nV/ $\sqrt{\text{Hz}}$ Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC and Passive CW Mixer

1 Features

- 16-Channel, Complete AFE:
 - Input Attenuator, LNA, LPF, ADC, and CW Mixer
 - Digital Time Gain Compensation (DTGC)
 - Gain Range: 6 dB to 45 dB
 - Linear Input Range: 1 V_{PP}
- Input Attenuator with DTGC:
 - 8-dB to 0-dB Attenuation with 0.125-dB Step
 - Supports Different Source Resistances:
 - 50 Ω to 800 Ω
- Low-Noise Amplifier (LNA) with DTGC:
 - 14-dB to 45-dB Gain with 0.125-dB Step
 - Low Input Current Noise: 1.2 pA/ $\sqrt{\text{Hz}}$
- 3rd-Order, Linear-Phase, Low-Pass Filter (LPF):
 - 10 MHz, 15 MHz, 20 MHz, and 25 MHz
- Analog-to-Digital Converter (ADC):
 - 14-Bit ADC: 75-dBFS SNR at 65 MSPS
 - 12-Bit ADC: 72-dBFS SNR at 80 MSPS
 - LVDS Interface Maximum Speed of 1 GBPS
- Noise and Power Optimizations (Full-Channel):
 - 90 mW/Ch at 0.95 nV/ $\sqrt{\text{Hz}}$, 65 MSPS
 - 55 mW/Ch at 1.3 nV/ $\sqrt{\text{Hz}}$, 40 MSPS
 - 59 mW/Ch at CW Mode
- Excellent Device-to-Device Gain Matching:
 - ± 0.5 dB (Typical) and ± 1 dB (Max)
- Low Harmonic Distortion
- Fast and Consistent Overload Recovery
- Passive Mixer for CWD:
 - Low Close-In Phase Noise:
 - 148 dBc/Hz at 1 kHz Off 2.5-MHz Carrier

- Phase Resolution: 1 / 16 λ
- Supports 16X, 8X, 4X, and 1X CW Clocks
- 12-dB Suppression on 3rd and 5th Harmonics
- Data Processing and Packing in the AFE58JD16
 - Digital I/Q Demodulator after ADC
 - Fractional Decimation Filter M = 1 to 63 with 0.25X Increment Step
 - RF Data Rate Reduction after Decimation
 - On-Chip RAM with 32 Preset Profiles
 - JESD204B Subclass 0, 1, and 2 Interfaces
 - Maximum Speed of 5 GBPS
 - 2, 4, and 8 Channels per Lane
- Small Package: 15-mm x 15-mm NFBGA-289

2 Applications

- Medical Ultrasound Imaging
- Nondestructive Evaluation Equipment
- Sonar Imaging Equipment
- Multichannel, High-Speed Data Acquisition

3 Description

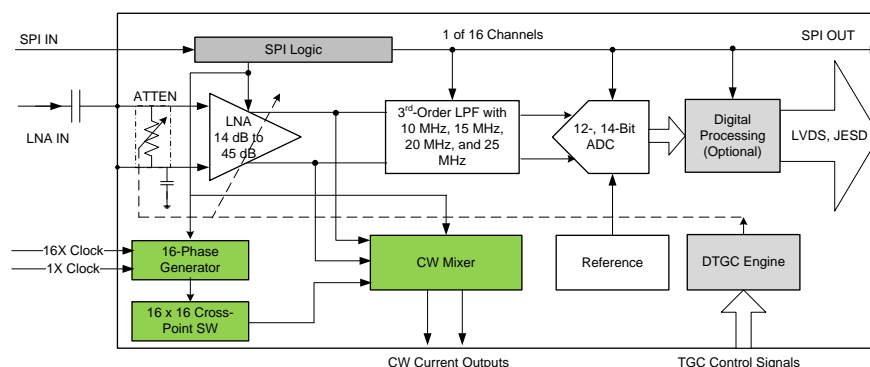
The AFE5816 and AFE58JD16 are highly-integrated, analog front-end (AFE) solutions specifically designed for ultrasound systems where high performance, low power, and small size are required.

Device Information⁽¹⁾

PART NUMBER	OUTPUT INTERFACE	DIGITAL I/Q DEMODULATOR
AFE5816	LVDS only	Not supported
AFE58JD16	LVDS and JESD	Supported

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Block Diagram



4 Description (continued)

The AFE5816 family has a total of 16 channels, with each channel consisting of a voltage-controlled amplifier (VCA) channel, a simultaneous-sampling 14-bit and 12-bit analog-to-digital converter (ADC), and a continuous-wave (CW) mixer. The VCA includes an attenuator (ATTEN), a variable-gain, low-noise amplifier (LNA), and a third-order, low-pass filter (LPF). The attenuator supports an attenuation range of 8 dB to 0 dB and the LNA supports gain ranges from 14 dB to 45 dB. The LPF cutoff frequency can be configured at 10 MHz, 15 MHz, 20 MHz, or 25 MHz to support ultrasound applications with different frequencies.

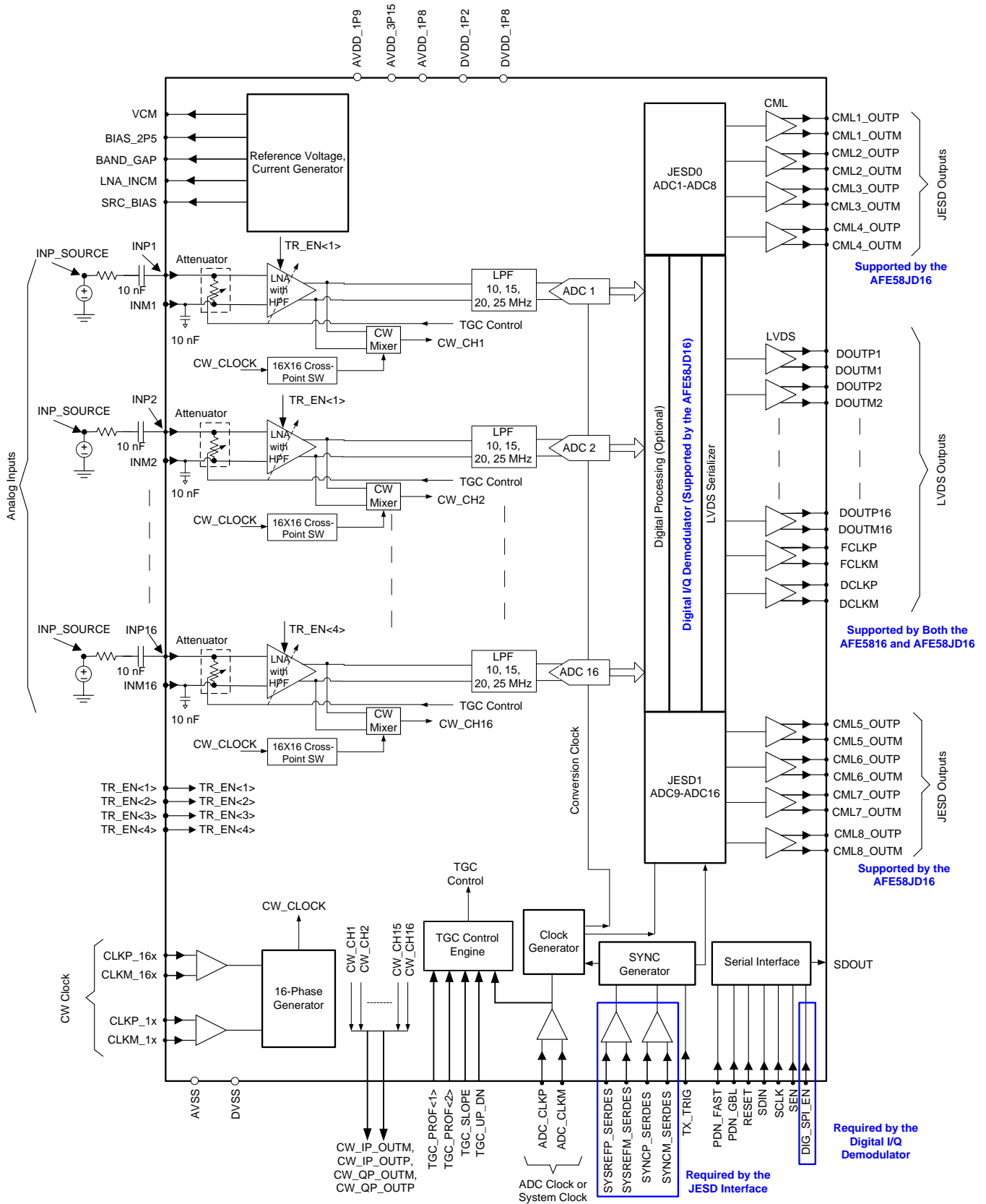
The AFE5816 family integrates a low-power passive mixer to create an on-chip CWD beamformer. 16 selectable phase delays can be applied to each analog input signal. Furthermore, a unique third- and fifth-order harmonic suppression filter is implemented to enhance CW sensitivity.

The high-performance, 14-bit ADC achieves 75-dBFS SNR. This ADC ensures excellent signal-to-noise ratio (SNR) at low-channel gain. The devices can operate at maximum speeds of 65 MSPS and 80 MSPS, providing a 14-bit and a 12-bit output, respectively. The ADC is designed to scale its power with sampling rate. Up to 1-GBPS low-voltage differential signaling (LVDS) outputs can easily interface with low-cost field-programmable gate arrays (FPGAs).

The AFE58JD16 includes an optional digital demodulator and JESD204B data packing blocks after the 12- or 14-bit ADC. The digital in-phase and quadrature (I/Q) demodulator with programmable fractional decimation filters accelerates computationally-intensive algorithms at low power. Up to a 5-GBPS JESD204B interface further reduces the circuit board routing challenges in high-channel count systems.

The AFE5816 and AFE58JD16 also allow various power and noise combinations to be selected for optimizing system performance. Therefore, these devices are suitable ultrasound AFE solutions for systems with strict battery life requirements. Both the AFE58JD16 and AFE5816 are available in a 15-mm × 15-mm NFBGA-289 package (ZAV package, S-PBGA-N289) and are specified for operation from –40°C to 85°C. The devices are also pin-to-pin compatible with the [AFE5818](#) family.

5 Functional Block Diagram



PRODUCT PREVIEW

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

AFE5818 Data Sheet, [SBAS687](#)

ADS8413 Data Sheet, [SLAS490](#)

ADS8472 Data Sheet, [SLAS514](#)

CDCE72010 Data Sheet, [SCAS858](#)

CDCM7005 Data Sheet, [SCAS793](#)

ISO7240 Data Sheet, [SLLS868](#)

LMK04803 Data Sheet, [SNAS489](#)

OPA1632 Data Sheet, [SBOS286](#)

OPA2211 Data Sheet, [SBOS377](#)

SN74AUP1T04 Data Sheet, [SCES800](#)

THS4130 Data Sheet, [SLOS318](#)

MicroStar BGA Packaging Reference Guide, [SSYZ015](#)

[WEBENCH® Filter Designer](#)

6.2 Trademarks

All trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE5816ZAV	PREVIEW	NFBGA	ZAV	289	126	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE5816	
AFE58JD16ZAV	PREVIEW			289		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

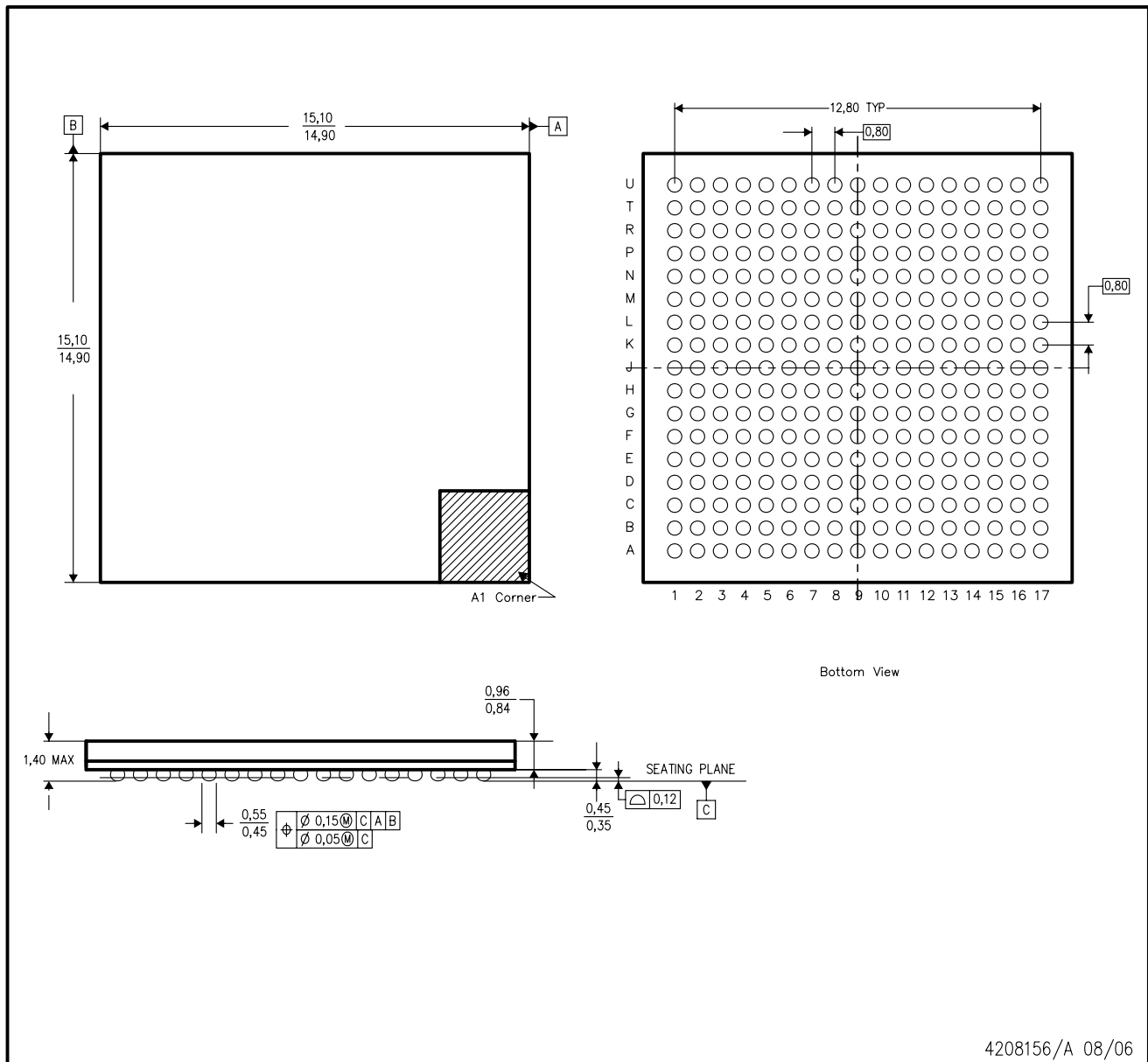
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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ZAV (S-PBGA-N289)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. This is a lead-free solder ball design.

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