ADS54J60 Dual-Channel, 16-Bit, 1.0-GSPS Analog-to-Digital Converter

1 Features

- 16-Bit Resolution, Dual-Chanel, 1-GSPS ADC
- Noise Floor: –159 dBFS/Hz
- Spectral Performance (f_{IN} = 170 MHz at –1 dBFS):
  - SNR: 70 dBFS
  - NSD: –157 dBFS/Hz
  - SFDR: 86 dBc
  - SFDR: 96 dBc (Except HD2, HD3, and Interleaving Tones)
- Spectral Performance (f_{IN} = 350 MHz at –1 dBFS):
  - SNR: 67.5 dBFS
  - NSD: –154.5 dBFS/Hz
  - SFDR: 75 dBc
  - SFDR: 85 dBc (Except HD2, HD3, and Interleaving Tones)
- Channel Isolation: 100 dBc at f_{IN} = 170 MHz
- Input Full-Scale: 1.9 V_{PP}
- Input Bandwidth (3 dB): 700 MHz
- On-Chip Dither
- Integrated Wideband DDC Block
- JESD204B Interface with Subclass 1 Support:
  - 2 Lanes per ADC at 10.0 Gbps
  - 4 Lanes per ADC at 5.0 Gbps
  - Support for Multi-Chip Synchronization
- Power Dissipation: 1.35 W/ch at 1 GSPS
- VQFNP-72 Package (10 mm × 10 mm)

2 Applications

- Radar and Antenna Arrays
- Broadband Wireless
- Cable Infrastructure
- Communications Test Equipment
- Microwave Receivers

3 Description

The ADS54J60 is a low-power, wide-bandwidth, 16-bit, 1.0-GSPS, dual-channel, analog-to-digital converter (ADC). Designed for high signal-to-noise ratio (SNR), the device delivers a noise floor of –159 dBFS/Hz for applications aiming for highest dynamic range over a wide instantaneous bandwidth. The device supports the JESD204B serial interface with data rates up to 10.0 Gbps, supporting two or four lanes per ADC. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. Each ADC channel optionally can be connected to a wideband digital down-converter (DDC) block. The ADS54J60 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with very low power consumption.

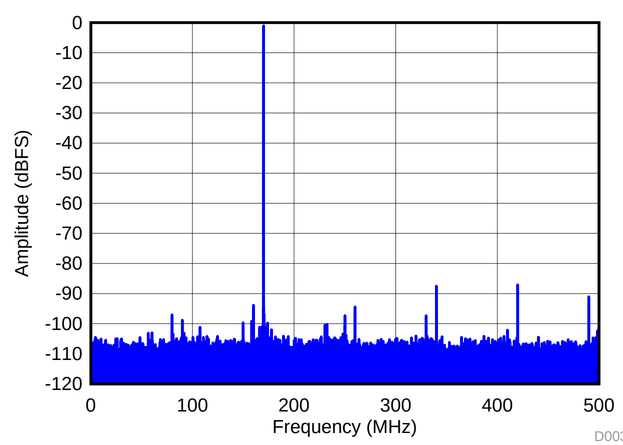
The JESD204B interface reduces the number of interface lines, allowing high system integration density. An internal phase-locked loop (PLL) multiplies the ADC sampling clock to derive the bit clock that is used to serialize the 16-bit data from each channel.

Device Comparison

PART NUMBER	SPEED GRADE (MSPS)	RESOLUTION (Bits)
ADS54J40	1000	14
ADS54J60	1000	16
ADS54J69	500	16

(1) For all available packages, see the orderable addendum at the end of the data sheet.

FFT for 170 MHz Input Signal (SNR = 70 dBFS; SFDR = 86 dBc; IL Spur = 87 dBc; Non HD2, HD3 Spur = 96 dBc)



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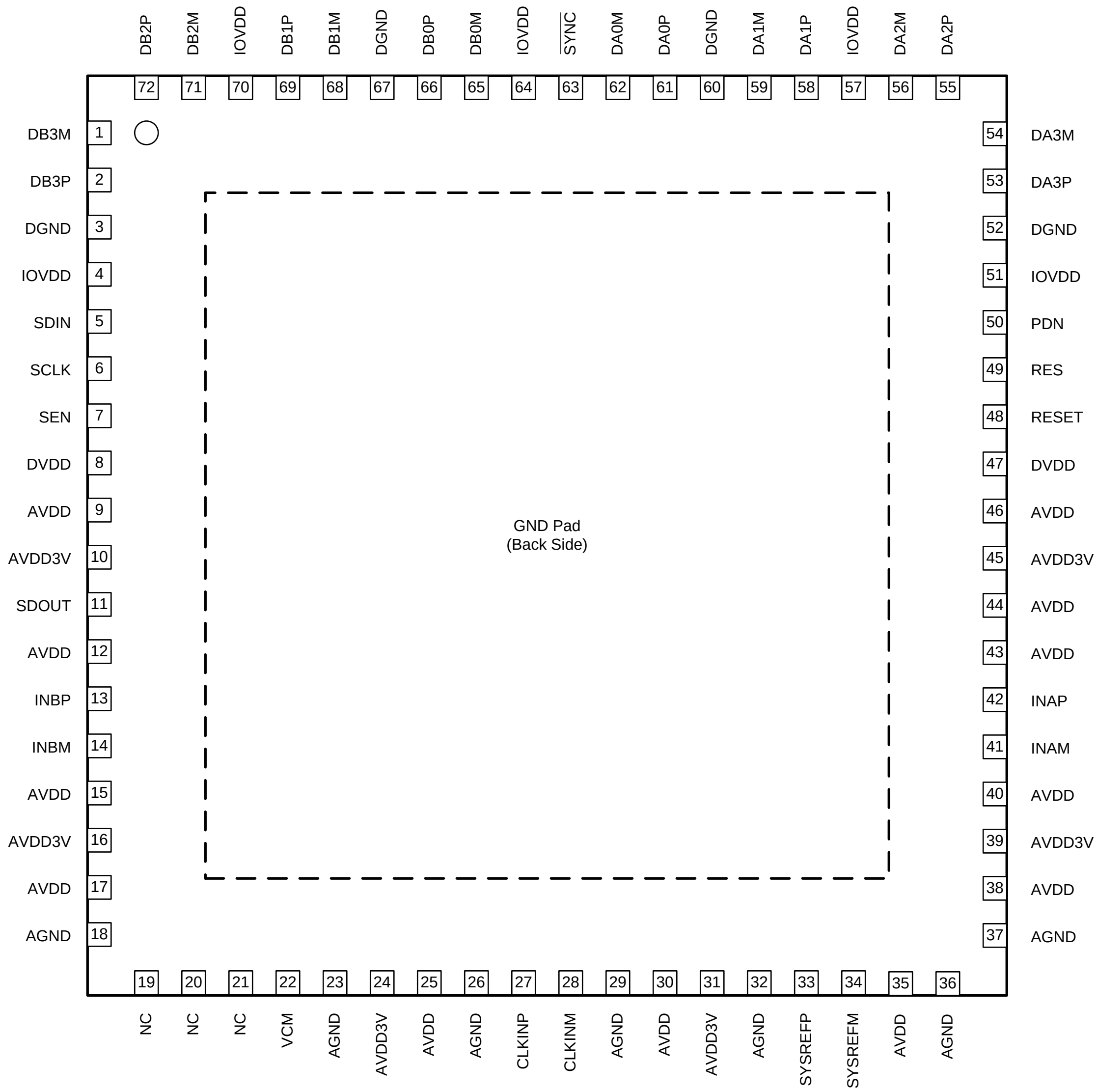
4 Revision History

DATE	REVISION	NOTES
April 2015	*	Initial release.

5 Pin Configuration and Functions

RMP Package
VQFNP-72
Top View



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Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLOCK, SYSREF			
CLKINM	28	I	Negative differential clock input for the ADC
CLKINP	27	I	Positive differential clock input for the ADC
NC	19-21	—	Unused pins, do not connect
SYSREFM	34	I	Negative external SYSREF input
SYSREFP	33	I	Positive external SYSREF input
CONTROL, SERIAL			
PDN	50	I/O	Power down. Can be configured via an SPI register setting. Can be configured to fast overrange output for channel A via the SPI.
RESET	48	I	Hardware reset; active high. This pin has an internal 150-kΩ pull-down resistor.
SCLK	6	I	Serial interface clock input
SDIN	5	I	Serial interface data input
SDOUT	11	O	Serial interface data output. Can be configured to fast overrange output for channel B via the SPI.
SEN	7	I	Serial interface enable
DATA INTERFACE			
DA0M	62	O	JESD204B serial data negative outputs for channel A
DA1M	59		
DA2M	56		
DA3M	54		
DA0P	61	O	JESD204B serial data positive outputs for channel A
DA1P	58		
DA2P	55		
DA3P	53		
DB0M	65	O	JESD204B serial data negative outputs for channel B
DB1M	68		
DB2M	71		
DB3M	1		
DB0P	66	O	JESD204B serial data positive outputs for channel B
DB1P	69		
DB2P	72		
DB3P	2		
$\overline{\text{SYNC}}$	63	I	Synchronization input for JESD204B port
INPUT, REFERENCE			
INAM	41	I	Differential analog negative input for channel A
INAP	42	I	Differential analog positive input for channel A
INBM	14	I	Differential analog negative input for channel B
INBP	13	I	Differential analog positive input for channel B
VCM	22	O	Common-mode voltage for analog inputs, 2.1 V
POWER SUPPLY			
AGND	18, 23, 26, 29, 32, 36, 37	I	Analog ground
AVDD	9, 12, 15, 17, 25, 30, 35, 38, 40, 43, 44, 46	I	Analog 1.9-V power supply
AVDD3V	10, 16, 24, 31, 39, 45	I	Analog 3.0-V power supply for the analog buffer
DGND	3, 52, 60, 67	I	Digital ground
DVDD	8, 47	I	Digital 1.9-V power supply
IOVDD	4, 51, 57, 64, 70	I	Digital 1.15-V power supply for the JESD204B transmitter
RES	49	I	Reserved pin. Connect to DGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range:	AVDD3V	–0.3	3.6	V
	AVDD	–0.3	2.1	V
	DVDD	–0.3	2.1	V
	IOVDD	–0.2	1.4	V
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins:	INAP, INBP, INAM, INBM	–0.3	AVDD3V + 0.4	V
	CLKINP, CLKINM	–0.3	AVDD + 0.3	V
	SYSREFP, SYSREFM	–0.3	AVDD + 0.3	V
	SCLK, SEN, SDIN, RESET, $\overline{SYNC}$, PDN	–0.2	2.1	V
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage range:		AVDD3V	2.85	3.0	3.6	V
		AVDD	1.8	1.9	2.0	V
		DVDD	1.7	1.9	2.0	V
		IOVDD	1.1	1.15	1.2	V
Analog inputs:	Differential input voltage range			1.9		V_{PP}
	Input common-mode voltage			VCM ± 0.025		V
Clock inputs:	Input clock frequency, device clock frequency		TBD		1000	MHz
	Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.75	1.5		V_{PP}
		LVPECL, ac-coupled	0.8	1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
	Input device clock duty cycle, default after reset		TBD	50%	TBD	
Temperature:		Operating free-air, T_A	–40		85	ºC
		Operating junction, T_J		105(3)	125	ºC

(1) SYSREF needs to be applied for the device bring up. See SYSREF Signal for details.
(2) After power-up, always use hardware RESET to reset the device for 1st time. See Table 62 for details.
(3) Prolonged use above this junction temperature can increase the device failure-in-time (FIT) rate.

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6.4 Thermal Information

THERMAL METRIC[1]		RMP (VQFNP) 72 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	22.3	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	5.1	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	2.4	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	0.1	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	2.3	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ADC sampling rate				1000	MSPS
	Resolution		16			Bits
POWER SUPPLIES						
AVDD3V	3.0-V analog supply		2.85	3.0	3.6	V
AVDD	1.9-V analog supply		1.8	1.9	2.0	V
DVDD	1.9-V digital supply		1.7	1.9	2.0	V
IOVDD	1.15-V SERDES supply		1.1	1.15	1.2	V
I_{AVDD3V}	3.0-V analog supply current	V_{IN} = full-scale on both channels		334		mA
I_{AVDD}	1.9-V analog supply current	V_{IN} = full-scale on both channels		359		mA
I_{DVDD}	1.9-V digital supply current	Four lanes per ADC (20x PLL)		197		mA
I_{IOVDD}	1.15-V SERDES supply current	Four lanes per ADC (20x PLL)		566		mA
P_{dis}	Total power dissipation	Four lanes per ADC (20x PLL)		2.71		W
I_{DVDD}	1.9-V digital supply current	Two lanes per ADC (40x PLL)		211		mA
I_{IOVDD}	1.15-V SERDES supply current	Two lanes per ADC (40x PLL)		618		mA
P_{dis}	Total power dissipation	Two lanes per ADC (40x PLL)		2.80		W
I_{DVDD}	1.9-V digital supply current	Four lanes per ADC (20x PLL), 2X decimation		197		mA
I_{IOVDD}	1.15-V SERDES supply current	Four lanes per ADC (20x PLL), 2X decimation		593		mA
P_{dis}	Total power dissipation			2.74		W
I_{DVDD}	1.9-V digital supply current	Four lanes per ADC (20x PLL), 4X decimation		176		mA
I_{IOVDD}	1.15-V SERDES supply current	Four lanes per ADC (20x PLL), 4X decimation		562		mA
P_{dis}	Total power dissipation			2.66		W
	Global power-down power dissipation			139		mW
	Standby power dissipation	PDN ADC channels A and B = 1, PDN channels A and B = 1		997		mW

Electrical Characteristics (continued)

Typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS (INAP, INAM, INBP, INBM)						
	Differential input full-scale voltage			1.9		V_{PP}
V_{IC}	Common-mode input voltage			VCM ± 0.025		V
R_{IN}	Differential input resistance	At 170 MHz input frequency		0.6		kΩ
C_{IN}	Differential input capacitance	At 170 MHz input frequency		4.7		pF
$V_{OC(VCM)}$	VCM common-mode output voltage			2.1	2.35	V
	Analog input bandwidth (3 dB)	50-Ω source driving ADC inputs terminated with 50-Ω		700		MHz
t_{or}	Overload recovery time	Recovery time from 3-dB overloaded condition, within an accuracy of 1% of full-scale.		TBD		Clock cycles
CLOCK INPUT (CLKINP, CLKINM)						
	Internal clock biasing	CLKINP and CLKINM are connected to internal biasing voltage through 400-Ω	TBD	1.15	TBD	V
DC ACCURACY						
E_O	Offset error			TBD		mV
α_{EO}	Temperature coefficient of offset error			TBD		µV/°C
E_G	Gain error			TBD		%FS
α_{EG}	Temperature coefficient of gain error			TBD		Δ%FS/°C

6.6 AC Characteristics

Typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		71.1		dBFS
		f_{IN} = 100 MHz		71		
		f_{IN} = 170 MHz	TBD	70		
		f_{IN} = 270 MHz		69		
		f_{IN} = 350 MHz		67.5		
	Small-signal SNR	A_{IN} = –40 dBFS		72		
NSD	Noise spectral density	f_{IN} = 10 MHz		–158.1		dBFS/Hz
		f_{IN} = 100 MHz		–158		
		f_{IN} = 170 MHz	TBD	–157		
		f_{IN} = 270 MHz		–156		
		f_{IN} = 350 MHz		–154.5		
	Small-signal NSD	A_{IN} = –40 dBFS		–159.0		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		70.8		dBFS
		f_{IN} = 100 MHz		70.5		
		f_{IN} = 170 MHz	TBD	69.7		
		f_{IN} = 270 MHz		68.4		
		f_{IN} = 350 MHz		67		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.6		Bits
		f_{IN} = 100 MHz		11.5		
		f_{IN} = 170 MHz	TBD	11.4		
		f_{IN} = 270 MHz		11.2		
		f_{IN} = 350 MHz		10.8		

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AC Characteristics (continued)

Typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion		f_{IN} = 10 MHz		82		dBc
			f_{IN} = 100 MHz		79		
			f_{IN} = 170 MHz	TBD	81		
			f_{IN} = 270 MHz		76		
			f_{IN} = 350 MHz		73		
SFDR	Spurious-free dynamic range		f_{IN} = 10 MHz		87		dBc
			f_{IN} = 100 MHz		83		
			f_{IN} = 170 MHz	TBD	86		
			f_{IN} = 270 MHz		80		
			f_{IN} = 350 MHz		75		
HD2, HD3	Second- and third-order harmonic distortion		f_{IN} = 10 MHz		88		dBc
			f_{IN} = 100 MHz		83		
			f_{IN} = 170 MHz	TBD	86		
			f_{IN} = 270 MHz		80		
			f_{IN} = 350 MHz		75		
	Interleaving spur		f_{IN} = 10 MHz		87		dBc
			f_{IN} = 100 MHz		87		
			f_{IN} = 170 MHz	TBD	87		
			f_{IN} = 270 MHz		83		
			f_{IN} = 350 MHz		78		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3, and interleaving spur)		f_{IN} = 10 MHz		93		dBc
			f_{IN} = 100 MHz		95		
			f_{IN} = 170 MHz	TBD	96		
			f_{IN} = 270 MHz		87		
			f_{IN} = 350 MHz		85		
IMD3	Two-tone, third-order intermodulation distortion		f_1 = 185 MHz, f_2 = 190 MHz, A_{IN} = –7 dBFS		86		dBFS
			f_1 = 185 MHz, f_2 = 190 MHz, A_{IN} = –10 dBFS		92		
	Crosstalk isolation between channels A and B	Full-scale signal input on aggressor channel, idle channel input on victim channel	f_{IN} = 10 MHz		110		dBc
			f_{IN} = 100 MHz		110		
			f_{IN} = 170 MHz		106		
			f_{IN} = 270 MHz		100		
			f_{IN} = 350 MHz		95		

6.7 Digital Characteristics

Typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (RESET, SCLK, SEN, SDIN, $\overline{SYNC}$, PDN)(1)						
V_{IH}	High-level input voltage	All digital inputs support 1.2-V and 1.8-V logic levels	0.8			V
V_{IL}	Low-level input voltage	All digital inputs support 1.2-V and 1.8-V logic levels			0.4	V
I_{IH}	High-level input current	SEN		0		µA
		RESET, SCLK, SDIN, PDN, $\overline{SYNC}$		50		µA
I_{IL}	Low-level input current	SEN		50		µA
		RESET, SCLK, SDIN, PDN, $\overline{SYNC}$		0		µA
DIGITAL INPUTS (SYSREFP, SYSREFM)						
V_D	Differential Input Voltage		0.35	0.45	1.4	V
$V_{(CM\_DIG)}$	Common-mode voltage for SYSREF			1.3		V
DIGITAL OUTPUTS (SDOUT, PDN(2))						
V_{OH}	High-level output voltage		DVDD – 0.1	DVDD		V
V_{OL}	Low-level output voltage				0.1	V
DIGITAL OUTPUTS (JESD204B Interface: DxP, DxM)(3)						
V_{OD}	Output differential voltage	With default swing setting.	TBD	700	TBD	mV_{PP}
V_{OC}	Output common-mode voltage			450		mV
	Transmitter short-circuit current	Transmitter pins shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
z_{os}	Single-ended output impedance			50		Ω
	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) RESET, SCLK, SDATA, and PDN pins have 150-kΩ (typical) internal pull-down resistor to ground, while SEN pin has 150-kΩ (typical) pull-up resistor to IOVDD.
(2) When functioning as OVR pin for channel B.
(3) 50-Ω, single-ended external termination to IOVDD.

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6.8 Timing Characteristics

Typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input, unless otherwise noted.

		MIN	TYP	MAX	UNITS
SAMPLE TIMING CHARACTERISTICS					
	Aperture delay	0.75		1.6	ns
	Aperture delay matching between two channels on the same device		± 70		ps
	Aperture delay matching between two devices at the same temperature and supply voltage		± 270		ps
	Aperture jitter		130		f_S rms
	Wake-up time to valid data after coming out of STANDBY mode		TBD	TBD	µs
	Wake-up time to valid data after coming out of global power-down		TBD	TBD	µs
t_{SU_SYSREF}	Setup time for SYSREF, referenced to input clock rising edge	300		900	ps
t_{H_SYSREF}	Hold time for SYSREF, referenced to input clock rising edge	100			ps
JESD OUTPUT INTERFACE TIMING CHARACTERISTICS					
	Unit interval	100		400	ps
	Serial output data rate	2.5		10	Gbps
	Total jitter for BER of 1E-15 and lane rate = 10 Gbps		26		ps
	Random jitter for BER of 1E-15 and lane rate = 10 Gbps		0.75		fs-rms
	Deterministic jitter for BER of 1E-15 and lane rate = 10 Gbps		12		ps, pk-pk
t_R, t_F	Data rise time, data fall time: rise and fall times measured from 20% to 80%, differential output waveform, 2.5 Gbps ≤ bit rate ≤ 10 Gbps		60		ps

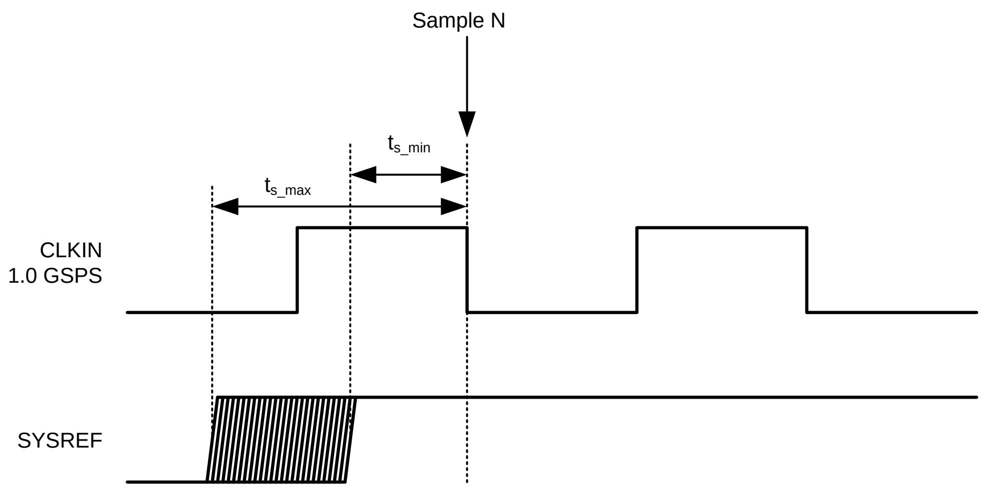

Figure 1. SYSREF Timing

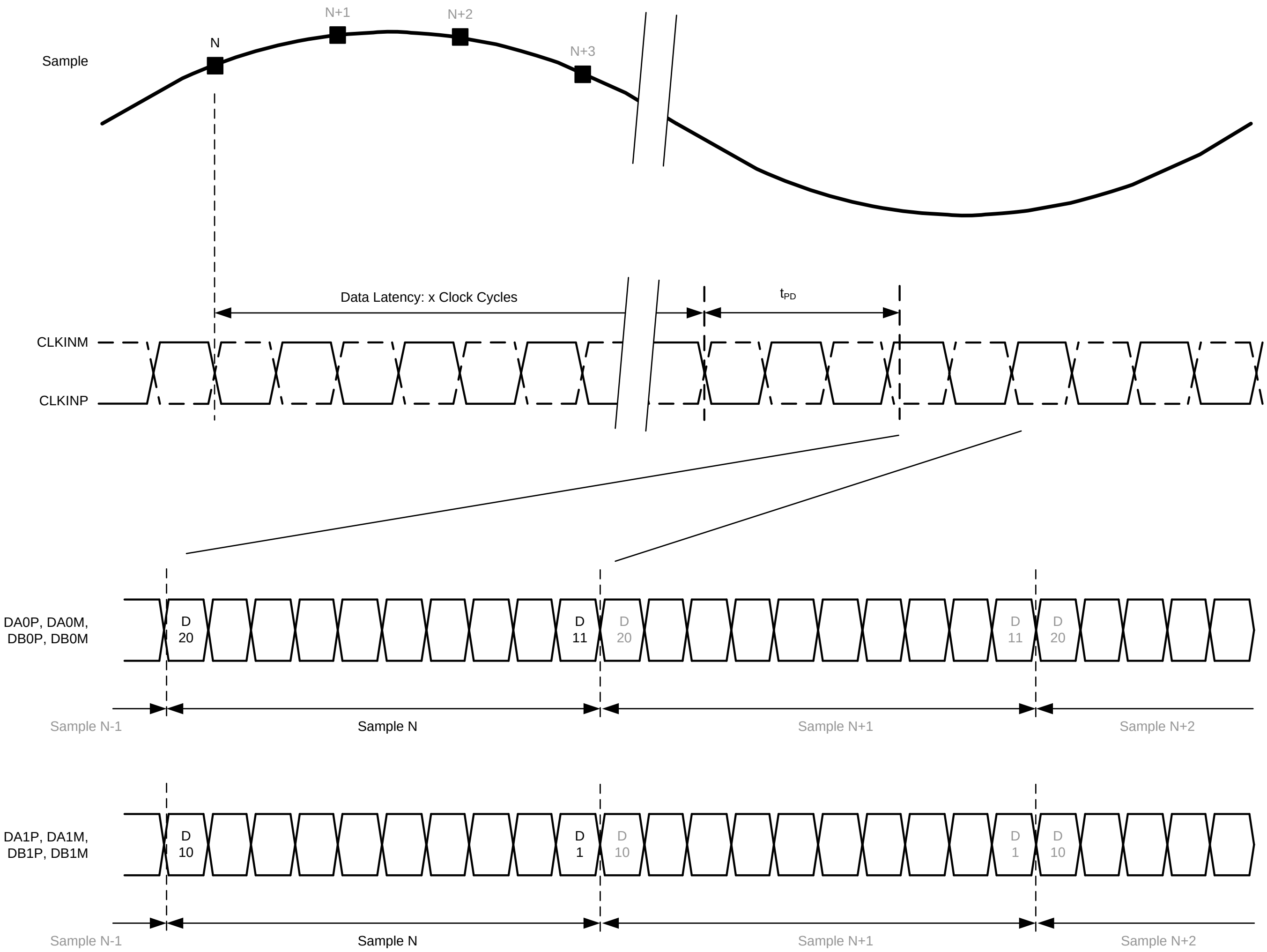

Figure 2. Sample Timing Requirements

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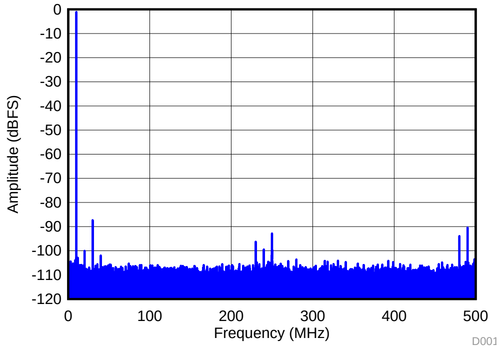
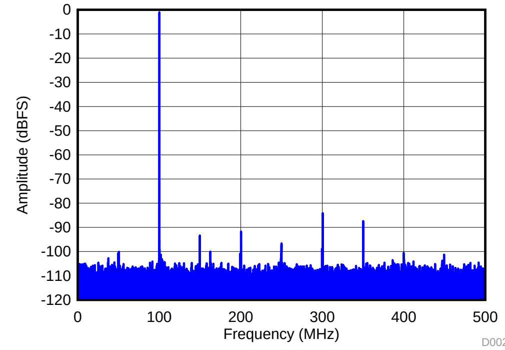
6.9 Typical Characteristics

Typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input, unless otherwise noted.



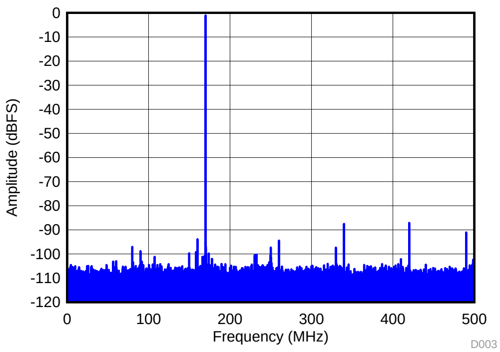
SNR = 71 dBFS; SFDR = 88 dBc;
IL spur = 87 dBc; non HD2, HD3 spur = 93 dBc

Figure 3. FFT for 10-MHz Input Signal



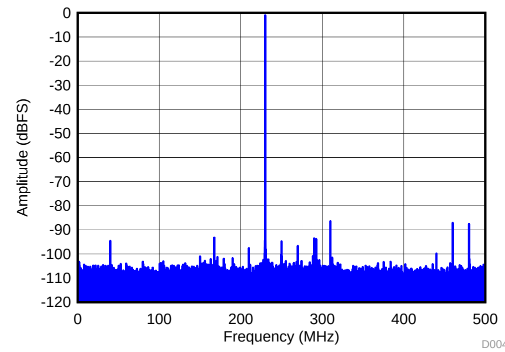
SNR = 71 dBFS; SFDR = 83 dBc;
IL spur = 87 dBc; non HD2, HD3 spur = 95 dBc

Figure 4. FFT for 100-MHz Input Signal



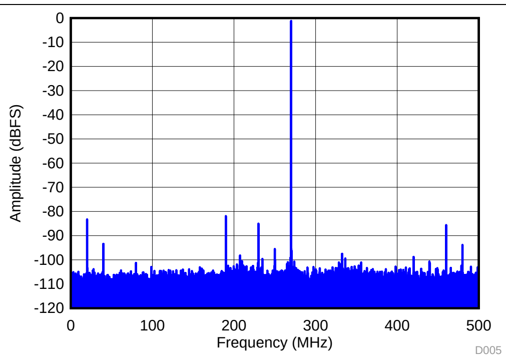
SNR = 70 dBFS; SFDR = 86 dBc;
IL spur = 87 dBc; non HD2, HD3 spur = 96 dBc

Figure 5. FFT for 170-MHz Input Signal



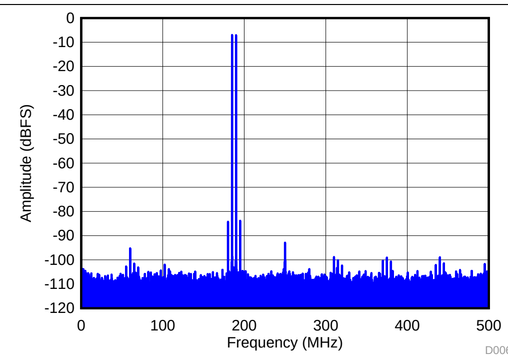
SNR = 69.5 dBFS; SFDR = 85 dBc;
IL spur = 87 dBc; non HD2, HD3 spur = 93 dBc

Figure 6. FFT for 230-MHz Input Signal



SNR = 69 dBFS; SFDR = 81 dBc;
IL spur = 83 dBc; non HD2, HD3 spur = 87 dBc

Figure 7. FFT for 270-MHz Input Signal



Two-tone IMD = 84 dBFS

Figure 8. FFT for Two-Tone input signal (185 MHz and 190 MHz, A_{IN}= –7 dBFS)

Typical Characteristics (continued)

Typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input, unless otherwise noted.

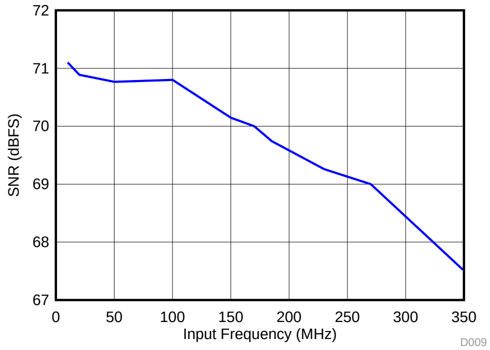


Figure 9. SNR vs Input Frequency

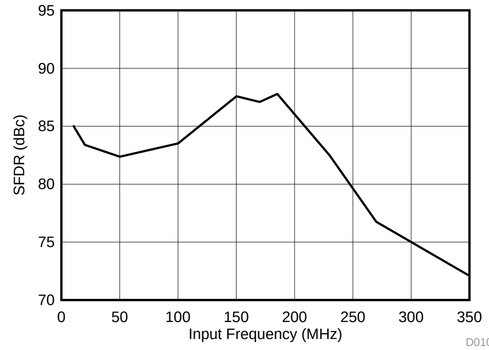


Figure 10. SFDR vs Input Frequency

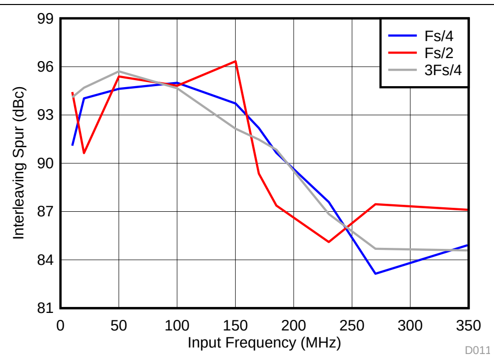


Figure 11. Interleaving Spur vs Input Frequency

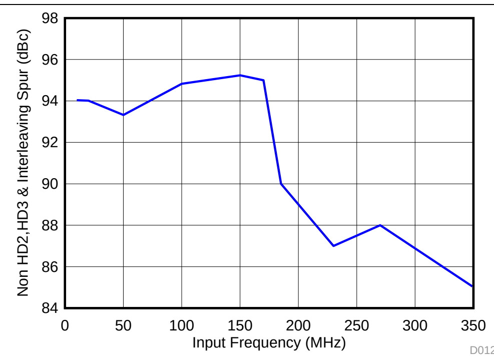
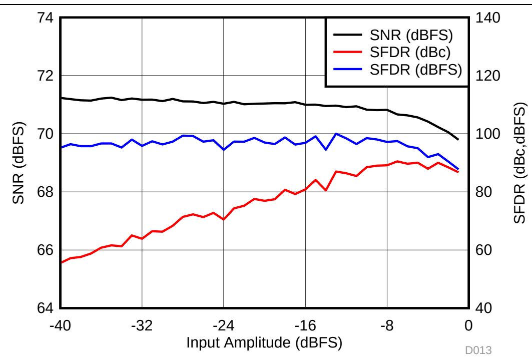
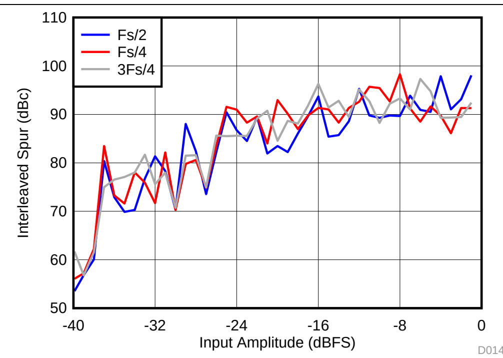


Figure 12. Non HD2, HD3 Spur vs Input Frequency



f_{IN} = 170 MHz

Figure 13. Performance vs Input Amplitude



f_{IN} = 170 MHz

Figure 14. Interleaving Spur vs Input Amplitude

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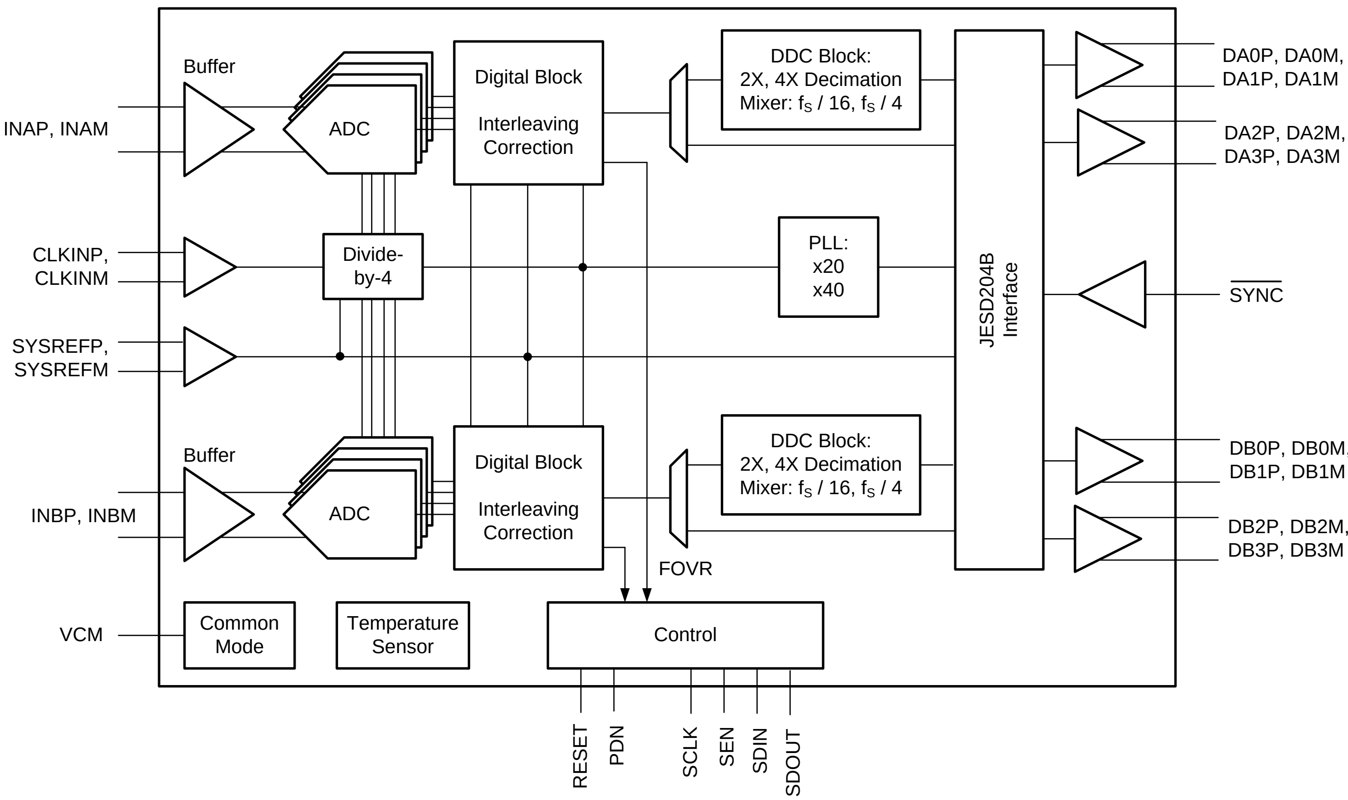
7 Detailed Description

7.1 Overview

The ADS54J60 is a low-power, wide-bandwidth, 16-bit, 1.0-GSPS, dual-channel, analog-to-digital converter (ADC). Designed for high signal-to-noise ratio (SNR), the device delivers a noise floor of –159 dBFS/Hz for applications aiming for highest dynamic range over a wide instantaneous bandwidth. The device supports the JESD204B serial interface with data rates up to 10.0 Gbps, supporting two or four lanes per ADC. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. Each ADC channel optionally can be connected to a wideband digital down converter (DDC) block. The ADS54J60 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with very low power consumption.

The JESD204B interface reduces the number of interface lines, allowing high system integration density. An internal phase-locked loop (PLL) multiplies the ADC sampling clock to derive the bit clock that is used to serialize the 16-bit data from each channel.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs

The ADS54J60 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source, which enables great flexibility in the external analog filter design as well as excellent 50-Ω matching for RF applications. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit, resulting in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to VCM using 600-Ω resistors, allowing for ac-coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.475 V) and (VCM – 0.475 V), resulting in a 1.9-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 700 MHz. An equivalent analog input network diagram is shown in Figure 15.

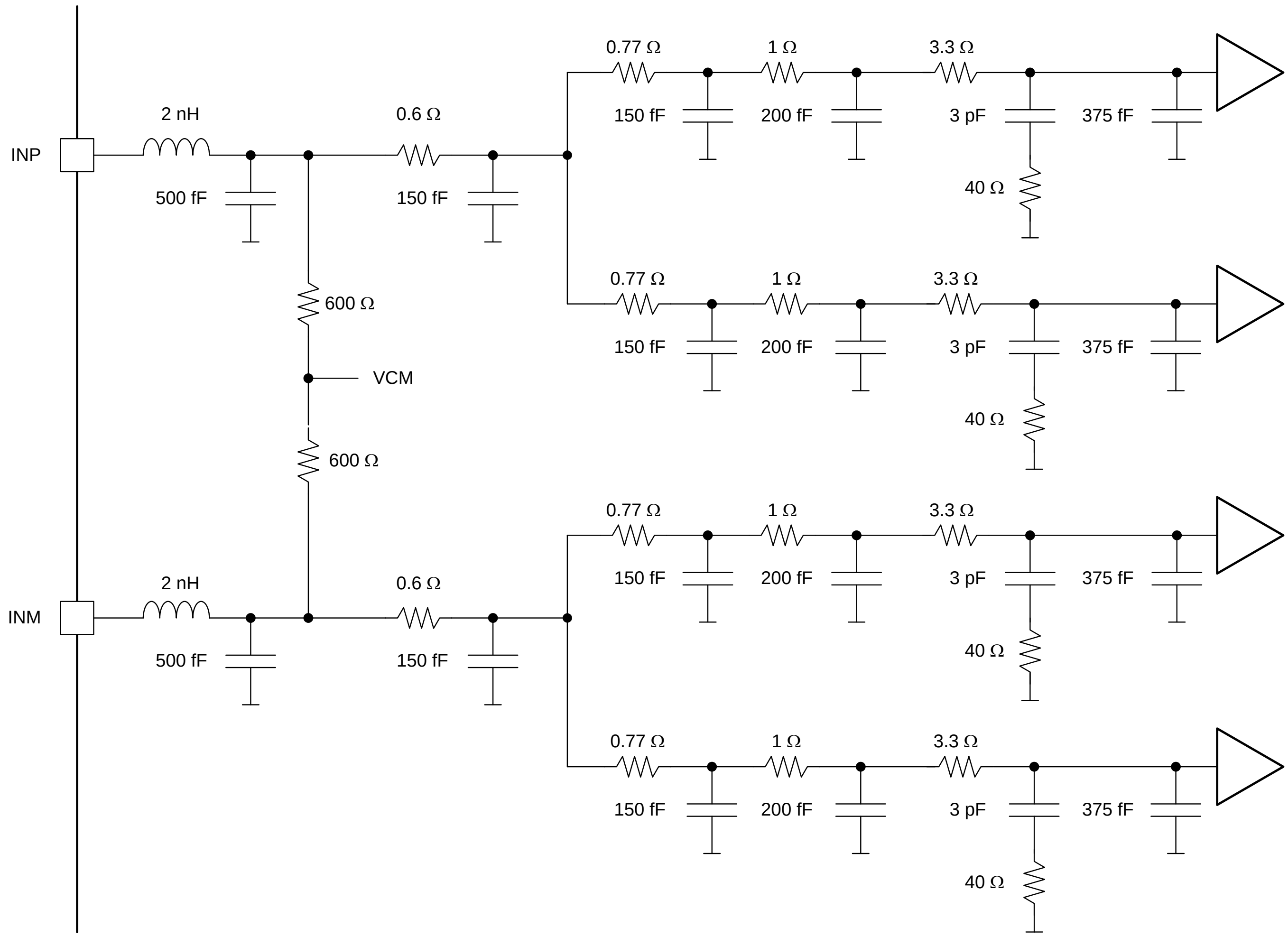


Figure 15. Analog Input Network

Feature Description (continued)

7.3.2 DDC Block

The ADS54J60 has an optional DDC block that can be enabled via an SPI register write. Each ADC channel is followed by a DDC block consisting of three different decimate-by-2 and by-4 finite impulse response (FIR) half-band filter options. The different decimation filter options can be selected via SPI programming.

7.3.2.1 Decimate-by-2 Filter

This decimation filter has 41 taps with a latency of approximately ten output clock cycles. The stop-band attenuation is approximately 90 dB and the pass-band flatness is ±0.05 dB. Table 1 shows corner frequencies for low-pass and high-pass filter options.

Table 1. Corner Frequencies for the Decimate-by-2 Filter

CORNERS (dB)	LOW PASS	HIGH PASS
–0.1	0.202 × f_S	0.298 × f_S
–0.5	0.210 × f_S	0.290 × f_S
–1	0.215 × f_S	0.285 × f_S
–3	0.227 × f_S	0.273 × f_S

Figure 16 and Figure 17 show the frequency response of a decimate-by-2 filter from dc to f_S / 2.

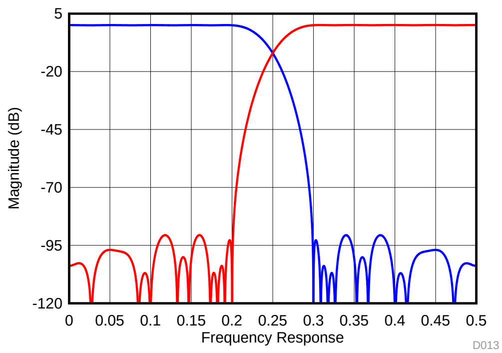


Figure 16. Decimate-by-2 Filter Response

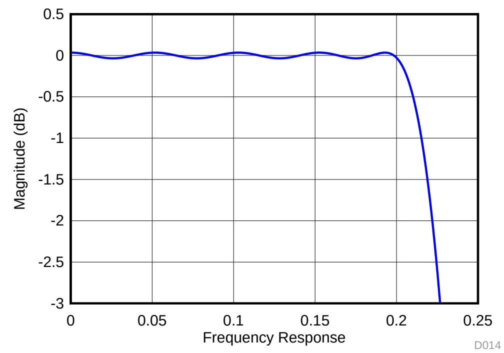


Figure 17. Decimate-by-2 Filter Response (Zoomed)

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7.3.2.2 Decimate-by-4 Filter Using a Digital Mixer

This band-pass decimation filter consists of a digital mixer and three concatenated FIR filters with a combined latency of approximately 28 output clock cycles. The alias band attenuation is approximately 55 dB and the pass-band flatness is ±0.1 dB. By default after reset, the band-pass filter is centered at f_S / 16. Using the SPI, the center frequency can be programmed at N × f_S / 16 (where N = 1, 3, 5, or 7). Table 2 shows corner frequencies for two extreme options.

Table 2. Corner frequencies for the Decimate-by-4 Filter

CORNERS (dB)	CENTER FREQUENCY AT LOWER SIDE (f_S / 16)	CENTER FREQUENCY AT HIGHER SIDE ($7f_S$ / 16)
–0.1	0.011 × f_S	0.114 × f_S
–0.5	0.010 × f_S	0.116 × f_S
–1	0.008 × f_S	0.117 × f_S
–3	0.006 × f_S	0.120 × f_S

Figure 18 and Figure 19 show the frequency response of a decimate-by-4 filter from dc to f_S / 2.

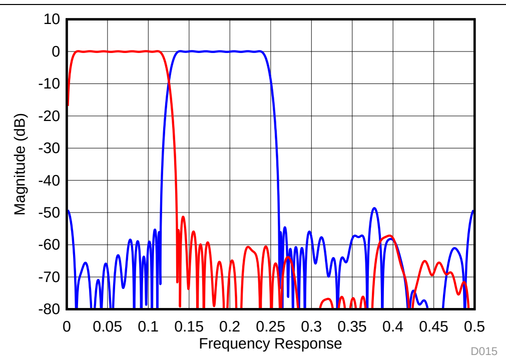

Figure 18. Decimate-by-4 Filter Response

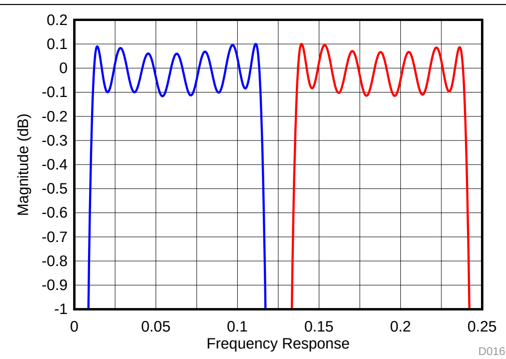

Figure 19. Decimate-by-4 Filter Response (Zoomed)

7.3.2.3 Decimate-by-4 Filter with IQ Outputs

In this configuration, the DDC block includes a fixed digital f_S / 4 mixer. Thus, the IQ pass band is approximately ±110 MHz, centered at f_S / 4. This decimation filter has 41 taps with a latency of approximately ten output clock cycles. The stop-band attenuation is approximately 90 dB and the pass-band flatness is ±0.05 dB. Table 3 shows the corner frequencies for a low-pass decimate-by-4 with IQ filter.

Table 3. Corner Frequencies for a Decimate-by-4 IQ Output Filter

CORNERS (dB)	LOW PASS
–0.1	0.107 × f_S
–0.5	0.112 × f_S
–1	0.115 × f_S
–3	0.120 × f_S

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Figure 20 and Figure 21 show the frequency response of a decimate-by-4 IQ output filter from dc to f_S / 2.

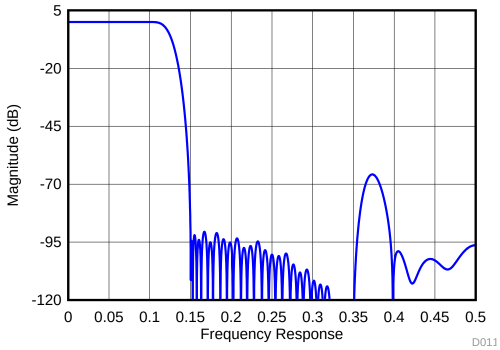

Figure 20. Decimate-by-4 with IQ Outputs Filter Response

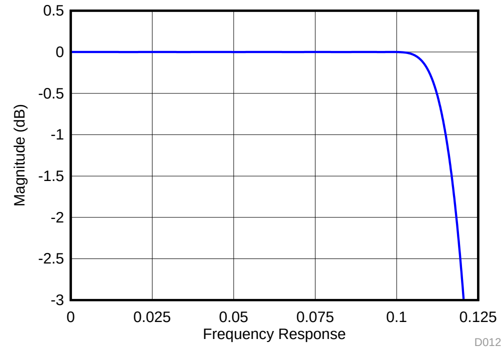

Figure 21. Decimate-by-4 with IQ Outputs Filter Response (Zoomed)

7.3.3 SYSREF Signal

The SYSREF signal is a periodic signal that is sampled by the ADS54J60 device clock and used to align the boundary of the local multi-frame clock inside the data converter. SYSREF is required to be a sub-harmonic of the local multiframe clock (LMFC) internal timing. To meet this requirement, the timing of SYSREF is dependent on the device clock frequency and the LMFC frequency, as determined by the selected DDC decimation and frames per multi-frame settings. TI recommends that the SYSREF signal be a low-frequency signal in the range of 1 MHz to 5 MHz in order to reduce coupling to the signal path both on the printed circuit board (PCB) as well as internal in the device.

The external SYSREF signal must be a sub-harmonic of the internal LMFC clock, as shown in Equation 1 and Table 4.

$$\text{SYSREF} = \text{LMFC} / 2^N$$

where

- N = 0, 1, 2, and so forth. (1)

Table 4. LMFSC Clock Frequency

LMFS CONFIGURATION	DECIMATION	LMFC CLOCK(1)(2)
4211	—	f_S / k
4244	—	f_S / (4 / k)
8224	—	f_S / (4 / k)
…	…	…
4222	2X	(f_S / 2) / (2 / k)
2242	2X	(f_S / 2) / (2 / k)
2242	4X	(f_S / 4) / (2 / k)
2441	4X	(f_S / 4) / k
4421	4X	(f_S / 4) / k
1241	4X	(f_S / 4) / k

(1) K = Number of frames per multi frame (JESD digital page 6900h, address 06h, bits 4-0).
(2) f_S = sampling (device) clock frequency.

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7.3.4 Overrange Indication

The ADS54J60 provides a fast overrange indication that can be presented in the digital output data stream via SPI configuration. Alternatively, if not used, the SDOUT (pin 11) and PDN (pin 50) pins can be configured via the SPI to output the fast OVR indicator.

When the FOVR indication is embedded in the output data stream, it replaces the LSB of the 16-bit data stream going to the 8b/10b encoder, as shown in Figure 22.

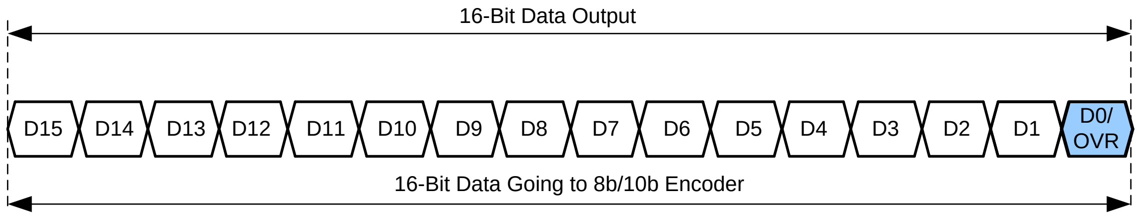

Figure 22. Overrange Indication in a Data Stream

7.3.4.1 Fast OVR

The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after only seven clock cycles, thus enabling a quicker reaction to an overrange event.

The input voltage level at which the overload is detected is referred to as the *threshold*. The threshold is programmable using the FOVR THRESHOLD bits, as shown in Figure 23. The FOVR is triggered seven output clock cycles after the overload condition occurs.

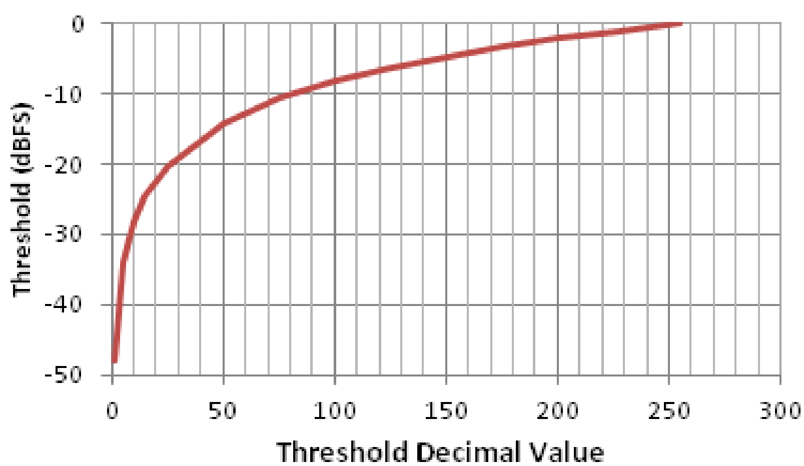

Figure 23. Programming Fast OVR Thresholds

The input voltage level at which the fast OVR is triggered is defined by Equation 2:

Full-Scale × [Decimal Value of the FOVR Threshold Bits] / 255) (2)

The default threshold is E3h (227d), corresponding to a threshold of –1 dBFS.

In terms of full-scale input, the fast OVR threshold can be calculated as Equation 3:

20log (FOVR Threshold / 255) (3)

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7.3.5 Power-Down Mode

The ADS54J60 provides a highly-configurable power-down mode. Power-down can be enabled using the PDN pin or SPI register writes.

A power-down mask can be configured, which allows a trade-off between wake-up time and power consumption in power-down mode. Two independent power-down masks can be configured: MASK 1 and MASK 2 as shown in Table 5. See the master page registers in Table 15 for further details.

Table 5. Register Address for Power-Down Modes

REGISTER ADDRESS	COMMENT	REGISTER DATA							
A[7:0] (Hex)		7	6	5	4	3	2	1	0
MASTER PAGE (80h)									
20	MASK 1	PDN ADC CHA				PDN ADC CHB			
21		PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
23	MASK 2	PDN ADC CHA				PDN ADC CHB			
24		PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
26	CONFIG	GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
53		0	MASK SYSREF	0	0	0	0	0	0
55		0	0	0	PDN MASK	0	0	0	0

To save power, the device can be put in complete power down by using the GLOBAL PDN register bit. However, when JESD must remain linked up while putting the device in power down, the ADC and analog buffer can be powered down by using the PDN ADC CHx and PDN BUFFER CHx register bits after enabling the PDN MASK register bit. The PDN MASK SEL register bit can be used to select between MASK 1 or MASK 2. Table 6 shows power consumption for different combinations of the GLOBAL PDN, PDN ADC CHx, and PDN BUFF CHx register bits.

Table 6. Power Consumption in Different Power-Down Settings

REGISTER BIT	COMMENT	IAVDD3V (mA)	IAVDD (mA)	IDVDD (mA)	IIOVDD (mA)	TOTAL POWER (W)
Default	After reset, with a full-scale input signal to both channels	334	359	197	566	2.74
GBL PDN = 1	The device is in complete power-down state	2	6	1	104	0.14
GBL PDN = 0, PDN ADC CHx = 1 (x = A or B)	The ADC of one channel is powered down	276	222	135	511	2.09
GBL PDN = 0, PDN BUFF CHx = 1 (x = A or B)	The input buffer of one channel is powered down	262	352	193	546	2.45
GBL PDN = 0, PDN ADC CHx = 1, PDN BUFF CHx = 1 (x = A or B)	The ADC and input buffer of one channel is powered down	199	221	135	503	1.85
GBL PDN = 0, PDN ADC CHx = 1, PDN BUFF CHx = 1 (x = A and B)	The ADC and input buffer of both channels are powered down	61	78	70	463	1.00

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7.4 Device Functional Modes

7.4.1 Device Configuration

The ADS54J60 can be configured by using a serial programming interface, as described in the *Serial Interface* section. In addition, the device has one dedicated parallel pin (PDN) for controlling the power-down mode.

The ADS54J60 supports a 24-bit (16-bit address, 8-bit data) SPI operation and uses paging (see the *Register Maps* section) to access all register bits.

7.4.1.1 Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDIN (serial interface data) pins, as shown in Figure 24. Legends used in Figure 24 are explained in Table 7. Serially shifting bits into the device is enabled when SEN is low. Serial data on SDIN are latched at every SCLK rising edge when SEN is active (low). The interface can function with SCLK frequencies from 2 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

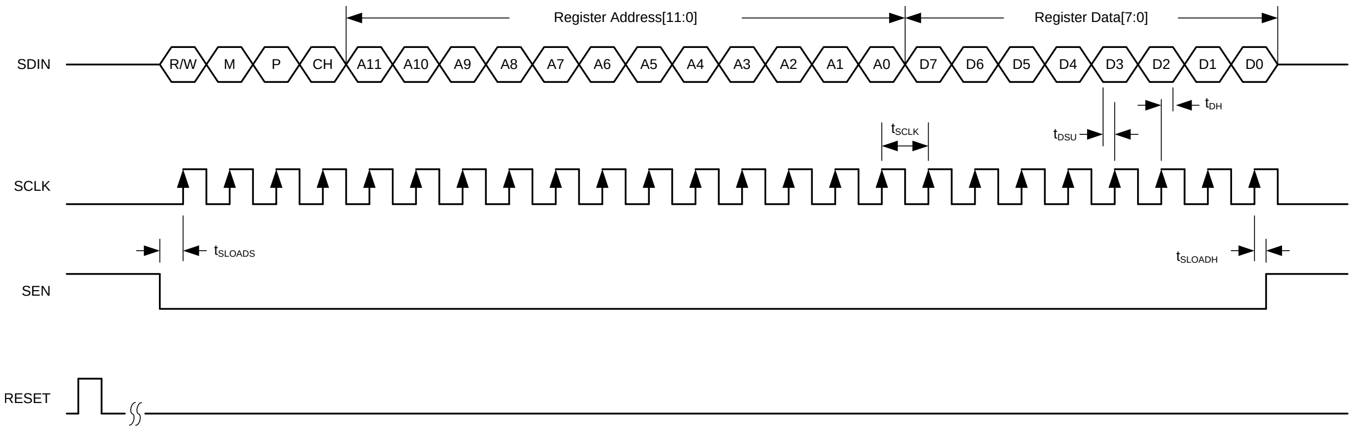

Figure 24. SPI Timing Diagram

Table 7. SPI Timing Diagram Legend

SPI BITS	DESCRIPTION	BIT SETTINGS
R/W	Read/write bit	0 = SPI write 1 = SPI read back
M	SPI bank access	0 = Analog SPI bank (master and ADC pages) 1 = JESD SPI bank (Main Digital, Interleaving Engine,, analog JESD, and digital JESD pages)
P	JESD page selection bit	0 = Page access 1 = Register access
CH	SPI access for a specific channel of the JESD SPI bank	0 = Channel A 1 = Channel B By default, both channels are being addressed.
A[11:0]	SPI address bits	—
D[7:0]	SPI data bits	—

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Table 8 shows the timing requirements for the serial interface signals in Figure 24.

Table 8. SPI Timing Requirements

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		2	MHz
t_{SLOADS}	SEN to SCLK setup time	100			ns
t_{SLOADH}	SCLK to SEN hold time	100			ns
t_{DSU}	SDIN setup time	100			ns
t_{DH}	SDIN hold time	100			ns

7.4.1.2 Serial Register Write: Analog Bank

The analog SPI bank contains of two pages (the master and ADC page). The internal register of the ADS54J60 analog SPI bank can be programmed by:

1. Drive the SEN pin low.
2. Initiate a serial interface cycle specifying the page address of the register whose content must be written.
   - Master page: write address 0011h with 80h.
   - ADC page: write address 0011h with 0Fh.
3. Write the register content as shown in Figure 25. When a page is selected, multiple writes into the same page can be done.

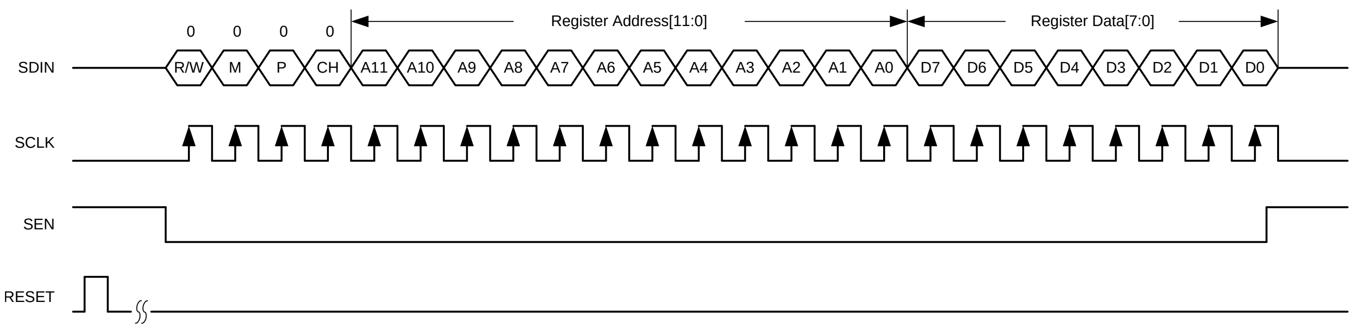

Figure 25. Serial Register Write Timing Diagram

7.4.1.3 Serial Register Readout: Analog Bank

The content from one of the two analog banks can be read out by:

1. Drive the SEN pin low.
2. Select the page address of the register whose content must be read.
   – Master page: write address 0011h with 80h.
   – ADC page: write address 0011h with 0Fh.
3. Set the R/W bit to 1 and write the address to be read back.
4. Read back the register content on the SDOUT pin, as shown in Figure 26. When a page is selected, multiple read backs from the same page can be done.

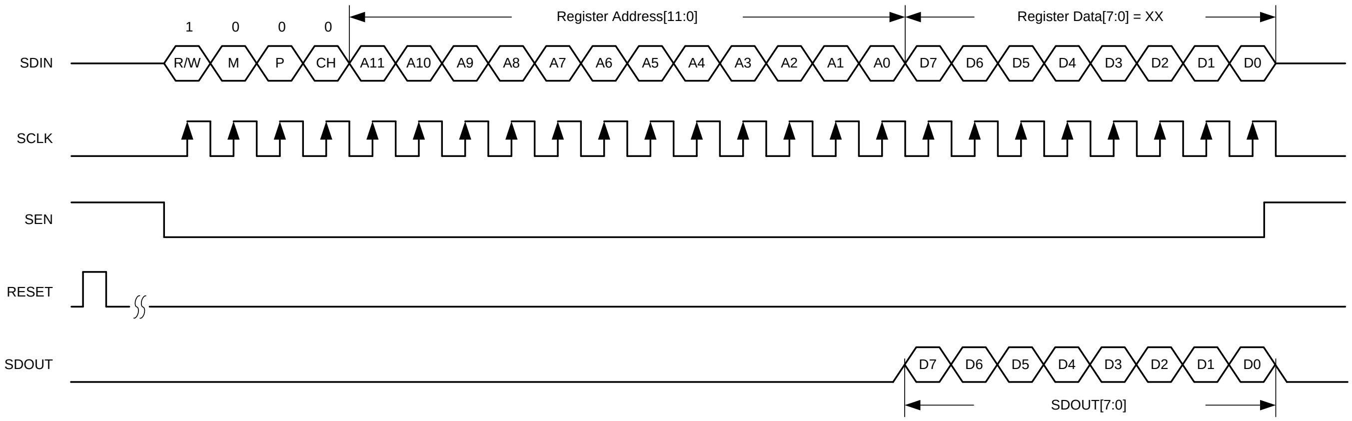

Figure 26. Serial Register Read Timing Diagram

7.4.1.4 JESD Bank SPI Page Selection

The JESD SPI bank contains four pages (main digital, interleaving engine, digital, and analog JESD pages). The individual pages can be selected by:

1. Drive the SEN pin low.
2. Set the M bit to 1 and specify the page with two register writes. Note that the P bit must be set to 0, as shown in Figure 27.
   – Write address 4003h with 00h (LSB byte of page address).
   – Write address 4004h with the MSB byte of the page address.
     – For Main digital page: write address 4004h with 68h.
     – For Digital JESD page: write address 4004h with 69h.
     – For Analog JESD page: write address 4004h with 6Ah.
     – For Interleaving engine page: write address 4004h with 61h.

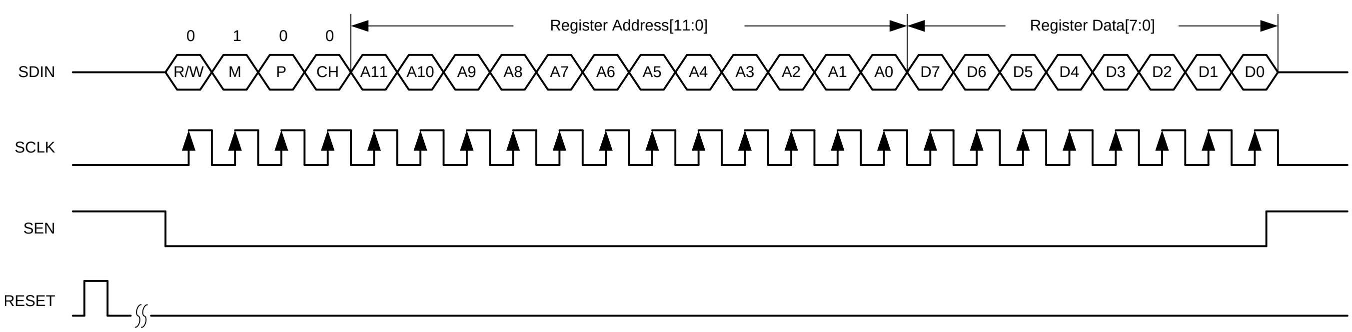

Figure 27. SPI Page Selection

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7.4.1.5 Serial Register Write: JESD Bank

The ADS54J60 is a dual-channel device and the JESD204B portion is configured individually for each channel by using the CH bit. Note that the P bit must be set to 1 for register writes.

1. Drive the SEN pin low.
2. Select the JESD bank page. Note that the M bit = 1 and the P bit = 0.
   – Write address 4003h with 00h.
   – Write address 4005h with 01h to enable separate control for both channels.
     – For Main digital page: write address 4004h with 68h.
     – For Digital JESD page: write address 4004h with 69h.
     – For Analog JESD page: write address 4004h with 6Ah.
     – For Interleaving engine page: write address 4004h with 61h.
3. Set the M and P bits to 1, select channel A (CH = 0) or channel B (CH = 1), and write the register content as shown in Figure 28. When a page is selected, multiple writes into the same page can be done.

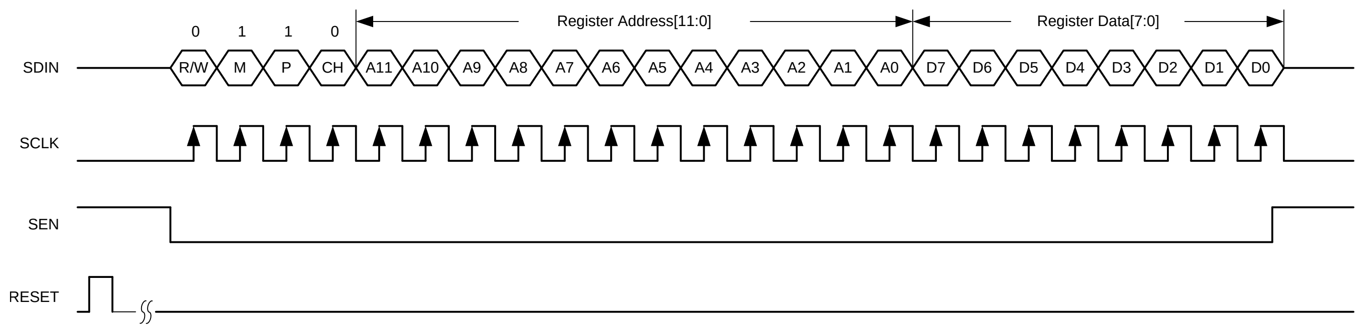

Figure 28. JESD Serial Register Write Timing Diagram

7.4.1.5.1 Individual Channel Programming

By default, register writes are applied to both channels. To enable individual channel writes, write address 4005h with 01h (default is 00h).

7.4.1.6 Serial Register Readout: JESD Bank

The content of one of the three JESD banks can be read out by:

1. Drive the SEN pin low.
2. Select the JESD bank page. Note that the M bit = 1 and the P bit = 0.
   – Write address 4003h with 00h.
   – Write address 4005h with 01h to enable separate control for both channels.
     – For Main digital page: write address 4004h with 68h.
     – For Digital JESD page: write address 4004h with 69h.
     – For Analog JESD page: write address 4004h with 6Ah.
     – For Interleaving engine page: write address 4004h with 61h.
3. Set the R/W, M, and P bits to 1, select channel A or channel B, and write the address to be read back.
4. Read back the register content on the SDOUT pin; see Figure 29. When a page is selected, multiple read backs from the same page can be done.

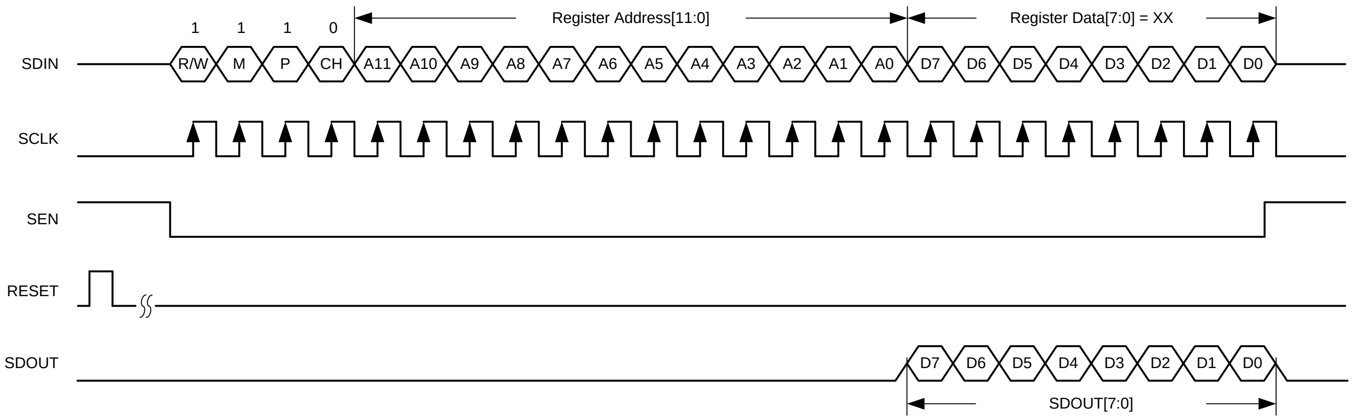

Figure 29. JESD Serial Register Read Timing Diagram

7.4.2 JESD204B Interface

The ADS54J60 supports device subclass 1 with a maximum output data rate of 10.0 Gbps for each serial transmitter.

An external SYSREF signal is used to align all internal clock phases and the local multi-frame clock to a specific sampling clock edge, allowing synchronization of multiple devices in a system and minimizing timing and alignment uncertainty. The $\overline{\text{SYNC}}$ input is used to control the JESD204B SERDES blocks.

Depending on the ADC output data rate, the JESD204B output interface can be operated with either two or four lanes per single ADC, as shown in Figure 30. The JESD204B setup and configuration of the frame assembly parameters is controlled via the SPI interface.

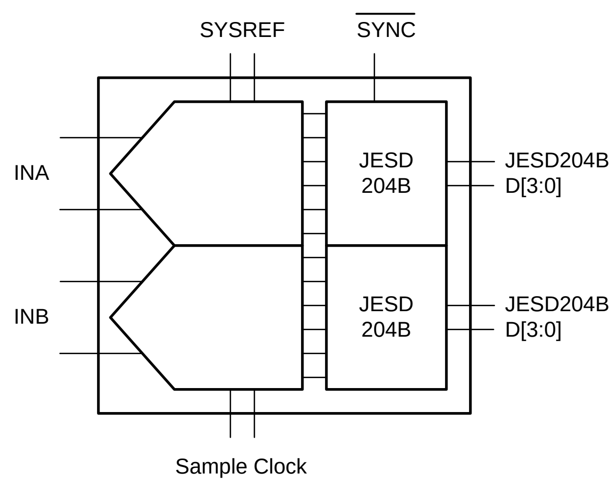

Figure 30. ADS54J60 Block Diagram

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The JESD204B transmitter block shown in Figure 31 consists of the transport layer, the data scrambler, and the link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format and manages if the ADC output data or test patterns are being transmitted. The link layer performs the 8b/10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer can be scrambled.

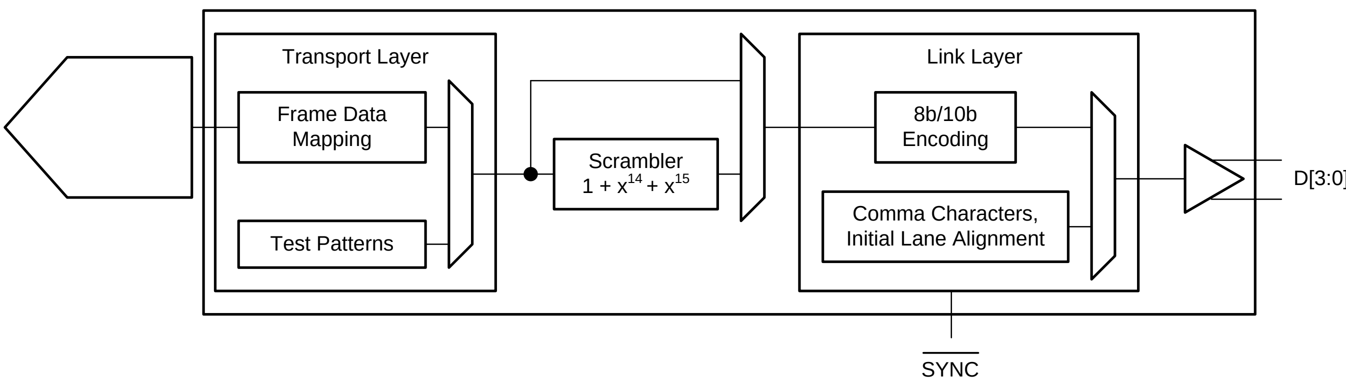

Figure 31. JESD204B Transmitter Block

7.4.2.1 JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started when the receiving device de-asserts the SYNC signal, as shown in Figure 32. When a logic low is detected on the SYNC input pin, the ADS54J60 starts transmitting comma (K28.5) characters to establish a code group synchronization.

When synchronization is complete, the receiving device asserts the SYNC signal and the ADS54J60 starts the initial lane alignment sequence with the next local multi-frame clock boundary. The ADS54J60 transmits four multi-frames, each containing K frames (K is SPI programmable). Each of the multi-frames contains the frame start and end symbols and the second multi-frame also contains the JESD204 link configuration data.

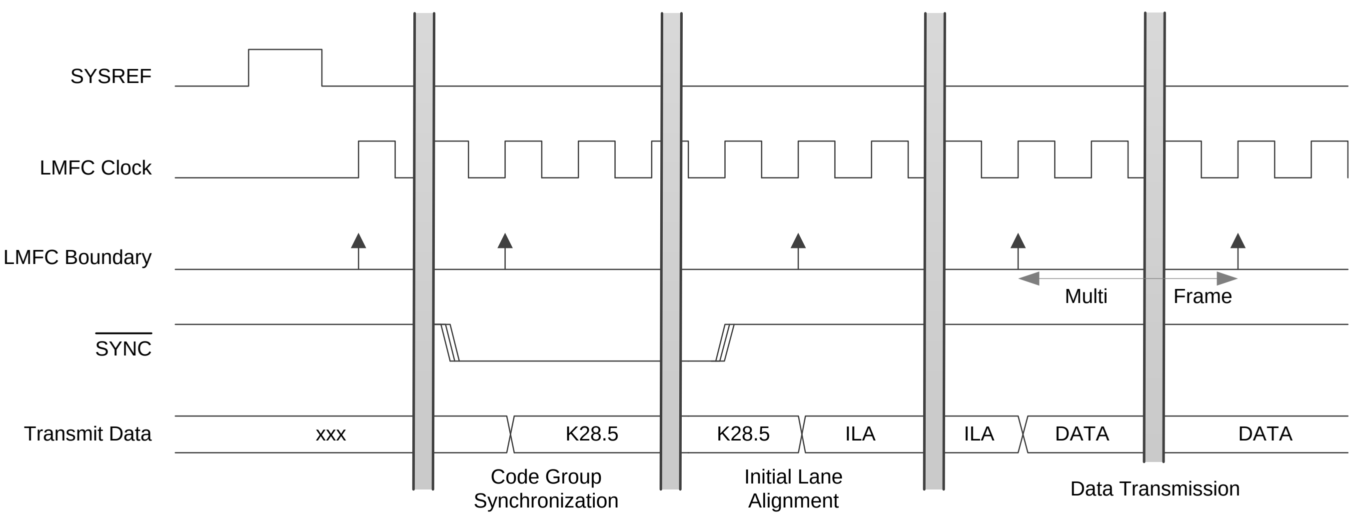

Figure 32. Lane Alignment Sequence

7.4.2.2 JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The ADS54J60 supports a clock output, encoded, and a PRBS (2^{15} – 1) pattern. These patterns can be enabled via an SPI register write and are located in address TBD.

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7.4.2.3 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per link.
- M is the number of converters per device.
- F is the number of octets per frame clock period, per lane.
- S is the number of samples per frame.

7.4.2.4 JESD204B Frame Assembly (Decimation Filter Bypassed)

Table 9 lists the available JESD204B formats and valid ranges for the ADS54J60 when the decimation filter is bypassed. The ranges are limited by the SERDES line rate and the maximum ADC sample frequency.

Table 9. Default Interface Rates (Decimation filter Bypassed)

L	M	F	S	JESD MODE	JESD PLL MODE SETTING	MIN ADC SAMPLING RATE (Msps)	MIN f_{SERDES} (Gbps)	MAX ADC SAMPLING RATE (Msps)	MAX f_{SERDES} (Gbps)
4	2	1	1	100	40x	250	2.5	1000	10.0
4	2	4	4	010	40x	250	2.5	1000	10.0
8	2	2	4	001	20x	500	2.5	1000	5.0

NOTE

In the LMFS = 8224 row of Table 9, the sample order in lane DA2 and DA3 are swapped.

The detailed frame assembly is shown in Table 10.

Table 10. Default Frame Assembly (Decimation Filter Bypassed)

PIN	LMFS = 4211				LMFS = 4244				LMFS = 8224			
DA0									A_3[15:8]	A_3[7:0]	A_7[15:8]	A_7[7:0]
DA1	A_0[7:0]	A_1[7:0]	A_2[7:0]	A_3[7:0]	A_2[15:8]	A_2[7:0]	A_3[15:8]	A_3[7:0]	A_2[15:8]	A_2[7:0]	A_6[15:8]	A_6[7:0]
DA2	A_0[15:8]	A_1[15:8]	A_2[15:8]	A_3[15:8]	A_0[15:8]	A_0[7:0]	A_1[15:8]	A_1[7:0]	A_0[15:8]	A_0[7:0]	A_4[15:8]	A_4[7:0]
DA3									A_1[15:8]	A_1[7:0]	A_5[15:8]	A_5[7:0]
DB0									B_3[15:8]	B_3[7:0]	B_7[15:8]	B_7[7:0]
DB1	B_0[7:0]	B_1[7:0]	B_2[7:0]	B_3[7:0]	B_2[15:8]	B_2[7:0]	B_3[15:8]	B_3[7:0]	B_2[15:8]	B_2[7:0]	B_6[15:8]	B_6[7:0]
DB2	B_0[15:8]	B_1[15:8]	B_2[15:8]	B_3[15:8]	B_0[15:8]	B_0[7:0]	B_1[15:8]	B_1[7:0]	B_0[15:8]	B_0[7:0]	B_4[15:8]	B_4[7:0]
DB3									B_1[15:8]	B_1[7:0]	B_5[15:8]	B_5[7:0]

7.4.2.5 JESD204B Frame Assembly with Decimation

Table 11 lists the available JESD204B formats and valid ranges for the ADS54J60 when enabling the decimation filter. The ranges are limited by the SERDES line rate and the maximum ADC sample frequency.

Table 12 lists the detailed frame assembly with different decimation options.

Table 11. Interface Rates with Decimation Filter

L	M	F	S	JESD MODE	LANE SHARE	JESD PLL MODE SETTING	DECIMATION	MAX ADC OUTPUT RATE (Msps)	MIN f_{SERDES} (Gbps)
4	4	2	1	001	0	20x	4X (IQ)	250 (IQ)	5.0
4	2	2	2	001	0	20x	2X	500	5.0
2	2	4	2	010	0	40x	2X	500	10.0
2	2	4	2	010	0	40x	4X	250	5.0
2	4	4	1	010	0	40x	4X (IQ)	250 (IQ)	10.0
1	2	4	1	010	1	40x	4X	250	10.0

Table 12. Frame Assembly with Decimation Filter

PIN	LMFS = 4222, 2X DECIMATION				LMFS = 2242 2X, 4X DECIMATION				LMFS = 2441, 4X DECIMATION (IQ)				LMFS = 4421, 4X DECIMATION (IQ)				LMFS = 1241, 4X DECIMATION			
DA0	A1 [15:8]	A1 [7:0]	A3 [15:8]	A3 [7:0]									AQ0 [15:8]	AQ0 [7:0]	AQ1 [15:8]	AQ1 [7:0]				
DA1	A0 [15:8]	A0 [7:0]	A2 [15:8]	A2 [7:0]	A0 [15:8]	A0 [7:0]	A1 [15:8]	A1 [7:0]	AI0 [15:8]	AI0 [7:0]	AQ0 [15:8]	AQ0 [7:0]	AI0 [15:8]	AI0 [7:0]	AI1 [15:8]	AI1 [7:0]	A0 [15:8]	A0 [7:0]	B0 [15:8]	B0 [7:0]
DA2																				
DA3																				
DB0	B1 [15:8]	B1 [7:0]	B3 [15:8]	B3 [7:0]									BQ0 [15:8]	BQ0 [7:0]	BQ1 [15:8]	BQ1 [7:0]				
DB1	B0 [15:8]	B0 [7:0]	B2 [15:8]	B2 [7:0]	B0 [15:8]	B0 [7:0]	B1 [15:8]	B1 [7:0]	BI0 [15:8]	BI0 [7:0]	BQ0 [15:8]	BQ0 [7:0]	BI0 [15:8]	BI0 [7:0]	BI1 [15:8]	BI1 [7:0]				
DB2																				
DB3																				

7.4.2.5.1 Lane Enable with Decimation

When using on-chip decimation, the digital output must be internally routed to the correct lane using the DEC LANE EN (register 52), DEC LANE0 (register 73), and DEC LANE1 (register 72) registers, as shown in Table 13.

Table 13. Lane Enable with Decimation

L	M	F	S	JESD MODE	LANE SHARE	DECIMATION	DEC LANE1	DEC LANE0
4	4	2	1	001	0	4X (IQ)	1	1
4	2	2	2	001	0	2X	1	1
2	2	4	2	010	0	2X	1	0
2	2	4	2	010	0	4X	1	0
2	4	4	1	010	0	4X (IQ)	1	0
1	2	4	1	010	1	4X	1	0

Table 14 details an example register write for configuring 2X decimation (LPF) with 20X PLL (two lanes per ADC, LMFS = 4222).

Table 14. Example Register Write

ADDRESS (Hex)	DATA (Hex)	COMMENT
4004h	68h	Select the main digital page (6800h)
4003h	00h	Select the main digital page (6800h)
6041h	12h	Set decimate-by-2 (low-pass filter)
604Dh	08h	Enable decimation filter control
6072h	80h	Enable lane 1 for decimated output data
6073h	04h	Enable lane 0 for decimated output data
6052h	80h	Enable lane reduction for decimation mode
6000h	01h	Pulse the digital core reset so the register writes to the main digital page (6800h goes into effect)
6000h	00h	Pulse the digital core reset so the register writes to the main digital page (6800h goes into effect)

7.4.2.5.2 JESD Transmitter Interface

Each of the 10.0-Gbps SERDES JESD transmitter outputs requires ac coupling between the transmitter and receiver. The differential pair must be terminated with 100-Ω resistors as close to the receiving device as possible to avoid unwanted reflections and signal degradation, as shown in Figure 33.

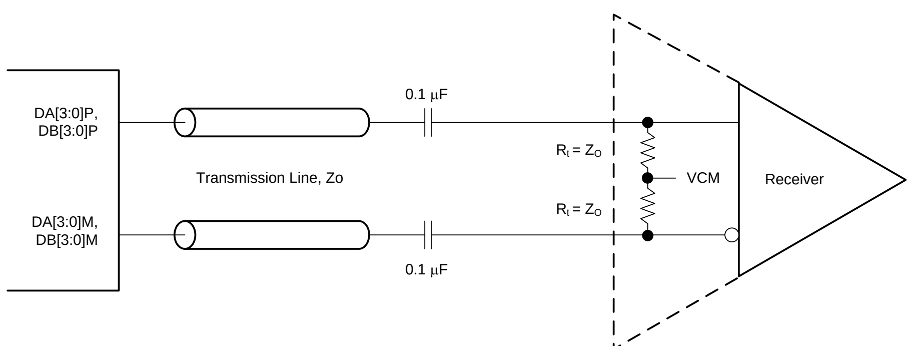

Figure 33. Output Connection to Receiver

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7.4.2.5.3 Eye Diagram

Figure 34 to Figure 37 show the serial output eye diagrams of the ADS54J60 at 5.0 Gbps and 10 Gbps with default and increased output voltage swing against the JESD204B mask.

Figure 34. Eye at 5-Gbps Bit Rate with Default Output Swing

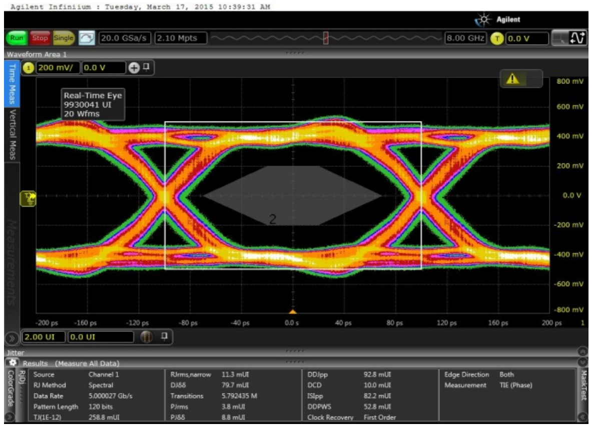

Figure 35. Eye at 5-Gbps Bit Rate with Increased Output Swing

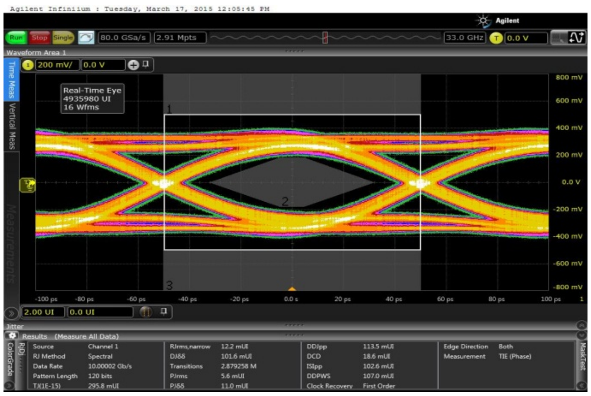

Figure 36. Eye at 10-Gbps Bit Rate with Default Output Swing

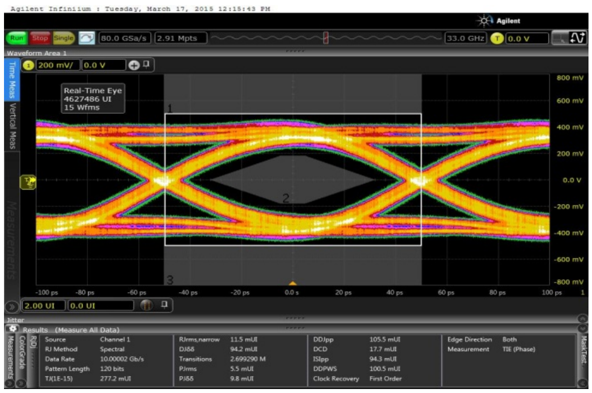

Figure 37. Eye at 10-Gbps Bit Rate with Increased Output Swing

7.5 Register Maps

The ADS54J60 contains two main SPI banks. The analog SPI bank gives access to the ADC analog blocks and the digital SPI bank controls the interleaving engine and anything related to the JESD204B serial interface. The analog SPI bank is divided into two pages (master and ADC) and the digital SPI bank is divided into four pages (main digital, interleaving engine page, JESD digital, and JESD analog). Table 15 lists a register map for the ADS54J60.

Table 15. Register Map

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GENERAL REGISTERS								
0	RESET	0	0	0	0	0	0	RESET
11	ANALOG PAGE SELECTION							
MASTER PAGE (80h)								
20	PDN ADC CHA				PDN ADC CHB			
21	PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
23	PDN ADC CHA				PDN ADC CHB			
24	PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
26	GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
4F	0	0	0	0	0	0	0	EN DC COUPL
53	0	MASK SYSREF	0	0	0	0	EN SYSREF DC	0
55	0	0	0	PDN MASK	0	0	0	0
59	FOVR CHB	0	FOVR CHB EN	0	0	0	0	0
ADC PAGE (0Fh)								
74	TEST PATTERN ON CHANNEL				0	0	0	0
75	CUSTOM PATTERN 1[15:8]							
76	CUSTOM PATTERN 1[7:0]							
77	CUSTOM PATTERN 2[15:8]							
78	CUSTOM PATTERN 2[7:0]							

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Register Maps (continued)

Table 15. Register Map (continued)

<table>
<tr><th>REGISTER ADDRESS</th><th colspan="8">REGISTER DATA</th></tr>
<tr><th>A[7:0] (Hex)</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="9">MAIN DIGITAL PAGE (6800h)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DIG CORE RESET</td></tr>
<tr><td>41</td><td>0</td><td>0</td><td>DECFIL MODE[3]</td><td>DECFIL EN</td><td>0</td><td colspan="3">DECFIL MODE[2:0]</td></tr>
<tr><td>42</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">NYQUIST ZONE</td></tr>
<tr><td>43</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>FORMAT SEL</td></tr>
<tr><td>44</td><td>0</td><td colspan="7">DIGITAL GAIN</td></tr>
<tr><td>4B</td><td>0</td><td>0</td><td>FORMAT EN</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>4D</td><td>0</td><td>0</td><td>CTRL LOOP EN</td><td>0</td><td>DEC MODE EN</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>4E</td><td>CTRL NYQUIST</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>52</td><td>DEC LANE EN</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DIG GAIN EN</td></tr>
<tr><td>68</td><td>0</td><td>LOOP EN</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>72</td><td>DEC LANE1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>73</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DEC LANE0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>AD</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">LSB SELECT</td></tr>
<tr><td>F7</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DIG RESET</td></tr>
<tr><td colspan="9">INTERLEAVING ENGINE PAGE (6100h)</td></tr>
<tr><td>18</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">IL BYPASS</td></tr>
<tr><td>68</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DC CORR DIS</td><td>DC CORR CTRL</td><td>0</td></tr>
<tr><td colspan="9">JESD DIGITAL PAGE (6900h)</td></tr>
<tr><td>0</td><td>CTRL K</td><td>0</td><td>0</td><td>TESTMODE EN</td><td>FLIP ADC DATA</td><td>LANE ALIGN</td><td>FRAME ALIGN</td><td>TX LINK DIS</td></tr>
<tr><td>1</td><td>SYNC REG</td><td>SYNC REG EN</td><td colspan="3">JESD FILTER</td><td colspan="3">JESD MODE</td></tr>
<tr><td>2</td><td colspan="3">LINK LAYER TESTMODE</td><td>LINK LAYER RPAT</td><td>LMFC MASK RESET</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>3</td><td>FORCE LMFC COUNT</td><td colspan="5">LMFC COUNT INIT</td><td colspan="2">RELEASE ILANE SEQ</td></tr>
<tr><td>5</td><td>SCRAMBLE EN</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>6</td><td>0</td><td>0</td><td>0</td><td colspan="5">FRAMES PER MULTI FRAME (K)</td></tr>
<tr><td>7</td><td>0</td><td>0</td><td>0</td><td>0</td><td>SUBCLASS</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>16</td><td>1</td><td>0</td><td>LANE SHARE</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

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Register Maps (continued)

Table 15. Register Map (continued)

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	7	6	5	4	3	2	1	0
JESD ANALOG PAGE (6A00h)								
12	SEL EMP Lane 1						0	0
13	SEL EMP Lane 0						0	0
14	SEL EMP Lane 2						0	0
15	SEL EMP Lane 3						0	0
16	0	0	0	0	0	0	JESD PLL MODE	
1A	0	0	0	0	0	0	FOVR CHA	0
1B	JESD SWING			0	FOVR CHA EN	0	0	0

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7.5.1 Example Register Writes

This section provides three different example register writes. Table 16 describes a global power-down register write, Table 17 describes a register write when the default lane setting (four lanes) is changed to two lanes, and Table 18 describes the register write for when 2X decimation is selected for channel B with two lanes per channel. In Table 18, channel A remains in normal output mode (LMFS = 4211) whereas channel B uses decimate-by-2 (LMFS = 2242).

Table 16. Global Power Down

ADDRESS (Hex)	DATA (Hex)	COMMENT
11h	80h	Set the master page
26h	80h	Set the global power down

Table 17. Two Lanes per Channel Mode (LMFS = 4211)

ADDRESS (Hex)	DATA (Hex)	COMMENT
4004h	69h	Select the digital JESD page
4003h	00h	Select the digital JESD page
6001h	02h	Select the digital to 40X mode
4004h	6Ah	Select the analog JESD page
6016h	02h	Set the SERDES PLL to 40X mode

Table 18. 2X Decimation for Channel B (LPF) with Two Lanes per Channel

ADDRESS (Hex)	DATA (Hex)	COMMENT
4004h	68h	Select the main digital page
4003h	00h	Select the main digital page
4005h	01h	Enable the individual channel programming mode
7041h	12h	Set the decimate-by-2 (low-pass filter) for channel B only
704Dh	08h	Enable the decimation filter control
7072h	80h	Enable lane 1 for decimated output data
7052h	80h	Enable lane reduction for decimation mode
4005h	00h	Disable the individual channel programming mode
6000h	01h	Pulse the digital core reset so the register writes to the main digital page (6800h goes into effect)
6000h	00h	Pulse the digital core reset so the register writes to the main digital page (6800h goes into effect)
4004h	69h	Select the digital JESD page
4003h	00h	Select the digital JESD page
6001h	02h	Select the digital to 40X mode
4004h	6Ah	Select the analog JESD page
6016h	02h	Set the SERDES PLL to 40X mode

7.5.2 Register Descriptions

7.5.2.1 General Registers

7.5.2.1.1 Register 0 (address = 0h)

Figure 38. Register 0h

7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value after reset

Table 19. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	W	0h	0 = Normal operation 1 = Internal software reset, clears back to 0
6-1	0	W	0h	Must write 0
0	RESET	W	0h	0 = Normal operation 1 = Internal software reset, clears back to 0

7.5.2.1.2 Register 11 (address = 11h)

Figure 39. Register 11h

7	6	5	4	3	2	1	0
ANALOG PAGE SELECTION							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 20. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANALOG PAGE SELECTION	R/W	0h	Register page (only one page at a time can be addressed). Master page = 80h. ADC page = 0Fh. The four digital pages (main digital, interleaving engine, analog JESD, and, Digital JESD) are selected via the M bit. See the *Serial Interface* section for more details.

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7.5.2.2 Master Page (080h) Registers

7.5.2.2.1 Register 20h (address = 20h), Master Page (080h)

Figure 40. Register 20h

7	6	5	4	3	2	1	0
PDN ADC CHA				PDN ADC CHB			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 21. Registers 20h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PDN ADC CHA	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register bit 5 in address 26h. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h.
3-0	PDN ADC CHB	R/W	0h	

7.5.2.2.2 Register 21h (address = 21h), Master Page (080h)

Figure 41. Register 21h

7	6	5	4	3	2	1	0
PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
R/W-0h		R/W-0h		W-0h	R/W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 22. Register 21h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PDN BUFFER CHB	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h.
5-4	PDN BUFFER CHA	R/W	0h	
3	0	W	0h	
2-0	0	W	0h	Must write 0.

7.5.2.2.3 Register 23h (address = 23h), Master Page (080h)

Figure 42. Register 23h

7	6	5	4	3	2	1	0
PDN ADC CHA				PDN ADC CHB			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 23. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PDN ADC CHA	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h.
3-0	PDN ADC CHB	R/W	0h	

7.5.2.2.4 Register 24h (address = 24h), Master Page (080h)

Figure 43. Register 24h

7	6	5	4	3	2	1	0
PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
R/W-0h		R/W-0h		W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 24. Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PDN BUFFER CHB	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h.
5-4	PDN BUFFER CHA	R/W	0h	
3	0	W	0h	
2-0	0	W	0h	Must write 0.

7.5.2.2.5 Register 26h (address = 26h), Master Page (080h)

Figure 44. Register 26h

7	6	5	4	3	2	1	0
GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 25. Register 26h Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL PDN	R/W	0h	Bit 6 (OVERRIDE PDN PIN) must be set before this bit can be programmed. 0 = Normal operation 1 = Global power-down via the SPI
6	OVERRIDE PDN PIN	R/W	0h	This bit ignores the power-down pin control. 0 = Normal operation 1 = Ignores inputs on the power-down pin
5	PDN MASK SEL	R/W	0h	This bit selects power-down mask 1 or mask 2. 0 = Power-down mask 1 1 = Power-down mask 2
4-0	0	R/W	0h	Must write 0

7.5.2.2.6 Register 4Fh (address = 4Fh), Master Page (080h)

Figure 45. Register 4Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EN DC COUPL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 26. Register 4Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0h	Must write 0
0	EN DC COUPL	R/W	0h	Input can be dc coupled using the VCM output of the ADC 0 = DC coupling support disabled 1 = DC coupling support enabled

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7.5.2.2.7 Register 53h (address = 53h), Master Page (080h)

Figure 46. Register 53h

7	6	5	4	3	2	1	0
0	MASK SYSREF	0	0	0	0	EN SYSREF DC	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 27. Register 53h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	Must write 0
6	MASK SYSREF	R/W	0h	0 = Normal operation 1 = Ignores the SYSREF input
5-2	0	R/W	0h	Must write 0
1	EN SYSREF DC	R/W	0h	Enables higher common mode voltage input on SYSREF signal (up to 1.6 V) 0 = Normal operation 1 = Enables higher SYSREF common mode voltage support
0	0	R/W	0h	Must write 0

7.5.2.2.8 Register 55h (address = 55h), Master Page (080h)

Figure 47. Register 55h

7	6	5	4	3	2	1	0
0	0	0	PDN MASK	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 28. Register 55h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0h	Must write 0
4	PDN MASK	R/W	0h	This bit enables power-down via a register bit. 0 = Normal operation 1 = Power-down is enabled by powering down internal blocks as specified in the selected power-down mask
3-0	0	R/W	0h	Must write 0

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7.5.2.2.9 Register 59h (address = 59h), Master Page (080h)

Figure 48. Register 59h

7	6	5	4	3	2	1	0
FOVR CHB	0	FOVR CHB EN	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 29. Register 59h Field Descriptions

Bit	Field	Type	Reset	Description
7	FOVR CHB	R/W	0h	Outputs FOVR signal for channel B on the SDOUT pin. FOVR CHB EN (D5) must be enabled. 0 = normal operation 1 = FOVR on SDOUT pin
6	0	R/W	0h	Must write 0
5	FOVR CHB EN			Enables overwrite of SDOUT pin with the FOVR signal from ChB. 0 = normal operation 1 = SDOUT is being overwritten
4-0	0	R/W	0h	Must write 0

7.5.2.3 ADC Page (0Fh) Registers

7.5.2.3.1 Register 74h (address = 74h), ADC Page (0Fh)

Figure 49. Register 74h

7	6	5	4	3	2	1	0
TEST PATTERN ON CHANNEL				0	0	0	0
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 30. Register 74h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TEST PATTERN ON CHANNEL	R/W	0h	Test pattern output on channels A and B. Need to bypass interleaving engine. 0000 = Normal operation 0001 = Outputs all 0s 0010 = Outputs all 1s 0011 = Outputs toggle pattern: output data are an alternating sequence of 1010101010101010 and 0101010101010101 0100 = Do not use. 0101 = Increment pattern: pattern is incremented by the step size set in the custom pattern 1 (75h and 76h, 16 bits) 0110 = Single pattern: output data are custom pattern 1 (75h and 76h) 0111 = Double pattern: output data alternate between custom pattern 1 and custom pattern 2 1000 = Deskew pattern: output data are AAAAh 1001 = SYNC pattern: output data are FFFFh 1010 = PRBS pattern: output data are PRBS 1011 = 8P sine: output data are an 8-point sine-wave
3-0	0	R/W	0h	Must write 0

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7.5.2.3.2 Registers 75h-76h (addresses = 75h-76h), ADC Page (0Fh)

Figure 50. Register 75h

7	6	5	4	3	2	1	0
CUSTOM PATTERN 1[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 51. Register 76h

7	6	5	4	3	2	1	0
CUSTOM PATTERN 1[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 31. Registers 75h-76h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOM PATTERN 1	R/W	0h	These registers (addresses 75h, 76h) program the custom pattern 1. These registers set the custom pattern 1[15:8] and [7:0] for all channels.

7.5.2.3.3 Registers 77h-78h (addresses = 77h-78h), ADC Page (0Fh)

Figure 52. Register 77h

7	6	5	4	3	2	1	0
CUSTOM PATTERN 2[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Figure 53. Register 78h

7	6	5	4	3	2	1	0
CUSTOM PATTERN 2[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 32. Registers 77h-78h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOM PATTERN 2	R/W	0h	These registers (addresses 77h, 78h) program the custom pattern 2. These registers set the custom pattern 2[15:8] and [7:0] for all channels.

7.5.2.4 Main Digital Page (6800h) Registers

7.5.2.4.1 Register 0h (address = 0h), Main Digital Page (6800h)

Figure 54. Register 0h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DIG CORE RESET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 33. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0h	Must write 0
0	DIG CORE RESET	R/W	0h	This bit resets the digital core but does not self-clear and, thus, must be pulsed(set, then reset). Any function in Main Digital Page gets applied only after this bit is pulsed . 0 = Normal operation 1 = Software reset

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7.5.2.4.2 Register 41h (address = 41h), Main Digital Page (6800h)

Figure 55. Register 41h

7	6	5	4	3	2	1	0
0	0	DECFIL MODE[3]	DECFIL EN	0	DECFIL MODE[2:0]		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 34. Register 41h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0h	Must write 0
5	DECFIL MODE[3]	R/W	0h	This bit selects the decimation filter mode. Table 35 lists the bit settings. The decimation filter control (DEC MODE EN, register 40h, bit 3) and decimation filter enable (DECFIL EN, register 41h, bit 4) must be enabled.
4	DECFIL EN	R/W	0h	Enables the digital decimation filter 0 = Normal operation, full rate output 1 = Digital decimation enabled
3	0	R/W	0h	Must write 0
2-0	DECFIL MODE[2:0]	R/W	0h	These bits select the decimation filter mode. Table 35 lists the bit settings. The decimation filter control (DEC MODE EN, register 40h, bit 3) and decimation filter enable (DECFIL EN, register 41h, bit 4) must be enabled.

Table 35. DECFIL MODE Bit Settings

BITS (5, 2-0)	FILTER MODE	DECIMATION
0000	Bandpass filter centered on 3 × f_S / 16	4X
0100	Bandpass filter centered on 5 × f_S / 16	4X
1000	Bandpass filter centered on 1 × f_S / 16	4X
1100	Bandpass filter centered on 7 × f_S / 16	4X
0010	Low-pass filter	2X
0110	High-pass filter	2X
0011	Low-pass filter with f_S / 4 mixer	4X (IQ)

7.5.2.4.3 Register 42h (address = 42h), Main Digital Page (6800h)

Figure 56. Register 42h

7	6	5	4	3	2	1	0
0	0	0	0	0	NYQUIST ZONE		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 36. Register 42h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0h	Must write 0
2-0	NYQUIST ZONE	R/W	0h	The Nyquist zone must be selected for proper interleaving correction. Control must be enabled (register 4Eh, bit 7). 000 = 1st Nyquist zone (0 MHz to 500 MHz) 001 = 2nd Nyquist zone (500 MHz to 1000 MHz) 010 = 3rd Nyquist zone (1000 MHz to 1500 MHz) All others = Not used

7.5.2.4.4 Register 43h (address = 43h), Main Digital Page (6800h)

Figure 57. Register 43h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FORMAT SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 37. Register 43h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0h	Must write 0
0	FORMAT SEL	R/W	0h	Changes the output format. Set the FORMAT EN bit to enable control using this bit. 0 = Twos complement 1 = Offset binary

7.5.2.4.5 Register 44h (address = 44h), Main Digital Page (6800h)

Figure 58. Register 44h

7	6	5	4	3	2	1	0
0	DIGITAL GAIN						
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 38. Register 44h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	Must write 0
6-0	DIGITAL GAIN	R/W	0h	Digital gain setting. Digital gain must be enabled (register 52h, bit 0). Gain in dB = 20log (digital gain / 32) 7Fh = 127 which equals digital gain of 9.5 dB

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7.5.2.4.6 Register 4Bh (address = 4Bh), Main Digital Page (6800h)

Figure 59. Register 4Bh

7	6	5	4	3	2	1	0
0	0	FORMAT EN	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 39. Register 4Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0h	Must write 0
5	FORMAT EN	R/W	0h	This bit enables control for data format selection using the FORMAT SEL register bit. 0 = Default, output is in twos complement format 1 = Output is in offset binary format after FORMAT SEL bit is also set
4-0	0	R/W	0h	Must write 0

7.5.2.4.7 Register 4Dh (address = 4Dh), Main Digital Page (6800h)

Figure 60. Register 4Dh

7	6	5	4	3	2	1	0
0	0	CTRL LOOP EN	0	DEC MOD EN	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 40. Register 4Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0h	Must write 0
5	CTRL LOOP EN	R/W	0h	This bit enables control of the analog loop correction (register 68h, bit 6). 0 = Control disabled 1 = Control enabled (allows overwrite)
4	0	R/W	0h	Must write 0
3	DEC MOD EN	R/W	0h	This bit enables control of decimation filter mode via the DECFIL MODE[3:0] register bits. 0 = Default 1 = Decimation modes control is enabled
2-0	0	R/W	0h	Must write 0

7.5.2.4.8 Register 4Eh (address = 4Eh), Main Digital Page (6800h)

Figure 61. Register 4Eh

7	6	5	4	3	2	1	0
CTRL NYQUIST	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 41. Register 4Eh Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL NYQUIST	R/W	0h	This bit enables selecting the Nyquist zone using register 42h, bits 2-0. 0 = Selection disabled 1 = Selection enabled
6-0	0	R/W	0h	Must write 0

7.5.2.4.9 Register 52h (address = 52h), Main Digital Page (6800h)

Figure 62. Register 52h

7	6	5	4	3	2	1	0
DEC LANE EN	0	0	0	0	0	0	DIG GAIN EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 42. Register 52h Field Descriptions

Bit	Field	Type	Reset	Description
7	DEC LANE EN	R/W	0h	When using on-chip decimation, this bit must be set to enable output data transmission with fewer lanes. This bit works in conjunction with DEC LANE0 (register 73) and DEC LANE1 (register 72). 0 = Lane reduction disabled (when not using decimation) 1 = Lane reduction enabled (used with decimation)
6-1	0	R/W	0h	Must write 0
0	DIG GAIN EN	R/W	0h	Enables selecting the digital gain for 44h. 0 = Digital gain disabled 1 = Digital gain enabled

7.5.2.4.10 Register 68h (address = 68h), Main Digital Page (6800h)

Figure 63. Register 68h

7	6	5	4	3	2	1	0
0	LOOP EN	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 43. Register 68h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	Must write 0
6	LOOP EN	R/W	0h	This bit enables the analog correction loop. CTRL LOOP EN (register 4Dh, bit 5) must be enabled. 0 = Analog loop correction disabled 1 = Analog loop correction enabled
5-0	0	R/W	0h	Must write 0

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7.5.2.4.11 Register 72h (address = 72h), Main Digital Page (6800h)

Figure 64. Register 72h

7	6	5	4	3	2	1	0
DEC LANE1	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 44. Register 72h Field Descriptions

Bit	Field	Type	Reset	Description
7	DEC LANE1	R/W	0h	This bit enables lane 1 for data output with decimation. Used with all decimation modes. This setting applies only for decimation output and not in bypass mode. DEC LANE EN (register 52) must be enabled. 0 = Lane 1 disabled with decimation 1 = Lane 1 output enabled with decimation
6-1	0	R/W	0h	Must write 0

7.5.2.4.12 Register 73h (address = 73h), Main Digital Page (6800h)

Figure 65. Register 73h

7	6	5	4	3	2	1	0
0	0	0	0	DEC LANE0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 45. Register 73h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must write 0
3	DEC LANE0	R/W	0h	This bit enables lane 0 for data output with decimation. Used only with decimation options that use a two-lane output (lanes 0 and 1), such as 2X decimation and 4X decimation (IQ). This setting applies only for decimation output and not in bypass mode. DEC LANE EN (register 52) must be enabled. 0 = Lane 0 disabled with decimation 1 = Lane 0 output enabled with decimation
2-0	0	R/W	0h	Must write 0

7.5.2.4.13 Register ADh (address = ADh), Main Digital Page (6800h)

Figure 66. Register ADh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LSB SELECT	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 46. Register ADh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0h	Must write 0
1-0	LSB SELECT	R/W	0h	Enables output of the FOVR flag instead of output data LSB. 00 = Output is 16-bit data 11 = Output data LSB is replaced by the FOVR info for each channel.

7.5.2.4.14 Register F7h (address = F7h), Main Digital Page (6800h)

Figure 67. Register F7h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DIG RESET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 47. Register F7h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0h	Must write 0
0	DIG RESET	R/W	0h	Self-clearing reset for the digital block. Does not include the interleaving correction. 0 = Normal operation 1 = Digital reset

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7.5.2.5 Interleaving Engine Page (6100h) Registers

7.5.2.5.1 Register 18h (address = 18h), Interleaving Engine Page (6100h)

Figure 68. Register 18h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	IL BYPASS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 48. Register 18h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0h	Must write 0
0	IL BYPASS	R/W	0h	To output the ADC test patterns properly, bypass the interleaving engine. Set this bit along with the DC CORR DIS and CTRL DC CORR register bits. 00 = Interleaving correction enabled 11 = Interleaving correction bypassed

7.5.2.5.2 Register 68h (address = 68h), Interleaving Engine Page (6100h)

Figure 69. Register 68h

7	6	5	4	3	2	1	0
0	0	0	0	0	DC CORR DIS	CTRL DC CORR	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 49. Register 68h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0h	Must write 0
2	DC CORR DIS	R/W	0h	To output the ADC test patterns properly, bypass the interleaving engine. Set this bit along with the IL BYPASS and CTRL DC CORR register bits. 0 = DC offset correction enabled 1 = DC offset correction disabled
1	CTRL DC CORR	R/W	0h	To output the ADC test patterns properly, bypass the interleaving engine. Set this bit along with the IL BYPASS and DC CORR DIS register bits. 0 = DC offset correction control disabled 1 = DC offset correction control enabled
0	0	R/W	0h	Must write 0

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7.5.2.6 JESD Digital Page (6900h) Registers

7.5.2.6.1 Register 0h (address = 0h), JESD Digital Page (6900h)

Figure 70. Register 0h

7	6	5	4	3	2	1	0
CTRL K	0	0	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TX LINK DIS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 50. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL K	R/W	0h	Enable bit for a number of frames per multi frame. 0 = Default is five frames per multi frame 1 = Frames per multi frame can be set in register 06h
6-5	0	R/W	0h	Must write 0
4	TESTMODE EN	R/W	0h	This bit generates the long transport layer test pattern mode, as per section 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled
3	FLIP ADC DATA	R/W	0h	0 = Normal operation 1 = Output data order is reversed: MSB to LSB.
2	LANE ALIGN	R/W	0h	This bit inserts the lane alignment character (K28.3) for the receiver to align to lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts lane alignment characters
1	FRAME ALIGN	R/W	0h	This bit inserts the lane alignment character (K28.7) for the receiver to align to lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts frame alignment characters
0	TX LINK DIS	R/W	0h	This bit disables sending the initial link alignment (ILA) sequence when $\overline{SYNC}$ is de-asserted. 0 = Normal operation 1 = ILA disabled

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7.5.2.6.2 Register 1h (address = 1h), JESD Digital Page (6900h)

Figure 71. Register 1h

7	6	5	4	3	2	1	0
SYNC REG	SYNC REG EN	JESD FILTER			JESD MODE		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 51. Register 1h Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC REG	R/W	0h	Register control for sync request. 0 = Normal operation 1 = ADC output data are replaced with K28.5 characters. Register bit SYNC REG EN must also be set to 1.
6	SYNC REG EN	R/W	0h	Enables register control for sync request 0 = Use the $\overline{\text{SYNC}}$ pin for sync requests 1 = Use the SYNC REG register bit for sync requests
5-3	JESD FILTER	R/W	0h	Enable bits for SYNC operation. 000 = Filter bypass mode 100 = Decimate-by-4 110 = Decimate-by-2 111 = Decimate-by-4 complex (IQ) All others = Not used
2-0	JESD MODE	R/W	0h	These bits select the number of serial JESD output lanes per ADC. The JESD PLL MODE register (JESD ANALOG page, register 16h) must be set accordingly. 001 = 20X mode, four lanes per ADC 010 = 40X mode, two lanes per ADC 100 = 40X mode, LMFS = 4211 only All others = Not used

7.5.2.6.3 Register 2h (address = 2h), JESD Digital Page (6900h)

Figure 72. Register 2h

7	6	5	4	3	2	1	0
LINK LAYER TESTMODE			LINK LAYER RPAT	LMFC MASK RESET	0	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 52. Register 2h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LINK LAYER TESTMODE	R/W	0h	These bits generate a pattern according to clause 5.3.3.8.2 of the JESD204B document. 000 = Normal ADC data 001 = D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed-frequency jitter pattern) 011 = Repeat initial lane alignment (generates a K28.5 character and continuously repeats lane alignment sequences) 100 = 12 octet RPAT jitter pattern All others = Not used
4	LINK LAYER RPAT	R/W	0h	This bit changes the running disparity in the modified RPAT pattern test mode (only when the link layer test mode = 100). 0 = Normal operation 1 = Changes disparity
3	LMFC MASK RESET	R/W	0h	Mask LMFC reset coming to digital block. 0 = LMFC reset is not masked 1 = Ignore LMFC reset request
2-0	0	R/W	0h	Must write 0

7.5.2.6.4 Register 3h (address = 3h), JESD Digital Page (6900h)

Figure 73. Register 3h

7	6	5	4	3	2	1	0
FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	
R/W-0h	R/W-0h					R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 53. Register 3h Field Descriptions

Bit	Field	Type	Reset	Description
7	FORCE LMFC COUNT	R/W	0h	This bit forces the LMFC count. 0 = Normal operation 1 = Enables using a different starting value for the LMFC counter
6-2	MASK SYSREF	R/W	0h	When SYSREF transmits to the digital block, the LMFC count resets to 0 and K28.5 stops transmitting when the LMFC count reaches 31. The initial value that the LMFC count resets to can be set using LMFC COUNT INIT. In this manner, the receiver can be synchronized early because it receives the LANE ALIGNMENT SEQUENCE early. The FORCE LMFC COUNT register bit must be enabled.
1-0	RELEASE ILANE SEQ	R/W	0h	These bits delay the generation of the lane alignment sequence by 0, 1, 2 or 3 multi frames after the code group synchronization. 00 = 0 01 = 1 10 = 2 11 = 3

7.5.2.6.5 Register 5h (address = 5h), JESD Digital Page (6900h)

Figure 74. Register 5h

7	6	5	4	3	2	1	0
SCRAMBLE EN	0	0	0	0	0	0	0
R/W-Undefined	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 54. Register 5h Field Descriptions

Bit	Field	Type	Reset	Description
7	SCRAMBLE EN	R/W	Undefined	Scramble enable bit in the JESD204B interface. 0 = Scrambling disabled 1 = Scrambling enabled
6-0	0	R/W	0h	Must write 0

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7.5.2.6.6 Register 6h (address = 6h), JESD Digital Page (6900h)

Figure 75. Register 6h

7	6	5	4	3	2	1	0
0	0	0	FRAMES PER MULTI FRAME (K)				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 55. Register 6h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0h	Must write 0
4-0	FRAMES PER MULTI FRAME (K)	R/W	0h	These bits set the number of multi frames. Actual K is the value in hex + 1 (that is, 0Fh is K = 16).

7.5.2.6.7 Register 7h (address = 7h), JESD Digital Page (6900h)

Figure 76. Register 7h

7	6	5	4	3	2	1	0
0	0	0	0	SUBCLASS	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 56. Register 7h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must write 0
3	SUBCLASS	R/W	0h	This bit sets the JESD204B subclass. 000 = Subclass 0 backward compatible with JESD204A 001 = Subclass 1 deterministic latency using the SYSREF signal
2-0	0	R/W	0h	Must write 0

7.5.2.6.8 Register 16h (address = 16h), JESD Digital Page (6900h)

Figure 77. Register 16h

7	6	5	4	3	2	1	0
1	0	LANE SHARE	0	0	0	0	0
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 57. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
7	1	R/W	1h	Must write 1
6	0	R/W	0h	Must write 0
5	LANE SHARE	R/W	0h	When using decimate-by-4, the data of both channels are output over one lane (LMFS = 1241). 0 = Normal operation (each channel uses one lane) 1 = Lane sharing is enabled, both channels share one lane (LMFS = 1241)
4-0	0	R/W	0h	Must write 0

7.5.2.7 JESD Analog Page (6A00h) Register

7.5.2.7.1 Register 12h-5h (address = 12h-5h), JESD Analog Page (6A00h)

Figure 78. Register 12h

7	6	5	4	3	2	1	0
SEL EMP LANE 1						0	0
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Figure 79. Register 13h

7	6	5	4	3	2	1	0
SEL EMP LANE 0						0	0
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Figure 80. Register 14h

7	6	5	4	3	2	1	0
SEL EMP LANE 2						0	0
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Figure 81. Register 15h

7	6	5	4	3	2	1	0
SEL EMP LANE 3						0	0
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 58. Register 12h-15h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	SEL EMP LANE 1, 0, 2, or 3	R/W	0h	Selects the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 = 0 dB 1 = –1 dB 3 = –2 dB 7 = –4.1 dB 15 = –6.2 dB 31 = –8.2 dB 63 = –11.5 dB
1-0	0	R/W	0h	Must write 0

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7.5.2.7.2 Register 16h (address = 16h), JESD Analog Page (6A00h)

Figure 82. Register 16h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	JESD PLL MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 59. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0h	Must write 0
1-0	JESD PLL MODE	R/W	0h	These bits select the JESD PLL multiplication factor and must match the JESD MODE setting. 00 = 20X mode, four lanes per ADC 01 = Not used 10 = 40X mode, two lanes per ADC 11 = Not used

7.5.2.7.3 Register 1Ah (address = 1Ah), JESD Analog Page (6A00h)

Figure 83. Register 1Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FOVR CHA	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 60. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0h	Must write 0
1	FOVR CHA	R/W	0h	Outputs FOVR signal for channel A on the PDN pin. FOVR CHA EN (register 1Bh, bit 3) must be enabled. 0 = Normal operation 1 = FOVR on the PDN pin
0	0	R/W	0h	Must write 0

7.5.2.7.4 Register 1Bh (address = 1Bh), JESD Analog Page (6A00h)

Figure 84. Register 1Bh

7	6	5	4	3	2	1	0
JESD SWING			0	FOVR CHA EN	0	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 61. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-5	JESD SWING	R/W	0h	Selects output amplitude VOD (mVpp) of the JESD transmitter (for all lanes) 0 = 860 mVpp 1 = 810 mVpp 2 = 770 mVpp 3 = 745 mVpp 4 = 960 mVpp 5 = 930 mVpp 6 = 905 mVpp 7 = 880 mVpp
4	0	R/W	0h	Must write 0
3	FOVR CHA EN	R/W	0h	Enables overwrite of PDN pin with the FOVR signal from ChA. 0 = Normal operation 1 = PDN is being overwritten
2-0	JESD PLL MODE	R/W	0h	Must write 0

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Start-Up Sequence

The steps described in Table 62 are recommended as the power-up sequence with the ADS54J60 in 20X mode (LMFS = 8224).

Table 62. Recommended Power-Up Sequence

STEP	DESCRIPTION	REGISTER ADDRESS	REGISTER DATA	COMMENT
1	Supply all supply voltages. A power-supply sequence is not required for the 1.2-V, 1.9-V, and 3.0-V supplies; these supply voltages can be supplied in any order.	—	—	—
2	Pulse a hardware reset (low to high to low) on pin 48.	—	—	—
3	Apply SYSREF signal			
4	Issue a software reset.	6000h 6000h	01h 00h	Digital software resets do not self-clear, thus a reset must be set and cleared for channels A and B.
5	Set the default registers for the digital JESD bank.	4003h 4004h 6000h 6006h	00h 69h 80h 0Fh	Set the CTRL K for channels A and B. (Set K = 16.)
6	Pulse the $\overline{\text{SYNC}}$ pin from low to high to transmit data from the K28.5 characters (TBD).	—	—	—

8.1.2 Hardware Reset

Figure 85 and Table 63 illustrate the timing for a hardware reset.

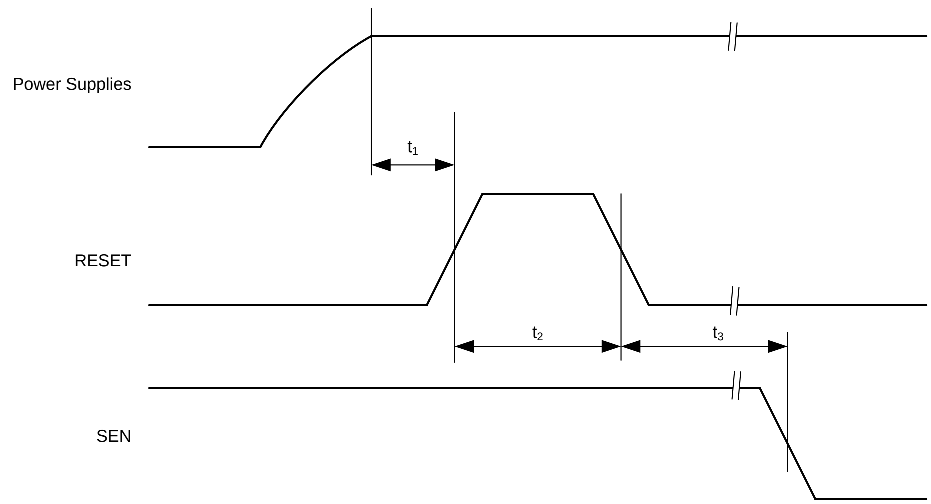

Figure 85. Hardware Reset Timing Diagram

Table 63. Timing Requirements for Figure 85

		MIN	TYP	MAX	UNIT
t_1	Power-on delay: delay from power up to active high RESET pulse	1			ms
t_2	Reset pulse duration: active high RESET pulse duration	10			ns
t_3	Register write delay: delay from RESET disable to SEN active	100			ns

8.1.3 Test Pattern Output

The steps described in Table 64 are recommended to generate a test pattern output.

Table 64. Steps to Generate a Test Pattern Output

Step	Description	Register Address	Register Data	Comment
To enable test patterns				
1	Bypass the interleaving engine.	4003h 4004h 6018h 6068h	00h 61h 03h 04h	—
2	Select the test pattern (see the test pattern description for register 74h).	0011h 0074h	0Fh 20h	Select all 1s
To enable normal data output				
3	Enable the interleaving engine.	4003h 4004h 6018h 6068h	00h 61h 00h 02h	—
4	Select normal ADC data.	0011h 0074h	0Fh 00h	—

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8.1.4 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors: quantization noise, thermal noise, and jitter, as shown in Equation 4. The quantization noise is typically not noticeable in pipeline converters and is 98 dB for a 16-bit ADC. The thermal noise limits the SNR at low input frequencies and the clock jitter sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20log\sqrt{\left(10^{-\frac{SNR_{Quantization\,Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\,Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \tag{4}$$

The SNR limitation resulting from sample clock jitter can be calculated by Equation 5:

$$SNR_{Jitter}[dBc] = -20log(2\pi \times f_{in} \times T_{Jitter}) \tag{5}$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (130 fs) is set by the noise of the clock input buffer and the external clock jitter. T_{Jitter} can be calculated by Equation 6:

$$T_{Jitter} = \sqrt{(T_{Jitter,\ Ext\_Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \tag{6}$$

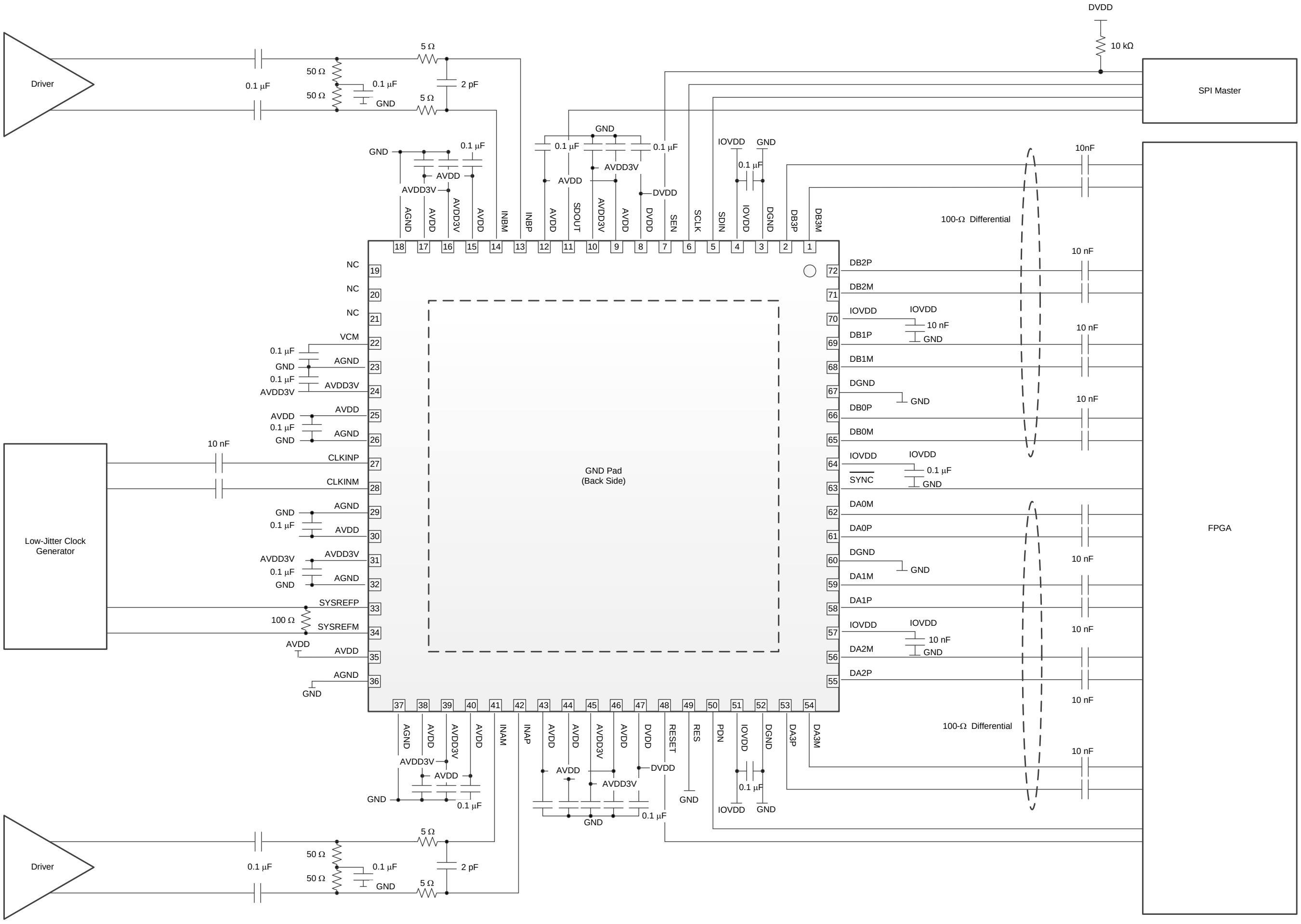
External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input. A faster clock slew rate also improves the ADC aperture jitter.

The ADS54J60 has a thermal noise of approximately 71.1 dBFS and an internal aperture jitter of 130 fs. The SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 86.

Figure 86. SNR versus Input Frequency and External Clock Jitter

8.2 Typical Application

The ADS54J60 is designed for wideband receiver applications demanding excellent dynamic range over a large input frequency range. A typical schematic for an ac-coupled receiver is shown in Figure 87.



NOTE: GND = AGND and DGND connected in the PCB layout.

Figure 87. AC-Coupled Receiver

8.2.1 Design Requirements

By using the simple drive circuit of Figure 87, uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

8.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics, as shown in Figure 87.

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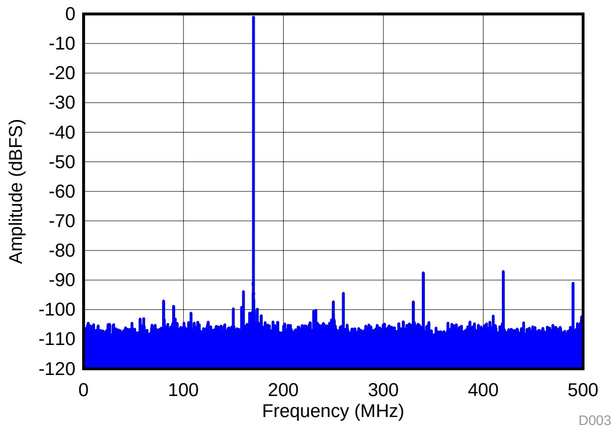
Typical Application (continued)

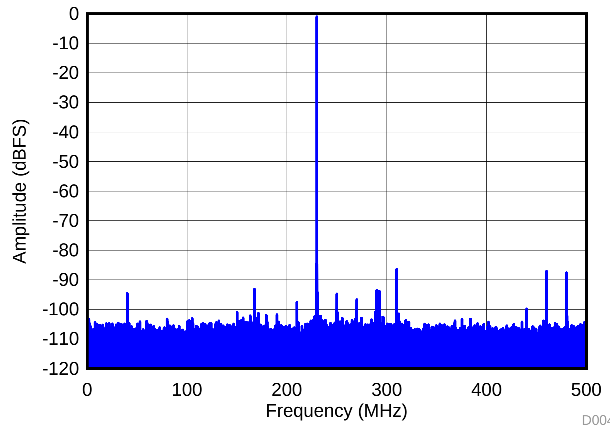
8.2.3 Application Curves

Figure 88 and Figure 89 show the typical performance at 170 MHz and 230 MHz, respectively.



SNR = 70 dBFS; SFDR = 86 dBc;
IL spur = 87 dBc; non HD2, HD3 spur = 96 dBc

Figure 88. FFT for 170-MHz Input Signal



SNR = 69.5 dBFS; SFDR = 85 dBc;
IL spur = 87 dBc; non HD2, HD3 spur = 93 dBc

Figure 89. FFT for 230-MHz Input Signal

9 Power Supply Recommendations

The device requires a 1.8-V nominal supply for DRVDD, a 1.9-V nominal supply for AVDD, and a 3.0-V nominal supply for AVDD3V. There is no specific sequence for power-supply requirements during device power-up. AVDD, DRVDD, and AVDD3V can power-up in any order.

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10 Layout

10.1 Layout Guidelines

The device evaluation module (EVM) layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 90. Complete layout of EVM is available at ADS54J60's EVM folder. Some important points to remember during board layout are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pinout in opposite directions, as shown in the reference layout of Figure 90 as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 90 as much as possible.
- Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD, DRVDD, or AVDDD3V), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

10.2 Layout Example

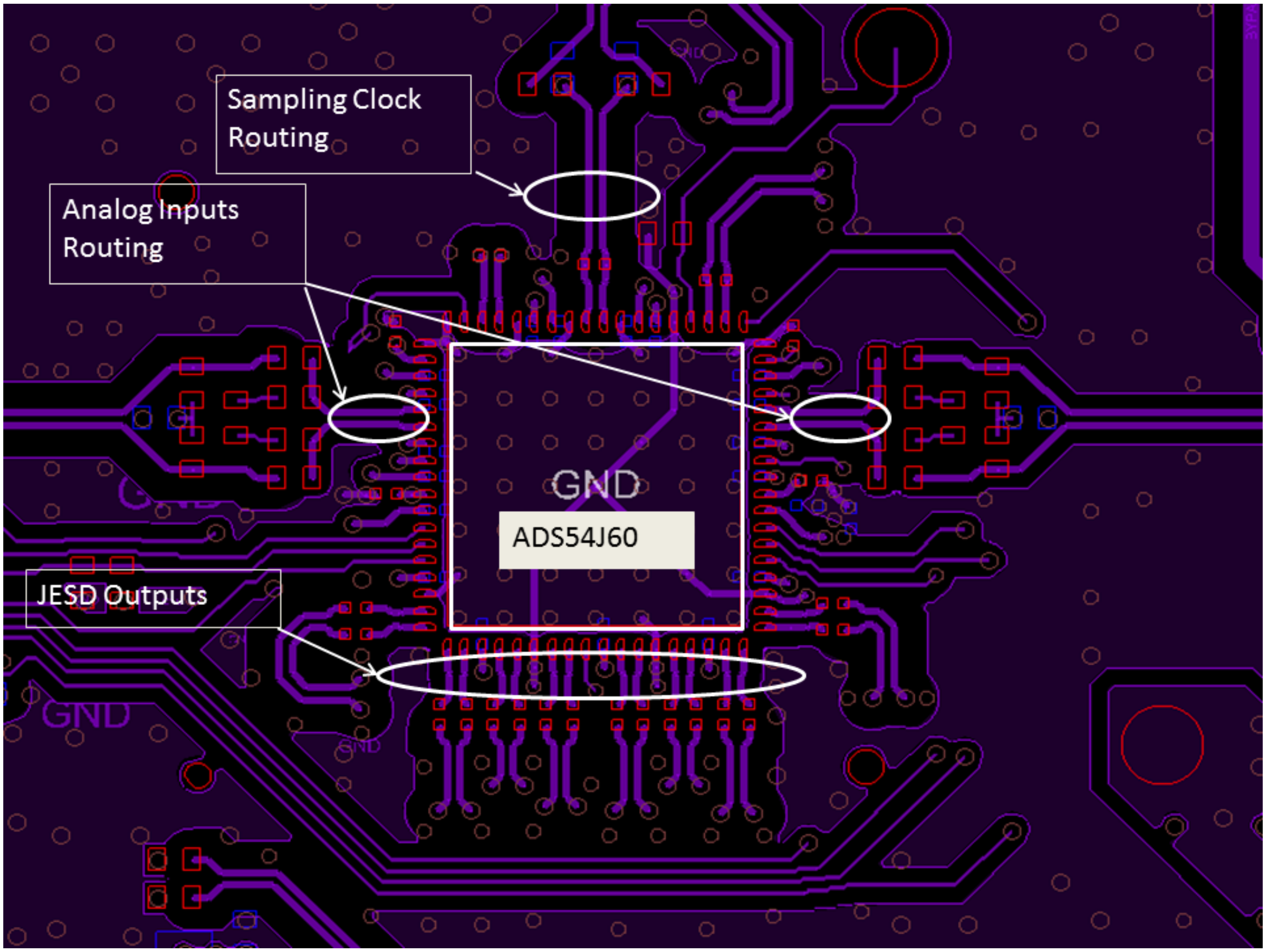

Figure 90. ADS54J60 EVM layout

11 Device and Documentation Support

11.1 Trademarks

11.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS54J60IRMPR	PREVIEW	VQFN	RMP	72	2000	TBD	Call TI	Call TI	-40 to 85		
ADS54J60IRMPT	PREVIEW	VQFN	RMP	72	250	TBD	Call TI	Call TI	-40 to 85		
PADS54J60IRMPT	PREVIEW	VQFN	RMP	72	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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