

ADS54J40 Dual-Channel, 14-Bit, 1.0-GSPS Analog-to-Digital Converter

1 Features

- 14-Bit Resolution, Dual-Chanel, 1-GSPS ADC
- Noise Floor: -158 dBFS/Hz
- Spectral Performance ($f_{IN} = 170$ MHz at -1 dBFS):
 - SNR: 68.0 dBFS
 - NSD: -155 dBFS/Hz
 - SFDR: 86 dBc
 - SFDR: 96 dBc (Except HD2, HD3, and Interleaving Tones)
- Spectral Performance ($f_{IN} = 350$ MHz at -1 dBFS):
 - SNR: 66.3 dBFS
 - NSD: -153.3 dBFS/Hz
 - SFDR: 75 dBc
 - SFDR: 85 dBc (Except HD2, HD3, and Interleaving Tones)
- Channel Isolation: 100 dBc at $f_{IN} = 170$ MHz
- Input Full-Scale: $1.9 V_{PP}$
- Input Bandwidth (3 dB): 1.2 GHz
- On-Chip Dither
- Integrated Wideband DDC Block
- JESD204B Interface with Subclass 1 Support:
 - 2 Lanes per ADC at 10.0 Gbps
 - 4 Lanes per ADC at 5.0 Gbps
 - Support for Multi-Chip Synchronization
- Power Dissipation: 1.30 W/ch at 1 GSPS
- VQFN-72 Package (10 mm x 10 mm)

2 Applications

- Radar and Antenna Arrays
- Broadband Wireless
- Cable Infrastructure
- Communications Test Equipment
- Microwave Receivers

3 Description

The ADS54J40 is a low-power, wide-bandwidth, 14-bit, 1.0-GSPS, dual-channel, analog-to-digital converter (ADC). Designed for high signal-to-noise ratio (SNR), the device delivers a noise floor of -158 dBFS/Hz for applications aiming for highest dynamic range over a wide instantaneous bandwidth. The device supports the JESD204B serial interface with data rates up to 10.0 Gbps, supporting two or four lanes per ADC. The buffered analog input provides uniform input impedance across a wide frequency range and minimizes sample-and-hold glitch energy. Each ADC channel optionally can be connected to a wideband digital down-converter (DDC) block. The ADS54J40 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with very low power consumption.

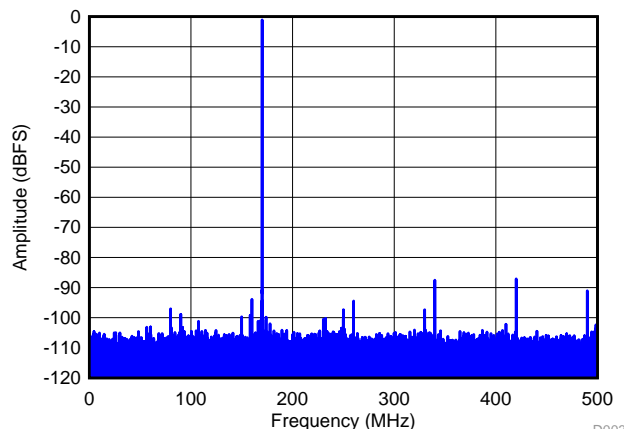
The JESD204B interface reduces the number of interface lines, allowing high system integration density. An internal phase-locked loop (PLL) multiplies the ADC sampling clock to derive the bit clock that is used to serialize the 14-bit data from each channel.

Device Information

PART NUMBER	SPEED GRADE (MSPS)	RESOLUTION (Bits)
ADS54J40	1000	14
ADS54J60	1000	16
ADS54J69	500	16

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**FFT for 170-MHz Input Signal
(SNR = 68.5 dBFS; SFDR = 86 dBc;
IL Spur = 87 dBc; Non HD2, HD3 Spur = 96 dBc)**



D003



4 Device and Documentation Support

4.1 Trademarks

4.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS54J40IRMPR	PREVIEW	VQFN	RMP	72	2000	TBD	Call TI	Call TI	-40 to 85		
ADS54J40IRMPT	PREVIEW	VQFN	RMP	72	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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