

## Quad Channel 16-Bit, 100-MSPS High-SNR ADC

Check for Samples: [ADS5263](#)

### FEATURES

- **Maximum Sample Rate: 100 MSPS**
- **Programmable Device Resolution**
  - Quad-Channel, 16-Bit, High-SNR Mode
  - Quad-Channel, 14-Bit, Low-Power Mode
- **16-Bit High-SNR Mode**
  - **1.4 W Total Power at 100 MSPS**
    - 355 mW / Channel
  - **4 Vpp Full-scale Input**
  - **85-dBFS SNR at  $f_{in} = 3$  MHz, 100 MSPS**
- **14-Bit Low-Power Mode**
  - **785 mW Total Power at 100 MSPS**
    - 195 mW/Channel
  - **2-Vpp Full-Scale Input**
  - **74-dBFS SNR at  $f_{in} = 10$  MHz**
  - **Integrated Clamp (for interfacing to CCD sensors)**
- **Low-Frequency Noise Suppression**
- **Digital Processing Block**
  - **Programmable FIR Decimation Filters**
  - **Programmable Digital Gain: 0 dB to 12 dB**
  - **2- or 4-Channel Averaging**
- **Programmable Mapping Between ADC Input Channels and LVDS Output Pins—Eases Board Design**
- **Variety of Test Patterns to Verify Data Capture by FPGA/Receiver**
- **Serialized LVDS Outputs**
- **Internal and External References**
- **3.3-V Analog Supply**
- **1.8-V Digital Supply**
- **Recovers From 6-dB Overload Within 1 Clock Cycle**
- **Package:**
  - **9-mm x 9-mm 64-Pin QFN**
  - **Non-magnetic package option for MRI systems**
- **CMOS Technology**

### APPLICATIONS

- **Medical Imaging – MRI**
- **Spectroscopy**
- **CCD Imaging**

### DESCRIPTION

Using CMOS process technology and innovative circuit techniques, the ADS5263 is designed to operate at low power and give very high SNR performance with a 4-Vpp full-scale input. Using a low-noise 16-bit front-end stage followed by a 14-bit ADC, the device gives 85-dBFS SNR up to 10 MHz and better than 80-dBFS SNR up to 30 MHz.

The device also has a 14-bit low power mode, where it operates as a quad-channel 14-bit ADC. The 16-bit front-end stage is powered down and the part consumes almost half the power, compared to the 16-bit mode. The 14-bit mode supports a 2-Vpp full-scale input signal, with typical 74-dBFS SNR. The ADS5263 can be dynamically switched between the two resolution modes. This allows systems to use the same part in a high-resolution, high-power mode or a low-resolution, low-power mode.

The ADS5263 has a digital processing block that integrates several commonly used digital functions, such as digital gain (up to 12 dB). It includes a digital filter module that has built-in decimation filters (with low-pass, high-pass and band-pass characteristics). The decimation rate is also programmable (by 2, by 4, or by 8). This makes it very useful for narrow-band applications, where the filters can be used to improve SNR and knock-off harmonics, while at the same time reducing the output data rate.

The device includes an averaging mode where two channels (or even four channels) can be averaged to improve SNR. A very unique feature is the programmable mapper module that allows flexible mapping between the input channels and the LVDS output pins. This helps to greatly reduce the complexity of LVDS output routing and can potentially result in cheaper system boards by reducing the number of PCB layers.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

The data from each channel ADC is serialized and output on two pairs of LVDS output lines, along with a bit clock and a frame clock. Serial LVDS outputs reduce the number of interface lines. This, together with the low-power design, enables four channels to be packaged in a compact 9-mm × 9-mm QFN, allowing high system integration densities.

In order to ease interfacing to CCD sensors, a clamp function is integrated in the device. Using this feature, the analog input pins can be clamped to an internal voltage, based on a SYNC signal. With this, the CCD sensor output can be easily ac-coupled to the ADS5263 analog inputs. The clamp feature and quad channels in a compact package make the ADS5263 attractive for industrial CCD imaging applications.

The device integrates an internal reference trimmed to accurately match across devices. Additionally, the device supports an external reference mode for applications that require very low temperature drift of reference. The ADS5263 is available in a non-magnetic QFN package that does not create any MRI signature. The device is specified over the full industrial temperature range.

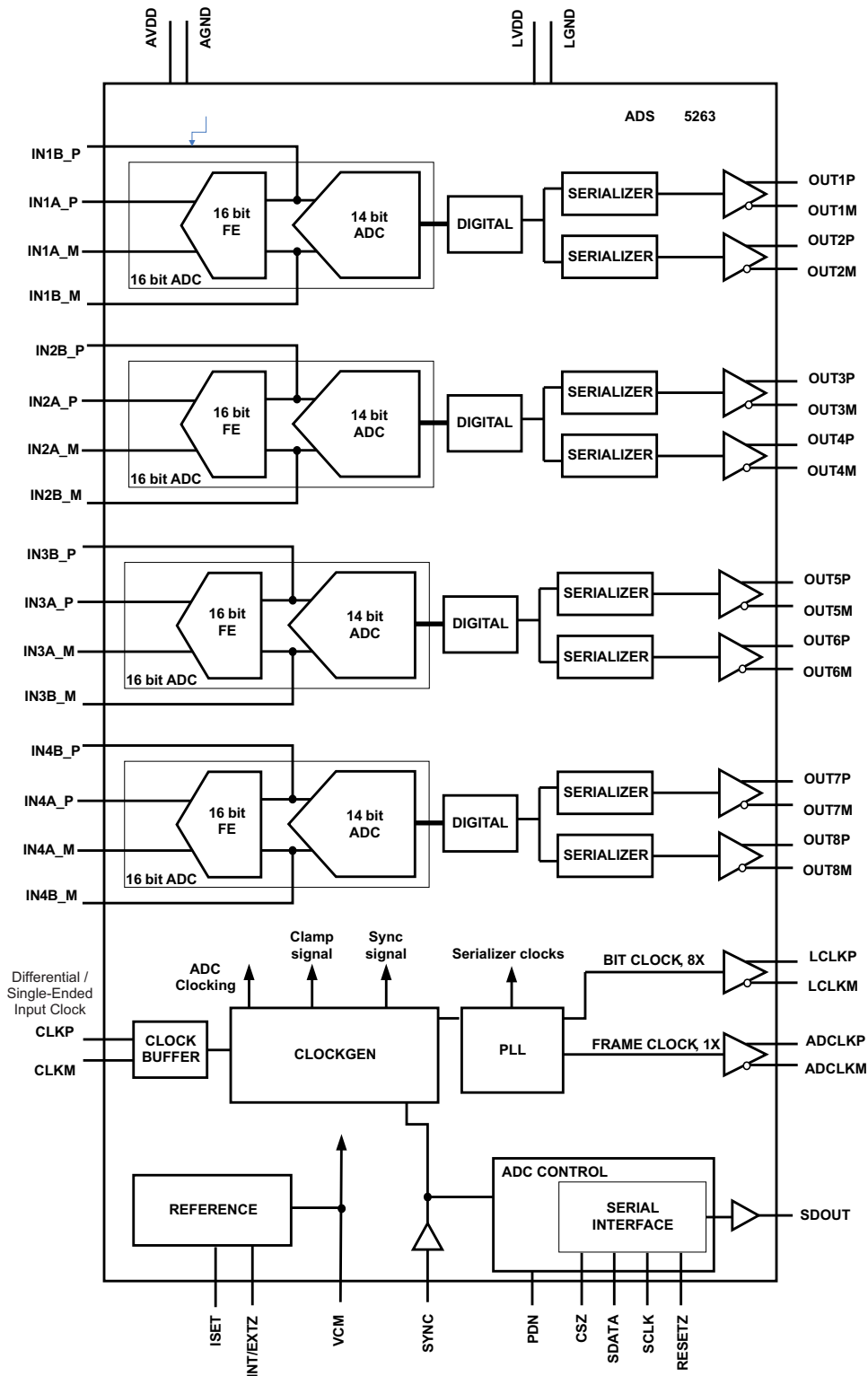


Figure 1. ADS5263 Block Diagram

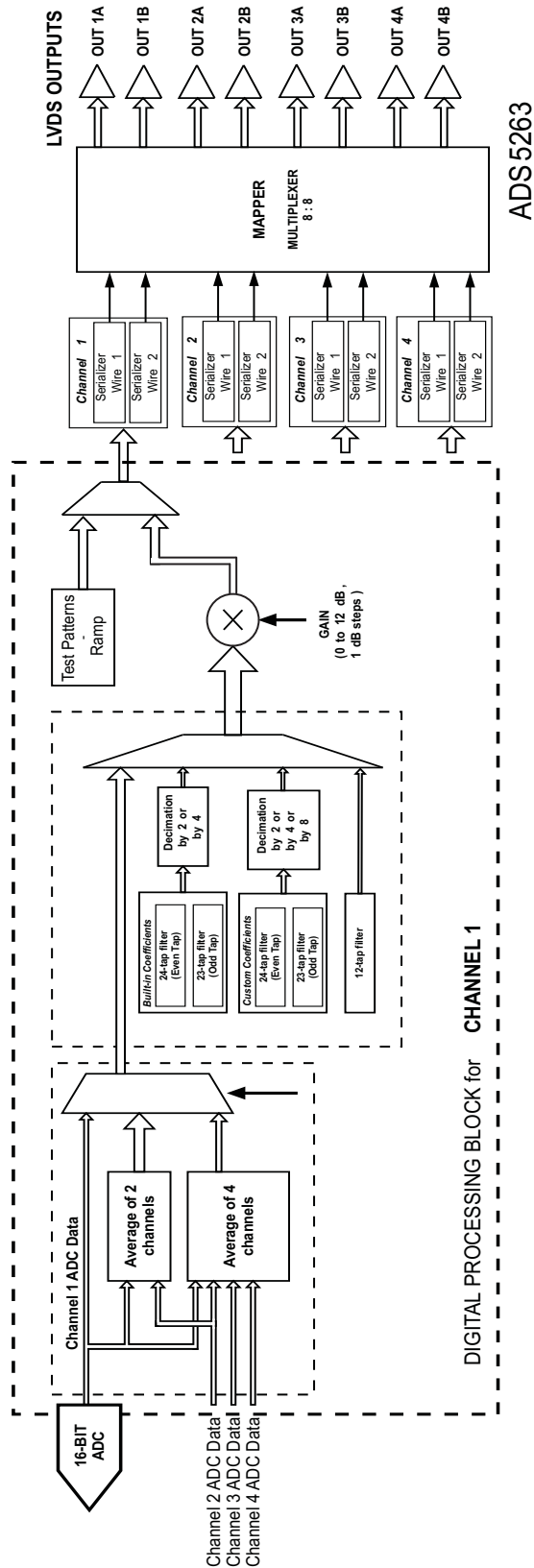
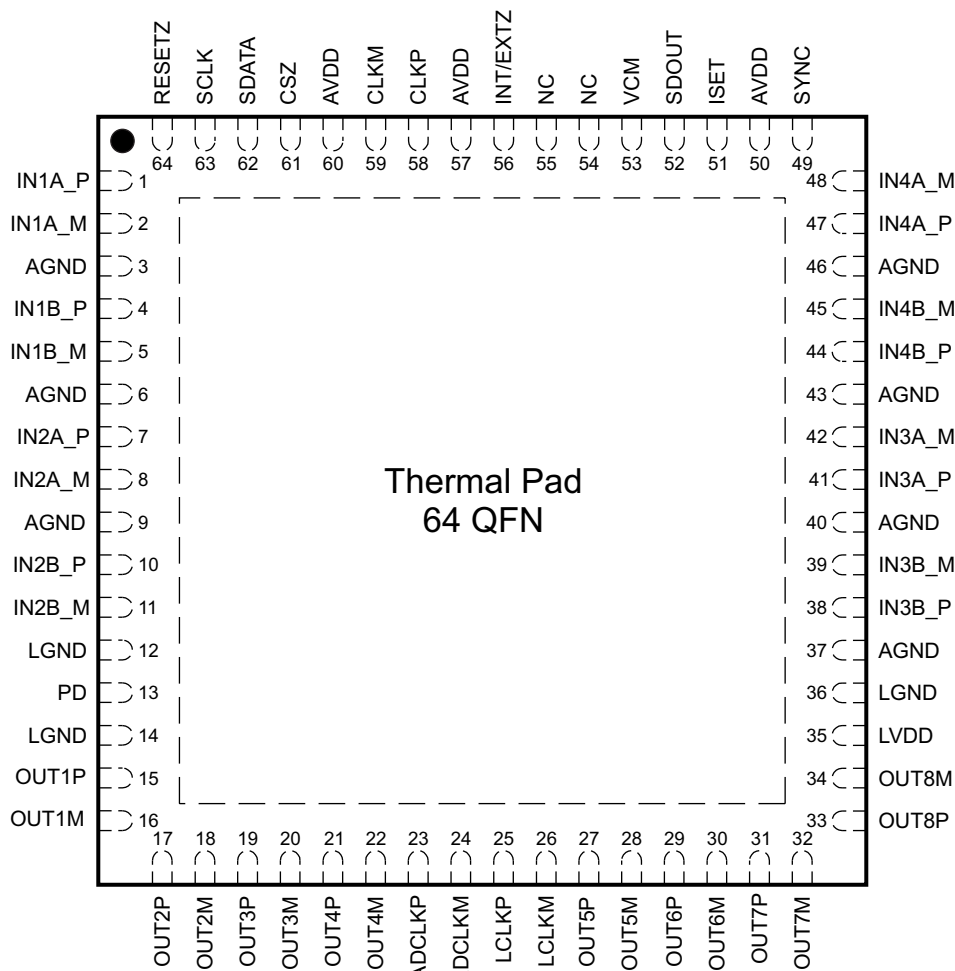


Figure 2. ADS5263 Digital Processing Block

**PIN CONFIGURATION – ADS5263  
64 QFN (THERMAL PAD)  
RGC Package  
(Top View)**



P0056-19

**PIN FUNCTIONS**

| PIN NAME        | DESCRIPTION  | PIN  |                         | NO. OF PINS |
|-----------------|--|------|-------------------------|-------------|
|                 |  | TYPE | NO.                     |             |
| ADCLKM          | LVDS frame clock (1X) – negative output  | O    | 24                      |             |
| ADCLKP          | LVDS frame clock (1X) – positive output  | O    | 23                      |             |
| AGND            | Analog ground  | I    | 3, 6, 9, 37, 40, 43, 46 | 7           |
| AVDD            | Analog power supply, 3.3 V   | I    | 50, 57, 60              | 3           |
| CLKM            | Negative differential clock input. For single-ended clock, tie CLKM to ground.                                 | I    | 59                      | 1           |
| CLKP            | Positive differential clock input  | I    | 58                      | 1           |
| $\overline{CS}$ | Serial interface enable input, active LOW. The pin has an internal 300-k $\Omega$ pull-down resistor to ground | I    | 61                      | 1           |
| IN1A_P, IN1A_M  | Differential analog input for channel 1, 16 bit ADC  | I    | 1, 2                    | 2           |
| IN1B_P, IN1B_M  | Differential analog input for channel 1, 14 bit ADC  | I    | 4, 5                    | 2           |
| IN2A_P, IN2A_M  | Differential analog input for channel 2, 16 bit ADC  | I    | 7, 8                    | 2           |
| IN2B_P, IN2B_M  | Differential analog input for channel 2, 14 bit ADC  | I    | 10, 11                  | 2           |
| IN3A_P, IN3A_M  | Differential analog input for channel 3, 16 bit ADC  | I    | 41, 42                  | 2           |
| IN3B_P, IN3B_M  | Differential analog input for channel 3, 14 bit ADC  | I    | 38, 39                  | 2           |
| IN4A_P, IN4A_M  | Differential analog input for channel 4, 16 bit ADC  | I    | 47, 48                  | 2           |

**PIN FUNCTIONS (continued)**

| PIN NAME       | DESCRIPTION  | PIN  |            | NO. OF PINS |
|----------------|--|------|------------|-------------|
|                |  | TYPE | NO.        |             |
| IN4B_P, IN4B_M | Differential analog input for channel 4, 14 bit ADC  | I    | 44, 45     | 2           |
| INT/EXT        | Internal/external reference mode select input<br>Logic HIGH – internal reference<br>Logic LOW – external reference   | I    | 56         | 1           |
| ISET           | Bias pin – 56.2 kΩ resistor (1% tolerance value) to ground   | I    | 51         | 1           |
| LCLKM          | LVDS bit clock (8X) – negative output  | O    | 26         | 1           |
| LCLKP          | LVDS bit clock (8X) – positive output  | O    | 25         | 1           |
| LGND           | Digital ground   | I    | 12, 14, 36 | 3           |
| LVDD           | Digital and I/O power supply, 1.8 V  | I    | 35         | 1           |
| OUT1P, OUT1M   | Wire 1, channel 1 LVDS differential output   | O    | 15, 16     | 2           |
| OUT2P, OUT2M   | Wire 2, channel 1 LVDS differential output   | O    | 17, 18     | 2           |
| OUT3P, OUT3M   | Wire 1, channel 2, LVDS differential output  | O    | 19, 20     | 2           |
| OUT4P, OUT4M   | Wire 2, channel 2 LVDS differential output   | O    | 21, 22     | 2           |
| OUT5P, OUT5M   | Wire 1, channel 3 LVDS differential output   | O    | 27, 28     | 2           |
| OUT6P, OUT6M   | Wire 2, channel 3 LVDS differential output   | O    | 29, 30     | 2           |
| OUT7P, OUT7M   | Wire 1, channel 4 LVDS differential output   | O    | 31, 32     | 2           |
| OUT8P, OUT8M   | Wire 2, channel 4 LVDS differential output   | O    | 33, 34     | 2           |
| PD             | Power-down input   | I    | 13         | 1           |
| NC             | Do not connect   |      | 54, 55     | 2           |
| RESET          | Serial interface RESET input, active LOW.<br>When using the serial interface mode, the user <i>must</i> initialize internal registers through hardware RESET by applying a low-going pulse on this pin or by using software reset option. See the <i>Serial Interface</i> section. | I    | 64         | 1           |
| SCLK           | Serial interface clock input. The pin has an internal 300-kΩ pull-down resistor.   | I    | 63         | 1           |
| SDATA          | Serial interface data input. The pin has an internal 300-kΩ pull-down resistor.  | I    | 62         | 1           |
| SDOUT          | Serial register readout<br>This pin is in the high-impedance state after reset. When the <READOUT> bit is set, the SDOOUT pin becomes active. This is a CMOS digital output running from the AVDD supply.  | O    | 52         | 1           |
| SYNC           | Input signal to synchronize channels and chips when used with reduced output data rates<br><b>Alternate function:</b> Clamp signal input (14-bit ADC mode only)  | I    | 49         | 1           |
| VCM            | <b>Internal reference mode:</b> Outputs the common-mode voltage (1.5 V) that can be used externally to bias the analog input.<br><b>External reference mode:</b> Apply voltage input that sets the reference for ADC operation.  | IO   | 53         | 1           |

**PACKAGE/ORDERING INFORMATION<sup>(1)</sup>**

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | LEAD/BALL FINISH | PACKAGE MARKING | ORDERING NUMBER                    | TRANSPORT MEDIA, QTY |
|---------|--------------|--------------------|-----------------------------|------------------|-----------------|------------------------------------|----------------------|
| ADS5263 | QFN-64       | RGC                | -40°C to 85°C               | Cu Matte Sn      | ADS5263         | ADS5263IRGCT<br>ADS5263IRGCR       | Tape and reel        |
|         |              |                    |                             |                  | ADS5263NM       | ADS5263IRGCT-NM<br>ADS5263IRGCR-NM |                      |

(1) Eco Plan – The planned eco-friendly classification:

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

|   | VALUE                                | UNIT |
|---|--------------------------------------|------|
| Supply voltage range, AVDD  | -0.3 V to 3.9                        | V    |
| Supply voltage range, LVDD  | -0.3 V to 2.2                        | V    |
| Voltage between AGND and DRGND  | -0.3 to 0.3                          | V    |
| Voltage applied to analog input pins – INP_A, INM_A, INP_B, INM_B                   | -0.3V to minimum (3.6, AVDD + 0.3 V) | V    |
| Voltage applied to input pins – CLKP, CLKM <sup>(2)</sup> , RESET, SCLK, SDATA, CSZ | -0.3 V to AVDD + 0.3 V               | V    |
| Voltage applied to reference input pins   | -0.3 to 2.8                          | V    |
| Operating free-air temperature range, T <sub>A</sub>                                | -40 to 85                            | °C   |
| Operating junction temperature range, T <sub>J</sub>                                | 125                                  | °C   |
| Storage temperature range, T <sub>stg</sub>   | -65 to 150                           | °C   |
| ESD, human body model   | 2                                    | kV   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- (2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is < |0.3V|. This prevents the ESD protection diodes at the clock input pins from turning on.

**THERMAL INFORMATION**

| THERMAL METRIC <sup>(1)</sup> |  | ADS5263 | UNITS |
|-------------------------------|--|---------|-------|
|                               |  | QFN     |       |
|                               |  | 64 PINS |       |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance       | 20.6    | °C/W  |
| $\theta_{JCTop}$              | Junction-to-case (top) thermal resistance    | 6.1     |       |
| $\theta_{JB}$                 | Junction-to-board thermal resistance         | 2.7     |       |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 0.2     |       |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 2.6     |       |
| $\theta_{JCbott}$             | Junction-to-case (bottom) thermal resistance | 0.4     |       |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

# ADS5263

SLAS760C – MAY 2011 – REVISED JANUARY 2013

[www.ti.com](http://www.ti.com)

## RECOMMENDED OPERATING CONDITIONS

|  |  | MIN      | TYP | MAX | UNIT            |
|--|--|----------|-----|-----|-----------------|
| <b>SUPPLIES</b>                                  |  |          |     |     |                 |
| AVDD   | Analog supply voltage  | 3        | 3.3 | 3.6 | V               |
| LVDD   | Digital supply voltage   | 1.7      | 1.8 | 1.9 | V               |
| <b>ANALOG INPUTS</b>                             |  |          |     |     |                 |
| Differential input voltage range                 | 16-bit ADC mode  | 4        |     |     | V <sub>PP</sub> |
|  | 14-bit ADC mode  | 2        |     |     | V <sub>PP</sub> |
| Input common-mode voltage                        |  | 1.5 ±0.1 |     |     | V               |
| Maximum analog input frequency                   | 4-V <sub>pp</sub> input amplitude, 16-bit ADC mode                     | 70       |     |     | MHz             |
|  | 2-V <sub>pp</sub> input amplitude, 16-bit ADC mode                     | 140      |     |     |                 |
| <b>CLOCK INPUT</b>                               |  |          |     |     |                 |
| Input clock sample rate                          |  | 10       |     | 100 | MSPS            |
| Input clock amplitude differential (VCLKP-VCLKM) | Sine wave, ac-coupled  | 0.2      | 1.5 |     | V <sub>PP</sub> |
|  | LVPECL, ac-coupled   | 0.2      | 1.6 |     | V <sub>PP</sub> |
|  | LVDS, ac-coupled   | 0.2      | 0.7 |     | V <sub>PP</sub> |
|  | LVC MOS, single-ended, ac-coupled                                      | 3.3      |     |     | V               |
| Input clock duty cycle                           |  | 35%      | 50% | 65% |                 |
| <b>DIGITAL OUTPUTS</b>                           |  |          |     |     |                 |
| C <sub>LOAD</sub>                                | Maximum external load capacitance from each output pin to DRGND        | 5        |     |     | pF              |
| R <sub>LOAD</sub>                                | Differential load resistance between the LVDS output pairs (LVDS mode) | 100      |     |     | Ω               |
| Operating free-air temperature, T <sub>A</sub>   |  | -40      |     | 85  | °C              |

**ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE – 16-BIT ADC**

Typical values are at 25°C, AVDD = 3.3V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input (unless otherwise noted).

MIN and MAX values are across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ , AVDD = 3.3 V, LVDD = 1.8 V

| PARAMETERS   | TEST CONDITIONS   | 100 MSPS |      |      | 80 MSPS |     |      | UNITS        |
|--|---|----------|------|------|---------|-----|------|--------------|
|  |   | MIN      | TYP  | MAX  | MIN     | TYP | MAX  |              |
| <b>SNR</b><br>Idle channel noise                     | With inputs tied to common-mode VCM   | 87.5     |      |      | 87.5    |     |      | dBFS         |
| <b>LSB</b><br>Idle channel noise                     | With inputs tied to common-mode VCM   | 0.98     |      |      | 0.98    |     |      | rms          |
| <b>SNR</b><br>Signal-to-noise ratio                  | $f_{in} = 5$ MHz at 25°C  | 81       | 84.5 | 85.5 |         |     | dBFS |              |
|  | $f_{in} = 5$ MHz across temperature   | 80       |      |      |         |     |      |              |
|  | $f_{in} = 10$ MHz   | 84.6     |      | 85.3 |         |     |      |              |
|  | $f_{in} = 30$ MHz   | 82.7     |      | 83.1 |         |     |      |              |
|  | $f_{in} = 65$ MHz   | 78.9     |      | 79.4 |         |     |      |              |
| <b>SINAD</b><br>Signal-to-noise and distortion ratio | $f_{in} = 5$ MHz  | 76.6     | 78.2 | 78.8 |         |     | dBFS |              |
|  | $f_{in} = 10$ MHz   | 77.5     |      | 79   |         |     |      |              |
|  | $f_{in} = 30$ MHz   | 74.8     |      | 76   |         |     |      |              |
|  | $f_{in} = 65$ MHz   | 71.6     |      | 72.5 |         |     |      |              |
| <b>ENOB</b><br>Effective number of bits              | $f_{in} = 5$ MHz  | 12.7     |      |      | 12.8    |     |      | LSB          |
| <b>DNL</b><br>Differential non-linearity             | $f_{in} = 5$ MHz  | ±0.1     |      |      | ±0.1    |     |      | LSB          |
| <b>INL</b><br>Integrated non-linearity               | $f_{in} = 5$ MHz Changed the INL values 100 MSPS From: TYP = ±2.2 To: ±5, Added MAX = ±12 | ±5       |      | ±12  | ±5      |     | LSB  |              |
| <b>SFDR</b><br>Spurious-free dynamic range           | $f_{in} = 5$ MHz  | 73.5     | 80   | 80   |         |     | dBc  |              |
|  | $f_{in} = 10$ MHz   | 80       |      | 81   |         |     |      |              |
|  | $f_{in} = 30$ MHz   | 76       |      | 77   |         |     |      |              |
|  | $f_{in} = 65$ MHz   | 74       |      | 75   |         |     |      |              |
| <b>THD</b><br>Total harmonic distortion              | $f_{in} = 5$ MHz  | 72.5     | 78   | 78.8 |         |     | dBc  |              |
|  | $f_{in} = 10$ MHz   | 77.4     |      | 79.2 |         |     |      |              |
|  | $f_{in} = 30$ MHz   | 74.5     |      | 76   |         |     |      |              |
|  | $f_{in} = 65$ MHz   | 71.4     |      | 72.4 |         |     |      |              |
| <b>HD2</b><br>Second harmonic Distortion             | $f_{in} = 5$ MHz  | 73.5     | 83.5 | 85   |         |     | dBc  |              |
|  | $f_{in} = 10$ MHz   | 81       |      | 84   |         |     |      |              |
|  | $f_{in} = 30$ MHz   | 80       |      | 83   |         |     |      |              |
|  | $f_{in} = 65$ MHz   | 75       |      | 76   |         |     |      |              |
| <b>HD3</b><br>Third harmonic distortion              | $f_{in} = 5$ MHz  | 73.5     | 80   | 80   |         |     | dBc  |              |
|  | $f_{in} = 10$ MHz   | 80       |      | 81   |         |     |      |              |
|  | $f_{in} = 30$ MHz   | 75       |      | 77   |         |     |      |              |
|  | $f_{in} = 65$ MHz   | 74       |      | 75   |         |     |      |              |
| <b>Worst Spur</b><br>Excluding HD2, HD3              | $f_{in} = 5$ MHz  | 80       |      | 90   |         |     | dBc  |              |
|  | $f_{in} = 10$ MHz   | 85       |      | 90   |         |     |      |              |
|  | $f_{in} = 30$ MHz   | 85       |      | 88   |         |     |      |              |
|  | $f_{in} = 65$ MHz   | 82       |      | 86   |         |     |      |              |
| <b>IMD</b><br>2-tone intermodulation distortion      | $f_1 = 8$ MHz, $f_2 = 10$ MHz, each tone at –7 dBFS                                       | 92       |      |      | 92      |     |      | dBFS         |
| Input overload recovery                              | Recovery to within 1% (of final value) for 6-dB overload with sine wave input             | 1        |      |      | 1       |     |      | clock cycles |

**ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE – 16-BIT ADC (continued)**

Typical values are at 25°C, AVDD = 3.3V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input (unless otherwise noted).

MIN and MAX values are across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ , AVDD = 3.3 V, LVDD = 1.8 V

| PARAMETERS                                     | TEST CONDITIONS   | 100 MSPS |     |     | 80 MSPS |     |     | UNITS |
|--|---|----------|-----|-----|---------|-----|-----|-------|
|  |   | MIN      | TYP | MAX | MIN     | TYP | MAX |       |
| <b>PSRR</b><br>AC power supply rejection ratio | For 50 mV signal on AVDD supply, up to 1 MHz ripple frequency |          | 30  |     |         | 30  |     | dB    |

**ELECTRICAL CHARACTERISTICS GENERAL – 16-BIT ADC MODE**

Typical values are at 25°C, AVDD = 3.3V, LVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input (unless otherwise noted).

MIN and MAX values are across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ , AVDD = 3.3V, LVDD = 1.8V

| PARAMETERS                             |   | 100 MSPS |       |      | 80 MSPS |       |      | UNITS   |
|--|---|----------|-------|------|---------|-------|------|---------|
|  |   | MIN      | TYP   | MAX  | MIN     | TYP   | MAX  |         |
| <b>ANALOG INPUT</b>                    |   |          |       |      |         |       |      |         |
|  | Differential input voltage range (0-dB gain)                                  |          | 4     |      | 4       |       |      | Vpp     |
|  | Differential input resistance (at dc)   |          | 2.5   |      | 2.5     |       |      | kΩ      |
|  | Differential input capacitance  |          | 12    |      | 12      |       |      | pF      |
|  | Analog input bandwidth  |          | 700   |      | 700     |       |      | MHz     |
|  | Analog input common-mode current (per input pin)                              |          | 8     |      | 8       |       |      | μA/MSPS |
|  | VCM common-mode output voltage, Internal reference mode                       |          | 1.5   |      | 1.5     |       |      | V       |
|  | VCM output current capability, Internal reference mode                        |          | 3     |      | 3       |       |      | mA      |
|  | VCM input voltage, external reference mode                                    | 1.45     | 1.5   | 1.55 | 1.45    | 1.5   | 1.55 | V       |
|  | VCM input current, external reference mode                                    |          | 0.5   |      |         | 0.5   |      | mA      |
| <b>DC ACCURACY</b>                     |   |          |       |      |         |       |      |         |
|  | Offset error  |          | ±10   | ±30  |         | ±10   |      | mV      |
| $E_{GREF}$                             | Gain error due to internal reference inaccuracy alone                         | ±1       | ±0.5  | 1    |         | ±0.5  |      | % FS    |
| $E_{GREF}$<br>Temperature Coefficient  | Internal reference mode   |          | 0.002 |      |         | 0.002 |      | Δ%/°C   |
|  | External reference mode   |          | 0.001 |      |         | 0.001 |      | Δ%/°C   |
| $E_{GCHAN}$                            | Gain error of channel alone   |          | 1     |      |         | 1     |      | % FS    |
| $E_{GCHAN}$<br>Temperature Coefficient |   |          | 0.002 |      |         | 0.002 |      | Δ%/°C   |
|  | Gain matching   |          | 0.5%  |      |         | 0.5%  |      |         |
| <b>POWER SUPPLY</b>                    |   |          |       |      |         |       |      |         |
| IAVDD                                  | Analog supply current   |          | 370   | 390  |         | 290   |      | mA      |
| ILVDD                                  | Digital and output buffer supply current with 100-Ω external LVDS termination |          | 110   | 150  |         | 100   |      | mA      |
|  | Analog power  |          | 1.22  |      |         | 0.96  |      | W       |
|  | Digital power   |          | 0.2   |      |         | 0.18  |      | W       |
|  | Global power down   |          | 63    | 110  |         | 63    |      | mW      |
|  | Standby   |          | 208   | 250  |         | 208   |      | mW      |

**ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE – 14-BIT ADC**

Typical values are at 25°C, AVDD = 3.3V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input (unless otherwise noted).

MIN and MAX values are across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ , AVDD = 3.3 V, LVDD = 1.8 V

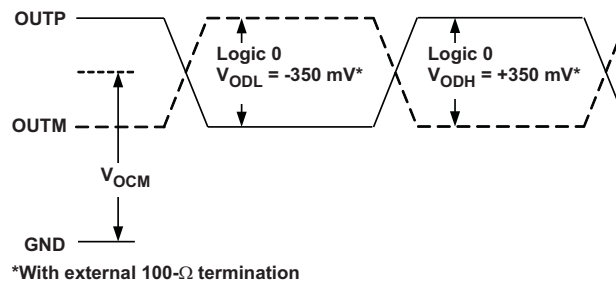
| PARAMETERS   | TEST CONDITIONS            | 100 MSPS |      |     | UNITS |
|--|----------------------------|----------|------|-----|-------|
|  |                            | MIN      | TYP  | MAX |       |
| <b>SNR</b><br>Signal-to-noise ratio                  | $f_{in} = 5 \text{ MHz}$   | 67.5     | 74   |     | dBFS  |
|  | $f_{inV} = 30 \text{ MHz}$ |          | 73   |     |       |
|  | $f_{in} = 65 \text{ MHz}$  |          | 71.3 |     |       |
| <b>SINAD</b><br>Signal-to-noise and distortion ratio | $f_{in} = 5 \text{ MHz}$   | 65.8     | 73.5 |     | dBFS  |
|  | $f_{in} = 30 \text{ MHz}$  |          | 71.9 |     |       |
|  | $f_{in} = 65 \text{ MHz}$  |          | 70.3 |     |       |
| <b>SFDR</b><br>Spurious-free dynamic range           | $f_{in} = 5 \text{ MHz}$   | 71.8     | 85   |     | dBc   |
|  | $f_{in} = 30 \text{ MHz}$  |          | 81   |     |       |
|  | $f_{in} = 65 \text{ MHz}$  |          | 78   |     |       |
| <b>THD</b><br>Total harmonic distortion              | $f_{in} = 5 \text{ MHz}$   | 69       | 83.5 |     | dBc   |
|  | $f_{in} = 30 \text{ MHz}$  |          | 78   |     |       |
|  | $f_{in} = 65 \text{ MHz}$  |          | 76.5 |     |       |
| <b>HD2</b><br>Second harmonic Distortion             | $f_{in} = 5 \text{ MHz}$   | 71.8     | 92   |     | dBc   |
|  | $f_{in} = 30 \text{ MHz}$  |          | 84   |     |       |
|  | $f_{in} = 65 \text{ MHz}$  |          | 80   |     |       |
| <b>HD3</b><br>Third harmonic distortion              | $f_{in} = 5 \text{ MHz}$   | 71.8     | 85   |     | dBc   |
|  | $f_{in} = 30 \text{ MHz}$  |          | 81   |     |       |
|  | $f_{in} = 65 \text{ MHz}$  |          | 78   |     |       |

## DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 3.3V, LVDD = 1.8V

| PARAMETER   |  | CONDITIONS  | MIN  | TYP         | MAX  | UNIT |
|---|--|---|------|-------------|------|------|
| <b>DIGITAL INPUTS – <math>\overline{\text{RESET}}</math>, SCLK, SDATA, <math>\overline{\text{CS}}</math>, PDN, SYNC, <math>\overline{\text{INT/EXT}}</math></b> |  |   |      |             |      |      |
| V <sub>IH</sub>   | High-level input voltage               | All digital inputs support 1.8-V and 3.3-V CMOS logic levels. | 1.3  |             |      | V    |
| V <sub>IL</sub>   | Low-level input voltage                |   |      |             | 0.4  | V    |
| I <sub>IH</sub>   | High-level input current               | SDATA, SCLK, $\overline{\text{CS}}$ <sup>(1)</sup>            |      | 5           |      | μA   |
| I <sub>IL</sub>   | Low-level input current                | SDATA, SCLK, $\overline{\text{CS}}$                           |      | 0           |      | μA   |
| <b>DIGITAL CMOS OUTPUT – SDOUT</b>  |  |   |      |             |      |      |
| V <sub>OH</sub>   | High-level output voltage              | I <sub>OH</sub> = 100 μA                                      |      | AVDD – 0.05 |      | V    |
| V <sub>OL</sub>   | Low-level output voltage               | I <sub>OL</sub> = 100 μA                                      |      | 0.05        |      | V    |
| <b>DIGITAL OUTPUTS – LVDS INTERFACE (OUT1P/M TO OUT8P/M, ADCLKP/M, LCLKP/M)</b>   |  |   |      |             |      |      |
| V <sub>ODH</sub>  | High-level output differential voltage | With external 100-Ω termination                               | 275  | 370         | 465  | mV   |
| V <sub>ODL</sub>  | Low-level output differential voltage  | With external 100-Ω termination                               | –465 | –370        | –275 | mV   |
| V <sub>OCM</sub>  | Output common-mode voltage             |   | 1000 | 1200        | 1400 | mV   |

(1)  $\overline{\text{CS}}$ , SDATA, SCLK have internal 300-kΩ pulldown resistor.



**Figure 3. LVDS Output Voltage Levels**

## TIMING REQUIREMENTS<sup>(1)</sup>

Typical values are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, sampling frequency = 100 MSPS, sine wave input clock = 1.5 Vpp clock amplitude,

$C_{LOAD} = 5 \text{ pF}^{(2)}$ ,  $R_{LOAD} = 100 \Omega^{(3)}$ , unless otherwise noted. MIN and MAX values are across the full temperature range

$T_{MIN} = -40^\circ\text{C}$  to  $T_{MAX} = 85^\circ\text{C}$ , AVDD = 3.3 V, LVDD = 1.7 V to 1.9 V

| PARAMETER   | CONDITIONS  | MIN  | TYP       | MAX  | UNIT          |
|---|---|------|-----------|------|---------------|
| $t_j$ Aperture jitter   |   |      | 220       |      | fs rms        |
| $t_A$ Aperture delay  | Time delay between rising edge of input clock and the actual sampling instant   |      | 3         |      | ns            |
| Wake-up time  | Time to valid data after coming out of STANDBY mode   |      | 10        |      | $\mu\text{s}$ |
|   | Time to valid data after coming out of global power down  |      | 60        |      |               |
| ADC latency   | Latency of ADC alone, excludes the delay from input clock to output clock ( $t_{PDI}$ ), <a href="#">Figure 5</a>                         |      | 16        |      | Clock cycles  |
| <b>2 WIRE, 8x SERIALIZATION<sup>(4)</sup></b>                                 |   |      |           |      |               |
| $t_{su}$ Data setup time  | Data valid (5) to zero-crossing of LCLKP  | 0.23 |           |      | ns            |
| $t_h$ Data hold time  | Zero-crossing of LCLKP to data becoming invalid <sup>(5)</sup>  | 0.31 |           |      | ns            |
| $t_{PDI}$ Clock propagation delay   | Input clock rising edge crossover to output frame clock ADCLKP rising edge crossover, $t_{PDI} = (t_s/4) + t_{delay}$                     | 6.8  | 8.8       | 10.8 | ns            |
| Variation of $t_{PDI}$  | Between two devices at same temperature and LVDD supply   |      | $\pm 0.6$ |      | ns            |
| LVDS bit clock duty cycle   | Duty cycle of differential clock, (LCLKP-LCLKM)   |      | 50%       |      |               |
| $t_{RISE}$ Data rise time,<br>$t_{FALL}$ Data fall time                       | Rise time measured from –100 mV to 100 mV,<br>Fall time measured from 100 mV to –100 mV<br><i>10 MSPS ≤ Sampling frequency ≤ 100 MSPS</i> |      | 0.17      |      | ns            |
| $t_{CLKRISE}$ Output clock rise time,<br>$t_{CLKFALL}$ Output clock fall time | Rise time measured from –100 mV to 100 mV<br>Fall time measured from 100 mV to –100 mV<br><i>10 MSPS ≤ Sampling frequency ≤ 100 MSPS</i>  |      | 0.2       |      | ns            |

(1) Timing parameters are ensured by design and characterization and not tested in production.

(2)  $C_{LOAD}$  is the effective external single-ended load capacitance between each output pin and ground.

(3)  $R_{LOAD}$  is the differential load resistance between the LVDS output pair.

(4) Measurements are done with a transmission line of 100- $\Omega$  characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.

(5) Data valid refers to logic HIGH of 100 mV and logic LOW of –100 mV.

**Table 1. LVDS Timing at Lower Sampling Frequencies - 2 Wire, 8x Serialization**

| SAMPLING FREQUENCY, MSPS | SETUP TIME, ns |     |     | HOLD TIME, ns |     |     |
|--------------------------|----------------|-----|-----|---------------|-----|-----|
|                          | Min            | Typ | Max | Min           | Typ | Max |
| 100                      | 0.23           |     |     | 0.31          |     |     |
| 80                       | 0.47           |     |     | 0.47          |     |     |
| 65                       | 0.56           |     |     | 0.7           |     |     |
| 50                       | 0.66           |     |     | 1             |     |     |
| 20                       | 2.7            |     |     | 2.8           |     |     |

**Table 2. LVDS Timing for 1 Wire 16x Serialization**

| SAMPLING FREQUENCY, MSPS | SETUP TIME, ns |     |     | HOLD TIME, ns |     |     |
|--------------------------|----------------|-----|-----|---------------|-----|-----|
|                          | Min            | Typ | Max | Min           | Typ | Max |
| 65                       | 0.15           |     |     | 0.31          |     |     |
| 50                       | 0.27           |     |     | 0.35          |     |     |
| 40                       | 0.45           |     |     | 0.55          |     |     |
| 20                       | 1.1            |     |     | 1.4           |     |     |

**Table 2. LVDS Timing for 1 Wire 16x Serialization (continued)**

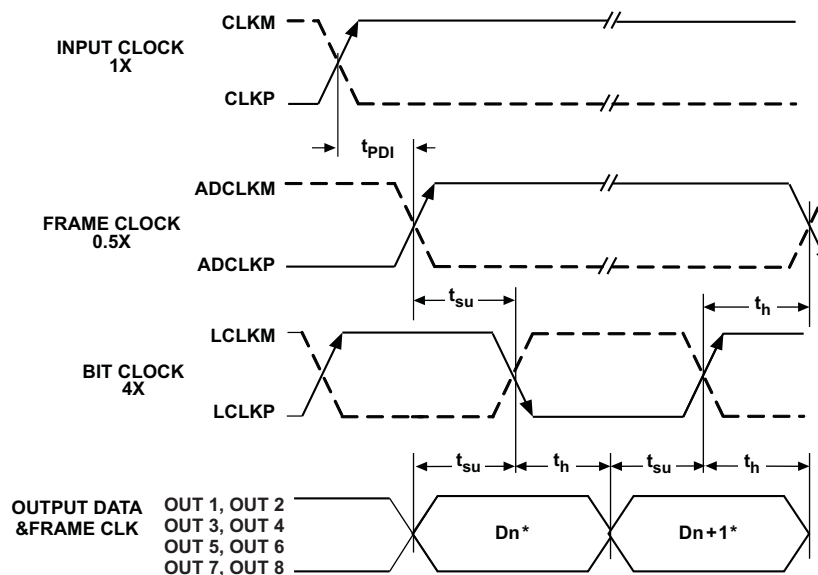
| SAMPLING FREQUENCY, MSPS   | SETUP TIME, ns  |     |      | HOLD TIME, ns |     |     |
|--|-----------------|-----|------|---------------|-----|-----|
|  | Min             | Typ | Max  | Min           | Typ | Max |
| Clock Propagation Delay<br>$t_{PDI} = (t_s/8) + t_{delay}$<br>10 MSPS < Sampling Frequency < 65 MSPS | $t_{delay}, ns$ |     |      |               |     |     |
|  | Typ             | Min | Max  |               |     |     |
|  | 6.8             | 8.8 | 10.8 |               |     |     |

**Table 3. LVDS Timing for 2 Wire, 7x Serialization**

| SAMPLING FREQUENCY, MSPS  | SETUP TIME, ns  |     |      | HOLD TIME, ns |     |     |
|---|-----------------|-----|------|---------------|-----|-----|
|   | Min             | Typ | Max  | Min           | Typ | Max |
| 100   | 0.29            |     |      | 0.39          |     |     |
| 80  | 0.51            |     |      | 0.60          |     |     |
| 65  | 0.58            |     |      | 0.82          |     |     |
| 50  | 0.85            |     |      | 1.20          |     |     |
| 20  | 3.2             |     |      | 3.3           |     |     |
| Clock Propagation Delay<br>$t_{PDI} = (t_s/3.5) + t_{delay}$<br>10 MSPS < Sampling Frequency < 100 MSPS | $t_{delay}, ns$ |     |      |               |     |     |
|   | Typ             | Min | Max  |               |     |     |
|   | 6.8             | 8.8 | 10.8 |               |     |     |

**Table 4. LVDS Timing for 1 Wire, 14x Serialization**

| SAMPLING FREQUENCY, MSPS   | SETUP TIME, ns  |     |      | HOLD TIME, ns |     |     |
|--|-----------------|-----|------|---------------|-----|-----|
|  | Min             | Typ | Max  | Min           | Typ | Max |
| 65   | 0.19            |     |      | 0.28          |     |     |
| 50   | 0.37            |     |      | 0.42          |     |     |
| 30   | 0.70            |     |      | 1.0           |     |     |
| 20   | 1.3             |     |      | 1.5           |     |     |
| Clock Propagation Delay<br>$t_{PDI} = (t_s/7) + t_{delay}$<br>10 MSPS < Sampling Frequency < 65 MSPS | $t_{delay}, ns$ |     |      |               |     |     |
|  | MIN             | Typ | Max  |               |     |     |
|  | 6.8             | 8.8 | 10.8 |               |     |     |



**Figure 4. LVDS Timing**

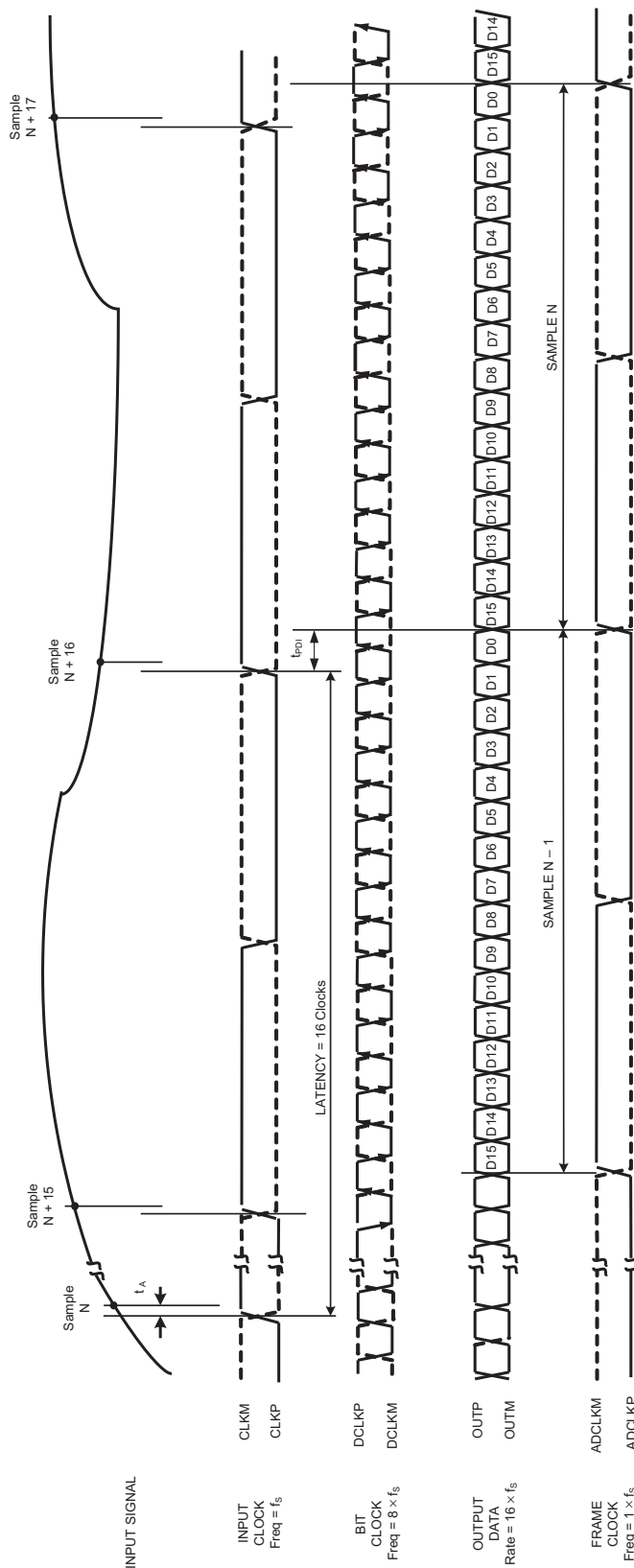


Figure 5. Latency Diagram

## DEVICE CONFIGURATION

ADS5263 has several modes that can be configured using a serial programming interface, as described below. In addition, the device has dedicated parallel pins for controlling common functions such as power down and internal or external reference selection.

**Table 5. PDN CONTROL PIN**

| VOLTAGE APPLIED ON PDN | STATE OF REGISTER BIT<br><CONFIG PDN pin> | DESCRIPTION                          |
|------------------------|---|--------------------------------------|
| 0 V                    | X (don't care)                            | Normal operation                     |
| Logic HIGH             | 0   | Device enters global power-down mode |
|                        | 1   | Device enters standby mode           |

**Table 6.  $\overline{\text{INT/EXT}}$  CONTROL PIN**

| VOLTAGE APPLIED ON $\overline{\text{INT/EXT}}$ | DESCRIPTION  |
|--|--|
| 0 V  | External reference mode. Apply voltage on VCM pin to set the references for ADC operation. |
| Logic HIGH                                     | Internal reference   |

## SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins  $\overline{\text{CS}}$  (serial interface enable), SCLK (serial interface clock) and SDATA (serial interface data).

When  $\overline{\text{CS}}$  is low,

- Serial shift of bits into the device is enabled.
- Serial data (on SDATA pin) is latched at every rising edge of SCLK.
- The serial data is loaded into the register at every 24<sup>th</sup> SCLK rising edge.

In case the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active  $\overline{\text{CS}}$  pulse.

The first 8 bits form the register address and the remaining 16 bits form the register data. The interface can work with SCLK frequencies from 20 MHz down to very low speeds (a few hertz) and also with non-50% SCLK duty cycle.

## Register Initialization

After power up, the internal registers MUST be initialized to their default values. This can be done in one of two ways:

1. Through a hardware reset by applying a low-going pulse on the  $\overline{\text{RESET}}$  pin (of width greater than 10 ns) as shown in [Figure 6](#).

OR

2. By applying software reset. Using the serial interface, set the <RESET> bit (D7 in register 0x00) to HIGH. This initializes internal registers to their default values and then self-resets the <RESET> bit to **low**. In this case, the RESET pin is kept high (inactive).

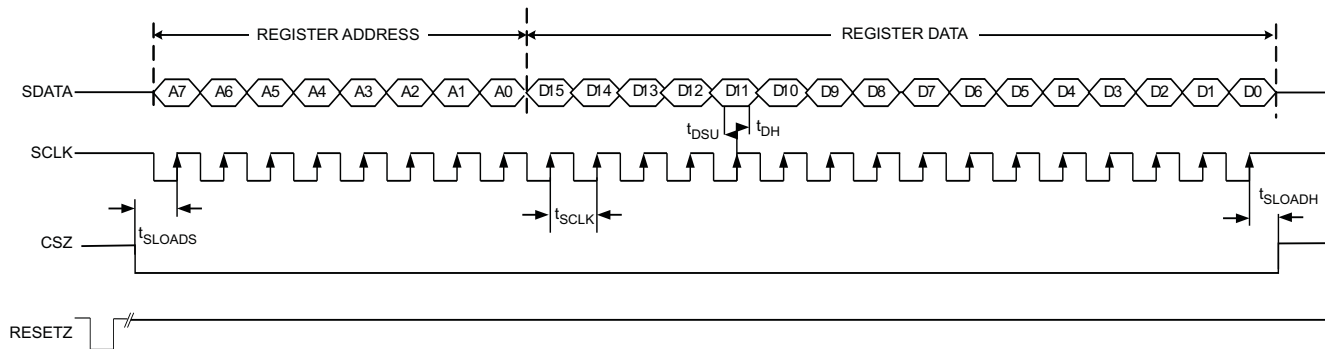


Figure 6. Serial Interface Timing

**SERIAL INTERFACE TIMING CHARACTERISTICS**

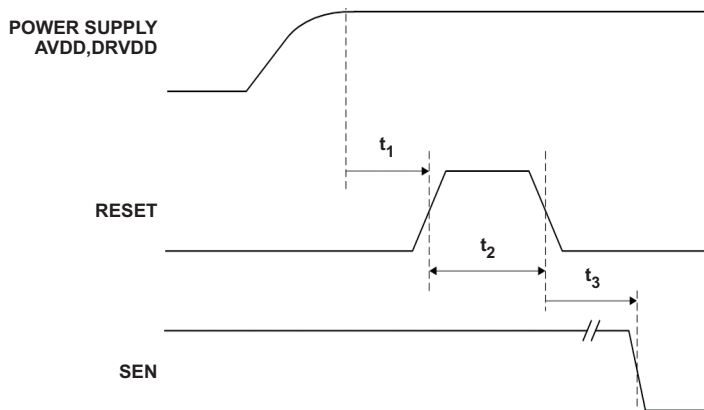
Typical values at 25°C, MIN and MAX values across the full temperature range T<sub>MIN</sub> = -40°C to T<sub>MAX</sub> = 85°C, AVDD = 3.3 V, LVDD = 1.8 V, unless otherwise noted.

| PARAMETER           |  | MIN  | TYP | MAX | UNIT |
|---------------------|--|------|-----|-----|------|
| f <sub>SCLK</sub>   | SCLK frequency (= 1/ t <sub>SCLK</sub> ) | > DC | 20  |     | MHz  |
| t <sub>SLOADS</sub> | $\overline{CS}$ to SCLK setup time       | 25   |     |     | ns   |
| t <sub>SLOADH</sub> | SCLK to $\overline{CS}$ hold time        | 25   |     |     | ns   |
| t <sub>DS</sub>     | SDATA setup time                         | 25   |     |     | ns   |
| t <sub>DH</sub>     | SDATA hold time                          | 25   |     |     | ns   |

**RESET TIMING**

Typical values at 25°C, MIN and MAX values across the full temperature range T<sub>MIN</sub> = -40°C to T<sub>MAX</sub> = 85°C (unless otherwise noted)

| PARAMETER      | TEST CONDITIONS      | MIN | TYP | MAX | UNIT |
|----------------|----------------------|-----|-----|-----|------|
| t <sub>1</sub> | Power-on delay       |     | 1   |     | ms   |
| t <sub>2</sub> | Reset pulse duration | 50  |     |     | ns   |
| t <sub>3</sub> | Register write delay |     | 100 |     | ns   |



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

Figure 7. Reset Timing Diagram



**SERIAL REGISTER MAP**
**Table 7. Summary of Functions Supported by Serial Interface<sup>(1)</sup>**

| Register Address | Register Data <sup>(2)</sup> |                    |           |     |            |                  |                   |           |             |                     |                       |                         |                                |                  |                 |                                |                 |  |
|------------------|------------------------------|--------------------|-----------|-----|------------|------------------|-------------------|-----------|-------------|---------------------|-----------------------|-------------------------|--------------------------------|------------------|-----------------|--------------------------------|-----------------|--|
| A7-A0 in HEX     | D15                          | D14                | D13       | D12 | D11        | D10              | D9                | D8        | D7          | D6                  | D5                    | D4                      | D3                             | D2               | D1              | D0                             |                 |  |
| 0                | 0                            | 0                  | 0         | 0   | 0          | 0                | 0                 | 0         | 0           | 0                   | 0                     | 0                       | 0                              | 0                | 0               | <RESET>                        |                 |  |
| 1                | 0                            | 0                  | 0         | 0   | 0          | 0                | 0                 | 0         | 0           | 0                   | 0                     | EN_HIGH_ADDR            | 0                              | 0                | 0               | <READOUT>                      |                 |  |
| 2                | 0                            | 0                  | <EN_SYNC> | 0   | 0          | 0                | 0                 | 0         | 0           | 0                   | 0                     | 0                       | 0                              | 0                | 0               | 0                              |                 |  |
| 9                | 0                            | 0                  | 0         | 0   | 0          | <EN_CLAMP>       | 0                 | 0         | 0           | 0                   | 0                     | 0                       | 0                              | 0                | 0               | 0                              |                 |  |
| F                | 0                            | 0                  | 0         | 0   | 0          | <CONFIG_PD_PIN>  | <GLOBAL_PD_N>     | <STANDBY> | <PDN_CH_4B> | <PDN_CH_3B>         | <PDN_CH_2B>           | <PDN_CH_1B>             | <PDN_CH_4A>                    | <PDN_CH_3A>      | <PDN_CH_2A>     | <PDN_CH_1A>                    |                 |  |
| 11               | 0                            | 0                  | 0         | 0   | 0          | <LVDS_CURR_DATA> |                   |           | 0           | <LVDS_CURR_ADCLK>   |                       |                         | 0                              | <LVDS_CURR_LCLK> |                 |                                |                 |  |
| 12               | 0                            | <ENABLE_LVDS_TERM> | 0         | 0   | 0          | <LVDS_TERM_DATA> |                   |           | 0           | <LVDS_TERM_ADCLK>   |                       |                         | 0                              | <LVDS_TERM_LCLK> |                 |                                |                 |  |
| 14               | 0                            | 0                  | 0         | 0   | 0          | 0                | 0                 | 0         | 0           | 0                   | 0                     | 0                       | <EN_LFNS_CH_4>                 | <EN_LFNS_CH_3>   | <EN_LFNS_CH_2>  | <EN_LFNS_CH_1>                 |                 |  |
| 25               | 0                            | 0                  | 0         | 0   | 0          | 0                | 0                 | 0         | 0           | <RAMP_TEST_PATTERN> | <DUAL_CUSTOM_PATTERN> | <SINGLE_CUSTOM_PATTERN> | CUSTOM_PATTERN_B_DATA[15...14] |                  |                 | CUSTOM_PATTERN_A_DATA[15...14] |                 |  |
| 26               | CUSTOM_PATTERN_A_DATA[13..0] |                    |           |     |            |                  |                   |           |             |                     |                       |                         |                                |                  |                 | 0                              | 0               |  |
| 27               | CUSTOM_PATTERN_B_DATA[13..0] |                    |           |     |            |                  |                   |           |             |                     |                       |                         |                                |                  |                 | 0                              | 0               |  |
| 28               | <EN_WORD-WISE_CONTROL>       |                    |           |     |            |                  |                   |           |             |                     |                       |                         |                                | <WORD-WISE_CH4>  | <WORD-WISE_CH3> | <WORD-WISE_CH2>                | <WORD-WISE_CH1> |  |
| 29               | 0                            | 0                  | 0         | 0   | 0          | 0                | 0                 | 0         | 0           | 0                   | 0                     | 0                       | 0                              | 0                | <EN_DIG_FILTER> | <EN_AVG>                       |                 |  |
| 2A               | <GAIN_CH4>                   |                    |           |     | <GAIN_CH3> |                  |                   |           | <GAIN_CH2>  |                     |                       |                         | <GAIN_CH1>                     |                  |                 |                                |                 |  |
| 2C               | 0                            | 0                  | 0         | 0   | 0          | 0                | 0                 | 0         | <AVG_OUT_4> |                     | <AVG_OUT_3>           |                         | <AVG_OUT_2>                    |                  | <AVG_OUT_1>     |                                |                 |  |
| 2E               | 0                            | 0                  | 0         | 0   | 0          | 0                | <FILTER_TYPE_CH1> |           |             | <DEC_by_RATE_CH1>   |                       |                         | 0                              | <ODD_TAP_CH1>    | 0               | <USE_FILTER_CH1>               |                 |  |
| 2F               | 0                            | 0                  | 0         | 0   | 0          | 0                | <FILTER_TYPE_CH2> |           |             | <DEC_by_RATE_CH2>   |                       |                         | 0                              | <ODD_TAP_CH2>    | 0               | <USE_FILTER_CH2>               |                 |  |
| 30               | 0                            | 0                  | 0         | 0   | 0          | 0                | <FILTER_TYPE_CH3> |           |             | <DEC_by_RATE_CH3>   |                       |                         | 0                              | <ODD_TAP_CH3>    | 0               | <USE_FILTER_CH3>               |                 |  |
| 31               | 0                            | 0                  | 0         | 0   | 0          | 0                | <FILTER_TYPE_CH4> |           |             | <DEC_by_RATE_CH4>   |                       |                         | 0                              | <ODD_TAP_CH4>    | 0               | <USE_FILTER_CH4>               |                 |  |
| 38               | 0                            | 0                  | 0         | 0   | 0          | 0                | 0                 | 0         | 0           | 0                   | 0                     | 0                       | 0                              | 0                | <OUTPUT_RATE>   |                                |                 |  |
| 42               | <EN_REG_42>                  | 0                  | 0         | 0   | 0          | 0                | 0                 | 0         | 0           | <PHASE_DDR>         |                       | 0                       | <EXT_REF_VCM>                  | 0                | 0               | 0                              |                 |  |

(1) Multiple functions in a register can be programmed in a single write operation.

(2) All registers are cleared to zero after software or hardware reset is applied.

**Table 7. Summary of Functions Supported by Serial Interface<sup>(1)</sup> (continued)**

| Register Address | Register Data <sup>(2)</sup> |     |     |                      |                                 |                      |    |    |                    |    |              |    |                    |            |                |                     |
|------------------|------------------------------|-----|-----|----------------------|---------------------------------|----------------------|----|----|--------------------|----|--------------|----|--------------------|------------|----------------|---------------------|
|                  | D15                          | D14 | D13 | D12                  | D11                             | D10                  | D9 | D8 | D7                 | D6 | D5           | D4 | D3                 | D2         | D1             | D0                  |
| 45               | 0                            | 0   | 0   | 0                    | 0                               | 0                    | 0  | 0  | 0                  | 0  | 0            | 0  | 0                  | 0          | <SYNC PATTERN> | <DESKEW PATTERN>    |
| 46               | <EN SERIALI ZATION>          | 0   | 0   | <18x SERIALI ZATION> | <16x SERIALI ZATION>            | <14x SERIALI ZATION> | 0  | 0  | 0                  | 0  | <PAD two 0s> | 0  | <MSB FIRST>        | <2S COMPL> | 0              | <2-WIRE 0.5X FRAME> |
| 50               | <EN MAP1>                    | 0   | 0   | 0                    | <MAP_Ch1234_OUT2A>              |                      |    |    | <MAP_Ch1234_OUT1B> |    |              |    | <MAP_Ch1234_OUT1A> |            |                |                     |
| 51               | <EN MAP2>                    | 0   | 0   | 0                    | <MAP_Ch1234_OUT3B>              |                      |    |    | <MAP_Ch1234_OUT3A> |    |              |    | <MAP_Ch1234_OUT2B> |            |                |                     |
| 52               | <EN MAP3>                    | 0   | 0   | 0                    | 0                               | 0                    | 0  | 0  | <MAP_Ch1234_OUT4B> |    |              |    | <MAP_Ch1234_OUT4A> |            |                |                     |
| 5A to 65         | <EN CUSTOM FILT CH1>         |     |     |                      | <COEFFn SET CH1> <sup>(3)</sup> |                      |    |    |                    |    |              |    |                    |            |                |                     |
| 66 to 71         | <EN CUSTOM FILT CH2>         |     |     |                      | <COEFFn SET CH2> <sup>(3)</sup> |                      |    |    |                    |    |              |    |                    |            |                |                     |
| 72 to 7D         | <EN CUSTOM FILT CH3>         |     |     |                      | <COEFFn SET CH3> <sup>(3)</sup> |                      |    |    |                    |    |              |    |                    |            |                |                     |
| 7E to 89         | <EN CUSTOM FILT CH4>         |     |     |                      | <COEFFn SET CH4> <sup>(3)</sup> |                      |    |    |                    |    |              |    |                    |            |                |                     |
| B3               | <EN ADC MODE>                | 0   | 0   | 0                    | 0                               | 0                    | 0  | 0  | 0                  | 0  | 0            | 0  | 0                  | 0          | 0              | 16B/14B ADC MODE    |
| F0               | EN_EXT_REF                   | 0   | 0   | 0                    | 0                               | 0                    | 0  | 0  | 0                  | 0  | 0            | 0  | 0                  | 0          | 0              | 0                   |

(3) Where n = 0 to 11

**Default State After Reset**

- Device is in normal operation mode with 16-bit ADC enabled for all 4 channels.
- Output interface is 1-wire, 16x serialization with 8x bit clock and 1x frame clock frequency
- Serial readout is disabled
- PD pin is configured as global power-down pin
- LVDS output current is set to 3.5 mA; internal termination is disabled.
- Digital gain is set to 0 dB.
- Digital modes such as LFNS, digital filters are disabled.

**DESCRIPTION OF SERIAL REGISTERS**

| REGISTER ADDRESS | REGISTER DATA |     |     |     |     |     |    |    |    |    |    |    |    |    |    |         |
|------------------|---------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|---------|
| A7-A0 IN HEX     | D15           | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0      |
| 0                | 0             | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | <RESET> |

**D0 <RESET>**

- 1 Software reset applied – resets all internal registers to their default values and self-clears to 0

| A7-A0 IN HEX | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4             | D3 | D2 | D1 | D0        |
|--------------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----------------|----|----|----|-----------|
| 1            | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | <EN_HIGH_ADDR> | 0  | 0  | 0  | <READOUT> |

**D4 <EN\_HIGH\_ADDR>**

See section [EXTERNAL REFERENCE MODE](#)

**D0 <READOUT>**

- 0 Serial readout of registers is disabled. Pin SDOOUT is in the high-impedance state.
- 1 Serial readout enabled, SDOOUT pin functions as serial data readout.

| A7-A0 IN HEX | D15 | D14 | D13       | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------|-----|-----|-----------|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 2            | 0   | 0   | <EN_SYNC> | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**D13 <EN\_SYNC>**

- 0 SYNC pin is disabled.
- 1 SYNC pin can be used to synchronize the decimation filters across channels and across multiple chips.

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| A7–A0<br>IN HEX | D15 | D14 | D13 | D12 | D11 | D10           | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|-----|-----|-----|-----|-----|---------------|----|----|----|----|----|----|----|----|----|----|
| 9               | 0   | 0   | 0   | 0   | 0   | <EN<br>CLAMP> | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

## D10 <EN\_CLAMP>

- 0 Internal clamp is disabled.
- 1 Internal clamp is enabled. The clamp works only for the 14-bit ADC input pins. The clamping is synchronized with the pulse applied on the SYNC pin (see *Clamp Function for CCD Signals* in the application section).

| A7–A0<br>IN HEX | D15 | D14 | D13 | D12 | D11 | D10                       | D9                  | D8                | D7                | D6                | D5                | D4                | D3                | D2                | D1                | D0                |
|-----------------|-----|-----|-----|-----|-----|---------------------------|---------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| F               | 0   | 0   | 0   | 0   | 0   | <CON<br>FIG<br>PD<br>PIN> | <GLO<br>BAL<br>PDN> | <STA<br>ND<br>BY> | <PDN<br>CH<br>4B> | <PDN<br>CH<br>3B> | <PDN<br>CH<br>2B> | <PDN<br>CH<br>1B> | <PDN<br>CH<br>4A> | <PDN<br>CH<br>3A> | <PDN<br>CH<br>2A> | <PDN<br>CH<br>1A> |

## D10 <CONFIG PDN PIN> Can be used to configure PDN pin as global power down or standby

- 0 PDN pin functions as global power down.
- 1 PDN pin functions as standby.

## D9 <GLOBAL PDN>

- 0 Normal ADC operation
- 1 Device is put in global power down. All four channels are powered down, including LVDS output data and clock buffers.

**D8 <STANDBY>**

- 0 Normal ADC operation
- 1 Device is put in standby. All four ADCs are powered down. Internal PLL, LVDS bit clock, and frame clock are running.

**D7– <PDN CH X> Individual channel power down**
**D0**

- 0 Channel X is powered up.
- 1 Channel X is powered down.

| REGISTER ADDRESS | REGISTER DATA |     |     |     |     |     |                  |    |    |    |                   |    |    |    |                  |    |    |
|------------------|---------------|-----|-----|-----|-----|-----|------------------|----|----|----|-------------------|----|----|----|------------------|----|----|
|                  | A7–A0 IN HEX  | D15 | D14 | D13 | D12 | D11 | D10              | D9 | D8 | D7 | D6                | D5 | D4 | D3 | D2               | D1 | D0 |
| 11               | 0             | 0   | 0   | 0   | 0   | 0   | <LVDS CURR DATA> |    |    | 0  | <LVDS CURR ADCLK> |    |    | 0  | <LVDS CURR LCLK> |    |    |

**D10–D8 <LVDS CURR DATA> LVDS current control for data buffers**

- 000 3.5 mA
- 001 2.5 mA
- 010 1.5 mA
- 011 0.5 mA
- 100 7.5 mA
- 101 6.5 mA
- 110 5.5 mA
- 111 4.5 mA

**D6–D4 <LVDS CURR LCLK> LVDS current control for frame-clock buffer**

- 000 3.5 mA
- 001 2.5 mA
- 010 1.5 mA
- 011 0.5 mA
- 100 7.5 mA
- 101 6.5 mA
- 110 5.5 mA
- 111 4.5 mA

**D2–D0 <LVDS CURR LCLK> LVDS current control for bit-clock buffer**

- 000 3.5 mA
- 001 2.5 mA
- 010 1.5 mA
- 011 0.5 mA
- 100 7.5 mA
- 101 6.5 mA
- 110 5.5 mA
- 111 4.5 mA

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| REGISTER ADDRESS | REGISTER DATA |                    |     |     |     |                  |    |    |    |                     |    |    |    |                  |    |    |
|------------------|---------------|--------------------|-----|-----|-----|------------------|----|----|----|---------------------|----|----|----|------------------|----|----|
|                  | D15           | D14                | D13 | D12 | D11 | D10              | D9 | D8 | D7 | D6                  | D5 | D4 | D3 | D2               | D1 | D0 |
| 12               | 0             | <ENABLE LVDS TERM> | 0   | 0   | 0   | <LVDS TERM DATA> |    |    | 0  | <LVDS TERM ADCLK> 0 |    |    | 0  | <LVDS TERM LCLK> |    |    |

## D14 <ENABLE LVDS TERM>

0 Internal termination disabled

1 Internal termination enabled

## D10–D8 <LVDS TERM DATA> Internal LVDS termination for data buffers

000 No internal termination

001 150 Ω

010 100 Ω

011 60 Ω

100 80 Ω

101 55 Ω

110 45 Ω

111 35 Ω

## D6–D4 <LVDS TERM ADCLK> Internal LVDS termination for frame clock buffer

000 No internal termination

001 150 Ω

010 100 Ω

011 60 Ω

100 80 Ω

101 55 Ω

110 45 Ω

111 35 Ω

## D2–D0 <LVDS TERM LCLK> Internal LVDS termination for bit clock buffer

000 No internal termination

001 150 Ω

010 100 Ω

011 60 Ω

100 80 Ω

101 55 Ω

110 45 Ω

111 35 Ω

| REGISTER ADDRESS | REGISTER DATA |     |     |     |     |     |    |    |    |    |    |    |               |               |               |               |
|------------------|---------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|---------------|---------------|---------------|---------------|
|                  | D15           | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3            | D2            | D1            | D0            |
| 14               | 0             | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | <EN LFNS CH4> | <EN LFNS CH3> | <EN LFNS CH2> | <EN LFNS CH1> |

**D3–D0 <EN LFNS CH X> low-frequency noise-suppression mode is enabled for channel X.**

0 LFNS mode is disabled.

1 LFNS mode is enabled for channel X.

In 16-bit ADC mode, <EN LFNS CH X> enables LFNS for channel CH X.

In 14-bit ADC mode, <EN LFNS CH X> enables LFNS for channel CH X B.

| A7–A0 IN HEX | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6                   | D5                     | D4                       | D3                             | D2                             | D1 | D0 |
|--------------|-----|-----|-----|-----|-----|-----|----|----|----|----------------------|------------------------|--------------------------|--------------------------------|--------------------------------|----|----|
| 25           | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | <RAMP TEST PATTERN > | <DUAL CUSTOM PATTERN > | <SINGLE CUSTOM PATTERN > | CUSTOM PATTERN B DATA[15...14] | CUSTOM PATTERN A DATA[15...14] |    |    |

**D6 <RAMP TEST PATTERN>**

0 Ramp test pattern is disabled.

1 Ramp test pattern is enabled; output code increments by one LSB every clock cycle.

**D5 <DUAL CUSTOM PATTERN>**

0 Dual custom pattern is disabled.

1 Dual custom pattern is enabled.

Two custom patterns can be specified in registers PATTERN A and PATTERN B. The two patterns are output one after the other (instead of ADC data).

**D5 <SINGLE CUSTOM PATTERN>**

0 Single custom pattern is disabled.

1 Single custom pattern is enabled.

The custom pattern can be specified in register A and is output every clock cycle instead of ADC data.

**D3–D2 <CUSTOM PATTERN B bits D15 and D14>**

**D1–D0 <CUSTOM PATTERN A bits D15 and D14>**

Specify bits D15 and D14 of custom pattern in these register bits.

| A7–A0 IN HEX | D15                          | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------|------------------------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 26           | CUSTOM PATTERN A DATA[13..0] |     |     |     |     |     |    |    |    |    |    |    |    |    | 0  | 0  |
| 27           | CUSTOM PATTERN B DATA[13..0] |     |     |     |     |     |    |    |    |    |    |    |    |    | 0  | 0  |

Specify bits D13 to D0 of custom pattern in these registers.

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| A7–A0<br>IN HEX | D15                           | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3                     | D2                     | D1                     | D0                     |
|-----------------|-------------------------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 28              | <EN WORD-<br>WISE<br>CONTROL> |     |     |     |     |     |    |    |    |    |    |    | <WORD-<br>WISE<br>CH4> | <WORD-<br>WISE<br>CH3> | <WORD-<br>WISE<br>CH2> | <WORD-<br>WISE<br>CH1> |

## D15 <EN WORD-WISE CONTROL>

- 0 Control of word-wise mode is disabled.
- 1 Control of word-wise mode is enabled.

## D3–D0 <WORD-WISE CH XL>

- 0 Output data is serially sent in byte-wise format.
- 1 Output data is serially sent in word-wise format ONLY when 2-wire mode is enabled (see register 0x46).

| A7–A0<br>IN HEX | D15        | D14 | D13 | D12 | D11        | D10 | D9 | D8 | D7         | D6 | D5 | D4 | D3         | D2 | D1 | D0 |
|-----------------|------------|-----|-----|-----|------------|-----|----|----|------------|----|----|----|------------|----|----|----|
| 2A              | <GAIN CH4> |     |     |     | <GAIN CH3> |     |    |    | <GAIN CH2> |    |    |    | <GAIN CH1> |    |    |    |

## <GAIN CH x> Individual channel gain control

In 16-bit ADC mode, <GAIN CH X> sets gain for channel CH X A.

In 14-bit ADC mode, <GAIN CH X> sets gain for channel CH X B.

|                 |        |
|-----------------|--------|
| 0000            | 0 dB   |
| 0001            | 1 dB   |
| 0010            | 2 dB   |
| 0011            | 3 dB   |
| 0100            | 4 dB   |
| 0101            | 5 dB   |
| 0110            | 6 dB   |
| 0111            | 7 dB   |
| 1000            | 8 dB   |
| 1001            | 9 dB   |
| 1010            | 10 dB  |
| 1011            | 11 dB  |
| 1100            | 12 dB  |
| 1101 to<br>1111 | Unused |

| A7–A0<br>IN HEX | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7          | D6          | D5          | D4          | D3 | D2 | D1 | D0 |
|-----------------|-----|-----|-----|-----|-----|-----|----|----|-------------|-------------|-------------|-------------|----|----|----|----|
| 2C              | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | <AVG OUT 4> | <AVG OUT 3> | <AVG OUT 2> | <AVG OUT 1> |    |    |    |    |

**<AVG OUT 1>** These bits determine which data stream is output on LVDS pins OUT1A/1B.  
(after global enable bit for averaging is enabled <EN AVG GLO> = 1)

- 00 LVDS OUT1A/1B buffers are powered down.
- 01 OUT1A/1B output digital data corresponding to the signal applied on analog input pin IN1.
- 10 OUT1A/1B output digital data corresponding to the average of signals applied on analog input pins IN1 and IN2.
- 11 OUT1A/1B output digital data corresponding to the average of signals applied on analog input pins IN1, IN2, IN3, and IN4.

**<AVG OUT 2>** These bits determine which data stream is output on LVDS pins OUT2A/2B  
(after global enable bit for averaging is enabled <EN AVG GLO> = 1)

- 00 LVDS OUT2A/2B buffers are powered down.
- 01 OUT2A/2B output digital data corresponding to the signal applied on analog input pin IN2.
- 10 OUT2A/2B output digital data corresponding to the signal applied on analog input pin IN3.
- 11 OUT2A/2B output digital data corresponding to the average of signals applied on analog input pins IN3 and IN4.

**<AVG OUT 3>** These bits determine which data stream is output on LVDS pins OUT3A/3B  
(after global enable bit for averaging is enabled <EN AVG GLO> = 1)

- 00 LVDS OUT3A/3B buffers are powered down.
- 01 OUT3A/3B output digital data corresponding to the signal applied on analog input pin IN3.
- 10 OUT3A/3B output digital data corresponding to the signal applied on analog input pin IN2.
- 11 OUT3A/3B output digital data corresponding to the average of signals applied on analog input pins IN1 and IN4.

**<AVG OUT 4>** These bits determine which data stream is output on LVDS pins OUT4A/4B  
(after global enable bit for averaging is enabled <EN AVG GLO> = 1)

- 00 LVDS OUT4A/4B buffers are powered down.
- 01 OUT4A/4B output digital data corresponding to the signal applied on analog input pin IN4.
- 10 OUT4A/4B output digital data corresponding to the average of signals applied on analog input pins IN3 and IN4.
- 11 OUT4A/4B output digital data corresponding to the average of signals applied on analog input pins IN1, IN2, IN3, and IN4.

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| A7–A0<br>IN HEX | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1                 | D0              |
|-----------------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|--------------------|-----------------|
| 29              | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | <EN DIG<br>FILTER> | <EN AVG<br>GLO> |

## D1 <EN DIG FILTER>

0 Digital filter mode is disabled.

1 Digital filter mode is enabled on all channels. To turn filter on or off for individual channels, also set the <USE FILTER CH X> register bit.

## D0 <EN AVG GLO>

0 Averaging mode is disabled.

1 Averaging mode is enabled on all channels.

| A7–A0<br>IN HEX | D15 | D14 | D13 | D12 | D11 | D10 | D9                   | D8 | D7 | D6                   | D5 | D4 | D3 | D2 | D1 | D0                  |
|-----------------|-----|-----|-----|-----|-----|-----|----------------------|----|----|----------------------|----|----|----|----|----|---------------------|
| 2E              | 0   | 0   | 0   | 0   | 0   | 0   | <FILTER TYPE<br>CH1> |    |    | <DEC by RATE<br>CH1> |    |    | 0  | 0  | 0  | <USE FILTER<br>CH1> |
| 2F              | 0   | 0   | 0   | 0   | 0   | 0   | <FILTER TYPE<br>CH2> |    |    | <DEC by RATE<br>CH2> |    |    | 0  | 0  | 0  | <USE FILTER<br>CH2> |
| 30              | 0   | 0   | 0   | 0   | 0   | 0   | <FILTER TYPE<br>CH3> |    |    | <DEC by RATE<br>CH3> |    |    | 0  | 0  | 0  | <USE FILTER<br>CH3> |
| 31              | 0   | 0   | 0   | 0   | 0   | 0   | <FILTER TYPE<br>CH4> |    |    | <DEC by RATE<br>CH4> |    |    | 0  | 0  | 0  | <USE FILTER<br>CH4> |

## D0 <USE FILTER CH X>

0 Filter is turned OFF on channel X

1 Filter is turned ON on channel X.

## D2 <ODD TAP CH X> select filter with even or odd tap for channel X

0 Even tap filter is selected.

1 Odd tap filter is selected.

## D6–D4 <DEC by RATE CH X> select decimation rates for channel X

000 Decimate-by-2 rate is selected.

001 Decimate-by-4 rate is selected.

100 Decimate-by-8 rate is selected.

Other combinations Do not use

## D9–D7 <FILTER TYPE CH X> select type of filter for channel X

000 Low-pass filter with decimate-by-2 rate

001 High-pass filter with decimate-by-2 rate

010 Low-pass filter with decimate-by-4 rate

011 Band-pass filter #1 with decimate-by-4 rate

100 Band-pass filter #2 with decimate-by-4 rate

101 High-pass filter with decimate-by-4 rate

| A7-A0<br>IN HEX | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1                         | D0 |
|-----------------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----------------------------|----|
| 38              | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | <b>&lt;OUTPUT RATE&gt;</b> |    |

**D1–D0 <OUTPUT RATE>**

- 00 Output data rate = 1× sample rate
- 01 Output data rate = 0.5× sample rate
- 02 Output data rate = 0.25× sample rate
- 03 Output data rate = 0.125× sample rate

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| REGISTER ADDRESS | REGISTER DATA |     |     |     |     |     |     |    |    |    |             |    |    |               |    |    |    |
|------------------|---------------|-----|-----|-----|-----|-----|-----|----|----|----|-------------|----|----|---------------|----|----|----|
|                  | A7-A0 IN HEX  | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6          | D5 | D4 | D3            | D2 | D1 | D0 |
| 42               | <EN_REG_42>   | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | <PHASE_DDR> | 0  | 0  | <EXT_REF_VCM> | 0  | 0  | 0  |

## D15 <EN\_REG\_42>

0 Disables register bits D6, D5 and D3

1 Enables register bits D6, D5 and D3

## D6-D5 <PHASE\_DDR>

Note that the default value of <PHASE\_DDR> bit = 10. However, in this condition, if the contents of the register 0x42 are readout, they will be read as 00.

If the value of <PHASE\_DDR> bit is now modified by writing into this register, then subsequent writes will read back the written value.

Register bit <PHASE\_DDR> can be used to control the phase of LCLK (with respect to the rising edge of the frame clock, ADCLK). See [Programmable LCLK Phase](#) for details.

## D3 EXT\_REF\_VCM

0 Internal reference mode

1 External reference mode, Apply voltage on VCM input

See section [EXTERNAL REFERENCE MODE](#)

To use this mode, the register bit <EN\_EXT\_REF> in register 0xF0 must also be set to 1.

| A7-A0 IN HEX | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1             | D0               |
|--------------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----------------|------------------|
| 45           | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | <SYNC PATTERN> | <DESKEW PATTERN> |

## D1 <SYNC PATTERN>

0 Sync pattern disabled

1 Sync pattern enabled.

All channels output a repeating pattern of 8 1s and 8 0s instead of ADC data.

Output data [15...0] = 0xFF00

## D1 <DESKEW PATTERN>

0 Deskew pattern disabled

1 Deskew pattern enabled.

All channels output a repeating pattern of 1010101010101010 instead of ADC data.

| A7-A0<br>IN HEX | D15                           | D14 | D13 | D12                        | D11                        | D10                        | D9 | D8 | D7 | D6 | D5              | D4 | D3             | D2            | D1 | D0                     |
|-----------------|-------------------------------|-----|-----|----------------------------|----------------------------|----------------------------|----|----|----|----|-----------------|----|----------------|---------------|----|------------------------|
| 46              | <ENABLE<br>SERIALI<br>ZATION> | 0   | 0   | <18b<br>SERIALI<br>ZATION> | <16b<br>SERIALI<br>ZATION> | <14b<br>SERIALI<br>ZATION> | 0  | 0  | 0  | 0  | <PAD<br>two 0s> | 0  | <MSB<br>FIRST> | <2S<br>COMPL> | 0  | <2-WIRE 0.5X<br>FRAME> |

**D15 <ENABLE SERIALIZATION> Enable bit for serialization bits in register 46>**

- 0 Disable control of serialization register bits in register 0x46.
- 1 Enable control of serialization register bits in register 0x46.

**D12 <18b SERIALIZATION> Enable 18-bit serialization, to be used to send 18-bit data when using digital processing modes (see section [PERFORMANCE WITH DIGITAL PROCESSING BLOCKS](#))**

- 0 Disable 18-bit serialization.
- 1 Enable 18-bit serialization. ADC data bits D[17..0] are serialized.

**D11 <16b SERIALIZATION> Enable 16-bit serialization, to be used in 16-bit ADC mode**

- 0 Disable 16-bit serialization.
- 1 Enable 16-bit serialization. ADC data bits D[15..0] are serialized.

**D10 <14b SERIALIZATION> Enable 14-bit serialization, to be used in 14-bit ADC mode**

- 0 Disable 14-bit serialization.
- 1 Enable 14-bit serialization. ADC data bits D[13..0] are serialized.

**D5 <PAD two 0s>**

- 0 Padding disabled
- 1 Two zero bits are padded to the ADC data on the LSB side and the combined data is then serialized. When the bit <4b SERIALIZATION> is also enabled, two zero bits are padded to the 14-bit ADC data. The combined data (= ADC[13..0],0,0) is serially output.

**D3 <MSB First>**

- 0 ADC data is output serially, with LSB bit first.
- 1 ADC data is output serially, with MSB bit first.

**D2 <2s COMPL>**

- 0 Output data format is offset binary.
- 1 Output data format is 2s complement.

**D0 <2-WIRE 0.5x frame clock>**

- 0 Enables 1-wire LVDS interface with 1x frame clock
- 1 Enables 2-wire LVDS interface with 0.5x frame clock

| A7-A0<br>IN HEX | D15                | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0                  |
|-----------------|--------------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|---------------------|
| B3              | ENABLE<br>ADC MODE | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 16B/14B<br>ADC MODE |

**D15 <ENABLE ADC MODE>**

- 0 Disable selection of 14-bit ADC mode
- 1 Enables selection of 14 bit ADC mode

**D0 <16B/14B ADC MODE>**

- 0 16-bit ADC operation is enabled
- 1 14-bit ADC operation is enabled

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| A7–A0<br>IN HEX | D15       | D14 | D13 | D12 | D11                | D10 | D9 | D8                 | D7 | D6 | D5                 | D4 | D3 | D2 | D1 | D0 |
|-----------------|-----------|-----|-----|-----|--------------------|-----|----|--------------------|----|----|--------------------|----|----|----|----|----|
| 50              | <EN MAP1> | 0   | 0   | 0   | <MAP_Ch1234_OUT2A> |     |    | <MAP_Ch1234_OUT1B> |    |    | <MAP_Ch1234_OUT1A> |    |    |    |    |    |

## D15 <EN MAP1>

- 0 Mapping function for outputs OUT1A, OUT1B, and OUT2A is disabled.
- 1 Mapping function for outputs OUT1A, OUT1B, and OUT2A is *enabled*.

## D3–D0 <MAP\_Ch1234\_OUT1A>

- 0000 MSB byte corresponding to input IN1 is output on OUT1A.
- 0001 LSB byte corresponding to input IN1 is output on OUT1A.
- 0010 MSB byte corresponding to input IN2 is output on OUT1A.
- 0011 LSB byte corresponding to input IN2 is output on OUT1A.
- 0100 MSB byte corresponding to input IN3 is output on OUT1A.
- 0101 LSB byte corresponding to input IN3 is output on OUT1A.
- 0110 MSB byte corresponding to input IN4 is output on OUT1A.
- 0111 LSB byte corresponding to input IN4 is output on OUT1A.
- 1xxx OUT1A LVDS buffer is powered down.

## D7–D4 <MAP\_Ch1234\_OUT1B>

- 0000 MSB byte corresponding to input IN1 is output on OUT1B.
- 0001 LSB byte corresponding to input IN1 is output on OUT1B.
- 0010 MSB byte corresponding to input IN2 is output on OUT1B.
- 0011 LSB byte corresponding to input IN2 is output on OUT1B.
- 0100 MSB byte corresponding to input IN3 is output on OUT1B.
- 0101 LSB byte corresponding to input IN3 is output on OUT1B.
- 0110 MSB byte corresponding to input IN4 is output on OUT1B.
- 0111 LSB byte corresponding to input IN4 is output on OUT1B.
- 1xxx OUT1B LVDS buffer is powered down.

## D11–D8 <MAP\_Ch1234\_OUT2A>

- 0000 MSB byte corresponding to input IN1 is output on OUT2A.
- 0001 LSB byte corresponding to input IN1 is output on OUT2A.
- 0010 MSB byte corresponding to input IN2 is output on OUT2A.
- 0011 LSB byte corresponding to input IN2 is output on OUT2A.
- 0100 MSB byte corresponding to input IN3 is output on OUT2A.
- 0101 LSB byte corresponding to input IN3 is output on OUT2A.
- 0110 MSB byte corresponding to input IN4 is output on OUT2A.
- 0111 LSB byte corresponding to input IN4 is output on OUT2A.
- 1xxx OUT2A LVDS buffer is powered down.

| A7–A0<br>IN HEX | D15       | D14 | D13 | D12 | D11                | D10 | D9 | D8                 | D7 | D6 | D5                 | D4 | D3 | D2 | D1 | D0 |
|-----------------|-----------|-----|-----|-----|--------------------|-----|----|--------------------|----|----|--------------------|----|----|----|----|----|
| 51              | <EN MAP2> | 0   | 0   | 0   | <MAP_Ch1234_OUT3B> |     |    | <MAP_Ch1234_OUT3A> |    |    | <MAP_Ch1234_OUT2B> |    |    |    |    |    |

**D15 <EN MAP2>**

- 0 Mapping function for outputs OUT3B, OUT3A, and OUT2B is disabled.  
 1 Mapping function for outputs OUT3B, OUT3A, and OUT2B is enabled.

**D3–D0 <MAP\_Ch1234\_OUT2B>**

- 0000 MSB byte corresponding to input IN1 is output on OUT2B.  
 0001 LSB byte corresponding to input IN1 is output on OUT2B.  
 0010 MSB byte corresponding to input IN2 is output on OUT2B.  
 0011 LSB byte corresponding to input IN2 is output on OUT2B.  
 0100 MSB byte corresponding to input IN3 is output on OUT2B.  
 0101 LSB byte corresponding to input IN3 is output on OUT2B.  
 0110 MSB byte corresponding to input IN4 is output on OUT2B.  
 0111 LSB byte corresponding to input IN4 is output on OUT2B.  
 1xxx OUT2B LVDS buffer is powered down.

**D7–D4 <MAP\_Ch1234\_OUT3A>**

- 0000 MSB byte corresponding to input IN1 is output on OUT3A.  
 0001 LSB byte corresponding to input IN1 is output on OUT3A.  
 0010 MSB byte corresponding to input IN2 is output on OUT3A.  
 0011 LSB byte corresponding to input IN2 is output on OUT3A.  
 0100 MSB byte corresponding to input IN3 is output on OUT3A.  
 0101 LSB byte corresponding to input IN3 is output on OUT3A.  
 0110 MSB byte corresponding to input IN4 is output on OUT3A.  
 0111 LSB byte corresponding to input IN4 is output on OUT3A.  
 1xxx OUT3A LVDS buffer is powered down.

**D11–D8 <MAP\_Ch1234\_OUT3B>**

- 0000 MSB byte corresponding to input IN1 is output on OUT3B.  
 0001 LSB byte corresponding to input IN1 is output on OUT3B.  
 0010 MSB byte corresponding to input IN2 is output on OUT3B.  
 0011 LSB byte corresponding to input IN2 is output on OUT3B.  
 0100 MSB byte corresponding to input IN3 is output on OUT3B.  
 0101 LSB byte corresponding to input IN3 is output on OUT3B.  
 0110 MSB byte corresponding to input IN4 is output on OUT3B.  
 0111 LSB byte corresponding to input IN4 is output on OUT3B.  
 1xxx OUT3B LVDS buffer is powered down.

| A7–A0<br>IN HEX | D15       | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7                 | D6 | D5 | D4                 | D3 | D2 | D1 | D0 |
|-----------------|-----------|-----|-----|-----|-----|-----|----|----|--------------------|----|----|--------------------|----|----|----|----|
| 52              | <EN MAP3> | 0   | 0   | 0   | 0   | 0   | 0  | 0  | <MAP_Ch1234_OUT4B> |    |    | <MAP_Ch1234_OUT4B> |    |    |    |    |

**D15 <EN MAP3>**

- 0 Mapping function for outputs OUT4A and OUT4B is disabled.  
 1 Mapping function for outputs OUT4A and OUT4B is enabled.

**D3–D0 <MAP\_Ch1234\_OUT4A>**

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0000 MSB byte corresponding to input IN1 is output on OUT4A.  
 0001 LSB byte corresponding to input IN1 is output on OUT4A.  
 0010 MSB byte corresponding to input IN2 is output on OUT4A.  
 0011 LSB byte corresponding to input IN2 is output on OUT4A.  
 0100 MSB byte corresponding to input IN3 is output on OUT4A.  
 0101 LSB byte corresponding to input IN3 is output on OUT4A.  
 0110 MSB byte corresponding to input IN4 is output on OUT4A.  
 0111 LSB byte corresponding to input IN4 is output on OUT4A.  
 1xxx OUT4A LVDS buffer is powered down.

### D7–D4 <MAP\_Ch1234\_OUT4B>

0000 MSB byte corresponding to input IN1 is output on OUT4B.  
 0001 LSB byte corresponding to input IN1 is output on OUT4B.  
 0010 MSB byte corresponding to input IN2 is output on OUT4B.  
 0011 LSB byte corresponding to input IN2 is output on OUT4B.  
 0100 MSB byte corresponding to input IN3 is output on OUT4B.  
 0101 LSB byte corresponding to input IN3 is output on OUT4B.  
 0110 MSB byte corresponding to input IN4 is output on OUT4B.  
 0111 LSB byte corresponding to input IN4 is output on OUT4B.  
 1xxx OUT4B LVDS buffer is powered down.

| A7–A0<br>IN HEX | D15                        | D14 | D13 | D12 | D11              | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|----------------------------|-----|-----|-----|------------------|-----|----|----|----|----|----|----|----|----|----|----|
| 5A to 65        | <EN<br>CUSTOM<br>FILT CH1> | 0   | 0   | 0   | <COEFFn SET CH1> |     |    |    |    |    |    |    |    |    |    |    |
| 66 to 71        | <EN<br>CUSTOM<br>FILT CH2> |     |     |     | <COEFFn SET CH2> |     |    |    |    |    |    |    |    |    |    |    |
| 72 to 7D        | <EN<br>CUSTOM<br>FILT CH3> |     |     |     | <COEFFn SET CH3> |     |    |    |    |    |    |    |    |    |    |    |
| 7E to 89        | <EN<br>CUSTOM<br>FILT CH4> |     |     |     | <COEFFn SET CH4> |     |    |    |    |    |    |    |    |    |    |    |

### D15 <EN CUSTOM FILT CH1> to <EN CUSTOM FILT CH4>

For description of these registers see [Table 12](#)

### D11–D0 <COEFFn SET CH1> to <COEFFn SET CH4>

For description of these registers see [Table 12](#)

| A7–A0<br>IN HEX | D15        | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------|------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| F0              | EN_EXT_REF | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |

### D15 <EN\_EXT\_REF>

0 Internal reference mode.

1 Enable external reference mode using VCM pin, set the register bits in register 0x42.

**TYPICAL CHARACTERISTICS – 16 BIT ADC MODE**

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted)

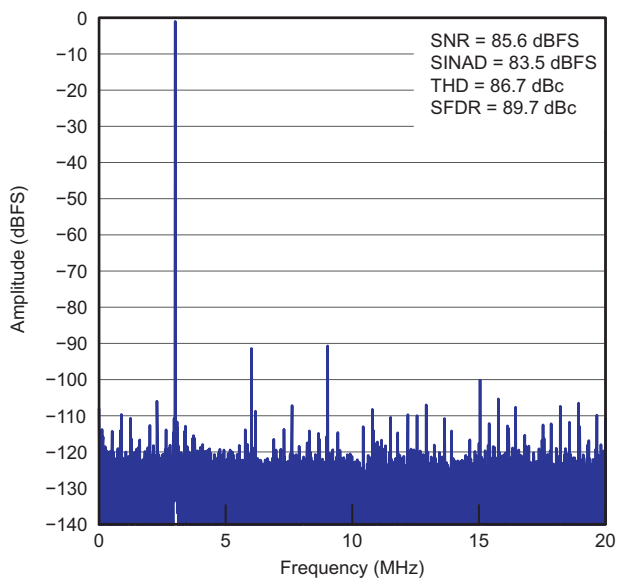


Figure 9. FFT for 3-MHz Input Signal,  $f_s = 40$  MSPS

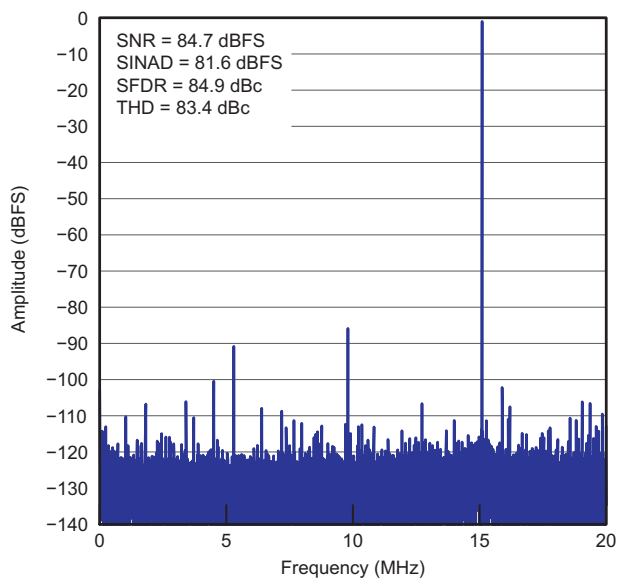


Figure 10. FFT for 15-MHz Input Signal,  $f_s = 40$  MSPS

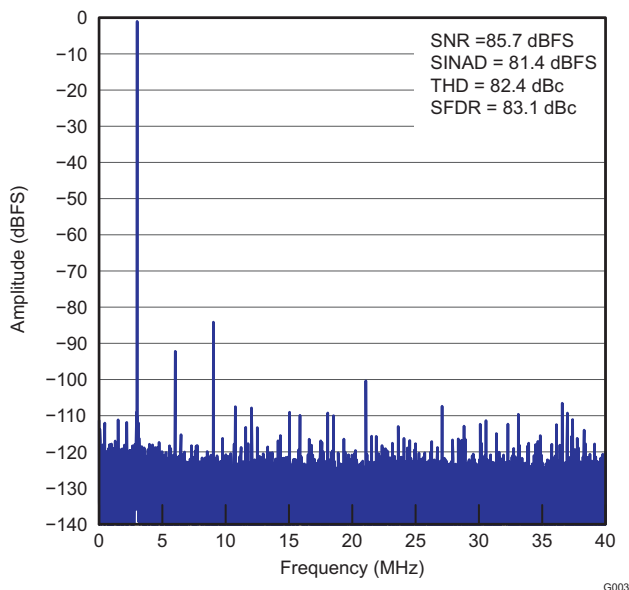


Figure 11. FFT for 3-MHz Input Signal,  $f_s = 80$  MSPS

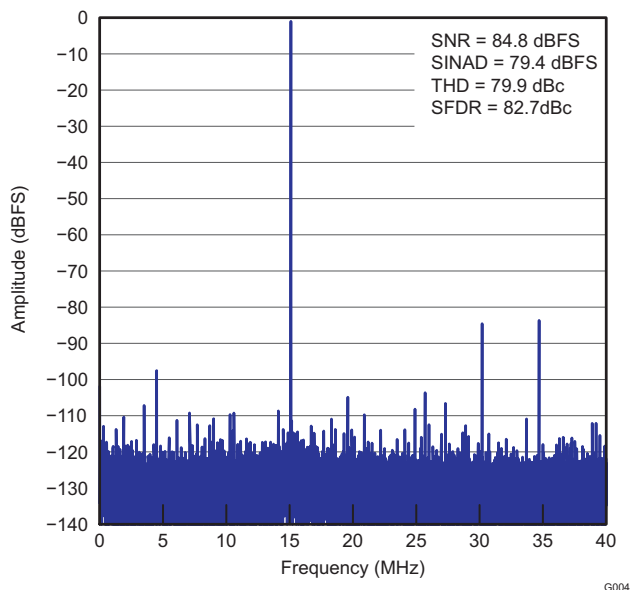


Figure 12. FFT for 15-MHz Input Signal,  $f_s = 80$  MSPS

**TYPICAL CHARACTERISTICS – 16 BIT ADC MODE (continued)**

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted)

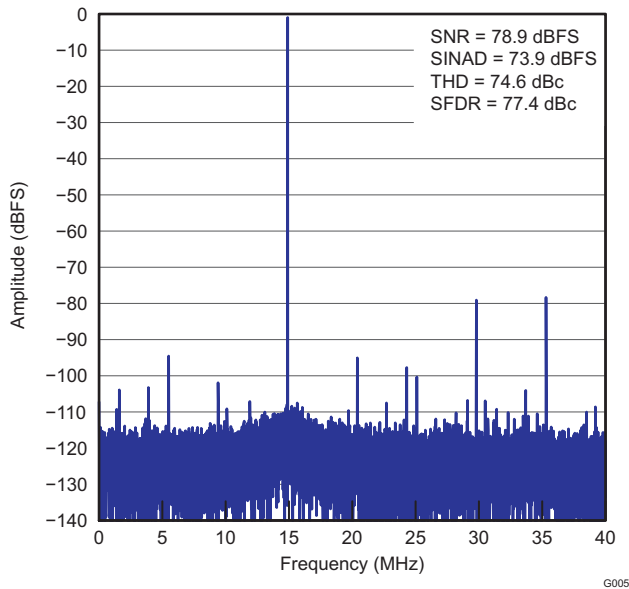


Figure 13. FFT for 65-MHz Input Signal,  $f_s = 80$  MSPS

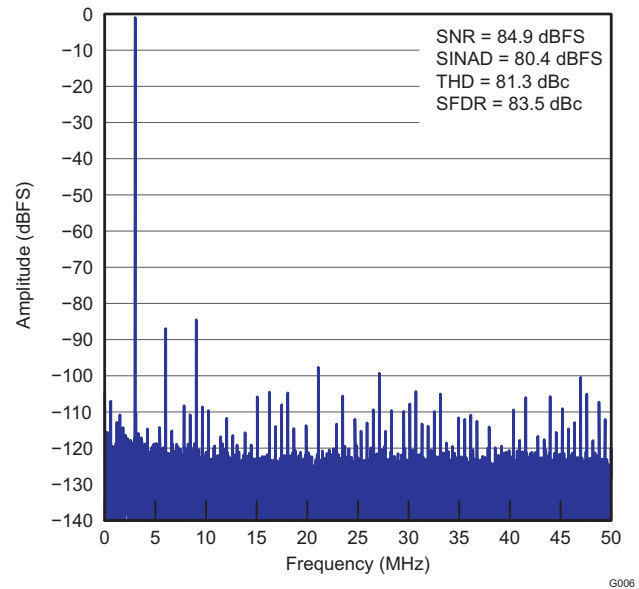


Figure 14. FFT for 3-MHz Input Signal,  $f_s = 100$  MSPS

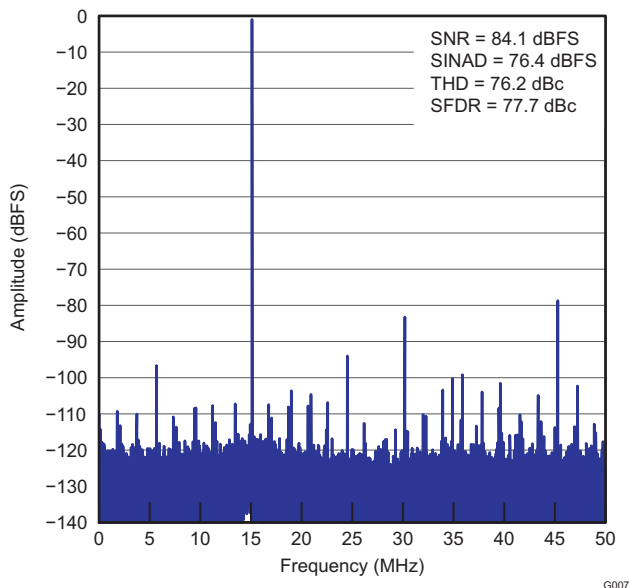


Figure 15. FFT for 15-MHz Input Signal,  $f_s = 100$  MSPS

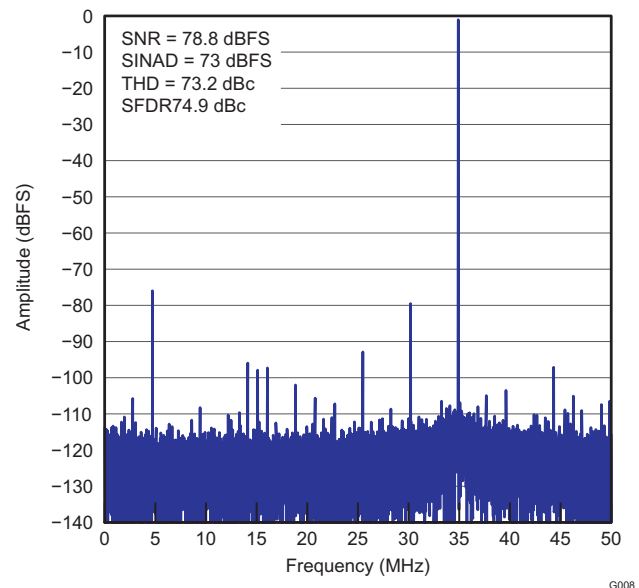


Figure 16. FFT for 65-MHz Input Signal,  $f_s = 100$  MSPS

**TYPICAL CHARACTERISTICS – 16 BIT ADC MODE (continued)**

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V<sub>pp</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted)

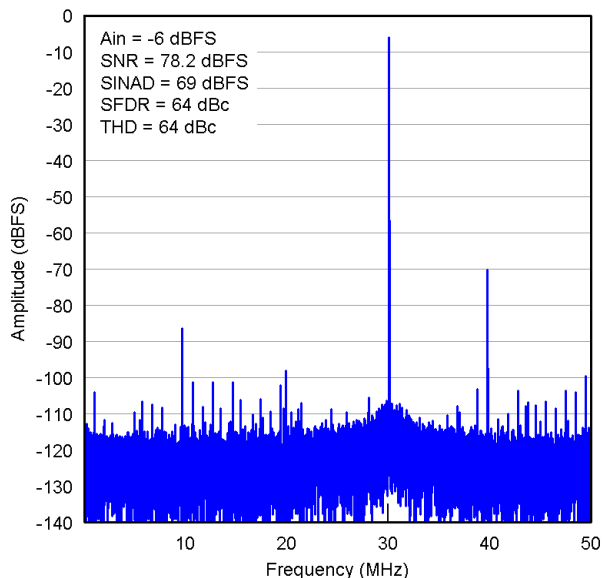


Figure 17. FFT for 130-MHz Input Signal,  $f_s = 100$  MSPS

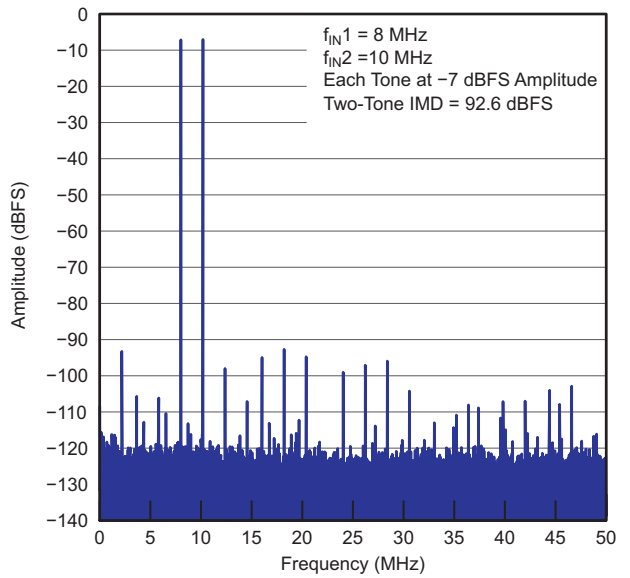


Figure 18. FFT for 2-Tone Input Signal

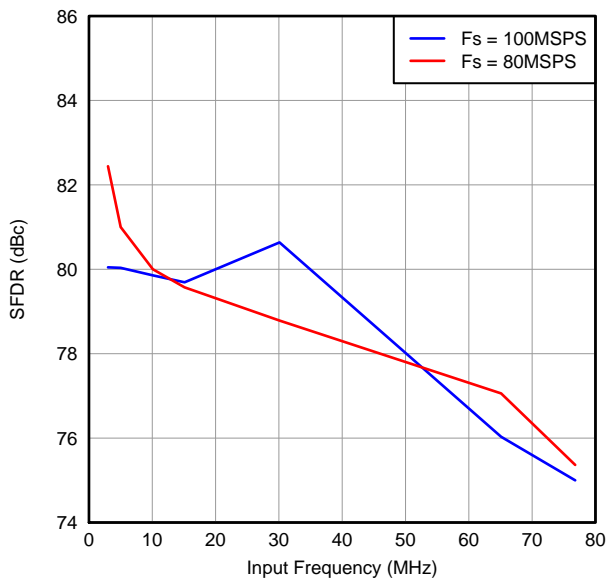


Figure 19. SFDR vs Input Frequency

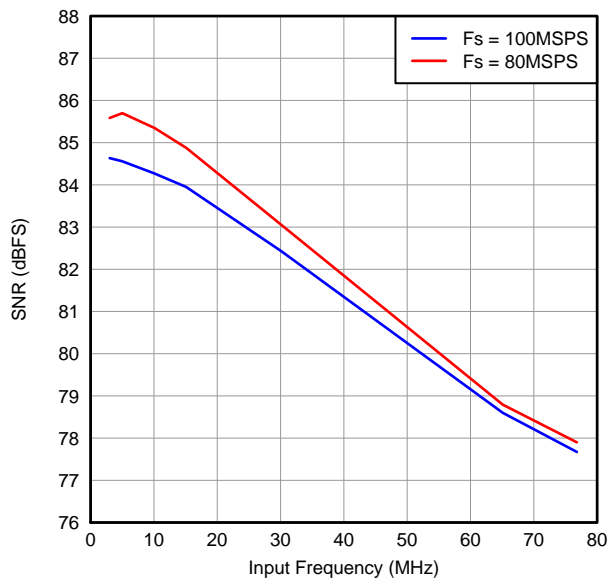


Figure 20. SNR vs Input Frequency

**TYPICAL CHARACTERISTICS – 16 BIT ADC MODE (continued)**

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V<sub>pp</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted)

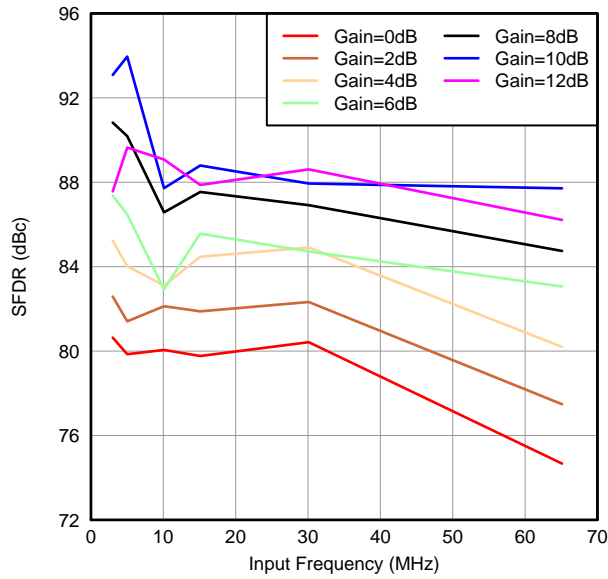


Figure 21. SFDR Across Gain

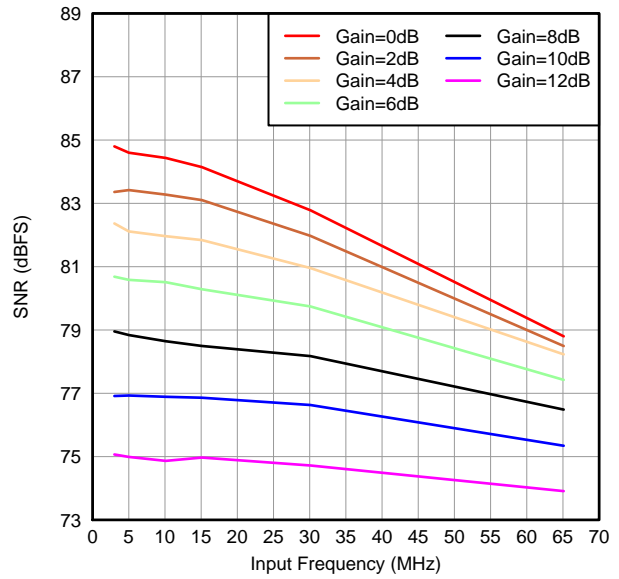


Figure 22. SNR Across Gain

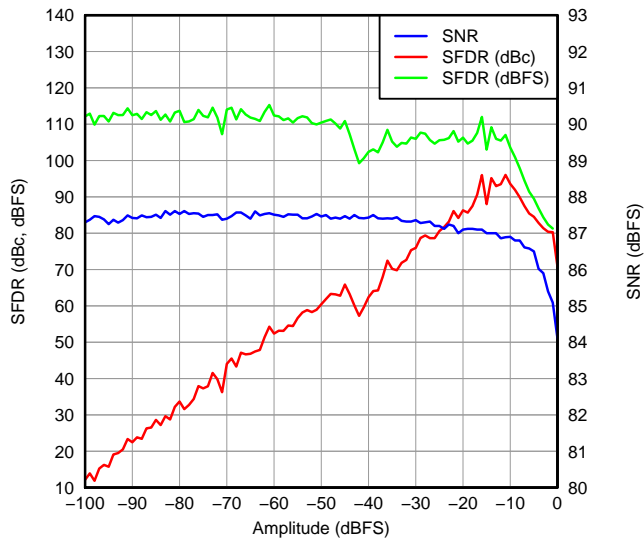


Figure 23. Performance Across Input Amplitude, Single Tone

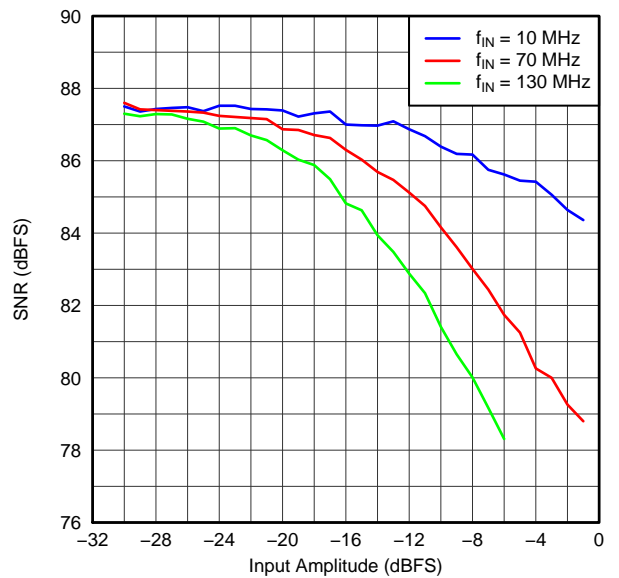


Figure 24. SNR Across Input Amplitude vs Input Frequency

**TYPICAL CHARACTERISTICS – 16 BIT ADC MODE (continued)**

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted)

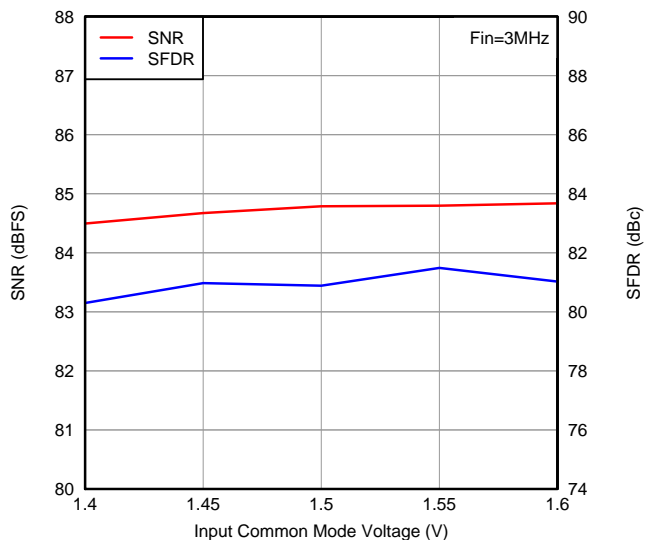


Figure 25. Performance vs Input Common-Mode Voltage

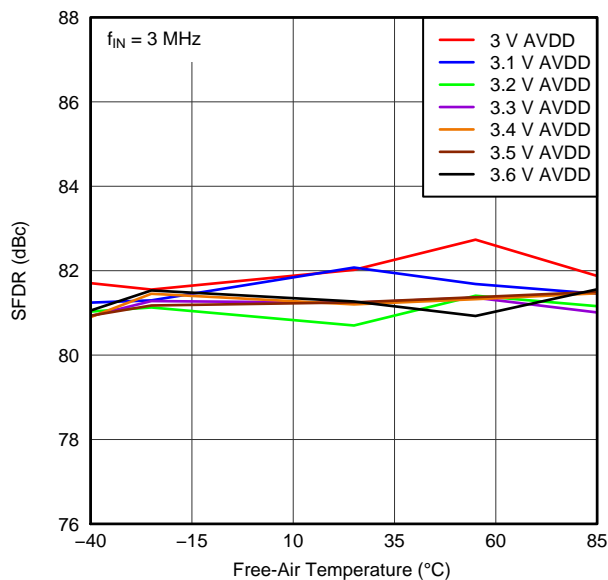


Figure 26. SFDR Across Temperature vs AVDD Supply, Sample Rate = 80 MSPS

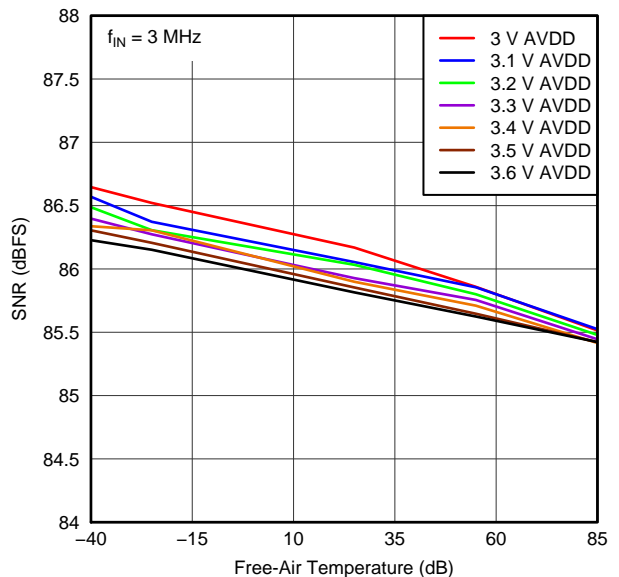


Figure 27. SNR Across Temperature vs AVDD Supply, Sample Rate = 80 MSPS

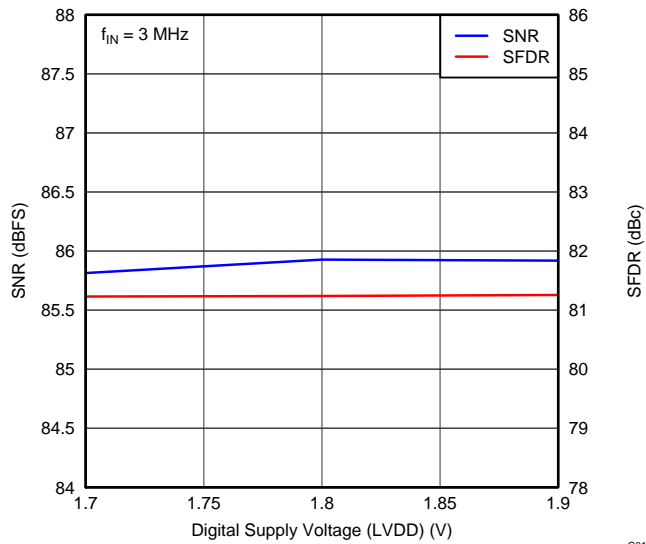


Figure 28. Performance Across LVDD Supply Voltage, Sample Rate = 80 MSPS

**TYPICAL CHARACTERISTICS – 16 BIT ADC MODE (continued)**

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted)

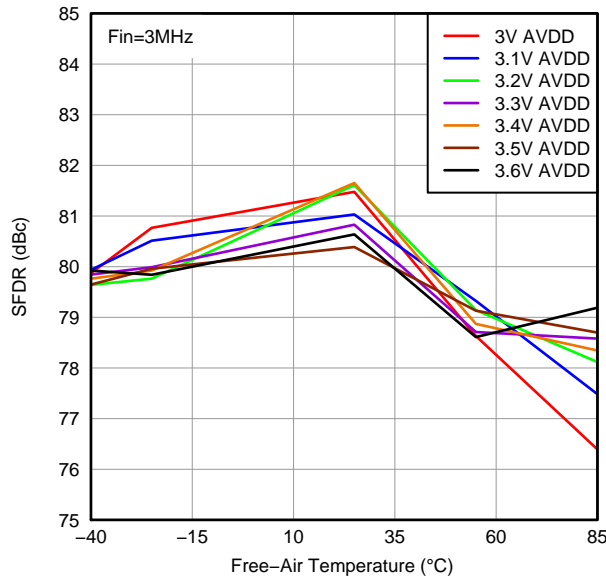


Figure 29. SFDR Across Temperature  
Sample Rate = 100 MSPS

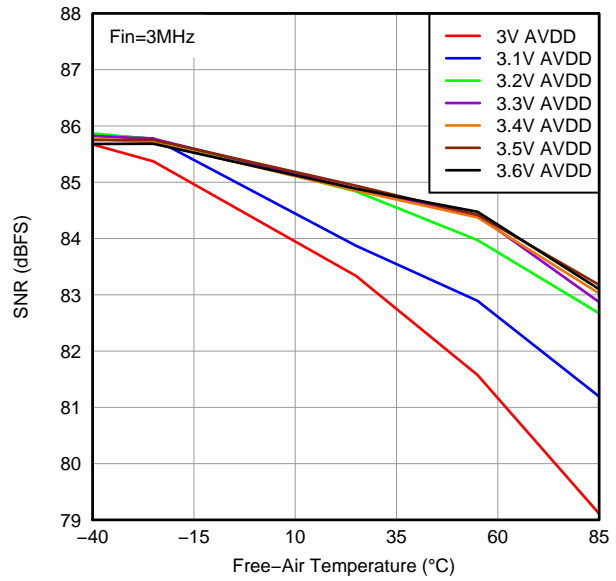


Figure 30. SNR Across Temperature  
Sample Rate = 100 MSPS

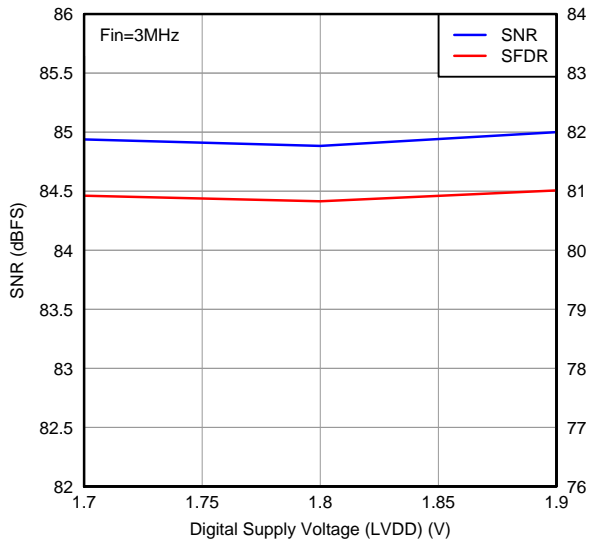


Figure 31. Performance Across LVDD Supply  
Sample Rate = 100 MSPS

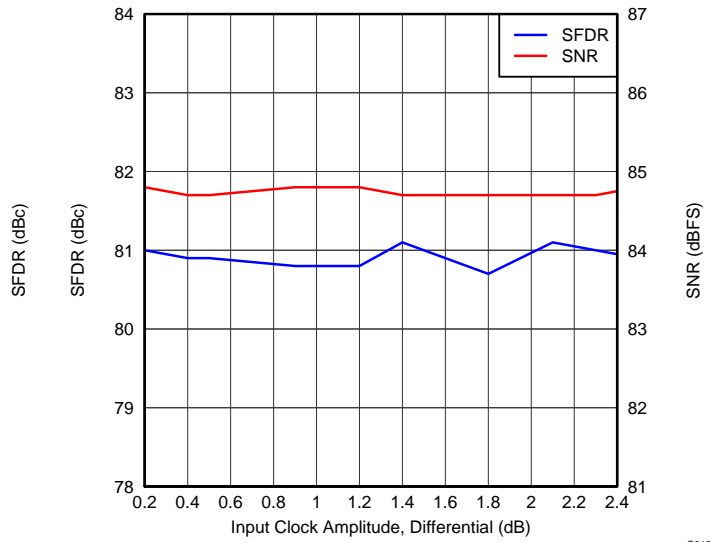


Figure 32. Performance Across Input Clock Amplitude,  
Sample Rate = 100 MSPS

TYPICAL CHARACTERISTICS – 16 BIT ADC MODE (continued)

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted)

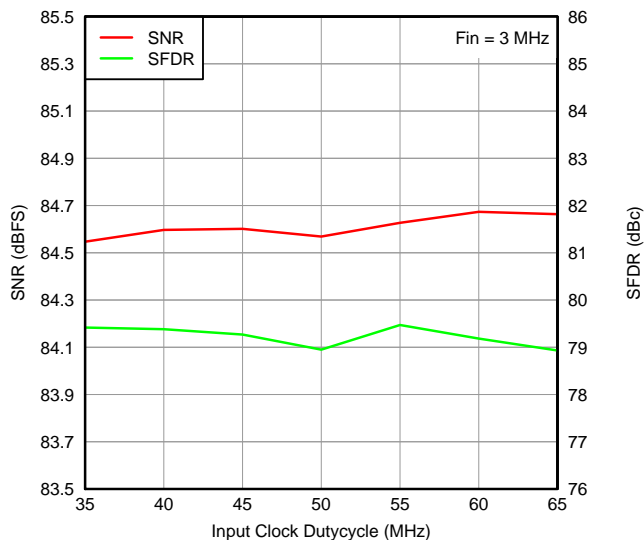


Figure 33. Performance Across Input Clock Duty Cycle, Sample Rate = 100 MSPS

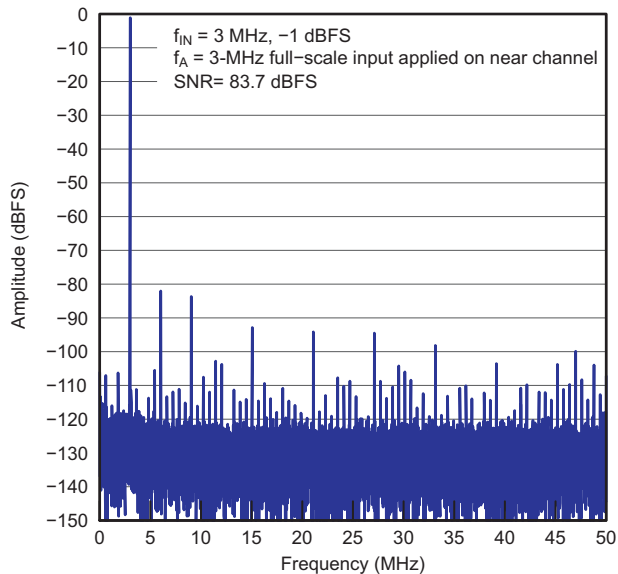


Figure 34. Near-Channel Crosstalk Spectrum, Sample Rate = 100 MSPS

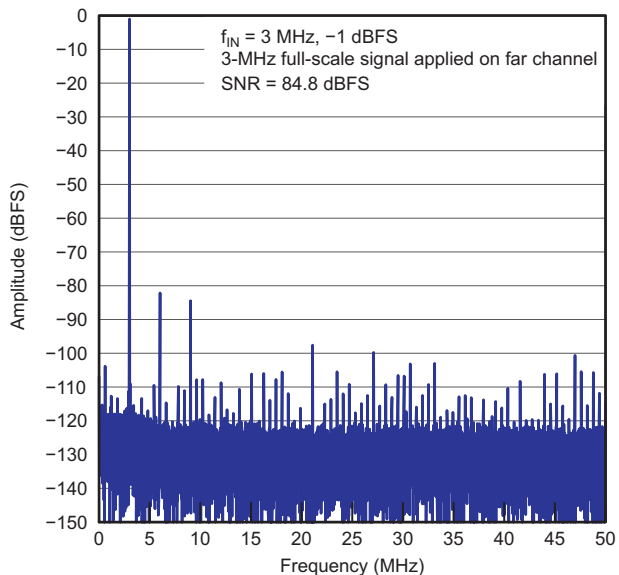


Figure 35. Far-Channel Crosstalk Spectrum

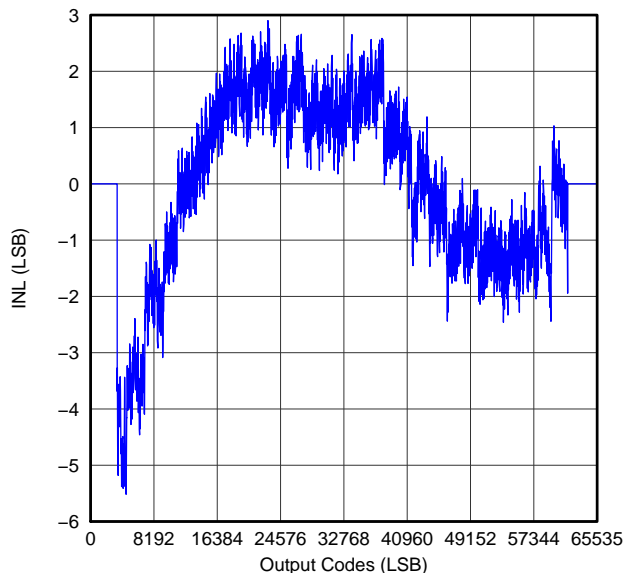
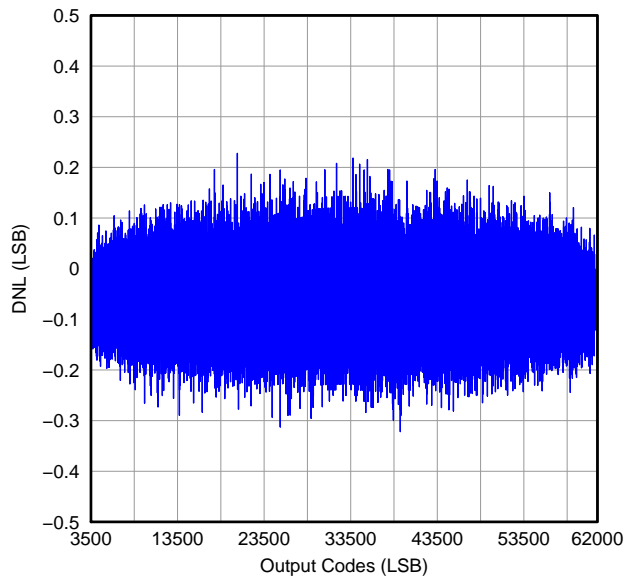


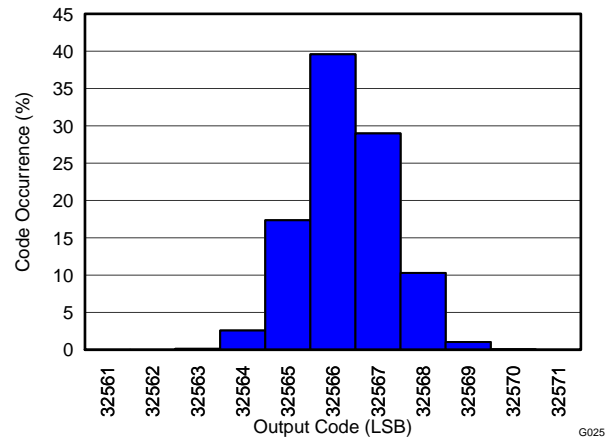
Figure 36. Integral Non-Linearity

### TYPICAL CHARACTERISTICS – 16 BIT ADC MODE (continued)

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted)



**Figure 37. Differential Non-Linearity**



**Figure 38. Histogram of Output Code With Analog Inputs Shorted**

TYPICAL CHARACTERISTICS – 14-BIT ADC MODE

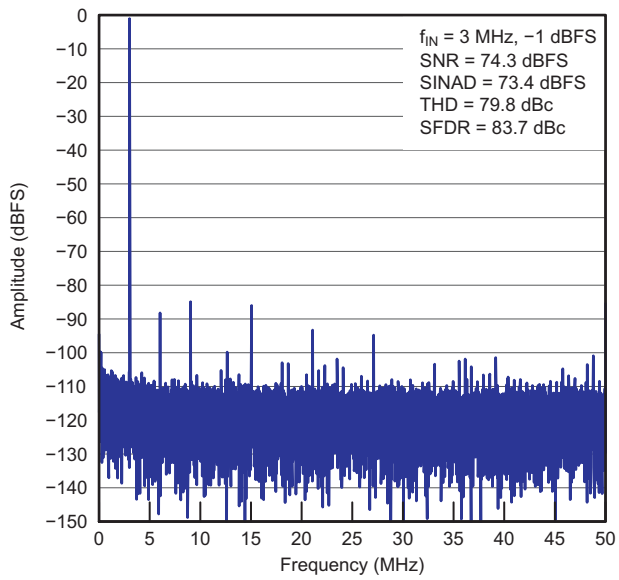


Figure 39. FFT for 3-MHz Input Signal,  $f_s = 100$  MSPS

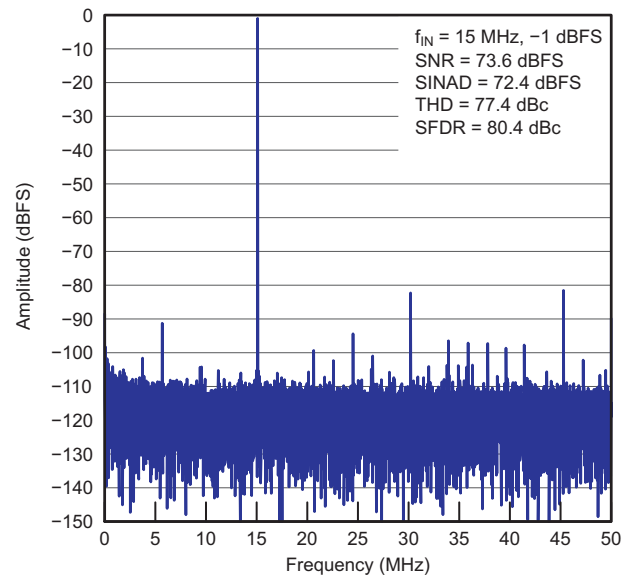


Figure 40. FFT for 15-MHz Input Signal,  $f_s = 100$  MSPS

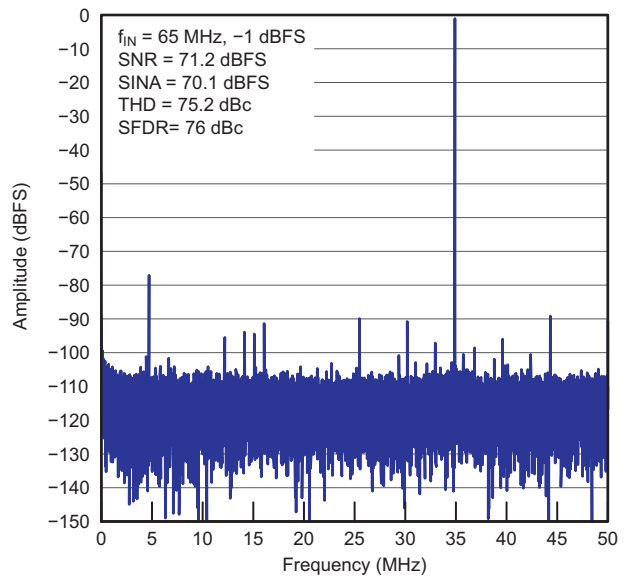


Figure 41. FFT for 65-MHz Input Signal,  $f_s = 100$  MSPS

TYPICAL CHARACTERISTICS – COMMON PLOTS

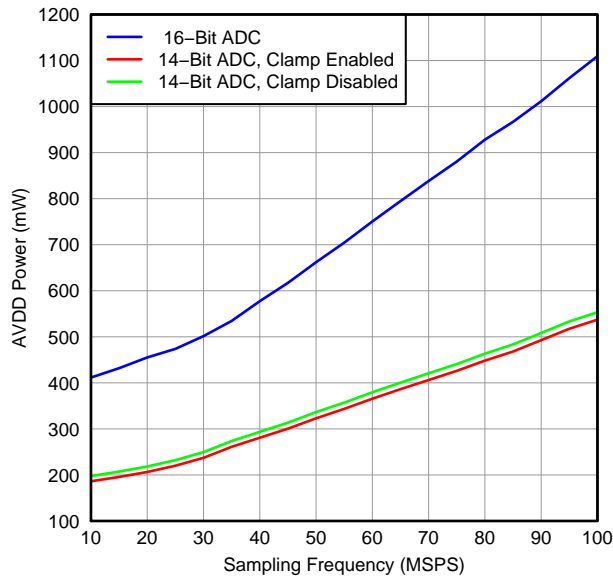


Figure 42. Analog Power Across Sampling Frequencies

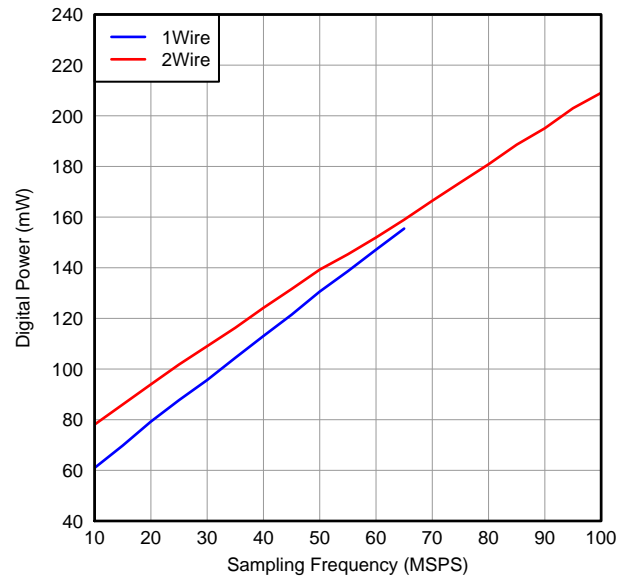


Figure 43. 16-Bit Digital Power Across Sampling Frequencies

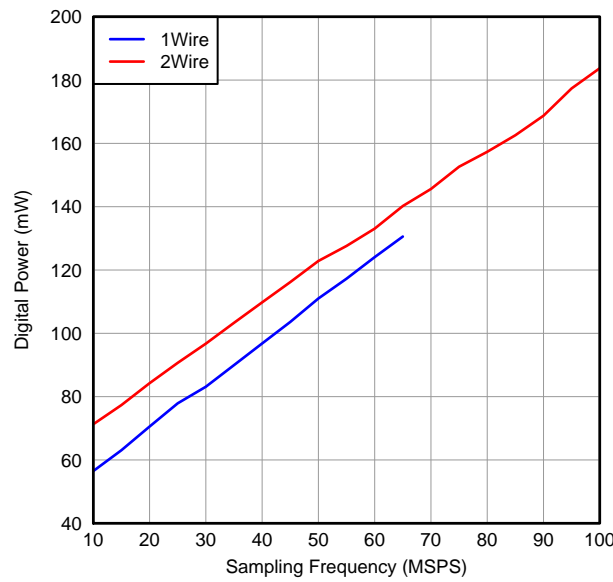


Figure 44. 14-Bit Digital Power Across Sampling Frequencies

TYPICAL CHARACTERISTICS – COMMON PLOTS (continued)

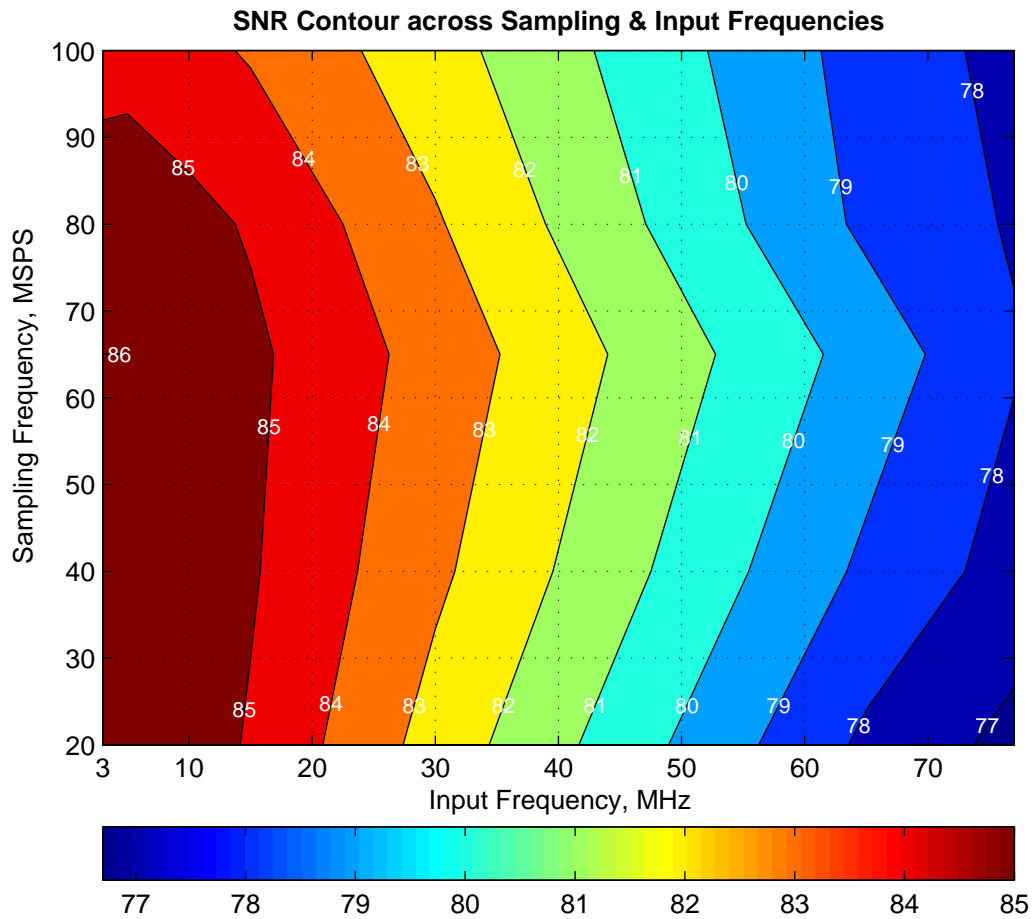


Figure 45. SNR Contour Across Sampling and Input Frequencies, 16-Bit ADC

TYPICAL CHARACTERISTICS – COMMON PLOTS (continued)

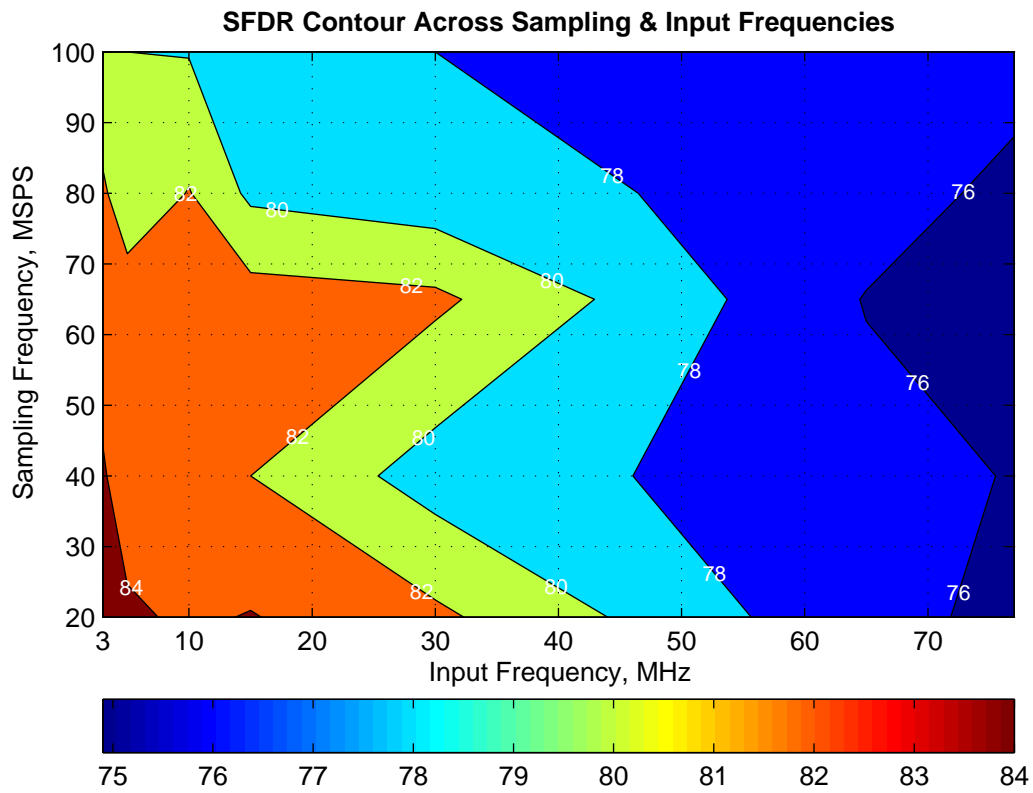


Figure 46. SFDR Contour Across Sampling and Input Frequencies, 16-Bit ADC

TYPICAL CHARACTERISTICS – COMMON PLOTS (continued)

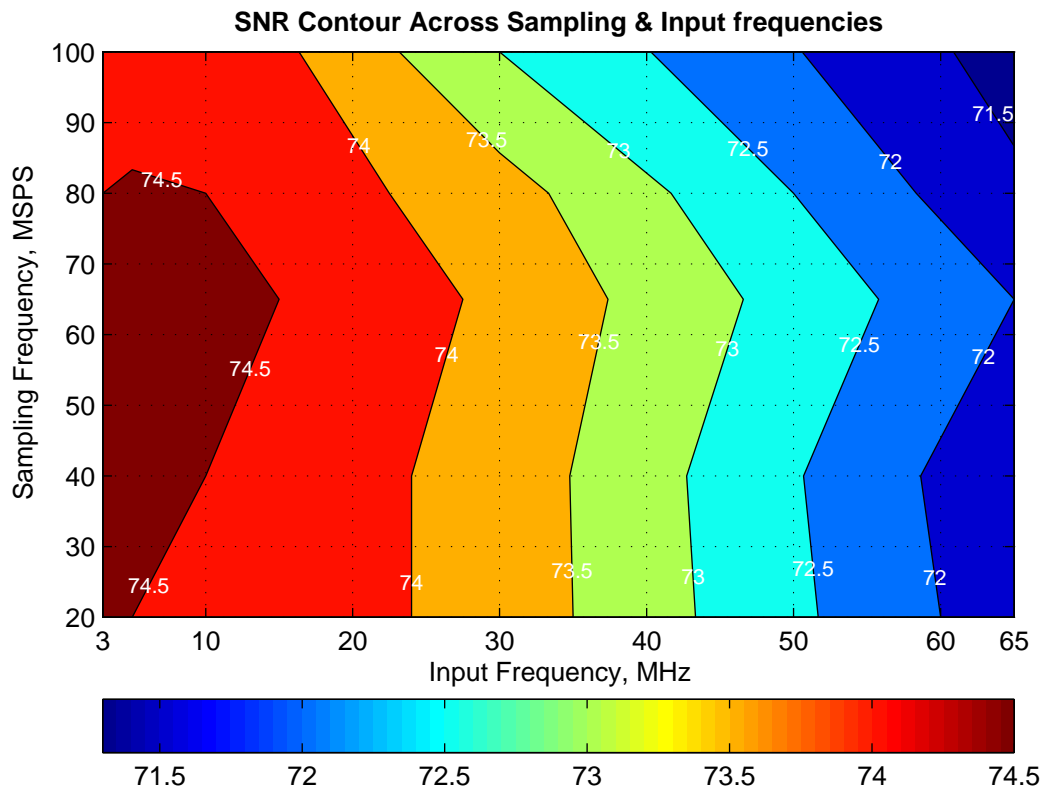


Figure 47. SNR Contour Across Sampling and Input Frequencies, 14-Bit ADC

TYPICAL CHARACTERISTICS – COMMON PLOTS (continued)

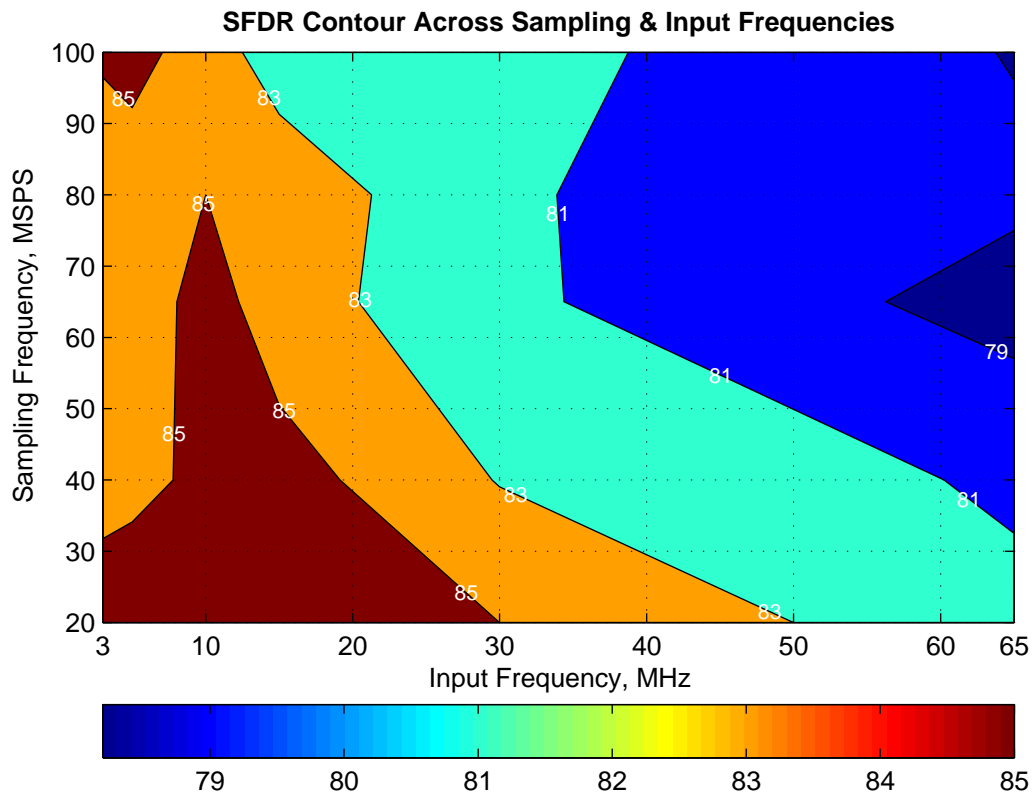


Figure 48. SFDR Contour Across Sampling and Input Frequencies, 14-Bit ADC

## APPLICATION INFORMATION

### THEORY OF OPERATION

ADS5263 is a high-performance 16-bit quad-channel ADC with sample rates up to 100 MSPS.

The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 16 clock cycles. The output is available as 16-bit data in serial LVDS format, coded in either offset binary or binary 2s-complement format.

The device also has a 14-bit low-power mode, where it operates as a quad-channel 14-bit ADC. The 16-bit front-end stage is powered down and the part consumes almost half the power, compared to the 16-bit mode. The ADS5263 can be dynamically switched between the two resolution modes. This allows systems to use the same part in a high-resolution, high-power mode or a low-resolution, low-power mode.

The INxA pins are used as the 16-bit ADC inputs, and the INxB pins function as the 14-bit ADC inputs.

### ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture.

This differential topology results in very good ac performance, even for high input frequencies at high sampling rates. The INxP and INxM pins must be externally biased around a common-mode voltage of 1.5 V, available on the VCM pin. For a full-scale differential input, each input pin INP, INM must swing symmetrically between  $V_{CM} + 1\text{ V}$  and  $V_{CM} - 1\text{ V}$ , resulting in a 4-Vpp differential input swing.

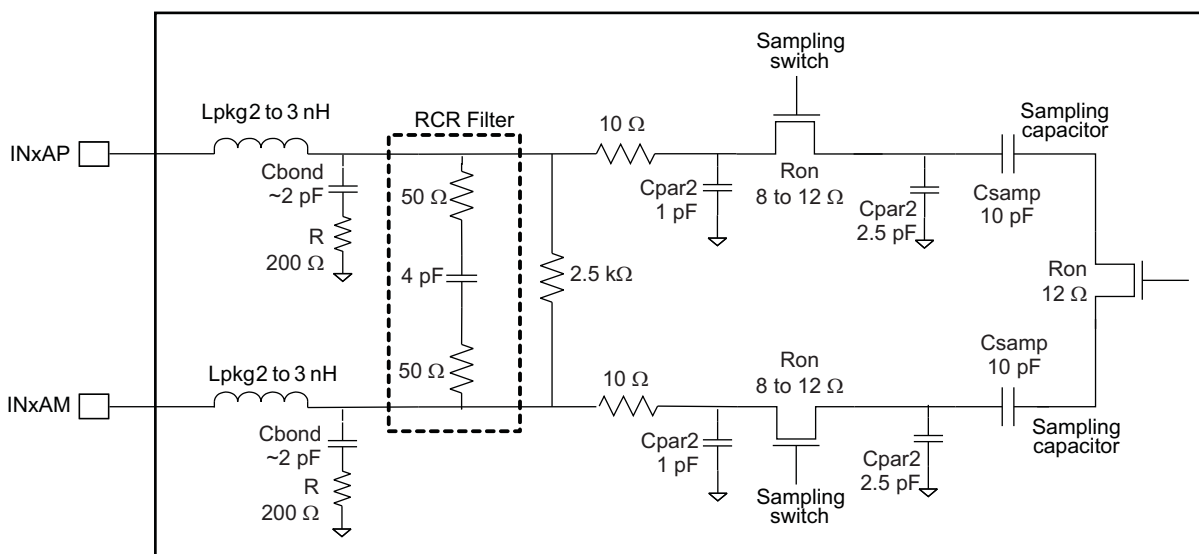


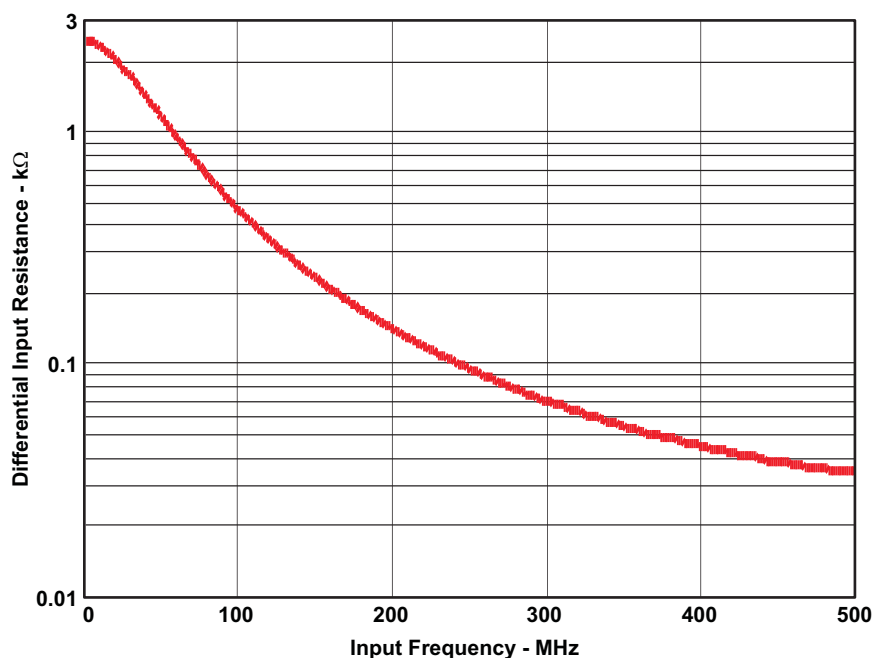
Figure 49. 16-Bit ADC – Analog Input Equivalent Circuit

### Drive Circuit Requirements

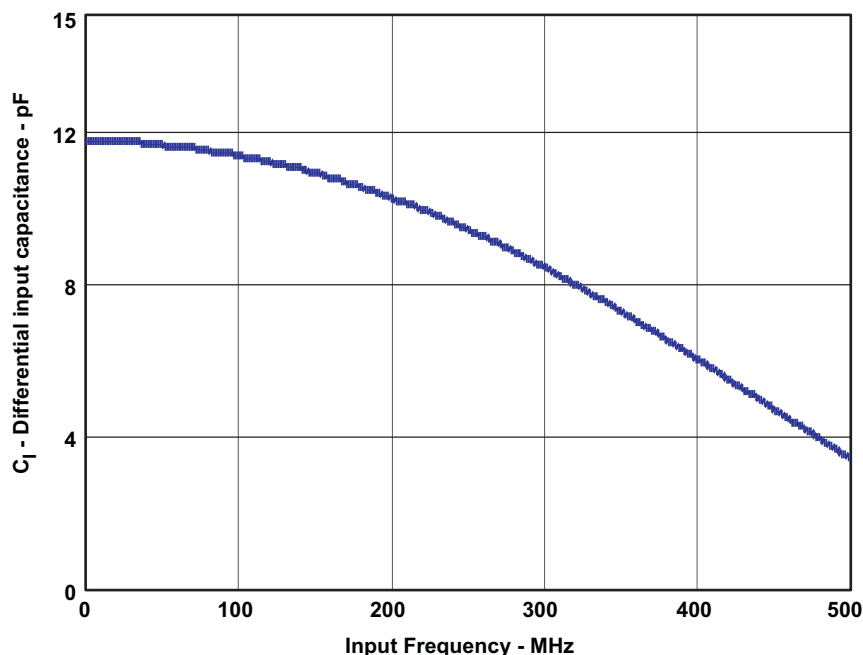
For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics. It is also necessary to present low impedance ( $<50\ \Omega$ ) for the common mode switching currents. This can be achieved by using two resistors from each input terminated to the common mode voltage (VCM).

Note that the device includes an internal R-C-R filter across the input pins. The purpose of the filter is to absorb the glitches caused by the opening and closing of the sampling capacitors. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but also reduces the input bandwidth and the maximum input frequency that can be supported. On the other hand, with no internal R-C filter, high input frequency can be supported, but now the sampling glitches must be supplied by the external driving circuit. The inductance of the package bond wires limits the ability of the drive circuit to support these glitches.

Figure 50 and Figure 51 show the impedance ( $Z_{in} = R_{in} \parallel C_{in}$ ) looking across the differential ADC input pins. While designing the external drive circuit, the ADC input impedance must be considered.



**Figure 50. ADC Analog Input Resistance ( $R_{in}$ ) Across Frequency**

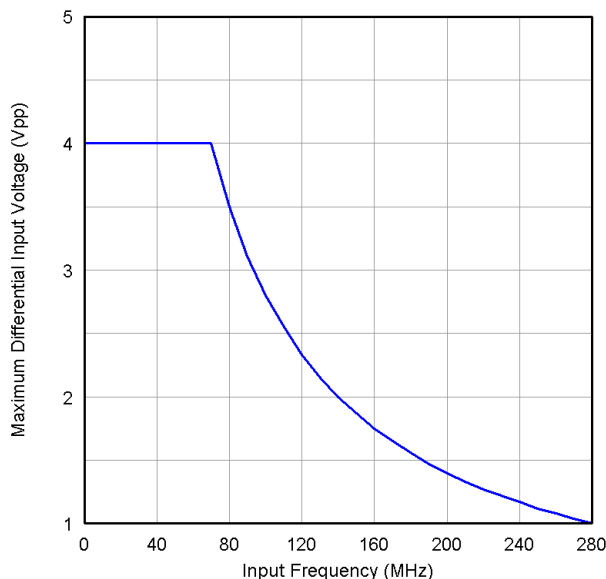


**Figure 51. ADC Analog Input Capacitance ( $C_{IN}$ ) Across Frequency**

## Large and Small Signal Input Bandwidth

The small signal bandwidth of the analog input circuit is high, around 700 MHz. When using an amplifier to drive the ADS5263, the total noise of the amplifier up to the small signal bandwidth must be considered.

The large signal bandwidth of the device depends on the amplitude of the input signal. The ADS5263 supports 4 V<sub>PP</sub> amplitude for input signal frequency up to 70 MHz. For higher frequencies (>70 MHz), the amplitude of the input signal must be decreased proportionally. For example, at 140 MHz, the device supports a maximum of 2 V<sub>PP</sub> signal and at 280 MHz, it can handle a maximum of 1 V<sub>PP</sub>.



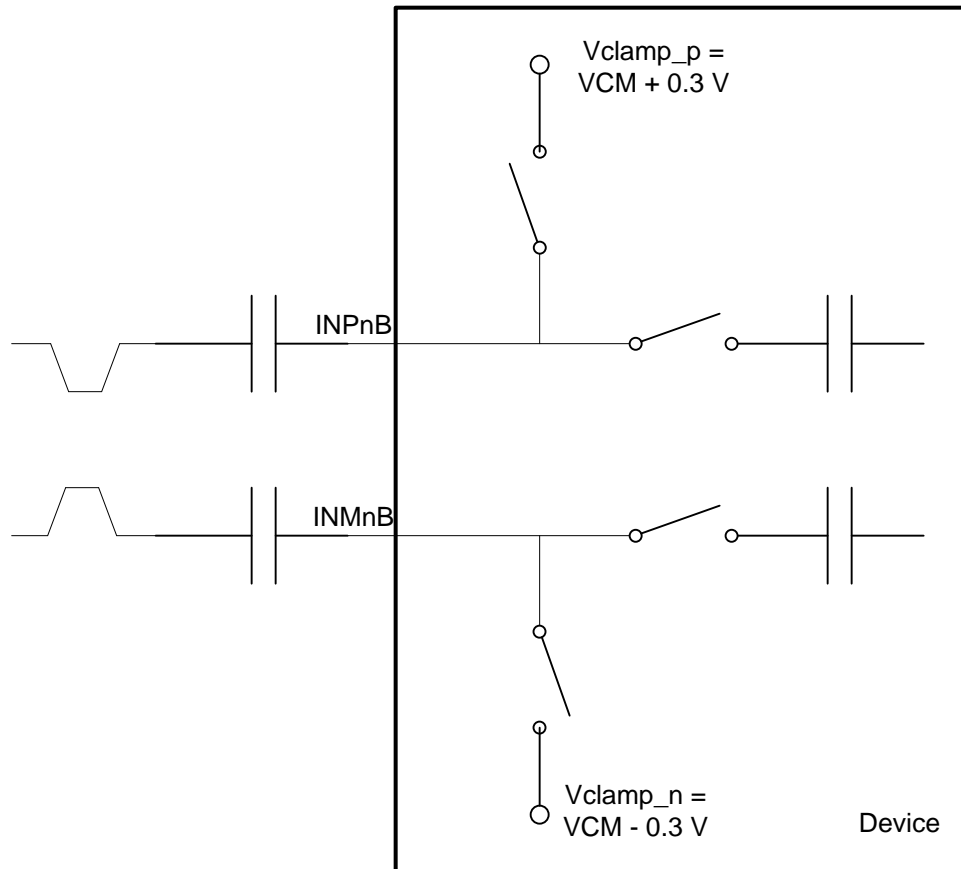
**Figure 52. FullScale Input Amplitude Across Input Frequency**

## CLAMP FUNCTION FOR CCD SIGNALS

The 14-bit ADC analog inputs have an integrated clamp function that can be used to interface to a CCD sensor output.

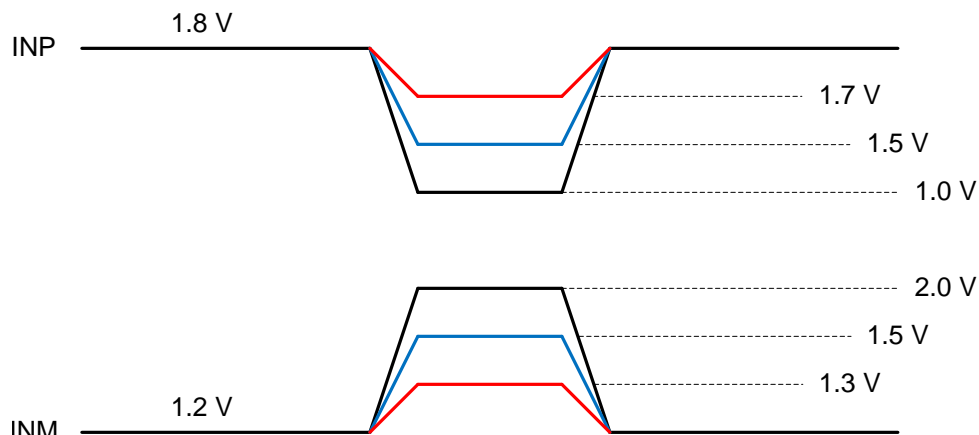
### Differential Input Drive

The clamp function can be used with a differential input signal only. As most CCD signals are single-ended, use either a fully differential amplifier or transformer to translate the single-ended CCD signal to a differential signal for applying to the ADS5263 analog inputs through ac-coupling capacitors, as [Figure 53](#) shows.



**Figure 53. Differential Input Drive with Internal Clamp Mode**

The analog inputs of the ADS5263 are internally clamped to voltages  $V_{clamp\_p}$  (1.8 V, typical) and  $V_{clamp\_n}$  (1.2 V, typical). With a differential input, the voltage on INP can swing from  $V_{clamp\_p}$  down to 1 V, whereas INM swings from  $V_{clamp\_n}$  up to 2 V. This ensures maintaining of the input common-mode at 1.5 V while supporting a differential input swing of 1.6 Vpp.



**Figure 54. Analog Input Voltage Range With Clamp Enabled**

### Clamp Operation

The clamp function can be enabled by setting the register bit <EN\_CLAMP> in register 0x09.

The effect of the clamp operation can be verified by measuring the voltage on the INP and INM pins. With no input signal applied, the voltages on INP and INM will be 1.8 V dc and 1.2 V dc, respectively.

### Synchronization to External CCD Timing

A typical CCD sensor output has three timing phases – a reset phase followed by a reference phase and the actual picture phase.

An internally generated CLAMP clock signal controls the clamping action. The CLAMP clock can be timed to happen during the reset phase of the CCD signal by applying a synchronized high-going pulse on SYNC pin. Once synchronized, the internal CLAMP signal remains high for one ADC clock cycle and low for two clock cycles and repeats in this fashion. Figure 55 shows an oscilloscope snapshot of the external input signals applied to the ADS5263 and the alignment of the CCD signal to the SYNC input. Figure 56 shows the relation between the external signals, the internally generated CLAMP signal, and the data actually sampled by the ADC.

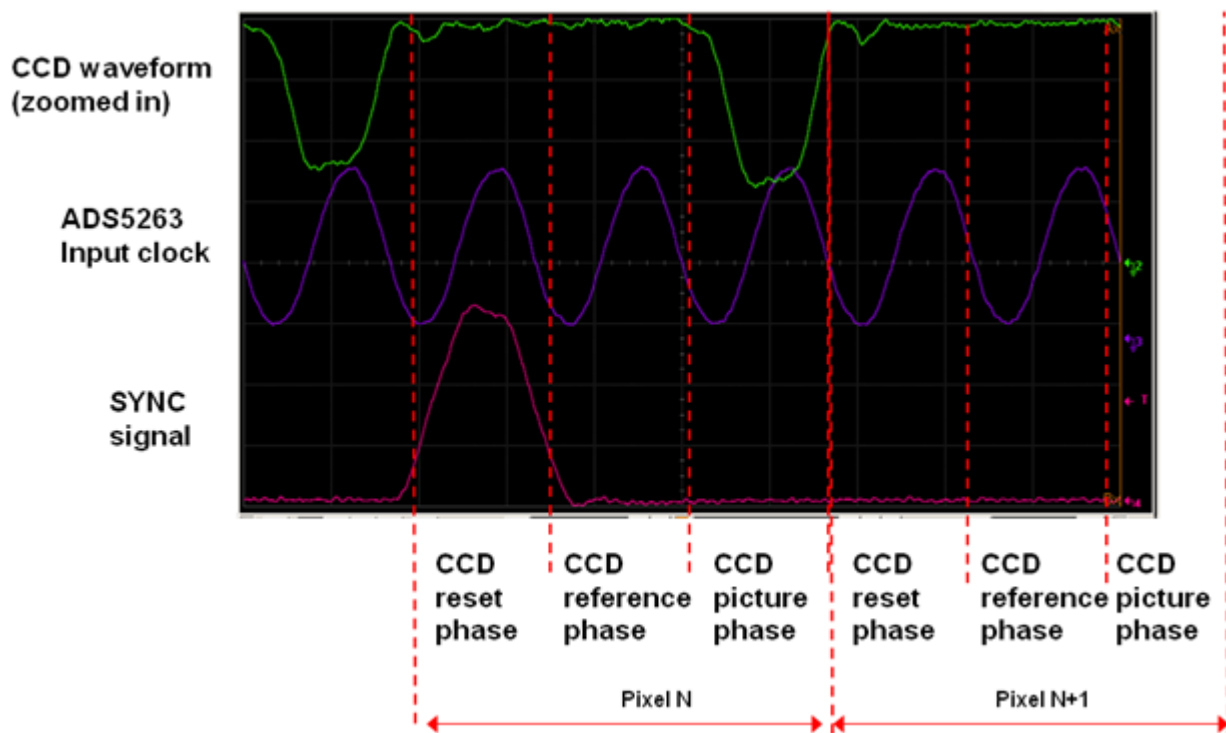
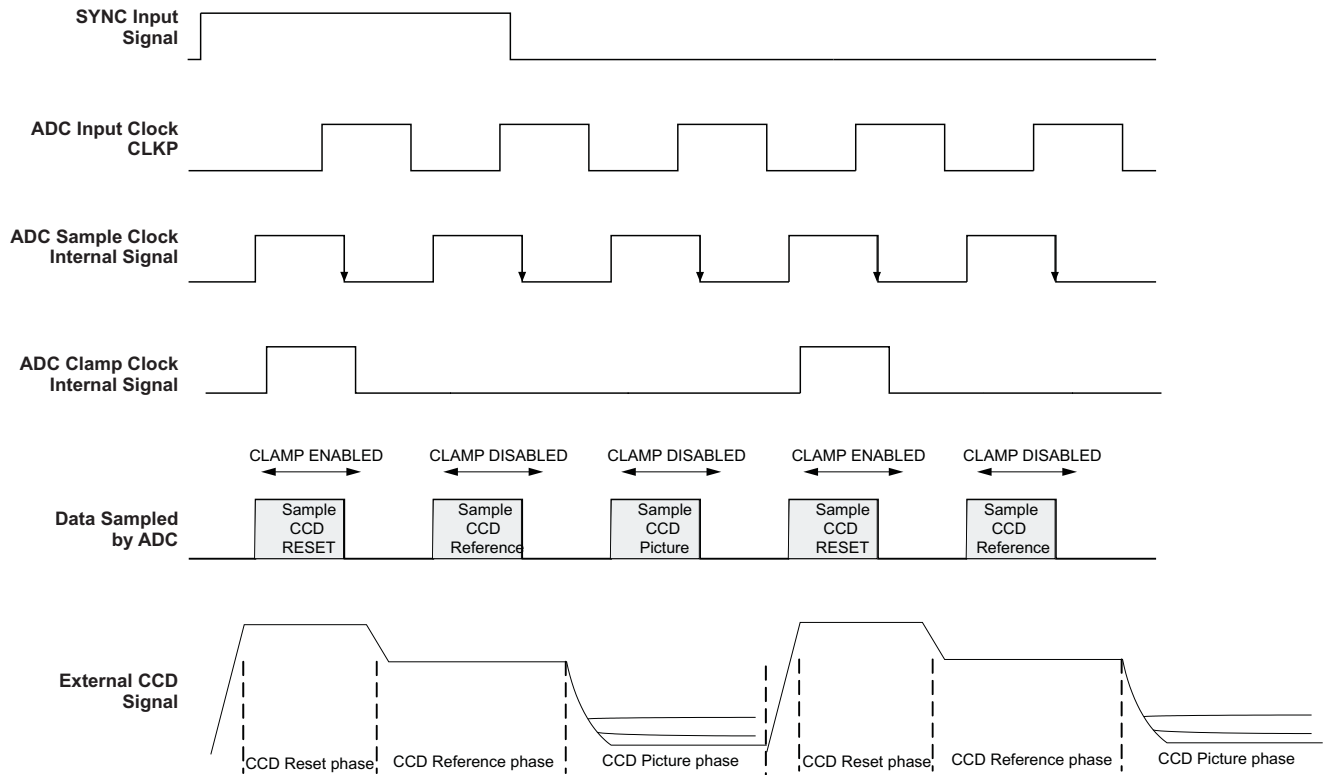


Figure 55. Synchronizing CCD Signal with ADS5263's Clamp Operation Using SYNC signal



**Figure 56. Clamp Timing Diagram**

## LOW-FREQUENCY NOISE SUPPRESSION

The low-frequency noise suppression mode is specifically useful in applications where good noise performance is desired in the low frequency band of dc to 1 MHz. By setting this mode, the low-frequency noise spectrum band around dc is shifted to a similar band around ( $f_s/2$  or Nyquist frequency). As a result, the noise spectrum from dc to about 1 MHz improves significantly as shown by the following spectrum plots.

This function can be selectively enabled in each channel using the register bits **<EN LFNS CH x>**. The following plots show the effect of this mode on the spectrum.

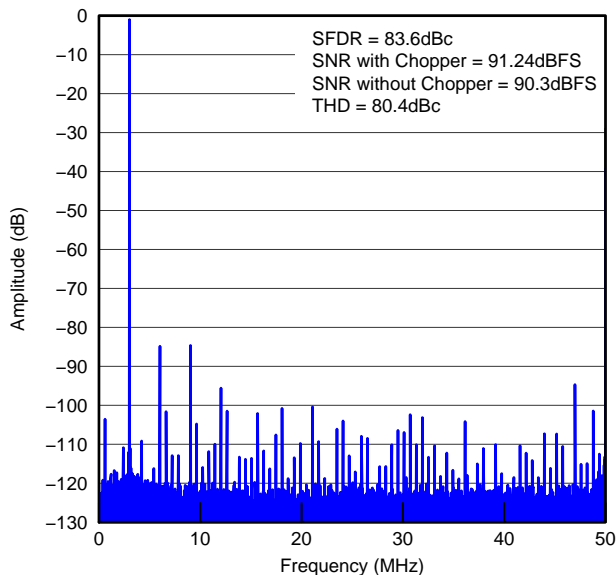


Figure 57. Full-Scale Input Amplitude

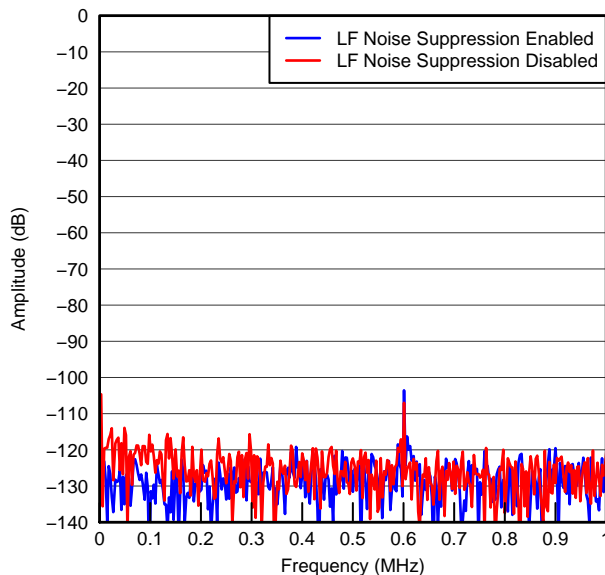


Figure 58. Spectrum (Zoomed) From DC to 1 MHz

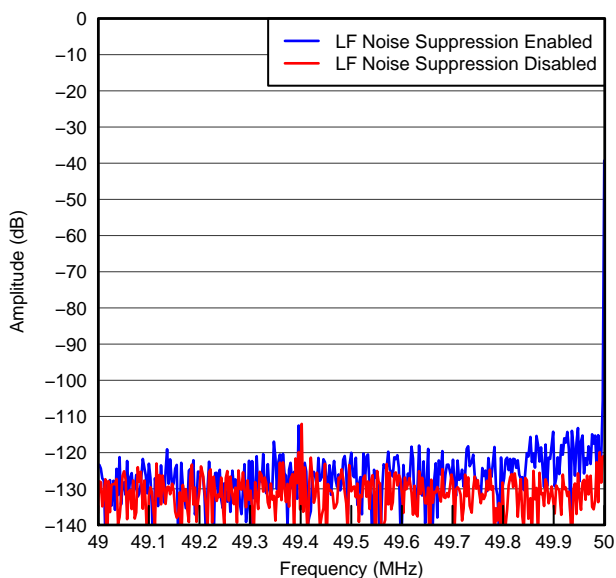


Figure 59. Spectrum (Zoomed) in 1-MHz Band From 49 MHz to 50 MHz ( $f_s=100$  MSPS)

## EXTERNAL REFERENCE MODE

The ADS5263 supports an external reference mode of operation by applying an input voltage on VCM pin.

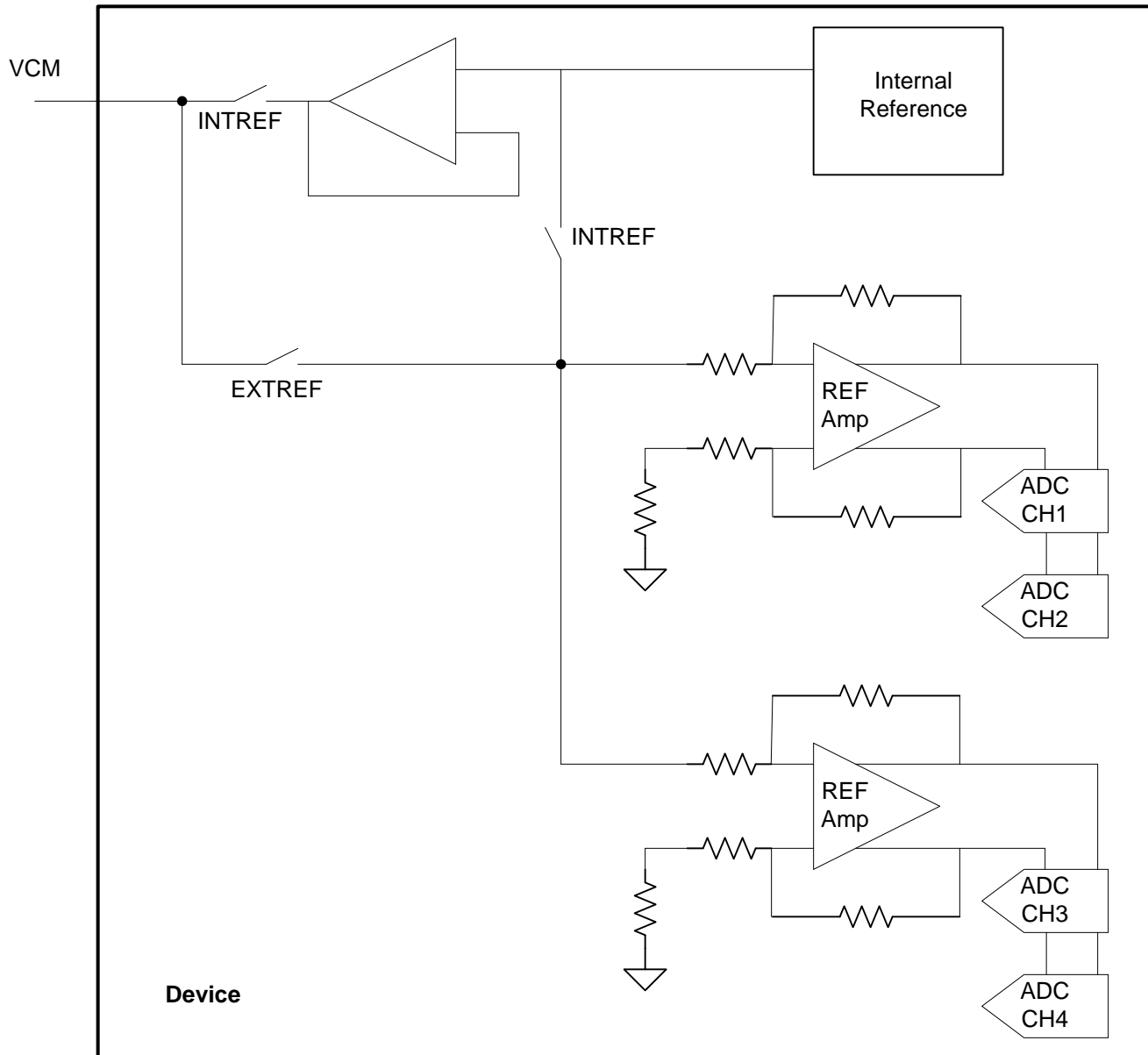
As shown in the figure, in this mode, the reference amplifier is still active. Instead of being driven by the internal band-gap voltage, the reference amplifier is driven by the voltage applied on the VCM pin. By driving the VCM pin with a low drift reference, it is possible to improve the reference temperature drift compared to the internal reference mode. The relation between the full-scale voltage of the ADC and the applied voltage on VCM is

$$\text{Full-scale input voltage} = (8/3) \times V_{\text{REFIN}}$$

To enable this mode, set the register bits as shown in Table 8. This changes the function of the VCM pin to an external reference input pin. The voltage applied on VCM must be  $1.5 \text{ V} \pm 50 \text{ mV}$ . The current drawn by VCM pin in this mode is around 0.5 mA.

**Table 8. Register Settings for External Reference Mode**

| Register Address | Field Name    | Value |
|------------------|---------------|-------|
| 0x01             | EN_HIGH_ADDRS | 1     |
| 0xF0             | EN_EXT_REF    | 1     |
| 0x42             | EN_REG_42     | 1     |
| 0x42             | EXT_REF_VCM   | 1     |


**Figure 60. Reference Block Diagram**

## DIGITAL PROCESSING BLOCKS

The ADS5263 integrates a set of commonly useful digital functions that can be used to ease system design. These functions are shown in the digital block diagram of [Figure 61](#) and described in the following sections.

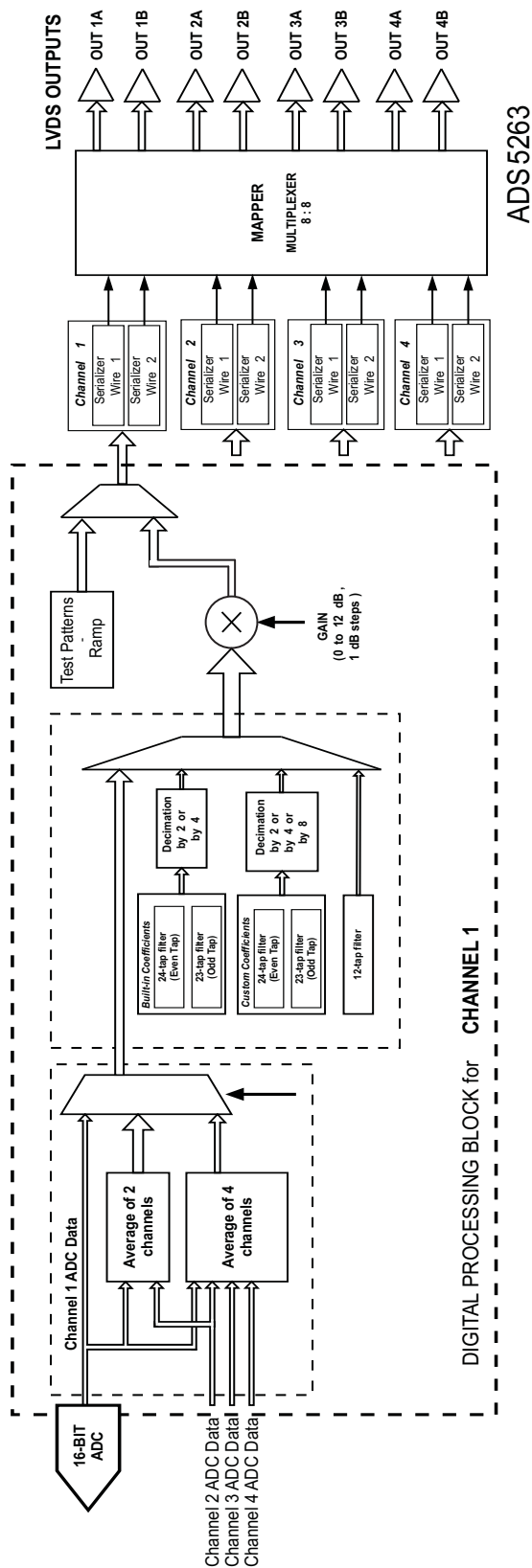


Figure 61. Block Diagram – Digital Processing

## DIGITAL GAIN

ADS5263 includes programmable digital gain settings from 0 dB to 12 dB in steps of 1 dB. The benefit of digital gain is to get improved SFDR performance. The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades by about 1 dB. So, the gain can be used to trade off between SFDR and SNR.

For each gain setting, the analog supported input full-scale range scales proportionally, as shown in [Table 9](#). The full-scale range depends on the ADC mode used (16-bit or 14-bit).

After a reset, the device comes up in the 0-dB gain mode. To use other gain settings, program the **<GAIN CH x>** register bits.

**Table 9. Analog Full-Scale Range Across Gains**

| DIGITAL GAIN,<br>dB | 16-BIT ADC MODE                          | 14-BIT ADC MODE                          |
|---------------------|--|--|
|                     | ANALOG FULL-SCALE INPUT, V <sub>pp</sub> | ANALOG FULL-SCALE INPUT, V <sub>pp</sub> |
| 0                   | 4.00                                     | 2  |
| 1                   | 3.57                                     | 1.78                                     |
| 2                   | 3.18                                     | 1.59                                     |
| 3                   | 2.83                                     | 1.42                                     |
| 4                   | 2.52                                     | 1.26                                     |
| 5                   | 2.25                                     | 1.12                                     |
| 6                   | 2.00                                     | 1.00                                     |
| 7                   | 1.79                                     | 0.89                                     |
| 8                   | 1.59                                     | 0.80                                     |
| 9                   | 1.42                                     | 0.71                                     |
| 10                  | 1.26                                     | 0.63                                     |
| 11                  | 1.13                                     | 0.56                                     |
| 12                  | 1.00                                     | 0.50                                     |

## DIGITAL FILTER

The digital processing block includes the option to filter and decimate the ADC data outputs digitally. Various filters and decimation rates are supported – decimation rates of 2, 4, and 8 and low-pass, high-pass, and band-pass filters are available. The filters are internally implemented as a 24-tap *asymmetric* FIR (even-tap) using pre-defined coefficients following the equation which is described in [Figure 62](#)

Alternatively, some of the filters can be configured as a 23-tap *asymmetric* FIR (or odd-tap filters) following the equation which is described in [Figure 63](#)

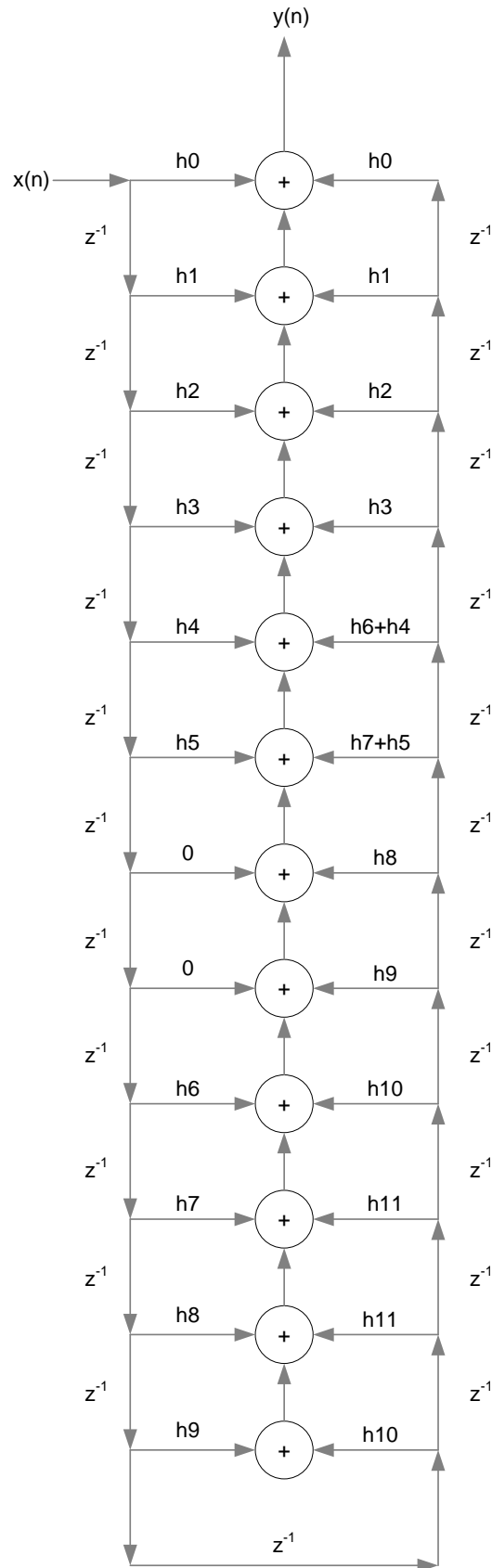


Figure 62. 24-tap Filter Equation

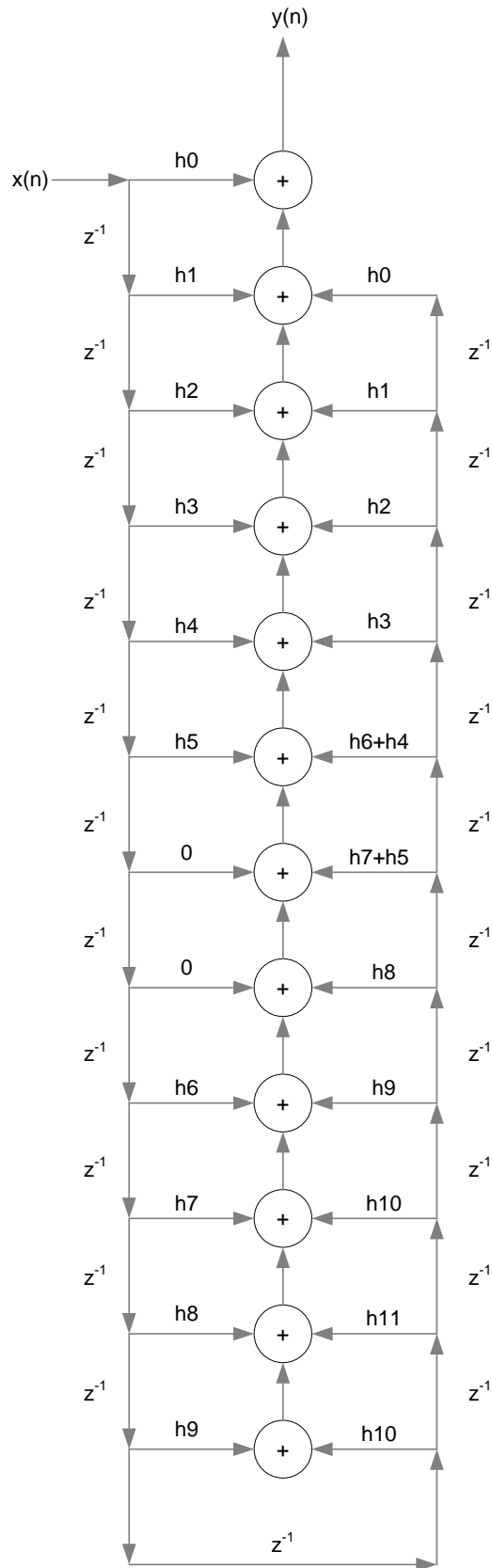


Figure 63. 23-tap Filter Equation

In the equations,

$h_0, h_1 \dots h_{11}$  are 12-bit signed 2s complement representation of the coefficients (-2048 to +2047)

$x(n)$  is the input data sequence to the filter

$y(n)$  is the filter output sequence

Details of the registers used for configuring the digital filters are show in [Table 10](#) and [Table 11](#).

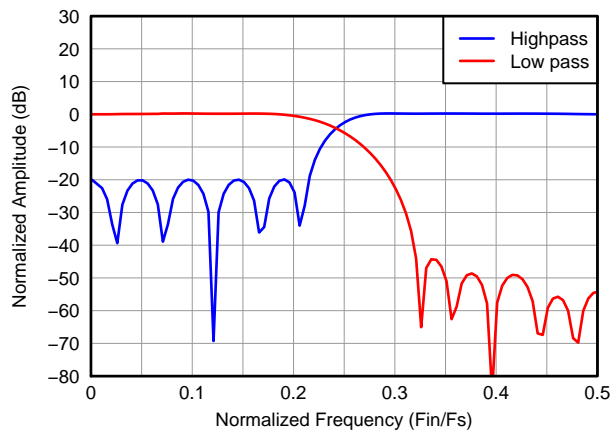
**Table 10. Digital Filter Registers**

| BIT                                     | NAME                 | DESCRIPTION   |
|---|----------------------|---|
| <b>ADDR: 2E, 2F, 30, 31 Default = 0</b> |                      |   |
| D9-D7                                   | FILTER TYPE CHn<2:0> | Selects low-pass, high-pass or band-pass filters        |
| D6-D4                                   | DEC by RATE CHn<2:0> | Selects the decimation rate                             |
| D2                                      | ODD TAP CHn          | Even tap or odd tap                                     |
| D0                                      | USE FILTER CHn       | Enables the filter                                      |
| <b>ADDR: 38, Default = 0</b>            |                      |   |
| D1-D0                                   | OUTPUT RATE<1:0>     | Select output data rate depending on the type of filter |
| <b>ADDR: 29, Default = 0</b>            |                      |   |
| D1                                      | EN DIG FILTER        | Enables digital filter – global control                 |

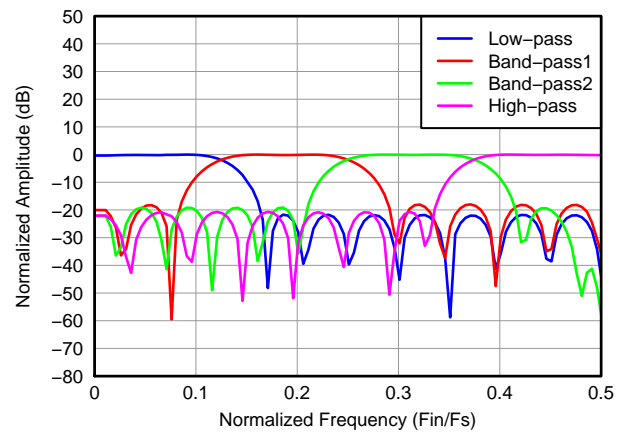
See [Table 11](#) for choosing the right combination of decimation rate and filter types.

**Table 11. Digital Filters**

| DECIMATION                       | TYPE OF FILTER   | <OUTPUT RATE> | DEC by RATE CHx> | <FILTER TYPE CHx> | <SEL ODD TAP> | <USE FILTER CHx> | <EN CUSTOM FILT> | <EN DIG FILTER> |
|----------------------------------|--|---------------|------------------|-------------------|---------------|------------------|------------------|-----------------|
| Decimate by 2                    | Built-in <b>low-pass odd-tap</b> filter (pass band = 0 to $f_s/4$ )                  | 001           | 000              | 000               | 1             | 1                | 0                | 1               |
|                                  | Built-in <b>high-pass odd-tap</b> filter (pass band = 0 to $f_s/4$ )                 | 001           | 000              | 001               | 1             | 1                | 0                | 1               |
| Decimate by 4                    | Built-in <b>low-pass even-tap</b> filter (pass band = 0 to $f_s/8$ )                 | 010           | 001              | 010               | 0             | 1                | 0                | 1               |
|                                  | Built-in first <b>band pass even tap</b> filter (pass band = $f_s/8$ to $f_s/4$ )    | 010           | 001              | 011               | 0             | 1                | 0                | 1               |
|                                  | Built-in second <b>band pass even tap</b> filter (pass band = $f_s/4$ to $3 f_s/8$ ) | 010           | 001              | 100               | 0             | 1                | 0                | 1               |
|                                  | Built-in <b>high pass odd tap</b> filter (pass band = $3 f_s/8$ to $f_s/2$ )         | 010           | 001              | 101               | 1             | 1                | 0                | 1               |
| Decimate by 2                    | Custom filter (user programmable coefficients)                                       | 001           | 000              | 000               | 0 or 1        | 1                | 1                | 1               |
| Decimate by 4                    | Custom filter (user programmable coefficients)                                       | 010           | 001              | 000               | 0 or 1        | 1                | 1                | 1               |
| Decimate by 8                    | Custom filter (user programmable coefficients)                                       | 011           | 100              | 000               | 0 or 1        | 1                | 1                | 1               |
| 12-tap filter without decimation | Custom filter (user programmable coefficients)                                       | 000           | 011              | 000               | 0             | 1                | 1                | 1               |



**Figure 64. Filter Response – Decimate by 2**



**Figure 65. Filter Response – Decimate by 4**

## CUSTOM FILTER COEFFICIENTS

In addition to these built-in filters, customers also have the option of using their own custom 12-bit signed coefficients. Only 12 coefficients can be specified according to [Figure 64](#) or [Figure 65](#). These coefficients (h0 to h11) must be configured in the custom coefficient registers as:

Register content = 12-bit signed representation of [real coefficient value  $\times 2^{11}$ ]

The 12 custom coefficients must be loaded into 12 separate registers for each channel (refer [Table 12](#) ). The MSB bit of each coefficient register decides if the built in filters or custom filters are used. If the MSB bit <EN CUSTOM FILT> is reset to 0, then built in filter coefficients are used. Else, the custom coefficients are used.

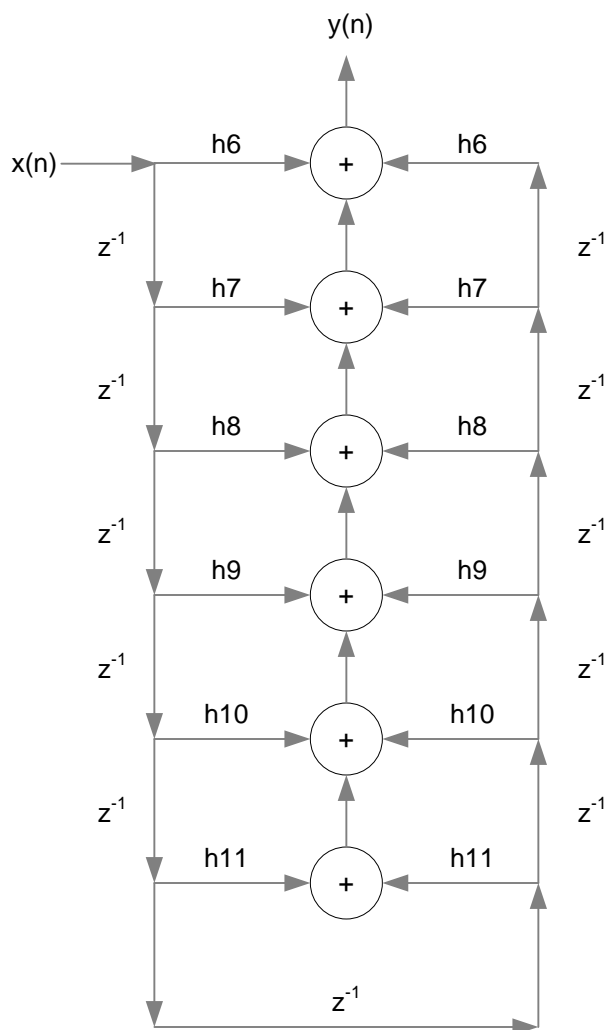
**Table 12. Custom Coefficient Registers** <sup>(1)</sup>

| BIT   | NAME                 | DESCRIPTION  |
|---|----------------------|--|
| <b>ADDR: 5A to 65</b> , Default = 0<br>Set value of h0 in register 0x5A, h1 in 0x5B & so on till h11 in register 0x65 |                      |  |
| D11-D0  | COEFFn SET CH1<11:0> | Custom coefficient for digital filter of channel 1                             |
| D15   | <EN CUSTOM FILT CH1> | 1: Enables custom coefficients to be used<br>0: Built in coefficients are used |
| <b>ADDR: 66 to 71</b> , Default = 0<br>Set value of h0 in register 0x66, h1 in 0x67 & so on till h11 in register 0x71 |                      |  |
| D11-D0  | COEFFn SET CH2<11:0> | Custom coefficient for digital filter of channel 2                             |
| D15   | <EN CUSTOM FILT CH2> | 1: Enables custom coefficients to be used<br>0: Built in coefficients are used |
| <b>ADDR: 72 to 7D</b> , Default = 0<br>Set value of h0 in register 0x72, h1 in 0x73 & so on till h11 in register 0x7D |                      |  |
| D11-D0  | COEFFn SET CH3<11:0> | Custom coefficient for digital filter of channel 3                             |
| D15   | <EN CUSTOM FILT CH3> | 1: Enables custom coefficients to be used<br>0: Built in coefficients are used |
| <b>ADDR: 7E to 89</b> , Default = 0<br>Set value of h0 in register 0x7E, h1 in 0x7F & so on till h11 in register 0x89 |                      |  |
| D11-D0  | COEFFn SET CH4<11:0> | Custom coefficient for digital filter of channel 4                             |
| D15   | <EN CUSTOM FILT CH4> | 1: Enables custom coefficients to be used<br>0: Built in coefficients are used |

(1) Where n = 0 to 11

**CUSTOM FILTER WITHOUT DECIMATION**

Another mode exists to use the digital filter without decimation. In this mode, the filter behaves like a 12-tap *symmetric* FIR filter as per the equation described by [Figure 66](#)



**Figure 66. 12-tap Symmetric Filter Equation**

Where,

$h_6, h_7 \dots h_{11}$  are 12-bit signed 2s complement representation of the coefficients (-2048 to +2047)

$x(n)$  is the input data sequence to the filter

$y(n)$  is the filter output sequence

In this mode, as the filter is implemented as a 12-tap symmetric FIR, only 6 custom coefficients need to be specified and must be loaded in registers  $h_6$  to  $h_{11}$ . [Table 12](#)

To enable this mode, use the register setting specified in the last row of [Table 11](#)

## DIGITAL AVERAGING

The ADS5263 includes an averaging function where the ADC digital data from two (or four) channels can be averaged. The averaged data is output on specific LVDS channels. [Table 13](#) shows the combinations of the input channels that can be averaged and the LVDS channels on which averaged data is available

**Table 13. Using Channel Averaging**

| Averaged Channels                          | Output on Which Averaged Data Is Available | Register Settings                         |
|--|--|---|
| Channel 1, Channel 2                       | OUT1A, OUT1B                               | Set <AVG OUT 1> = 10 and <EN AVG GLO> = 1 |
| Channel 1, Channel 2                       | OUT3A, OUT3B                               | Set <AVG OUT 3> = 11 and <EN AVG GLO> = 1 |
| Channel 3, Channel 4                       | OUT4A, OUT4B                               | Set <AVG OUT 4> = 10 and <EN AVG GLO> = 1 |
| Channel 3, Channel 4                       | OUT2A, OUT2B                               | Set <AVG OUT 2> = 11 and <EN AVG GLO> = 1 |
| Channel 1, Channel 2, Channel 3, Channel 4 | OUT1A, OUT1B                               | Set <AVG OUT 1> = 11 and <EN AVG GLO> = 1 |
| Channel 1, Channel 2, Channel 3, Channel 4 | OUT1A, OUT1B                               | Set <AVG OUT 4> = 11 and <EN AVG GLO> = 1 |

## PERFORMANCE WITH DIGITAL PROCESSING BLOCKS

The ADS5263 provides very high SNR along with high sampling rates. In applications where even higher SNR performance is desired, digital processing blocks such as averaging and decimation filters can be used advantageously to achieve this. [Table 14](#) shows the improvement in SNR that can be achieved compared to the default value, using these modes.

**Table 14. SNR Improvement Using Digital Processing <sup>(1)</sup>**

| MODE   | TYPICAL SNR, dBFS | TYPICAL IMPROVEMENT in SNR, dB |
|--|-------------------|--------------------------------|
| Default  | 84.5              |                                |
| With decimation-by-2 filter enabled                            | 86.7              | 2.2                            |
| With decimation-by-4 filter enabled                            | 87.7              | 3.2                            |
| With decimation-by-8 filter enabled                            | 88.6              | 4.1                            |
| With two channels averaged and decimation-by-8 filter enabled  | 91.3              | 6.8                            |
| With four channels averaged                                    | 89.6              | 5.1                            |
| With four channels averaged and decimation-by-8 filter enabled | 93                | 8.5                            |

(1) Custom coefficients used for decimation-by-8 filter.

### 18-Bit Data Output With Digital Processing

As shown in [Table 14](#), very high SNR can be achieved using the digital blocks. Now, the overall SNR is limited by the quantization noise of the 16-bit output data. (16-bit quantization SNR =  $6n + 1.76 = 16 \times 6 + 1.76 = 97.76$  dBFS.) To overcome this, the digital processing blocks (averaging and digital filters) automatically output 18-bit data. With the two additional bits, the quantization SNR improves by 12 dB and no longer limits the maximum SNR that can be achieved using the ADS5263. For example, with four channels averaged and the decimation-by-8 filter, the typical SNR improves to about 94.5 dBFS using 18-bit data (an improvement of 1.5 dB over the SNR with 16-bit data).

The 18-bit data can be output using the special 18x serialization mode (see [Output LVDS Interface](#)). Note that the user can choose either the default 16x serialization (which takes the upper 16 bits of the 18-bit data) or the 18x serialization mode (that outputs all 18 bits).

## FLEXIBLE MAPPING OF CHANNEL DATA TO LVDS OUTPUTS

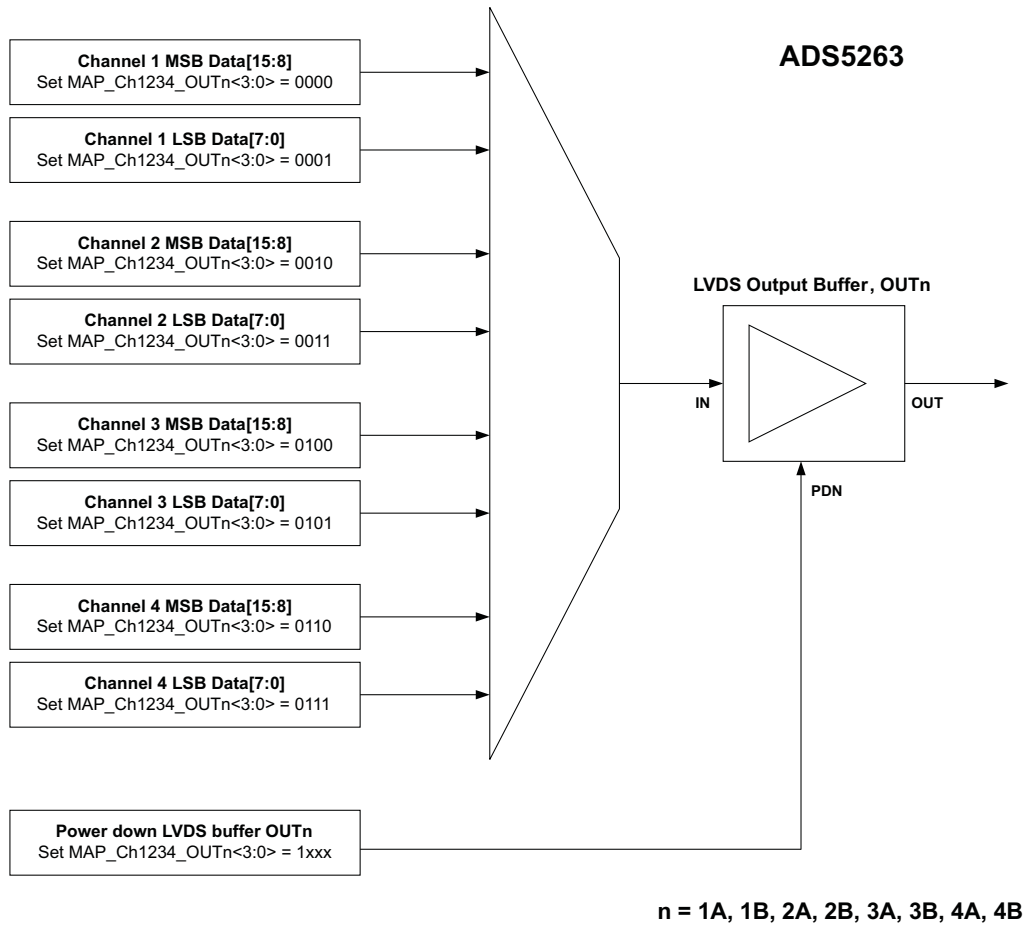
ADS5263 has a mapping function by the use of which the digital data for any channel can be routed to any LVDS output. So, as an example, in the 1-wire interface, the channel-1 ADC output can be output either on OUT1 pins or on OUT2 or OUT3 or OUT4 pins.

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This flexibility in mapping simplifies board designs by avoiding complex routing that would be caused by a rigid mapping of input channels and output pins. This can also lead to potential saving in PCB layers and hence cost. The mapping is programmable using the register bits **<MAP\_Ch1234\_OUTn>** as shown in [Figure 67](#) and [Figure 68](#).



**Figure 67. Mapping in 2-Wire Interface**

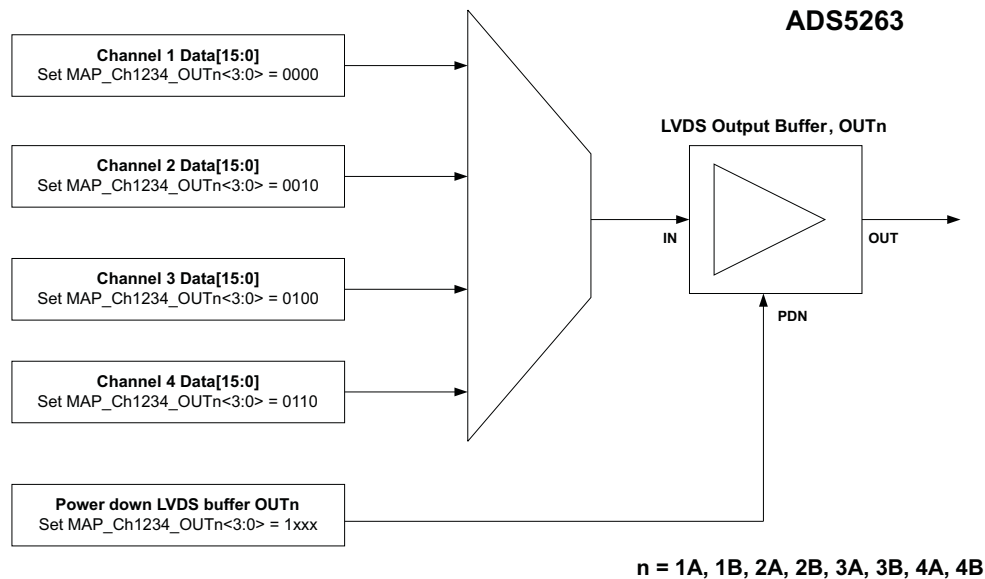


Figure 68. Mapping in 1-Wire Interface

## OUTPUT LVDS INTERFACE

The ADS5263 offers several flexible output options, making it easy to interface to an ASIC or an FPGA. Each of these options can be easily programmed using the serial interface. A summary of all the options is presented in [Table 15](#), along with the default values after power up and reset. Following this, each option is described in detail.

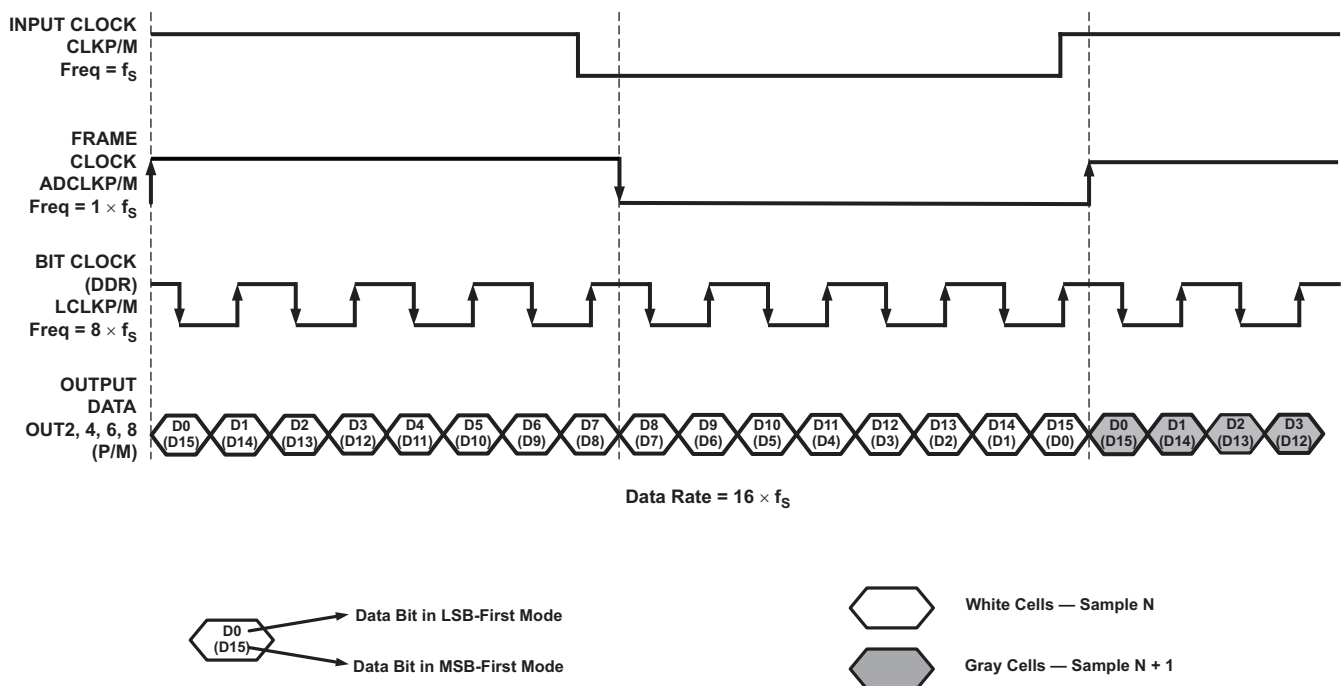
The output interface options are:

1. 1-wire, 16x serialization with DDR bit clock and 1x frame clock
  - The 16-bit ADC data is serialized and output over one LVDS pair per channel together with an 8x bit clock and 1x frame clock. The output data rate is 16x sample rate; hence, it is suited for low sample rates, typically up to 50 MSPS.
2. 2-wire, 8x serialization with DDR bit clock and 0.5x frame clock (16 bit ADC mode, [Figure 70](#) and [Figure 71](#))
  - Here, the 16 bit ADC data is serialized and output over two LVDS pairs per channel. The output data rate is 8x sample rate, with a 4x bit clock and 0.5x frame clock. Because the output data rate is half compared to the 1-wire case, this interface can be used up to the maximum sample rate of the device.
3. 2-wire, 8x serialization with DDR bit clock and 0.5x frame clock (14-bit ADC mode)
  - Here, the 14-bit ADC data is padded with two zero bits. The combined 16-bit data is then serialized and output over two LVDS pairs per channel. The output data rate is 8x sample rate, with a 4x bit clock and 0.5x frame clock. Because the output data rate is half compared to the 1-wire case, this interface can be used up to the maximum sample rate of the device.
4. 1-wire, 14x serialization with DDR bit clock and 1x frame clock (14-bit ADC mode)
  - The 14-bit ADC data is serialized and output over one LVDS pair per channel together with a 7x bit clock and 1x frame clock. The output data rate is 14x sample rate; hence, it is suited for low sample rates, typically up to 50 MSPS.
5. 2-wire, 7x serialization with DDR bit clock and 0.5x frame clock (14-bit ADC mode, [Figure 73](#) and [Figure 74](#))
  - Here, the 14-bit ADC data is serialized and output over two LVDS pairs per channel. The output data rate is 7x sample rate, with a 3.5x bit clock and 0.5x frame clock. Because the output data rate is half compared to the 1-wire case, this interface can be used up to the maximum sample rate of the device.
6. 1-wire, 18x serialization with DDR bit clock and 1x frame clock – Here, the 18-bit data from the digital processing block is serialized and output over one LVDS pair per channel, together with a 9x bit clock and 1x frame clock. The output data rate is 18x sample rate; hence, it is suited for low sample rates, typically up to

40 MSPS. This interface is primarily intended to be used when the averaging and digital filters are enabled.

**Table 15. Summary of Output Interface Options**

| FEATURE                 | OPTIONS           | AVAILABLE IN |        | DEFAULT AFTER POWER UP AND RESET | BRIEF DESCRIPTION   |
|-------------------------|-------------------|--------------|--------|----------------------------------|---|
|                         |                   | 1 wire       | 2 wire |                                  |   |
| Wire interface          | 1 wire and 2 wire |              |        | 1 wire                           | 1 wire – ADC data is sent serially over one pair of LVDS pins<br>2 wire – ADC data is split and sent serially over two pairs of LVDS pins   |
| Serialization factor    | 16x               | X            | X      | 16x                              | For 16-bit ADC mode<br>Can also be used with 14-bit ADC mode – the 14-bit ADC data is padded with two zeros and the combined 16-bit data is serialized.   |
|                         | 18x               | X            |        |                                  | 18-bit data is available when 16-bit ADC mode is used with averaging and decimation filters enabled.  |
|                         | 14x               | X            | X      |                                  | For 14-bit ADC mode only  |
| DDR bit-clock frequency | 8x                | X            |        | 8x                               | 16x serialization   |
|                         | 4x                |              | X      |                                  | 16x serialization<br>Only with 2-wire interface   |
|                         | 9x                | X            |        |                                  | 18x serialization   |
|                         | 7x                | X            |        |                                  | 14x serialization   |
|                         | 3.5x              |              | X      |                                  | 14x serialization<br>Only with 2-wire interface   |
| Frame-clock frequency   | 1x sample rate    | X            |        | 1x                               |   |
|                         | 1/2x sample rate  |              | X      |                                  |   |
| Bit sequence            | Bytewise          |              | X      | —                                | Bytewise – The ADC data is split into upper and lower bytes, which are output on separate wires.<br>Bitwise – The ADC data is split into even and odd bits, which are output on separate wires.<br>Wordwise – Successive ADC data samples are sent over separate wires. These options are available only with 2-wire interface. |
|                         | Bitwise           |              | X      |                                  |   |
|                         | Wordwise          |              | X      |                                  |   |



**Figure 69. Output LVDS Interface, 1-Wire, 16x Serialization**

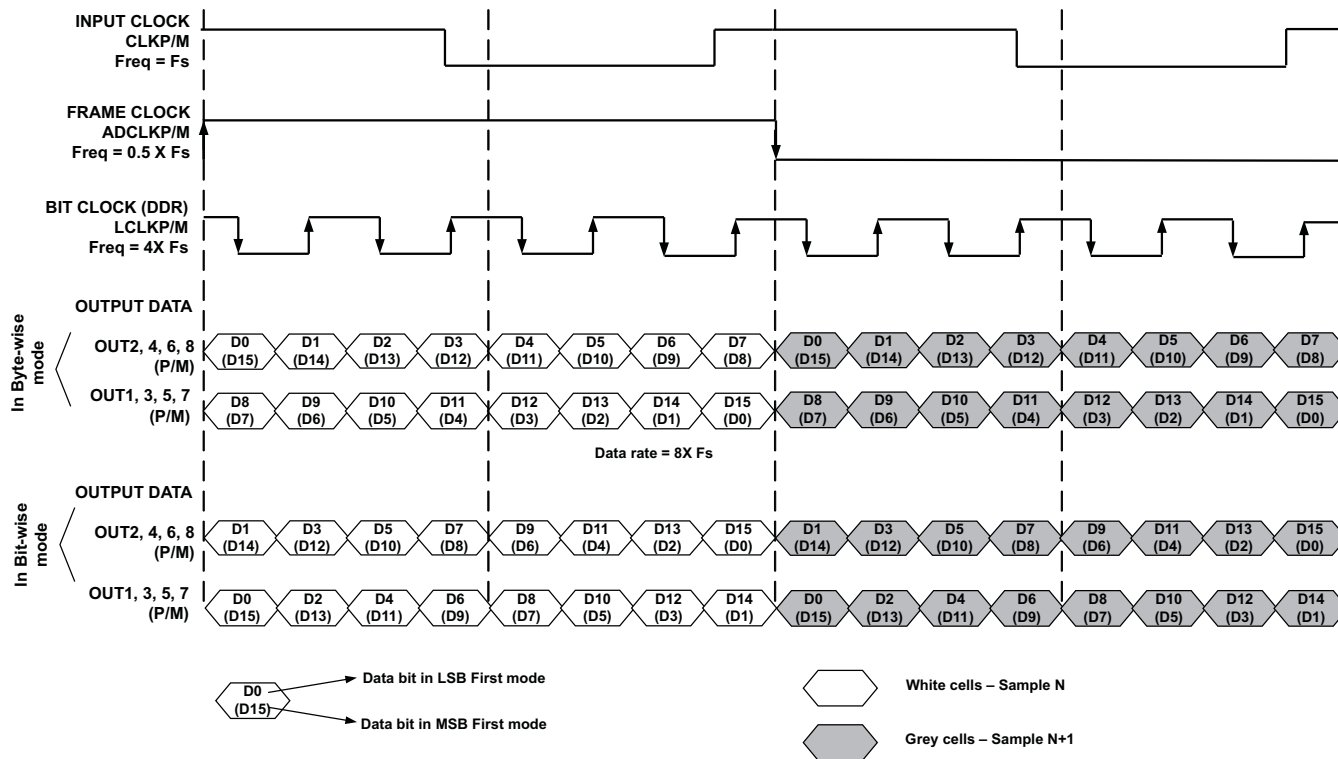


Figure 70. LVDS Output Interface, 2-Wire, 8x Serialization, Byte-wise and Bit-wise Modes

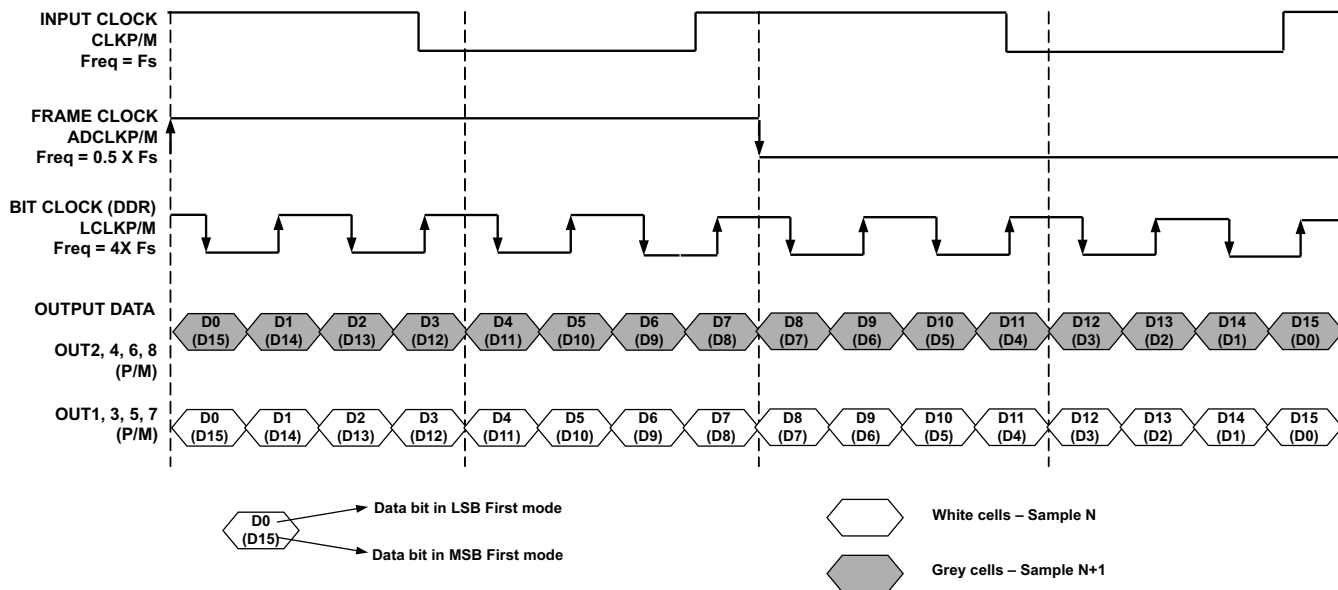


Figure 71. LVDS Output Interface, 2-Wire, 8x Serialization, Word-wise Mode

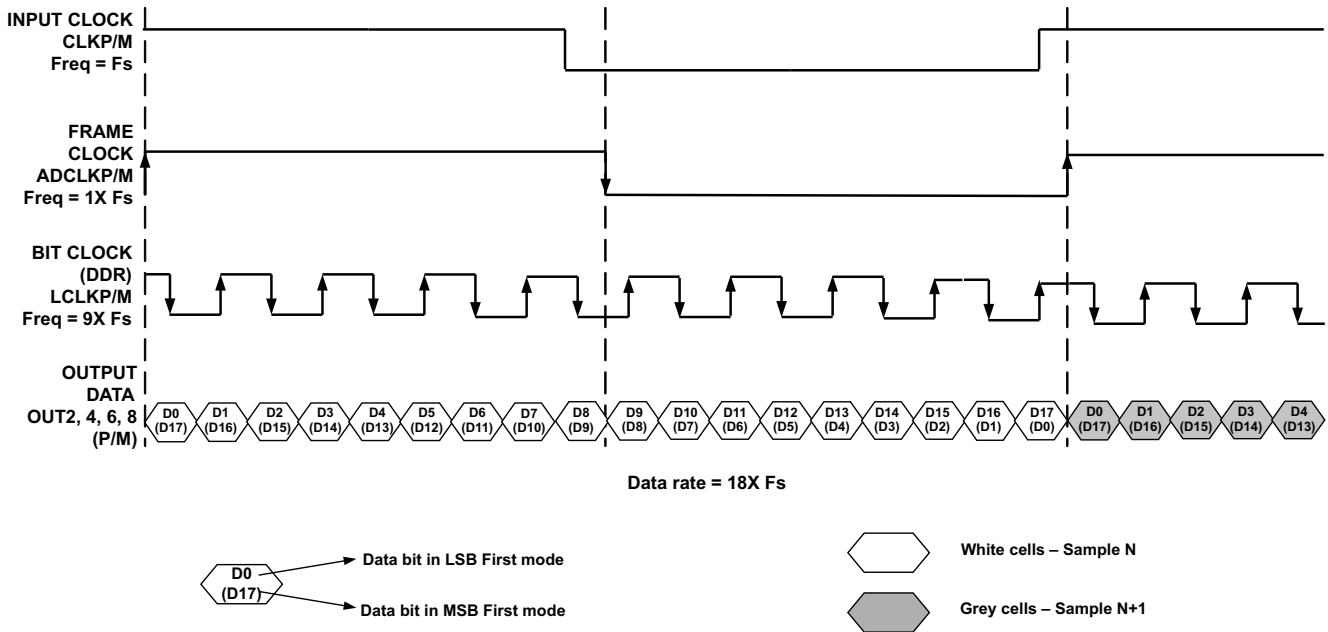


Figure 72. LVDS Output Interface, 1-Wire, 18x Serialization

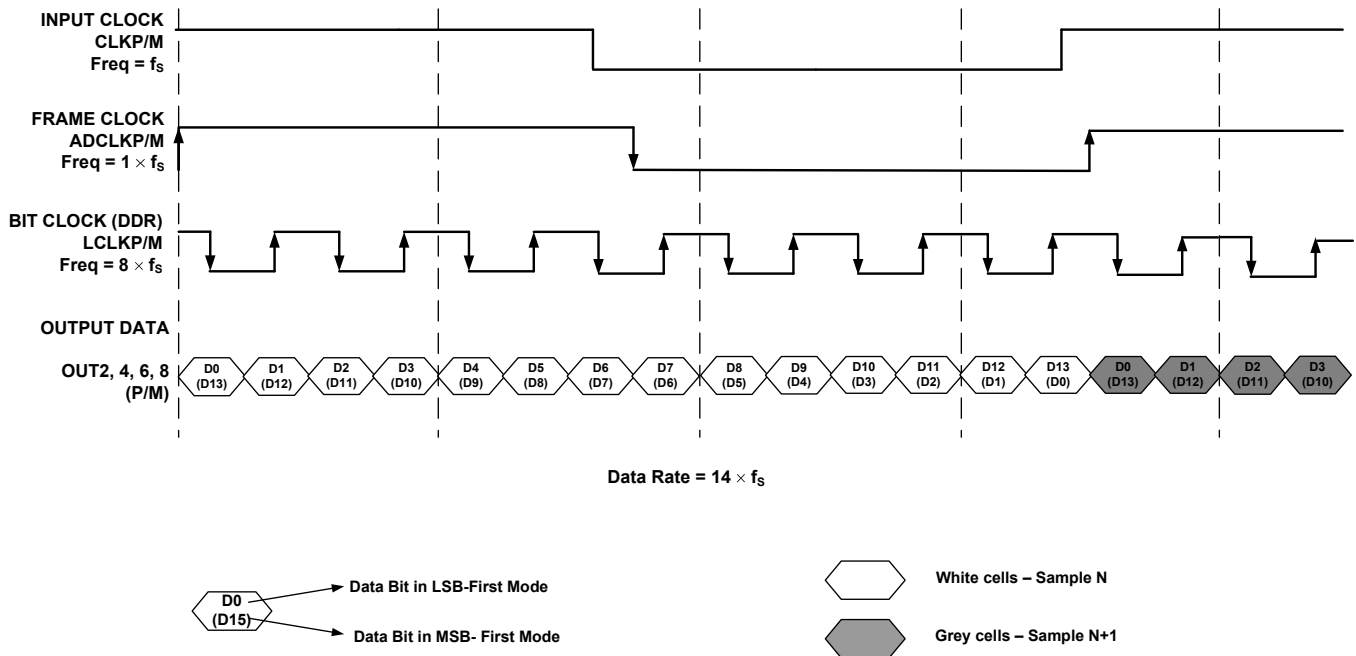


Figure 73. LVDS Output Interface, 1-Wire, 14x Serialization

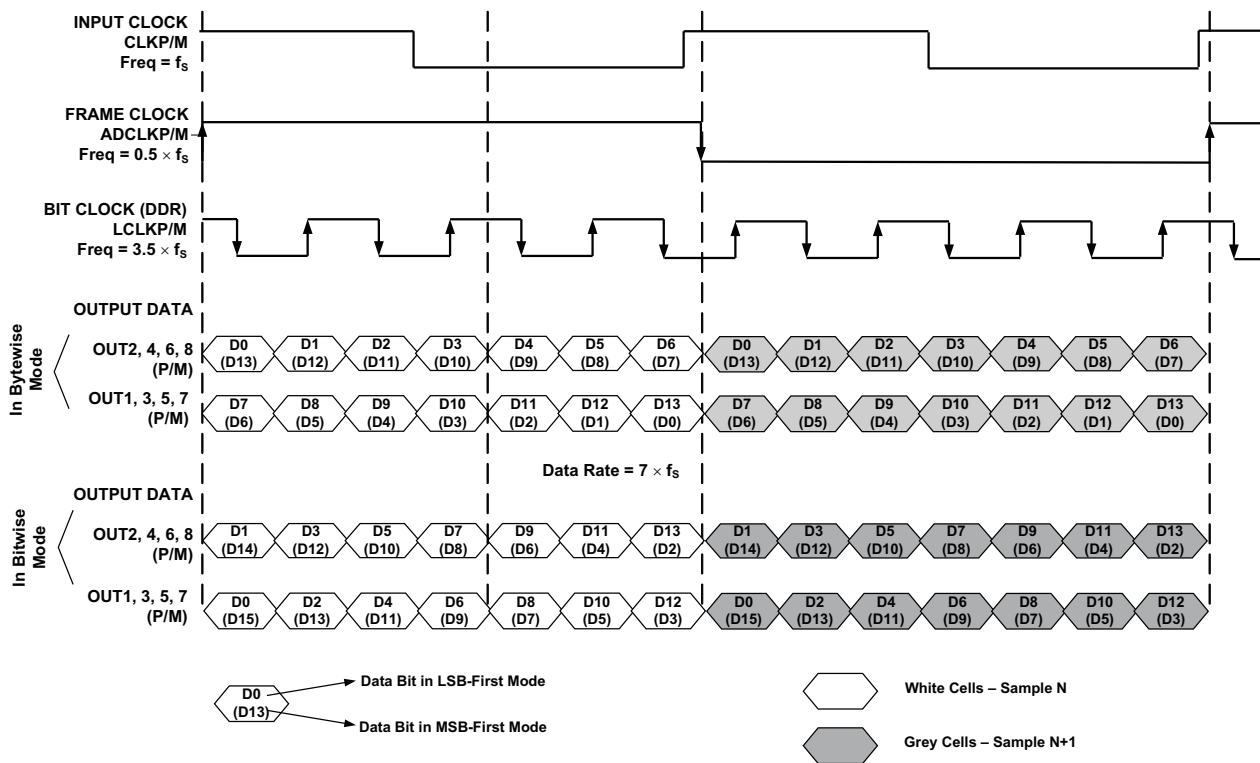


Figure 74. LVDS Output Interface, 2-Wire, 7x Serialization

### PROGRAMMABLE LCLK PHASE

The ADS5263 allows programmability of the edge of the output bit clock (LCLK) using register bits <PHASE\_DDR> as follows:

The default value of PHASE\_DDR after reset is 10, and the default phase corresponds to [Figure 75](#).

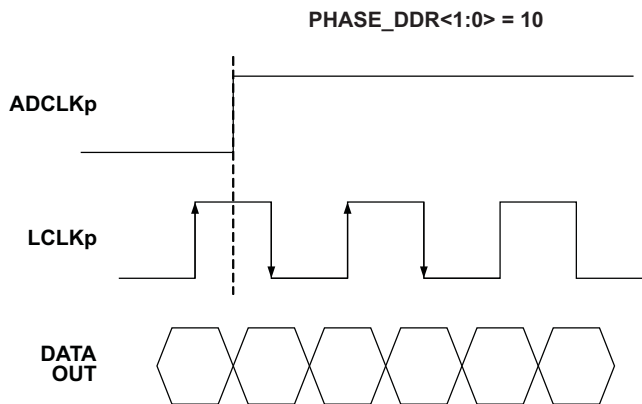
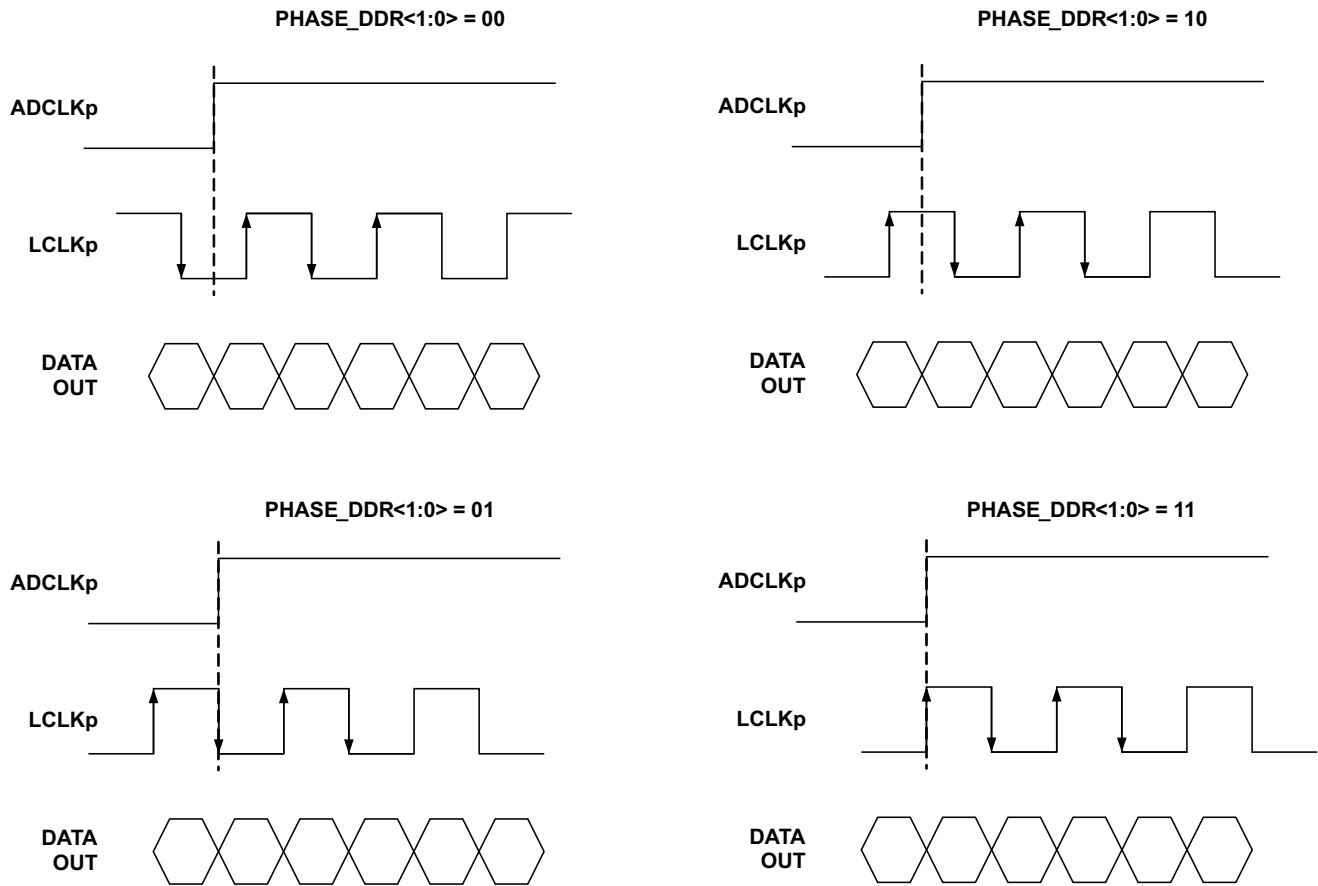


Figure 75. Default LCLK Phase

The phase can also be changed to one of the following states by changing the value of the <PHASE\_DDR1:0> bits (and setting register bit EN\_REG\_42 = 1).



**Figure 76. Programmable LCLK Phases**

## Board Design Considerations

### Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See *ADS5263EVM Evaluation Module* ([SLAU344](#)) for placement of components, routing and grounding.

### Supply Decoupling

Because the ADS5263 already includes internal decoupling, minimal external decoupling can be used without loss in performance. For example, the ADS5263EVM uses a single 0.1µF decoupling capacitor for each supply, placed close to the device supply pins.

### Packaging

#### Exposed Pad

The exposed pad at the bottom of the package is the main path for heat dissipation. Therefore, the pad must be soldered to a ground plane on the PCB for best thermal performance. The pad must be connected to the ground plane through the optimum number of vias.

For detailed information, see application notes *QFN Layout Guidelines* ([SLOA122](#)) and *QFN/SON PCB Attachment* ([SLUA271](#)), both available for download at the TI web site ([www.ti.com](#)). One can also visit TI's thermal website at [www.ti.com/thermal](#).

#### Non-Magnetic Package

An important requirement in magnetic resonance imaging (MRI) applications is the magnetic compatibility of components mounted close to the RF coil area. Any ferromagnetic material in the component package introduces an artifact in the MRI image. Therefore, it is preferred to have components with non-magnetic packages.

The ADS5263 is available in a special non-magnetic package that does not create any image artifacts, even in the presence of high magnetic fields. The non-magnetic part is orderable with the suffix “-NM”.

## DEFINITION OF SPECIFICATIONS

**Analog Bandwidth** – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

**Aperture Delay** – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

**Aperture Uncertainty (Jitter)** – The sample-to-sample variation in aperture delay.

**Clock Pulse Width/Duty Cycle** – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

**Maximum Conversion Rate** – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

**Minimum Conversion Rate** – The minimum sampling rate at which the ADC functions.

**Differential Nonlinearity (DNL)** – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

**Integral Nonlinearity (INL)** – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

**Gain Error** – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as  $E_{GREF}$  and  $E_{GCHAN}$ .

To a first-order approximation, the total gain error is  $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$ .

For example, if  $E_{TOTAL} = \pm 0.5\%$ , the full-scale input varies from  $(1 - 0.5/100) \times FS_{ideal}$  to  $(1 + 0.5/100) \times FS_{ideal}$ .

**Offset Error** – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

**Temperature Drift** – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from  $T_{MIN}$  to  $T_{MAX}$ . It is calculated by dividing the maximum deviation of the parameter across the  $T_{MIN}$  to  $T_{MAX}$  range by the difference  $T_{MAX} - T_{MIN}$ .

**Signal-to-Noise Ratio** – SNR is the ratio of the power of the fundamental ( $P_S$ ) to the noise floor power ( $P_N$ ), excluding the power at dc and the first nine harmonics.

$$SNR = 10 \log_{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**Signal-to-Noise and Distortion (SINAD)** – SINAD is the ratio of the power of the fundamental ( $P_S$ ) to the power of all the other spectral components including noise ( $P_N$ ) and distortion ( $P_D$ ), but excluding dc.

$$SINAD = 10 \log_{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**Effective Number of Bits (ENOB)** – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (3)$$

**Total Harmonic Distortion (THD)** – THD is the ratio of the power of the fundamental ( $P_S$ ) to the power of the first nine harmonics ( $P_D$ ).

$$\text{THD} = 10\text{Log}^{10} \frac{P_S}{P_N} \quad (4)$$

THD is typically given in units of dBc (dB to carrier).

**Spurious-Free Dynamic Range (SFDR)** – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

**Two-Tone Intermodulation Distortion** – IMD3 is the ratio of the power of the fundamental (at frequencies  $f_1$  and  $f_2$ ) to the power of the worst spectral component at either frequency  $2f_1 - f_2$  or  $2f_2 - f_1$ . IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**DC Power-Supply Rejection Ratio (DC PSRR)** – DC PSRR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

**AC Power-Supply Rejection Ratio (AC PSRR)** – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If  $\Delta V_{\text{SUP}}$  is the change in supply voltage and  $\Delta V_{\text{OUT}}$  is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{SUP}}} \quad (\text{Expressed in dBc}) \quad (5)$$

**Voltage Overload Recovery** – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

**Common-Mode Rejection Ratio (CMRR)** – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If  $\Delta V_{\text{CM\_IN}}$  is the change in the common-mode voltage of the input pins and  $\Delta V_{\text{OUT}}$  is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{CM}}} \quad (\text{Expressed in dBc}) \quad (6)$$

**Crosstalk (only for multi-channel ADCs)** – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

## REVISION HISTORY

| <b>Changes from Original (May 2011) to Revision A</b>   | <b>Page</b> |
|---|-------------|
| • Changed Features List Item - From: 1.35 W Total Power at 100 MSPS To: 1.4 W Total Power at 100 MSPS ..... | 1           |
| • Changed Features List Item - From: 338 mW / Channel To: 355 mW / Channel .....                            | 1           |
| • Added "Non-magnetic package option for MRI systems" to Features .....                                     | 1           |
| • Added Package Marking ADS5263NM and Ordering Number ADS5263IRGC-NM .....                                  | 7           |
| • Changed the CLOCK INPUT values in the ROC table .....   | 8           |
| • Changed the ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE – 16-BIT ADC table .....                       | 9           |
| • Changed the ELECTRICAL CHARACTERISTICS GENERAL – 16-BIT ADC MODE table .....                              | 10          |
| • Added the ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE – 14-BIT ADC .....                               | 11          |
| • Changed the values in DIGITAL OUTPUTS – LVDS INTERFACE .....  | 12          |
| • Added <a href="#">Table 2</a> , <a href="#">Table 3</a> , and <a href="#">Table 4</a> .....               | 13          |
| • Added <a href="#">Figure 29</a> , <a href="#">Figure 30</a> , and <a href="#">Figure 31</a> .....         | 39          |
| • Added section - Large and Small Signal Input Bandwidth .....  | 51          |
| • Added Section - Board Design Considerations .....   | 73          |
| • Added Section - Packaging .....   | 73          |
| • Added Section - DEFINITION OF SPECIFICATIONS .....  | 74          |

| <b>Changes from Revision A (August 2011) to Revision B</b>  | <b>Page</b> |
|---|-------------|
| • Added register 42 between register 38 and register 45 .....   | 30          |
| • Added new Figure below Figure 16 .....  | 36          |
| • Added new Figure below Figure 22 (now Figure 24) .....  | 38          |
| • Added new figure 52 in Large and Small Signal Input Bandwidth section .....                                   | 51          |
| • Added new section below Digital Averaging titled: Performance with Digital Processing Blocks .....            | 65          |
| • Added listitem 6. to the OUTPUT LVDS INTERFACE section .....  | 67          |
| • Added Added new figure in section Output LVDS Interface ( <a href="#">Figure 71</a> ) .....                   | 69          |
| • Added new section after Output LVDS Interface titled: Programmable LCLK Phase, also 2 new figures added. .... | 71          |

| <b>Changes from Revision B (October 2011) to Revision C</b>  | <b>Page</b> |
|--|-------------|
| • Changed description paragraph From: "The device can optionally be driven with external references. Best performance can be achieved through the internal reference mode. To: "Additionally, the device supports an external reference mode for applications that require very low temperature drift of reference." .....   | 2           |
| • Changed Pin 54 From: REFB To: NC .....   | 6           |
| • Changed Pin 55 From: REFC To: NC .....   | 6           |
| • Changed the VCM Pin description To: "Internal reference mode: Outputs the common-mode voltage (1.5 V) that can be used externally to bias the analog input External reference mode: Apply voltage input that sets the reference for ADC operation." From: "Outputs the common-mode voltage (1.5 V) that can be used externally to bias the analog input pins." ..... | 6           |
| • Added "Idle channel noise" To SNR .....  | 9           |
| • Added "Idle channel noise" To LSB .....  | 9           |
| • Changed the INL values- 100 MSPS From: TYP = $\pm 2.2$ To: $\pm 5$ , Added MAX = $\pm 12$ .....  | 9           |
| • to Changed the INL values- 80 MSPS From: TYP = $\pm 2.2$ To: $\pm 5$ .....   | 9           |
| • Added From: VCM common-mode output voltage To: VCM common-mode output voltage, Internal reference mode .....   | 10          |
| • Added From: VCM output current capability To: VCM output current capability, Internal reference mode .....   | 10          |
| • Added From: VCM input voltage To: VCM input current, external reference mode .....   | 10          |

|   |    |
|---|----|
| • Added VCM input current, external reference mode Typical value - 80 MSPS of 0.5 .....   | 10 |
| • Changed $E_{GREF}$ - 100 MSPS MIN value From: $\pm 2.5$ To: $\pm 1$ .....   | 10 |
| • Added Temperature Coefficient to $E_{GREF}$ .....   | 10 |
| • Added Temperature Coefficient to $E_{GCHAN}$ .....  | 10 |
| • Changed SNR $f_{in} = 5$ MHz MIN value From: 68.8 To: to 67.5 .....   | 11 |
| • Added $t_A$ Aperture delay to the Timing Requirements Table .....   | 13 |
| • Changed From: 2 WIRE, 16x SERIALIZATION To: 2 WIRE, 8x SERIALIZATION .....  | 13 |
| • Added 100 MSPS to the SAMPLING FREQUENCY, MSPS column of <a href="#">Table 1</a> .....  | 13 |
| • Changed to 8x from 16x .....  | 13 |
| • Changed <a href="#">Table 3</a> title From: LVDS Timing for 2 Wire, 14x Serialization To: LVDS Timing for 2 Wire, 7x Serialization ...  | 14 |
| • Changed <a href="#">Table 6</a> Description From: Reference voltage must be forced on REFT and REFB pins To: Apply voltage on VCM pin to set the references for ADC operation ..... | 16 |
| • <a href="#">Table 7</a> Added: <EN_HIGH_ADDRS> as bit D4. Added: Register 0x09 to Serial Register Ma; .....   | 19 |
| • <a href="#">Table 7</a> Added: Register bit EXT_REF_VCM. Added: D12 <18x SERIALIZATION> .....   | 19 |
| • <a href="#">Table 7</a> Added: new register entries from Address 5A to 89. Added: new register F0 .....   | 19 |
| • Added D4 <EN_HIGH_ADDRS> .....  | 21 |
| • Added Added register description table (D10 <EN_CLAMP>) for register 0x09 .....   | 22 |
| • Added description for register EXT_REF_VCM .....  | 30 |
| • Added Description for <EN_REG_42>, <PHASE_DDR> and EXT_REF_VCM .....  | 30 |
| • Added Decsription for 18b SERIALIZATION .....   | 31 |
| • Changed D11, D10, and D5 To: SERIALIZATION From: SERIAL'N .....   | 31 |
| • Changed the register for A7-A0 IN HEX .....   | 34 |
| • Added description for register F0 for A7-A0 IN HEX .....  | 34 |
| • Replaced the Clamp Function section with the Clamp Functon for CCD Signals section .....  | 51 |
| • Deleted Figure - CCD Sensor Connections .....   | 54 |
| • Added External Reference Mode .....   | 55 |
| • Changed the Digital Filter Section .....  | 58 |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| ADS5263IRGCR     | ACTIVE        | VQFN         | RGC             | 64   | 2000        | Green (RoHS & no Sb/Br) | CU SN            | Level-3-260C-168 HR  | -40 to 85    | ADS5263                  | <a href="#">Samples</a> |
| ADS5263IRGCR-NM  | ACTIVE        | VQFN         | RGC             | 64   | 2000        | Green (RoHS & no Sb/Br) | CU SN            | Level-3-260C-168 HR  | -40 to 85    | ADS5263NM                | <a href="#">Samples</a> |
| ADS5263IRGCT     | ACTIVE        | VQFN         | RGC             | 64   | 250         | Green (RoHS & no Sb/Br) | CU SN            | Level-3-260C-168 HR  | -40 to 85    | ADS5263                  | <a href="#">Samples</a> |
| ADS5263IRGCT-NM  | ACTIVE        | VQFN         | RGC             | 64   | 250         | Green (RoHS & no Sb/Br) | CU SN            | Level-3-260C-168 HR  | -40 to 85    | ADS5263NM                | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

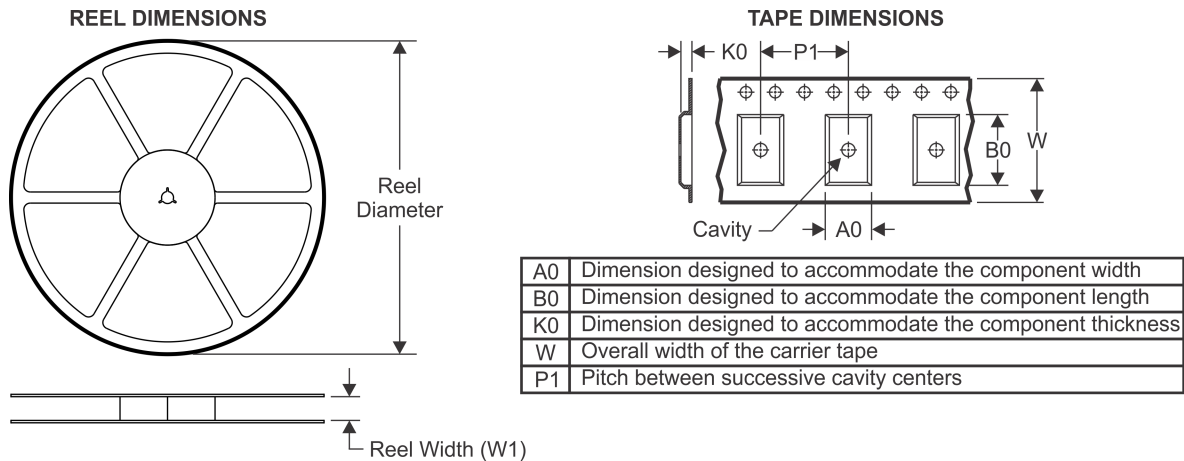
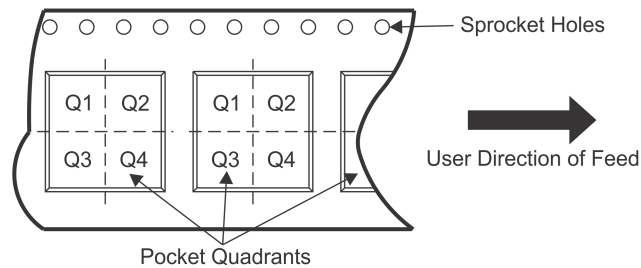
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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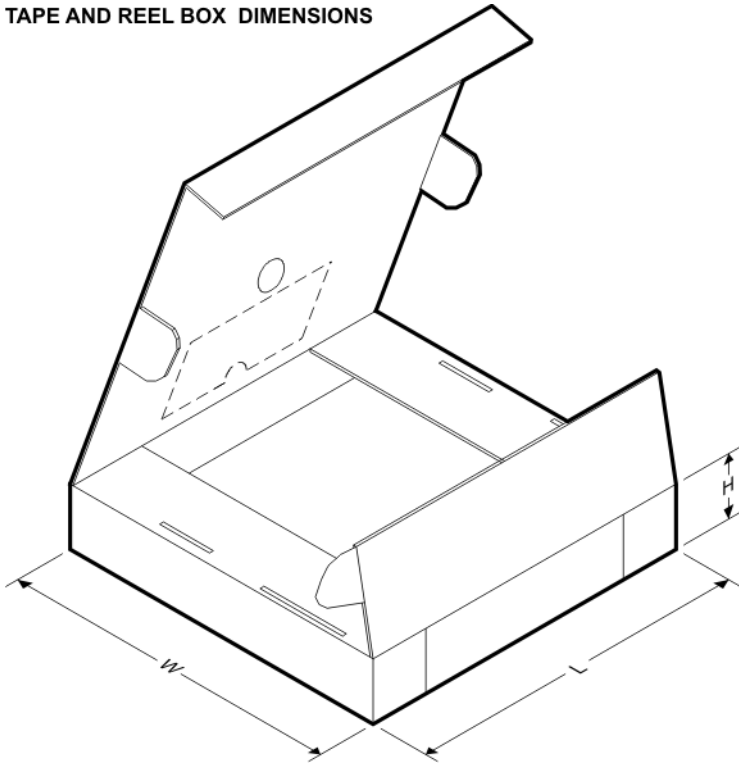
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS5263IRGCR    | VQFN         | RGC             | 64   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.5     | 12.0    | 16.0   | Q2            |
| ADS5263IRGCR-NM | VQFN         | RGC             | 64   | 2000 | 330.0              | 16.4               | 9.3     | 9.3     | 1.5     | 12.0    | 16.0   | Q2            |
| ADS5263IRGCT    | VQFN         | RGC             | 64   | 250  | 180.0              | 16.4               | 9.3     | 9.3     | 1.5     | 12.0    | 16.0   | Q2            |
| ADS5263IRGCT-NM | VQFN         | RGC             | 64   | 250  | 180.0              | 16.4               | 9.3     | 9.3     | 1.5     | 12.0    | 16.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS5263IRGCR    | VQFN         | RGC             | 64   | 2000 | 336.6       | 336.6      | 28.6        |
| ADS5263IRGCR-NM | VQFN         | RGC             | 64   | 2000 | 336.6       | 336.6      | 28.6        |
| ADS5263IRGCT    | VQFN         | RGC             | 64   | 250  | 213.0       | 191.0      | 55.0        |
| ADS5263IRGCT-NM | VQFN         | RGC             | 64   | 250  | 213.0       | 191.0      | 55.0        |



# THERMAL PAD MECHANICAL DATA

RGC (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD

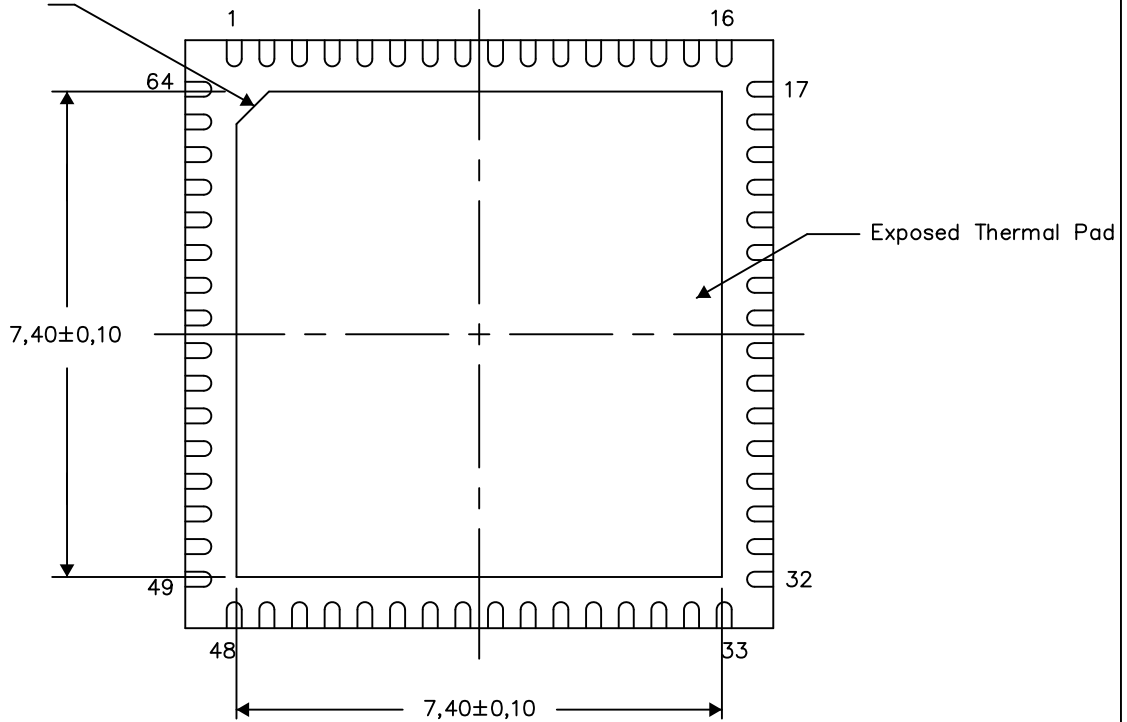
## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR  
CO,35



Bottom View

Exposed Thermal Pad Dimensions

4206192-4/AD 10/14

NOTE: A. All linear dimensions are in millimeters



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