ADS42JBx9 System Evaluation Kit

This document outlines the basic steps and functions that are required to ensure the proper operation of the ADS42JBx9 System Evaluation Kit (SEK). The kit includes an ADS42JBx9EVM, a JESD204B Translation Card, two 5-VDC power supplies, and a mini-USB cable. This kit is designed for use with the Texas Instruments (TI) TSW1400 High Speed Data Capture/Pattern Generator Card (not included) running with the High Speed Data Converter Pro GUI software. The ADS42JBx9EVM contains either an ADS42JB49 (14-bit) or ADS42JB69 (16-bit) dual-channel, 250-MSPS, analog-to-digital converter. The EVM also contains a TI LMK04828 clock jitter cleaner. The TI JESD204B Translation card receives JESD204B standard output data from the ADC EVM and translates it to parallel LVDS data that can be captured by the TSW1400 for analysis. This guide helps users to quickly evaluate the performance of the ADS42JBx9EVM boards by capturing and displaying waveforms using the TSW1400. The EVM schematics, BOMs, and layout files are found in the design package under the ADS42JBx9SEK product folder on www.ti.com.

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1 Introduction

1.1 Overview

The ADS42JBx9EVM is an evaluation module (EVM) used to evaluate Texas Instruments' ADS42JBx9 and LMK04828 clock jitter cleaner. The ADS42JB69 is a low-power, 16-bit, 250-MSPS analog-to-digital converter (ADC) with a buffered analog input and outputs featuring a JESD204B interface. The EVM has transformer-coupled analog inputs accommodating a wide range of signal sources and frequencies. The LMK04828 provides an ultra-low-jitter and phase-noise ADC sample clock along with system reference clocks and a device sample clock for a complete JESD204B subclass 1 clocking solution.

The ADS42JB69 and LMK04828 are controlled through an easy-to-use software GUI enabling quick configuration for a variety of uses.

The JESD204B translation card connects between the ADS42JBx9EVM and a TSW1400EVM data capture card. The High Speed Data Converter Pro software GUI processes the data from the TSW1400EVM to quickly assess the performance of the ADS42JBx9. The FMC output interface connector of the ADS42JBx9EVM has also been verified to be compatible with the Xilinx KC705 evaluation platform.

1.2 Block Diagram

The block diagram for the ADS42JBx9SEK is shown in Figure 1. The various inputs, outputs, and jumpers of the ADS42JBx9SEK are described in Table 1.

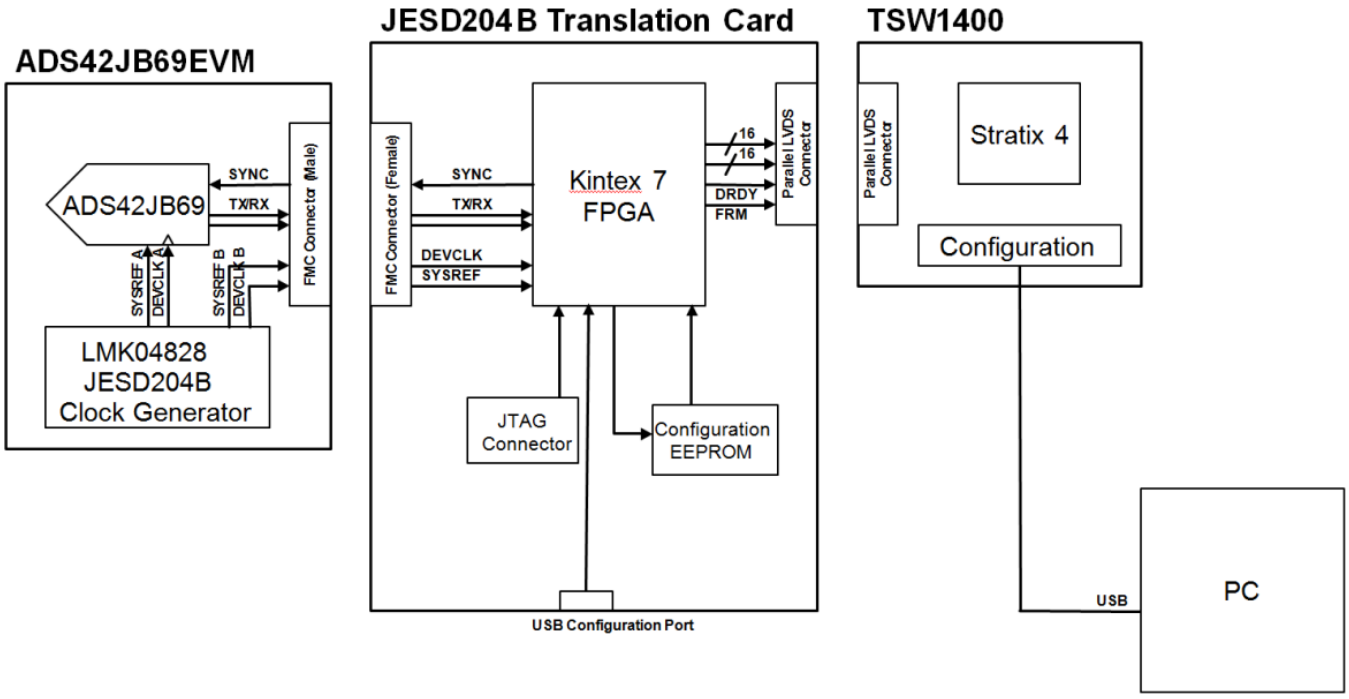

Figure 1. Block Diagram of the ADS42JBx9SEK

Table 1. Input and Output Connectors and Jumper Descriptions of the ADS42JBx9SEK

Component	Description
J1 (AINP)	Single-ended analog input for channel A
J2 (BINP)	Single-ended analog input for channel B
J19 (EXT_ADC_CLK)	Single-ended ADC clock input
J8 (+5V)	Positive power connection (5 V)
J9 (GND)	Negative power connection (GND)
J13 (Main PWR)	5-V input from provided 5-VDC power supply
J14 (REF OSC_IN)	External reference option for LMK04828, REFOUT1 source on J16 and CPLD_CLK
J16 (REFOUT1)	10-MHz CMOS level reference output or frequency of REF OSC_IN if option selected
J6 (USB)	USB connection
J3	JESD204B FMC interface connector
J5 (LMK SYNC)	LMK04828 sync input
J7 (LMK CLKIN1_P)	CLKIN0 input for LMK04828. Option to provide an external clock source to the LMK in place of on-board 100-MHz VCXO.
J10 (CLKOUT10P)	DCLKOUT6p from LMK04828. Default is LVPECL at 250 MHz.
J15 (CLKOUT10N)	DCLKOUT6n from LMK04828. Default is LVPECL at 250 MHz.
J17 (CLKOUT12P)	SDCLKOUT7p from LMK04828. Default is LVPECL at 6.25 MHz.
J4 (CLKOUT12M)	SDCLKOUT7p from LMK04828. Default is LVPECL at 6.25 MHz.
J18 (PROG CPLD)	JTAG interface for CPLD U3
SW1 (ADC_RESET)	Switch to reset the ADC using the RESET input pin
SW3 (CPLD)	Switch inputs to CPLD. Currently not used.
SW2 (Reset CPLD)	CPLD reset
SJP12	ADC CNTRL1 pin. Not used by ADC. Connected to GND.
JP3	ADC CNTRL2 pin. Not used by ADC. Connected to GND.
JP6 (XO_PWR)	Provides power to VCXO Y2 or oscillator Y3
SJP3 (REF_SEL)	Selects input or external reference source for LMK, J16 and CPLD. Default is internal 10-MHz source.
JP2 (CDC_CLK)	Reference clock buffer output enable
JP5 (REF_PWR)	Power enable for 10-MHz reference oscillator
SJP1 (REF_EN)	Enable for 10-MHz reference oscillator
SJP4-SJP11	USB/FMC Interface select. Default is using USB.
SJP2 (WP)	EEPROM write protect.
JP4 (ENABLE)	U11 enable. Install jumper to disable switcher U11. Default is uninstalled.
JP1 (PWRGD)	Test point for power good output pin from U11.

2 Software Control

This section provides installation instructions for the ADS42JBx9 GUI and descriptions of the various controls.

2.1 Installation Instructions

1. Download the software from the ADS42JBx9EVM resource page: http://www.ti.com/ww/en/analog/dataconverters/jesd204b/resources.shtml. There are links here to the ADS42JBx9 EVM and SEK.
2. Extract the files from the zip file named *ADS42JBx9 GUI vXpY installer.zip* where *XpY* represents the version number.
3. Run *setup.exe* and follow the installation prompts.

4. Start the GUI by going to **Start Menu → All Programs → Texas Instruments ADCs → ADS42JBx9 GUI**.
5. When plugging the board into the computer for the first time through the USB cable, you are prompted to install the USB drivers.
   - Windows® XP: If Windows XP does not automatically install the drivers, follow the prompts on the screen to do so. Do not let Windows XP search Microsoft Update for the drivers, but do let Windows XP install the drivers automatically.
   - Windows 7: After installing the GUI, Windows 7 should automatically be able to install the drivers for the ADS42JBx9EVM with no user input.

2.2 Software Operation

The software GUI allows full programming control of the ADS42JBx9 and LMK04828 devices. Figure 2 shows the GUI front panel which contains a block diagram of the ADS42JBx9. Clicking on the various blocks of the ADS42JBx9 allows configuration of the settings for that block. Detailed descriptions for each screen of the GUI are given in this section. Please refer to the ADS42JBx9 datasheet (SLAS904) for more detailed explanations of the register fields.

2.2.1 Top Level GUI Controls

Figure 2 shows the top-level view of the GUI which contains the block diagram of the ADS42JBx9. Clicking the blue blocks in the diagram brings up the controls for that block. Along the top of the GUI are **SEND**, **READ**, **SAVE**, and **LOAD** buttons. The **SEND** and **READ** buttons write or read all of the registers of the ADS42JBx9 and LMK04828. The **SAVE** and **LOAD** buttons can be used to save or load a text file of the registers. The flashing **RESET** button can be clicked to reset the USB port connection. This same button reads **CONNECTED** when the GUI is successfully connected to the EVM. On the right side is a white text box that shows the registers as they are written to the device and also shows the results of a read command. The user can write and read from individual registers from both parts using this text box. Select which device to target by using the drop down arrow in the box labeled *Filename* just below this text box. After the device is selected, enter an address, then click on the **READ** button. The results are displayed in the text box. The address needs to be entered in hex format. To read address f, enter *xf*. To do a write, enter a valid address followed with a 16-bit data value. To write a 5a to address 1e for example, enter *x5a x1e*.

The ADS42JBx9 reset and powerdown controls are available in the top-left corner, for easy access. The reset control automatically clears in the device, so only a single mouse click is needed. The **DEVICE ON** button displays **DEVICE OFF** when clicked and the device has been powered down. Monitoring the power supply current when toggling the power down mode is a simple way to verify that the GUI is communicating with the device. The **Data Format** button allows the user to set the ADC output data to either 2's Complement or Offset Binary. The *Divide by 1,2,4* block is a control that sets the internal clock divider. The clock divider value is shown above the block. Note that clicking on this block does not take the GUI away from the top-level screen.

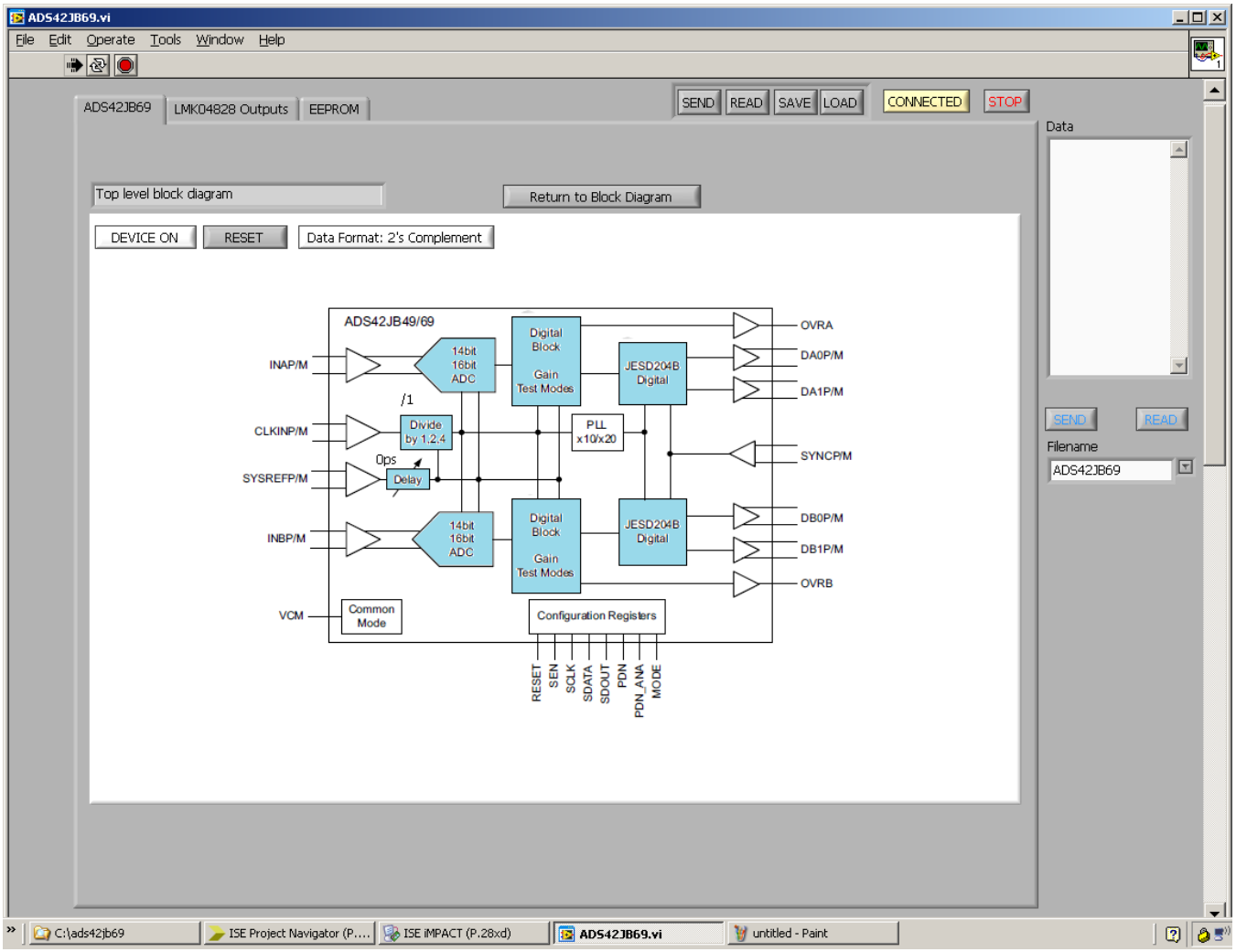

Figure 2. Top-Level Block Diagram Window of the ADS42JBx9 GUI

2.2.2 ADC Controls

Clicking on either the *14bit or 16bit ADC* block in Figure 2 takes the user to the *ADC Controls* window, shown in Figure 3. The *ADC Controls* window controls various ADC functions such as the over-range detection, output enable, and power enable. Table 2 describes the controls seen in this window. Select the **Return to Top** button to return to the top-level block diagram. Clicking the *16bit ADC* block opens a new window as shown in Figure 4.

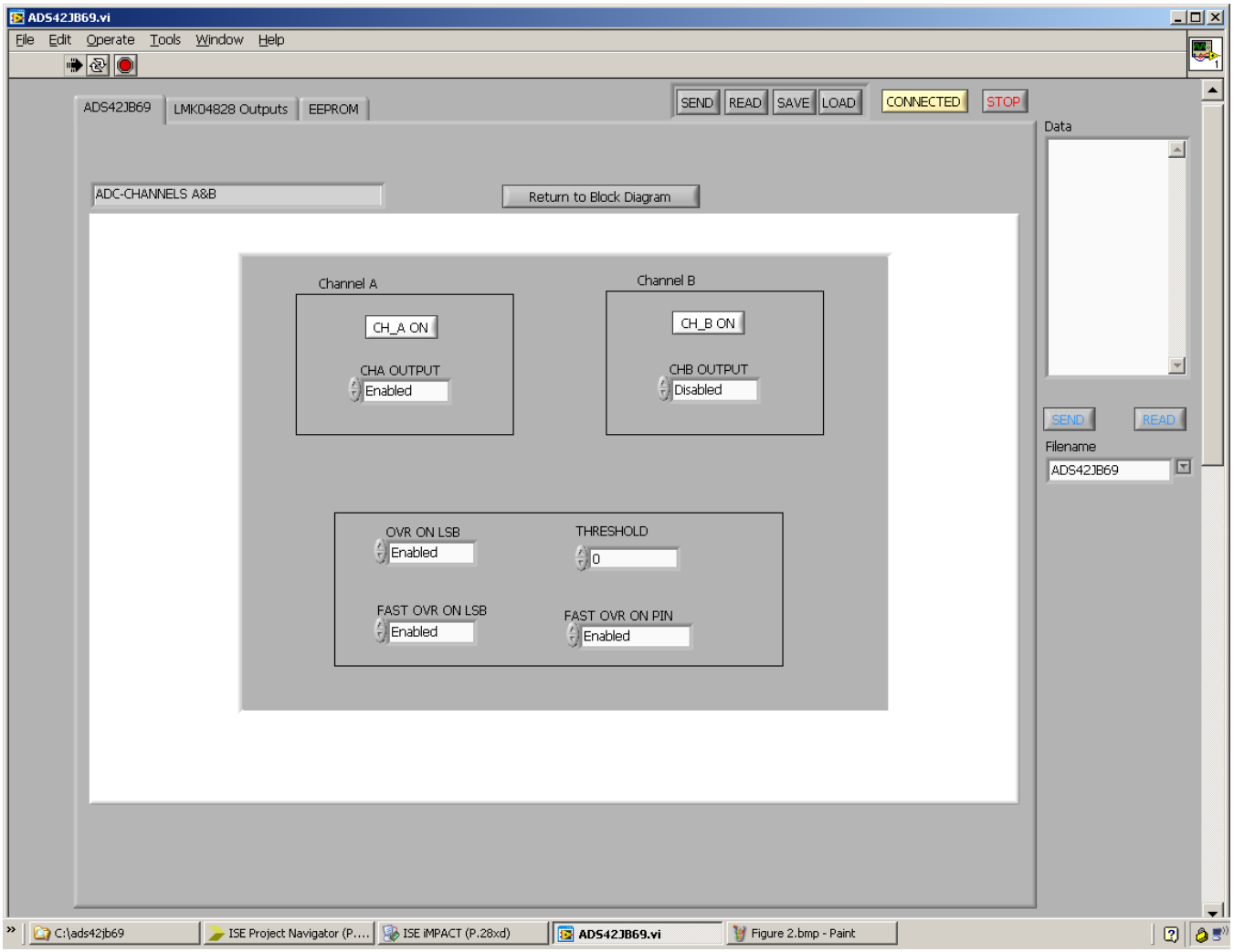

Figure 3. ADC Controls Window of the ADS42JBx9 GUI

Table 2. ADC Controls Window Descriptions

Control	Description
OVR ON LSB	Use the LSB as the normal OVR output
Fast OVR ON LSB	Use the LSB as the fast OVR output
FAST OVR ON Pin	Select which OVR signal should be output on the OVR pin
Threshold	Set the threshold for the fast OVR function
CH_A ON	Turn on and off channel A
CHA OUTPUT	Enables or disables channel A output
CH_B ON	Turn on and off channel B
CHB OUTPUT	Enables or disables channel B output

2.2.3 Digital Block Controls

Clicking either *Digital Block* block brings up the *Digital Block Controls* window, shown in Figure 4. Descriptions for the various controls are given in Table 3.

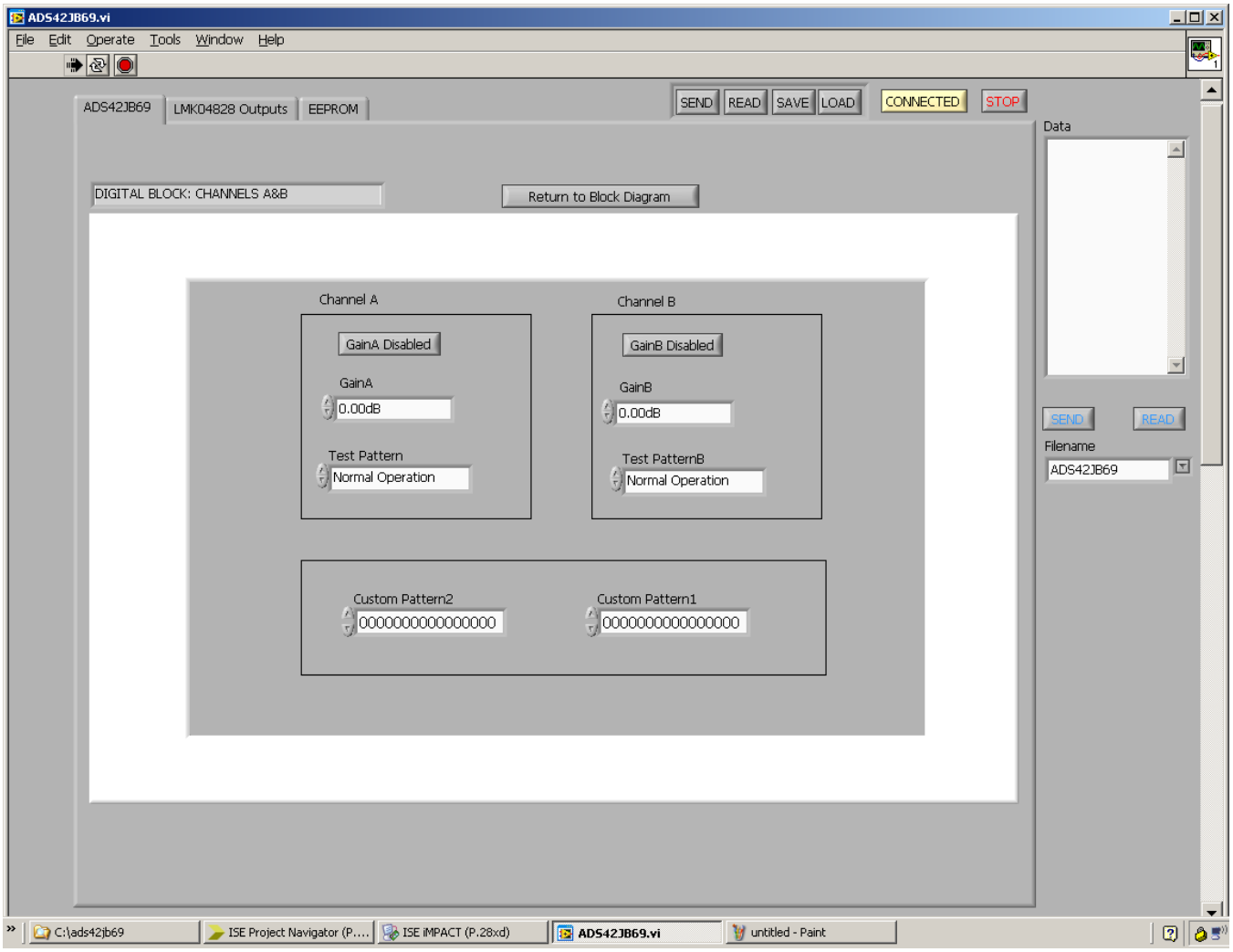

Figure 4. Digital Block Controls Window of the ADS42JBx9 GUI

Table 3. Digital Block Controls Window Descriptions

Control	Description
Ch A Gain Enable	Enable or disable the gain feature of channel A
Ch A Gain	Set the gain of channel A
Ch B Gain Enable	Enable or disable the gain feature of channel B
Ch B Gain	Set the gain of channel B
Test Pattern A	Selects a known test pattern, a custom test pattern or normal operation for channel A
Test Pattern B	Selects a known test pattern, a custom test pattern or normal operation for Channel B
Custom Pattern1	Allows the user to generate a custom pattern, which uses the value programmed here
Custom Pattern2	Allows the user to generate a custom pattern, which uses the value programmed here

2.2.4 JESD204B Controls

Clicking on either JESD204B Digital block opens the *JESD204B Controls* window, shown in Figure 5. Use the ADS42JBx9 data sheet for reference to assist with the descriptions of these various controls.

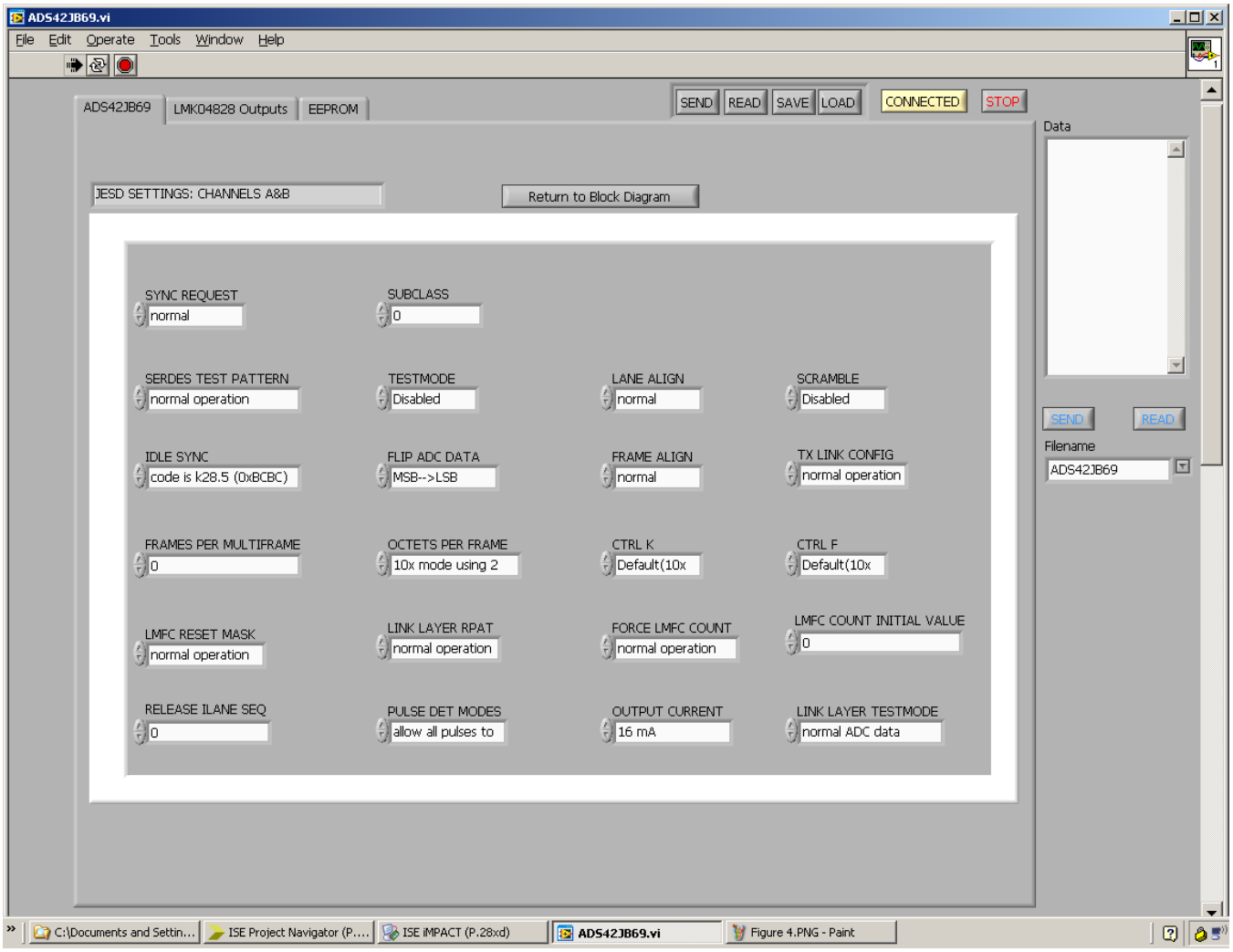

Figure 5. JESD204B Controls Window of the ADS42JBx9 GUI

2.2.5 LMK Controls

Click the *LMK04828 Outputs* tab located at the top left of the GUI. A new window opens as shown in Figure 6. The top panel displays a block diagram of the LMK04828. Clicking on a blue colored option opens a new panel in the lower section of the GUI for control of that section.

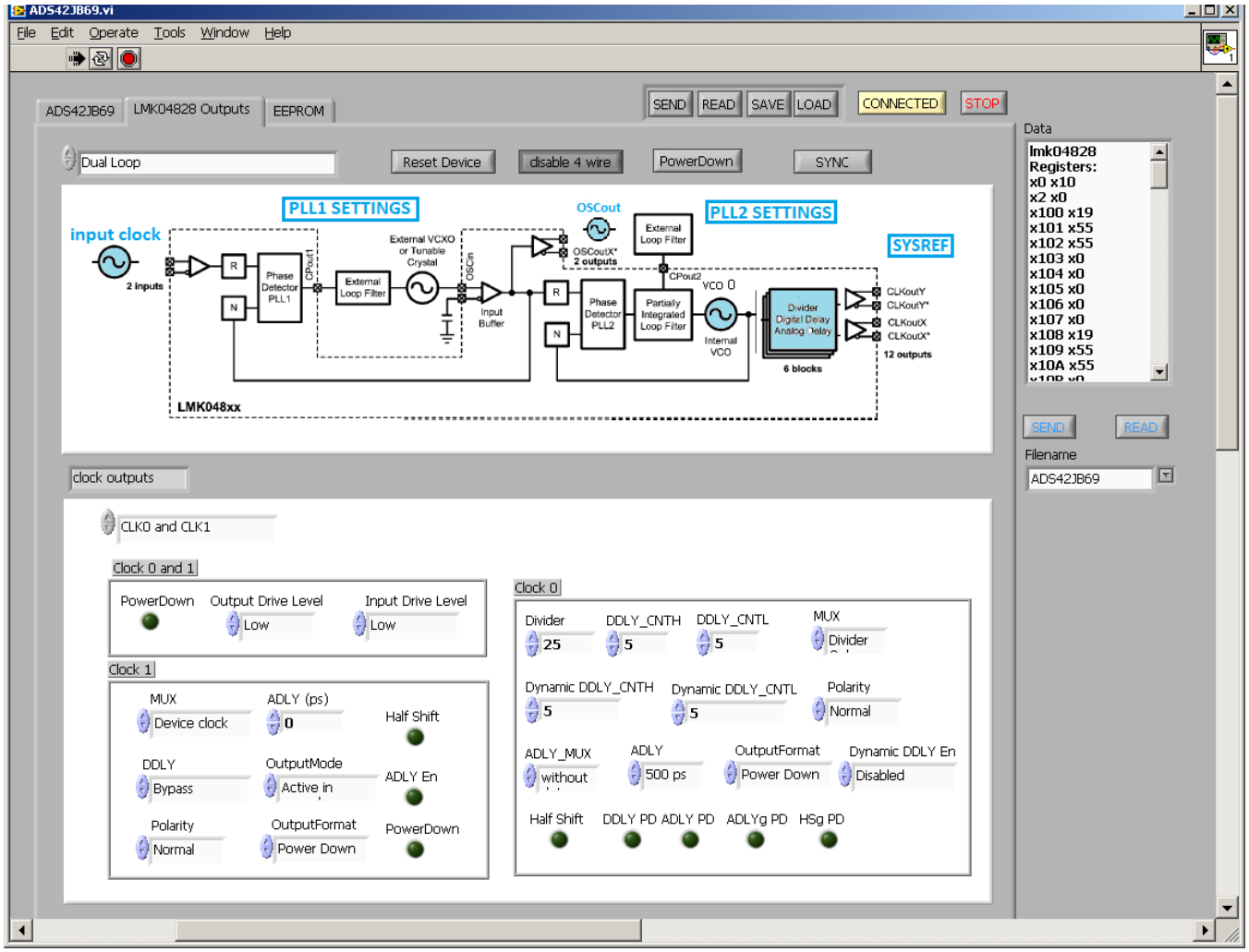

Figure 6. LMK04828 Outputs Control Window of the ADS42JBx9 GUI

2.2.5.1 Divider, Digital Delay, Analog Delay Controls

The default lower panel is for output control. This is the block called *Divider, Digital Delay, Analog Delay* in the block diagram. In this panel the desired parameters are set for all Device clocks and SYSREF clocks. These controls include divide value, format, delay, and power down, for example. Consult the LMK04828 data sheet and design tools for more information regarding these outputs and the options available for controlling these outputs.

2.2.5.2 Input Clock

Clicking *Input clock* in the block diagram opens a new window as shown in Figure 7. This panel controls the input clock settings of the LMK04828. The input clock is used by PLL1 to lock the input reference clock to the VCXO which is used by PLL2 of the LMK04828.

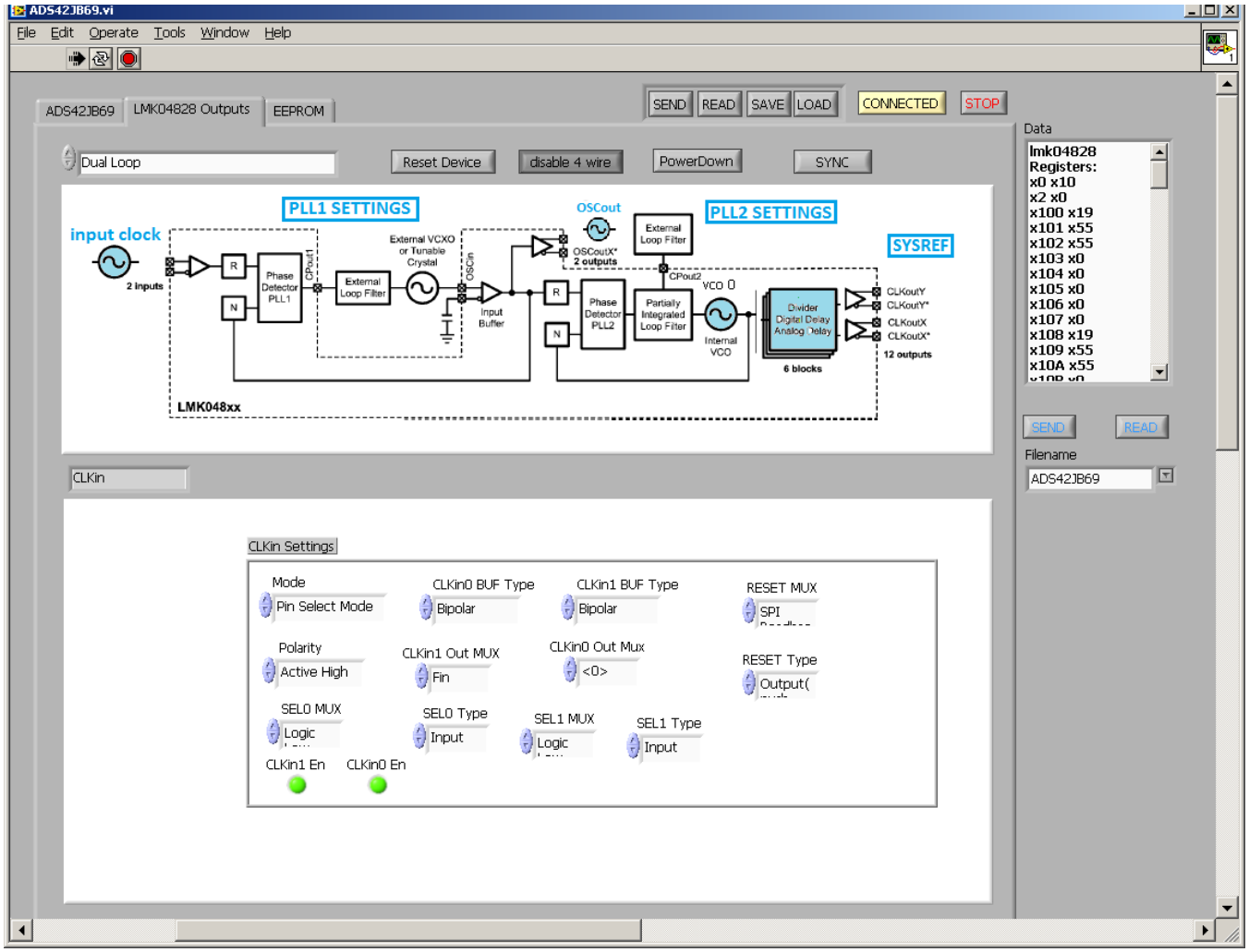

Figure 7. LMK04828 Input Clock Settings

2.2.5.3 PLL1 Settings Controls

Clicking *PLL1 SETTINGS* in the block diagram opens a new window, shown in Figure 8. This panel controls the PLL1 settings of the LMK04828. Once these values are properly entered and PLL1 becomes locked, LED D1 (LMK Locked) on the ADS42JBx9EVM illuminates. Some reasons for this not illuminating are using the wrong divider values or the reference oscillator tolerance (ppm) is too large.

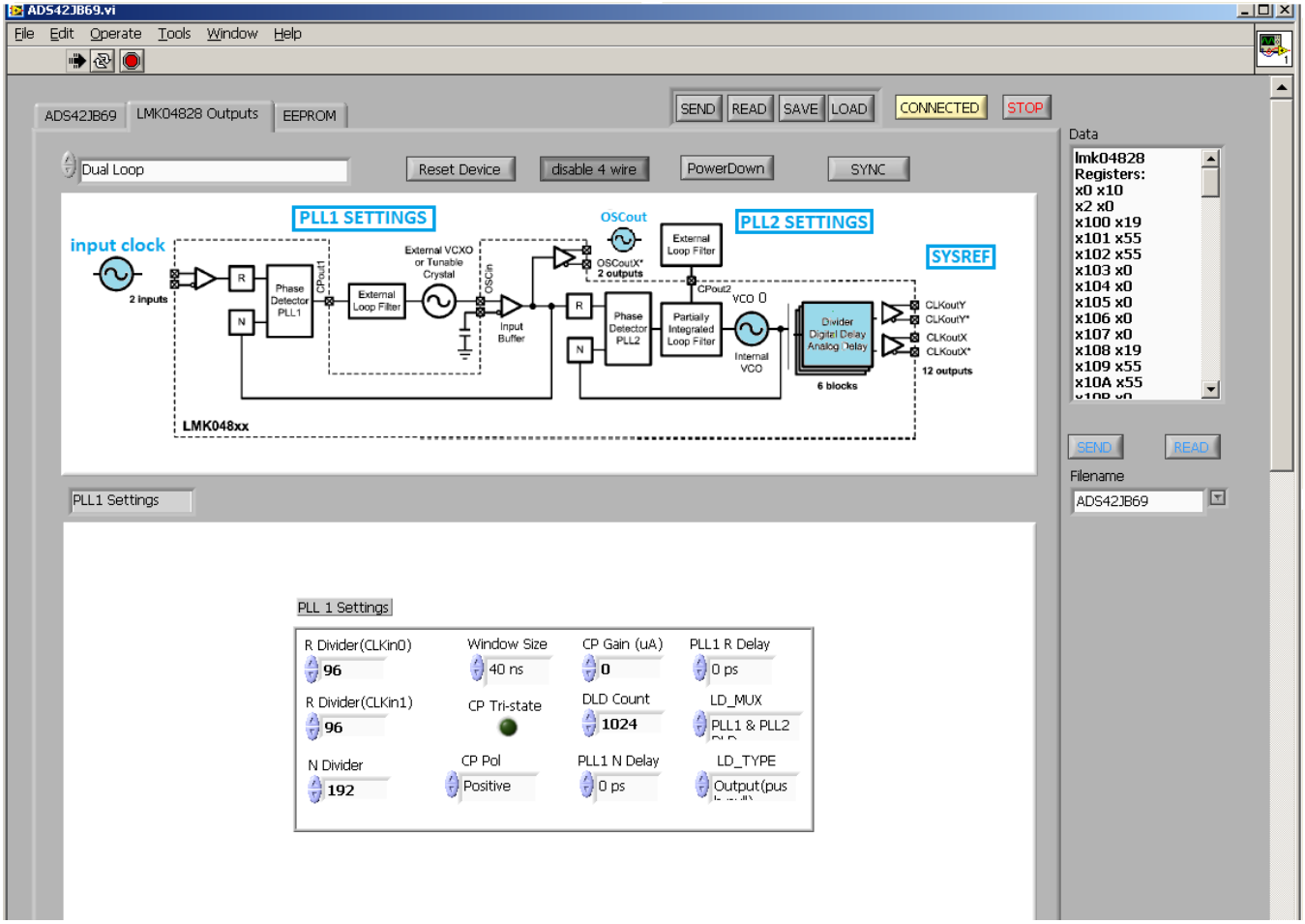

Figure 8. LMK04828 PLL1 Controls

2.2.5.4 PLL2 Settings Controls

Clicking *PLL2 SETTINGS* in the block diagram opens a new window, shown in Figure 9. This panel controls the PLL2 settings of the LMK04828. Once these values are properly entered and PLL2 becomes locked, LED D4 (PLL2 Locked) on the ADS42JBx9EVM illuminates. A reason this does not illuminate is using the wrong divider values. Use the LMK clock design tools when determining external PLL loop filter components. Go to the LMK04828 product folder on the TI website to download this tool and other application notes.

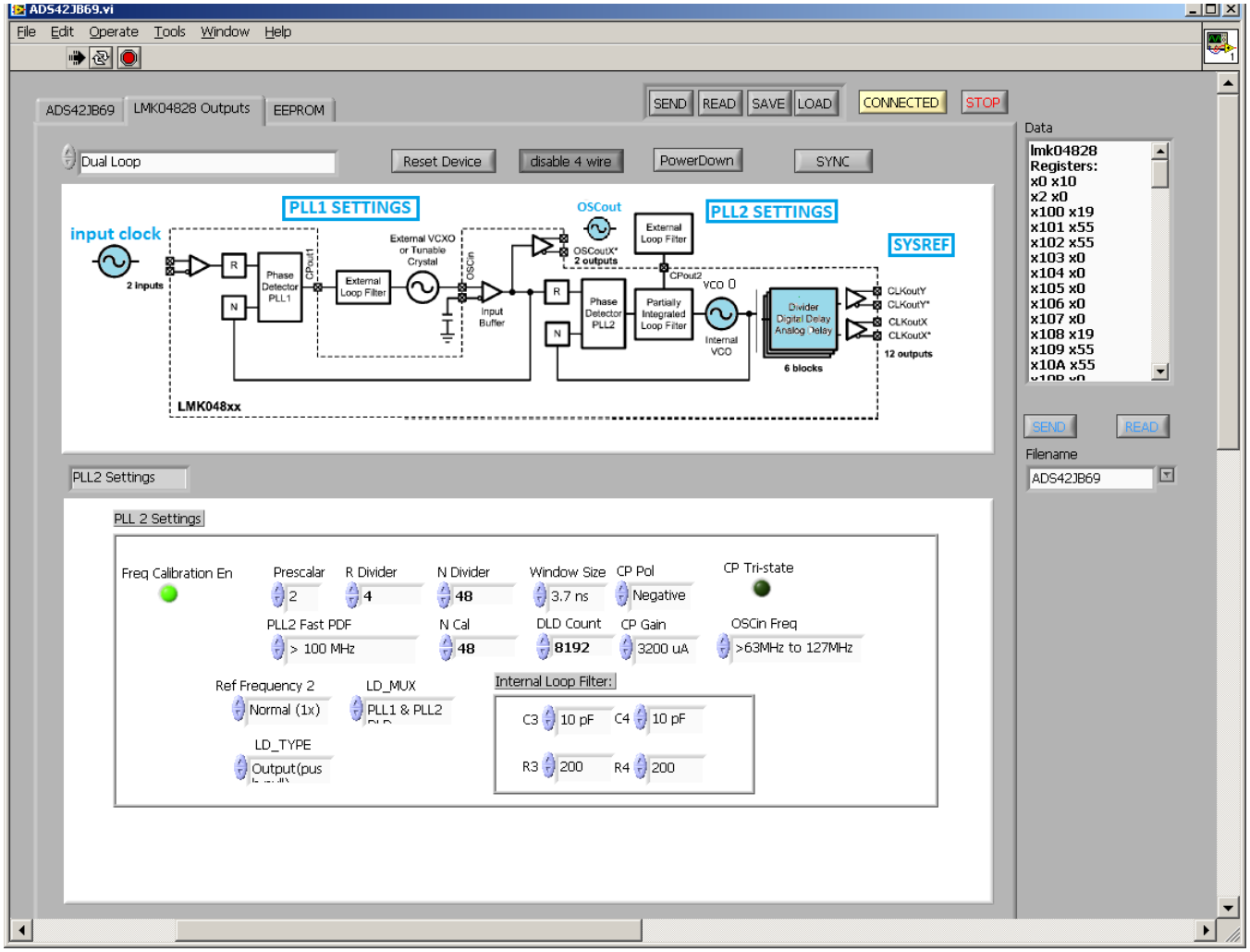

Figure 9. LMK04828 PLL2 Controls

2.2.5.5 Internal VCO Controls

Clicking *Internal VCO* in the block diagram allows selection of either internal VCO0 or VCO1.

2.2.5.6 OSCout Controls

Clicking *OSCout* in the block diagram provides control of the OSC output (currently not used on the EVM).

2.2.5.7 SYSREF Controls

Clicking *SYSREF* in the block diagram opens a new window, shown in Figure 10. This panel controls the SYSREF output global settings of the LMK04828. The settings made in this panel apply to all SYSREF outputs.

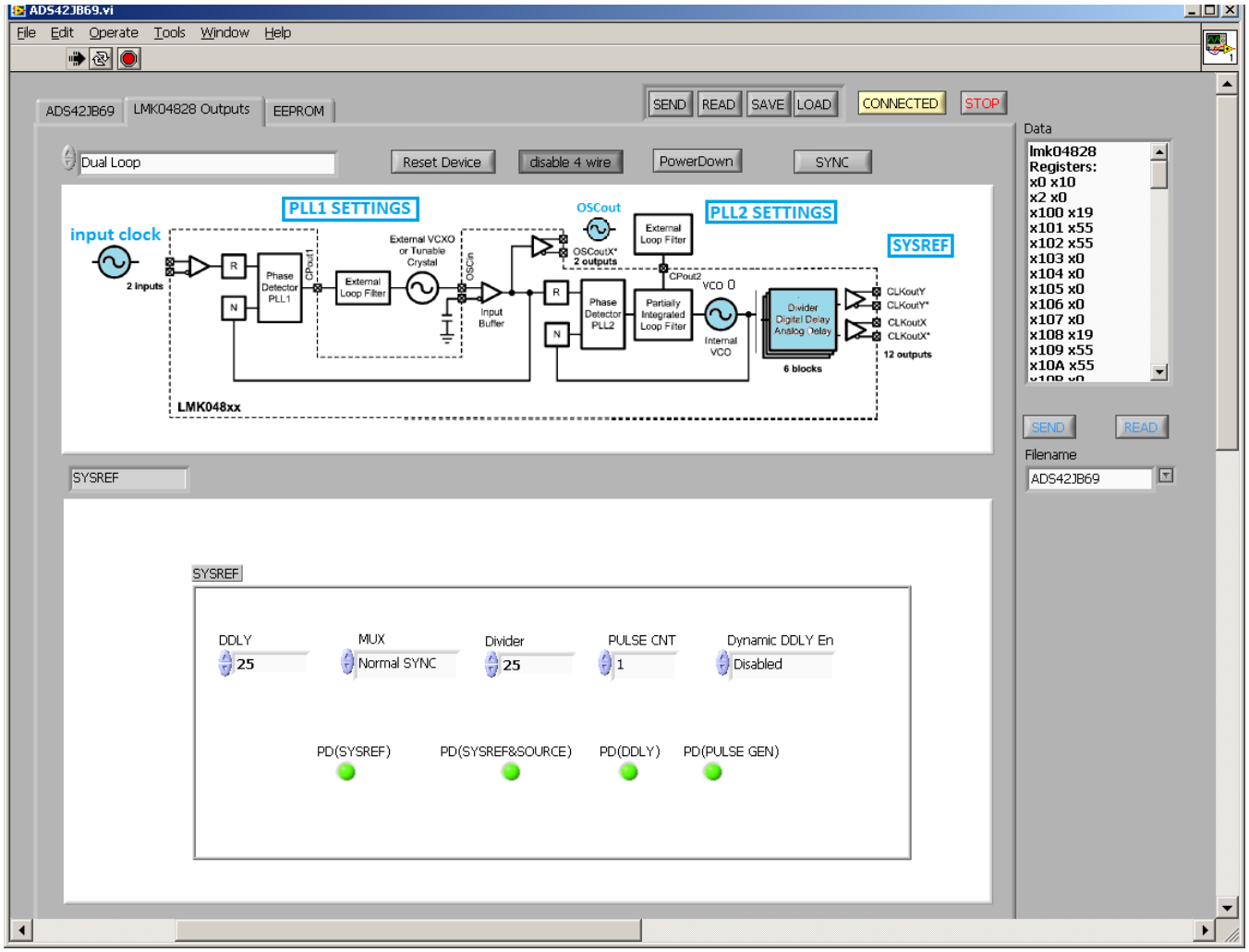

Figure 10. LMK04828 SYSREF Settings

2.3 JESD204B Translation Card

The block diagram for the JESD204B Translation card is shown in Figure 1. The various inputs, outputs, switches and jumpers are described in Table 4. The configuration file required by the FPGA is stored in the on-board EEPROM U8. Upon power up or pressing switch SW9, the contents of U8 are loaded into the FPGA. This process takes about 5-10 seconds, once completed, the FPGA_DONE LED illuminates. The current configuration only supports one mode of JESD204B operation. This mode is as follows:

- 4 lanes per link (L)
- 2 converters per device (M)
- 1 octet per frame clock period (F)
- 20 frames per multiframe (K)
- 1 sample per frame (S)
- Subclass 1
- ADC sample rate 250 MHz
- SerDes rate 2500 MHz

Future GUI software releases will support multiple configurations using a USB interface to configure the FPGA.

The design of the JESD204B Translation card is similar to the Xilinx Kintex-7 FPGA KC705 Evaluation Kit. The JESD204B receive function inside the Kintex 7 FPGA on the JESD204B Translation card implements the Xilinx Core Generator JESD204 function. Details about this core, Xilinx devices, software tools, and license required by this core, can be found at www.xilinx.com”

Table 4. Input and Output Connectors, Jumpers and Switches Description of the JESD204B Translation Card

Component	Description
J4	JESD204B FMC connector. Interfaces to ADS42JBx9EVM J3
J2 (TSW1400 ADC)	LVDS connector. Interfaces to TSW1400 ADC_INTERFACE connector J3
J3 (TSW1400 DAC)	LVDS connector. Interfaces to TSW1400 DAC_INTERFACE connector J4
J10 (Test connector)	Test header
J11 (JTAG)	JTAG interface to FPGA
J12 (EEPROM PROG)	EEPROM programming interface connector
J15 (+5V IN)	5-V power supply input
J13 (USB)	USB interface connector. Not used.
J17-J20	Spare transceiver I/O’s
J7 (SPARE1)	CMOS 10-MHz output
J8, J6	Spare I/O connectors
J5	Spare input clock or I/O connector
J9	Spare Input clock connector
J16	Spare TSW1400 DAC clock source
J1 (FAN PWR)	For use with FPGA fan. Currently not required.
J14 (PWR MON)	Power monitor U12 programming interface connector
SW2 & SW4	Spare dipswitches connected to spare FPGA inputs
SW1, SW3 & SW5	Spare pushbutton connected to spare FPGA inputs
SW6 (CPU RESET)	FPGA hardware reset
SW9 (FPGA_PROG_B)	FPGA reconfiguration switch. Causes the FPGA to load configuration from EEPROM.
SW8 (MSEL)	Sets programming mode of FPGA. Default is 1, 2, 3, 5 off and 4 on
SW10 (UCD Reset)	Power monitor U12 reset

Table 4. Input and Output Connectors, Jumpers and Switches Description of the JESD204B Translation Card (continued)

Component	Description
JP1 (Y1 PWR)	Power enable to 10-MHz oscillator Y1. Default is power on.
JP2 (REF SEL)	Selects SMA J9 or Y1 for use as an input clock source to FPGA. Default is Y1.
SJP12	Selects either 3.3 V or 1.8 V for Bank 0 VCC I/O reference. Default is 3.3 V.
SJP14	Selects either 3.3 V or 1.8 V for Bank 14 VCC I/O reference. Default is 3.3 V.
SJP15	Selects either 3.3 V or 1.8 V for Bank 15 VCC I/O reference. Default is 3.3 V.
SJP16	Selects either 2.5 V or 1.8 V for Bank 16 VCC I/O reference. Default is 2.5 V.
SJP17	Selects either 2.5 V or 1.8 V for Bank 17 VCC I/O reference. Default is 2.5 V.
SJP18	Selects either 2.5 V or 1.8 V for Bank 18 VCC I/O reference. Default is 2.5 V.
SJP2-SJP7, SJP20	USB or J12 control of EEPROM programming. Default is neither.
JP10-JP13	USB or JTAG control of FPGA programming. Default is JTAG
SJP13	FPGA or USB control of EEPROM chip select. Default is FPGA
SJP19	Sets CFGBVS pin voltage to either 3.3 V or GND. Default is 3.3 V.
SJP8-SJP11	Power monitor program pin interface. Selects either J14 or USB. Default is J14

3 Basic Test Setup

This section outlines basic testing of the ADS42JB69SEK.

3.1 Test Block Diagram

The test setup for the ADS42JBx9SEK is shown in Figure 11. The TSW1400EVM is used to capture data from the ADS42JBx9EVM through the JESD204B Translation card, which is then transferred to the computer for analysis in the HSDCPro software. The analog signal source shown is an HP8644B signal generator, however any analog signal source can be used. The clock source is from the LMK04828, but the board provides an option to use an external clock source, such as a HP8644B for the ADC sample clock. This involves a different setup, which is described in more detail, in the TI application note called "**Achieve 16bit Performance with ADS42JB69 and LMK04828".**

Note that there are filters on the analog source, which is necessary to achieve the best performance. The performance can be increased using external clock mode as this allows for the use of a filter on the clock source.

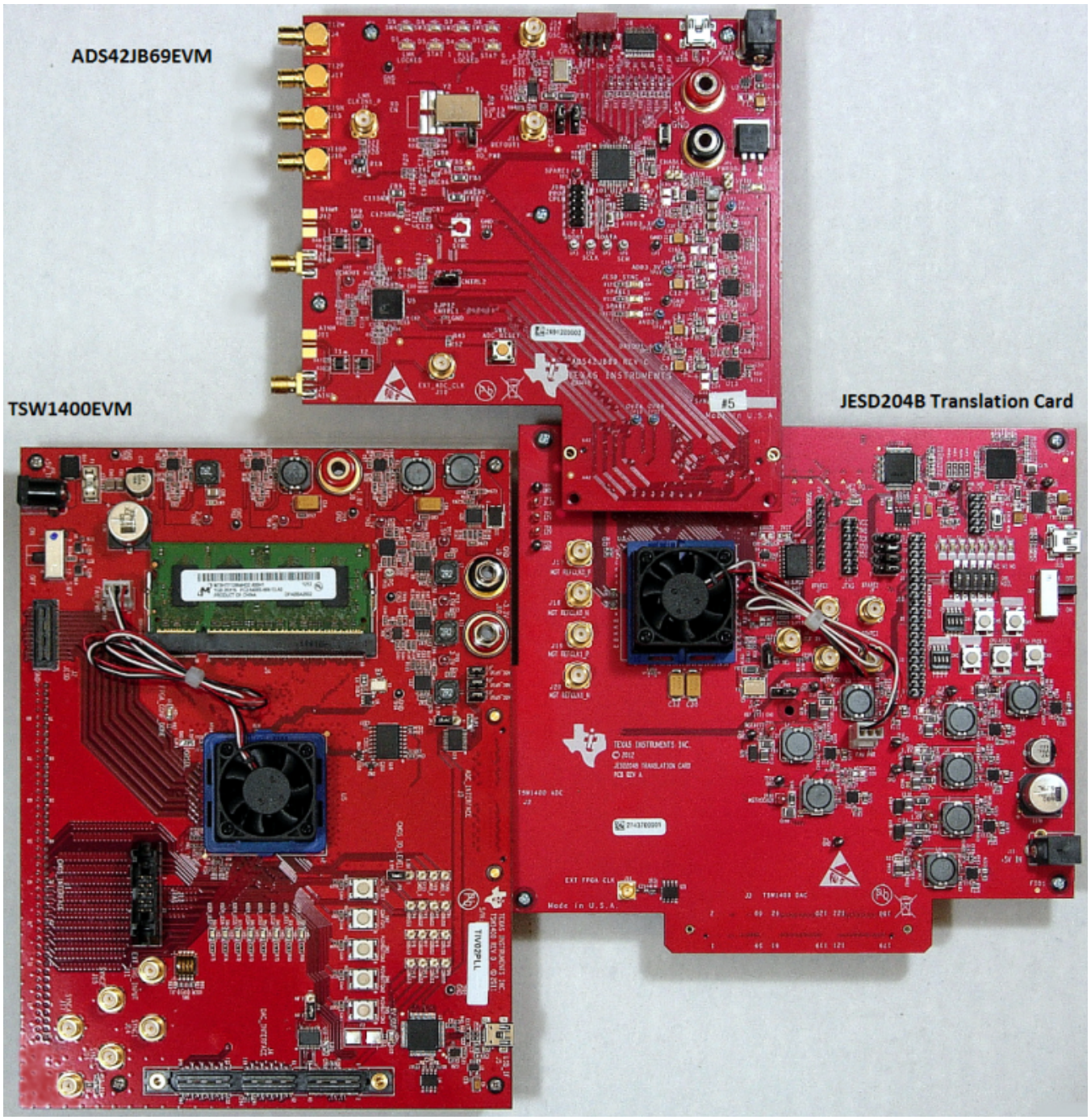

Figure 11. Test Setup

3.2 TSW1400EVM Setup

See the TSW1400EVM User's Guide (SLWU079) for a more detailed explanation of the TSW1400 setup and its features. This document assumes that the HSDCPro software and the TSW1400 pattern capture and generation board are both installed and functioning properly. This information can be found at http://www.ti.com/tool/tsw1400evm.

3.3 ADS42JBx9SEK Quick-Start Procedure

Connect J3 of a TSW1400EVM into J2 of a JESD204B Translation card. Connect J3 of a ADS42JBx9EVM into J4 of a JESD204B Translation card.

3.3.1 TSW1400EVM Data Capture Card

1. Connect a 5-V power supply to connector *J12* of the TSW1400EVM.
2. Flip switch *SW7* to the *ON* position.
3. Insert a USB cable into the USB port on the TSW1400. Connect the other end to the PC.

3.3.2 JESD204B Translation card

1. Connect a 5-V power supply to connector J15 of a JESD204B Translation card.
2. Flip switch SW7 to the *ON* position. Verify that the LED labeled “FPGA_DONE” turns on after about 10 seconds after power is applied.

3.3.3 ADS42JBx9EVM

1. Connect a 5-V power supply to connector J13.
2. Connect a USB cable to the USB port on the ADS42JBx9EVM and connect the other end to the PC.
3. Connect a signal source to either analog input SMA connector J1 (*AINP*) or J2 (*BINP*). For single-tone testing, a bandpass filter should be used to achieve the best SNR and harmonic performance
4. Press the *RESET* switch, *SW1*.

3.3.4 ADS42JBx9 GUI

1. Start the ADS42JBx9 GUI by selecting **Start Menu → Program Files → Texas Instruments ADCs → ADS42JBx9 GUI**.
2. In the upper right-hand corner, there is either a flashing red and yellow button labeled **RESET** or a yellow button labeled **CONNECTED**. If it says **RESET**, then click the button until it reads **CONNECTED** and stops flashing. This indicates that the ADS42JBx9EVM is connected to the computer.
3. In the top section of the GUI, click on *SEND* to verify connection. If the connection is valid, the DATA panel on the far right side of the GUI shall display the current settings of the GUI for both the LMK and ADC devices and send them to the parts.
4. In the top section of the GUI, click on *LOAD*. A new file browser opens. Navigate to were the GUI was installed and click on *ADS42JB69_LMK04828_settings.txt*. Click on *SEND* to load the device registers with the new values.
5. The two PLL's of the LMK04828 should now be locked. This is indicated by the illuminated LED's, D4 (PLL2 LOCKED) and D1 labeled (LMK LOCKED).
6. Click on the tab labeled *LMK0428 Outputs* located at the top of the GUI. A new window opens. Click the **SYNC** button.
7. The JESD204B Translation card should now be receiving a DEVICE clock and a SYSREF clock. The SYSREF signal can be observed on either SMA's J4 or J17 of the ADC EVM. The default frequency is 6.25 MHz.
8. On the JESD204B Translation card, press the **FPGA PROG B** switch SW9 to restart the FPGA. After about 10 seconds, the **FPGA DONE** LED will turn on indicating the FPGA has completed programming from the EEPROM.
9. After configuration is complete, the receiver FPGA will now assert the JESD204B SYNC high, since synchronization has not been established with the transmitter ADC. This is indicated by LED D3

(JESD_SYNC) illuminating on the ADS42JBx9EVM.

10. Once synchronization has been established, LED D3 on the ADS42JBx9EVM will turn off. The status LED's on the JESD204B Translation card should have the following states:

    D8 - On (OSERDES MMCM lock)
    D7 - On (GTX CDR lock)
    D6 - Off (not used)
    D5 - On (~SYNC)
    D4 - On (Data Valid)
    D3 - Off (not used)
    D2 - Blinking (devclkA indicator)
    D1 - Blinking (devclkB indicator)

11. If the status of the LED's are not as shown above, press the **CPU RESET** button (SW6) on the JESD204B Translation card to reset the firmware. Once the status of the LED's is as shown above, the JESD204B Translation will now be receiving valid data from the ADC and sending valid data and a clock to the TSW1400EVM.

12. Since a periodic SYSREF signal acts as a sub-harmonic clock of the converter sampling clock and may have spurious effect on the converter performance, it may be turned off during normal operation once synchronization has been achieved.

    To turn off SYSREF, click on the LMK04828 Outputs tab, then click on the **SYSREF** button. In the lower panel, go to the MUX panel and set this to **SYSREF PULSES**. This will turn off all of the SYSREF outputs of the LMK device.

    NOTE: If SYSREF is turned off during normal operation, TX and RX devices must have the ability to generate a *SYSREF* request to the LMK04828 clock generator whenever a synchronization request is detected at the SYNC interface.

13. If the JESD204B link does not get established, make sure the SYSREF MUX panel on the ADS42JBx9 GUI is set to **SYSREF CONTINUOUS**. If this is set to any other value, the SYSREF outputs will be disabled from the LMK04828, thus possibly preventing synchronization from occurring. If SYSREF MUX is set properly and the link is still invalid, press the **FPGA_PROG_B** switch (SW9) on the JESD204B Translation card. After the **FPGA DONE** LED illuminates, press the **CPU RESET**. If this does not provide synchronization, cycle power to the ADC EVM to reset all of the ADC and LMK internal registers and repeat steps 1-10.

3.3.5 High Speed Data Converter Pro (HSDCPro)

1. Start the HSDCPro software tool by selecting **Start Menu → All Programs → Texas Instruments ADCs → High Speed Data Converter Pro**.
2. When prompted for the serial number of the board, select the serial number that represents the TSW1400 that has been connected to the ADS42JBx9. This number is on a sticker on the TSW1400 board.
3. In the *Select ADC* drop-down box select *ADS42JB69*. If the GUI asks to download the firmware, select *Yes*.
4. Once the firmware has finished downloading, LED's D2-D9 on the TSW1400 should be illuminated except for USER_LED4.
5. Select *Single Tone* from the *Test Selection* drop-down menu.
6. At the bottom-left corner, enter *250M* in the *ADC Sampling Rate (Fs)* box. If using a coherent frequency input, select *Auto Calculation of Coherent Frequencies* and use the ADC Input Target Frequency value for the input frequency
7. If a windowing function is desired, then *Blackman* should be selected above the plot window. If the signals are synchronized and coherent, select *Rectangular*.
8. All boards and software are now setup. Click the **Capture** button. A sample capture is shown in Figure 12 for the ADS42JB69 with a 250-MHz clock and 100-MHz input frequency.

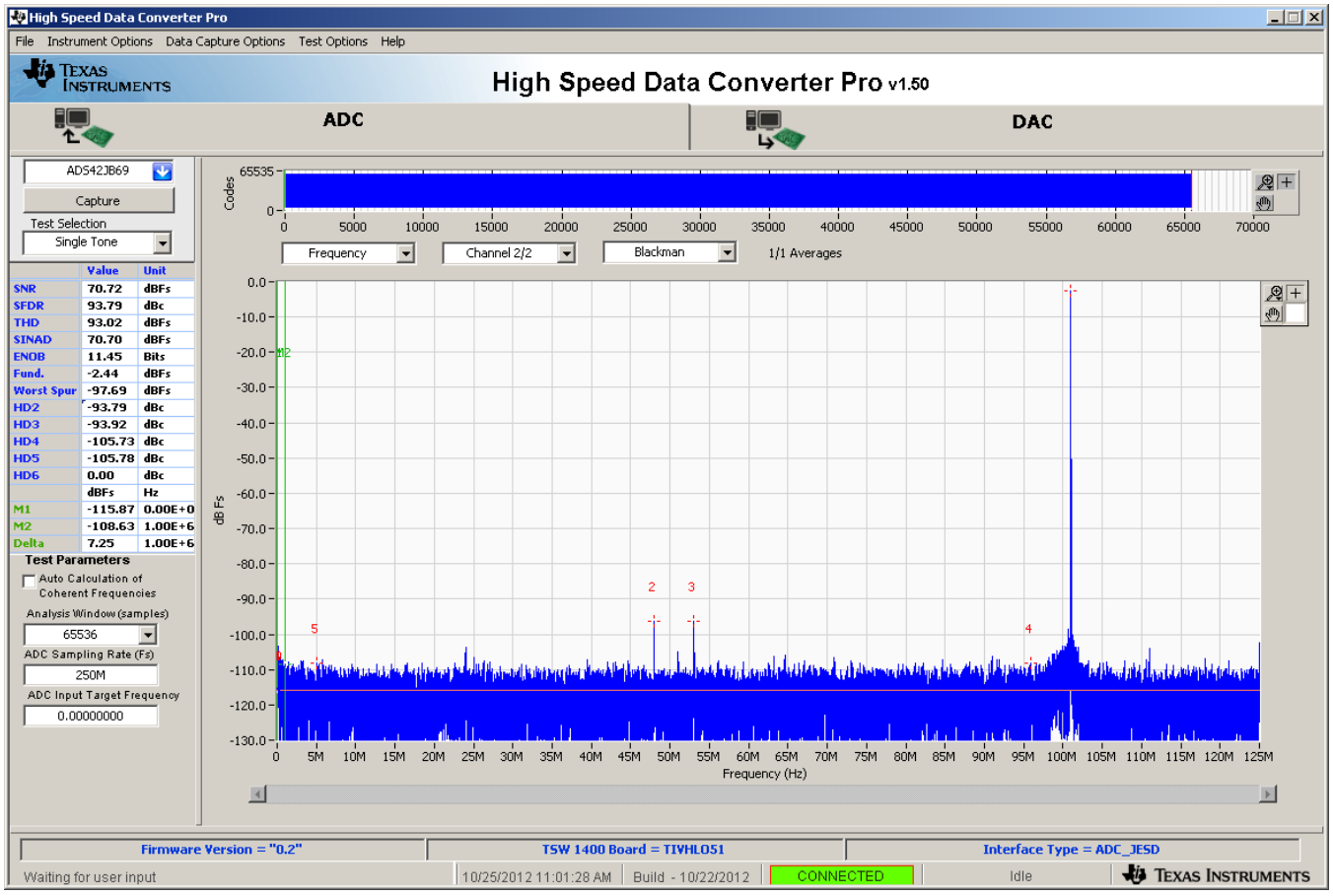

Figure 12. High Speed Data Converter Pro (HSDCPro) Sample Capture

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General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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