

ADS126x 32-Bit, Precision, 38-kSPS, Analog-to-Digital Converters with PGA and Voltage Reference

1 Features

- Precision, 32-bit, $\Delta\Sigma$ ADC
- Second 24-Bit Auxiliary $\Delta\Sigma$ ADC (ADS1263)
- Data Rates: 2.5 SPS to 38400 SPS
- Differential Input, CMOS PGA
- 11 Multifunction Analog Inputs
 - Ten Single-Ended or Five Differential
- High-Accuracy Architecture
 - Offset Drift: 1 nV/°C
 - Gain Drift: 1 ppm/°C
 - Noise: 7 nV RMS (2.5 SPS, Gain = 32)
 - Linearity: 2 ppm
- Internal Reference Drift: 2 ppm/°C
- Dual Sensor Excitation Current Sources
- Integrated Fault Detection/Data CRC
- Internal ADC Test Voltage
- Eight General-Purpose Input/Outputs

2 Applications

- High-Resolution PLCs
- Temperature, Pressure Measurement
- Weigh Scales and Strain-Gauge Digitizers
- Panel Meters, Chart Recorders
- Analytical Instrumentation

3 Description

The ADS1262 and ADS1263 are low-noise, low-drift, 38.4 kSPS, delta-sigma ($\Delta\Sigma$), analog-to-digital converters (ADCs) with an integrated PGA, reference, and internal fault monitors. The ADS1263 integrates an auxiliary, 24-bit, $\Delta\Sigma$ ADC intended for background measurements. The sensor-ready ADCs provide complete, high-accuracy, one-chip measurement solutions for the most-demanding sensor applications, including weigh scales, strain-gauge sensors, thermocouples, and resistance temperature devices (RTD).

The ADCs are comprised of a low-noise, CMOS PGA (gains from 1 to 32), a $\Delta\Sigma$ modulator, followed by a programmable digital filter. The flexible analog front-end (AFE) incorporates two sensor excitation current sources suitable for direct RTD measurement.

A single-cycle settling digital filter maximizes multiple-input conversion throughput, while providing 130-dB rejection of 50-Hz and 60-Hz line cycle interference.

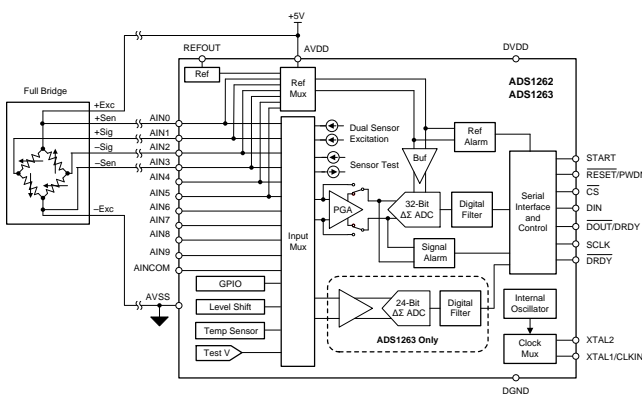
The ADS1262 and ADS1263 are pin and functional compatible. The ADCs are available in a 28-pin TSSOP package and are fully specified over the -40°C to $+125^{\circ}\text{C}$ operating range.

Device Information⁽¹⁾

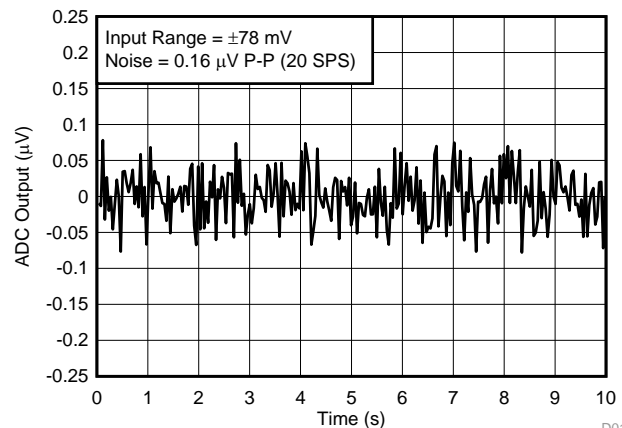
PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS1262	TSSOP (28)	9.70 mm x 4.40 mm
ADS1263	TSSOP (28)	9.70 mm x 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Schematic



ADC Conversion Noise



D017



Table of Contents

1 Features	1	5.1 Trademarks	3
2 Applications	1	5.2 Electrostatic Discharge Caution	3
3 Description	1	5.3 Glossary	3
4 Revision History	2	6 Mechanical, Packaging, and Orderable Information	3
5 Device and Documentation Support	3		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2015	*	Initial release.

5 Device and Documentation Support

5.1 Trademarks

All trademarks are the property of their respective owners.

5.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1262IPW	PREVIEW	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1262	
ADS1262IPWR	PREVIEW	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1262	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

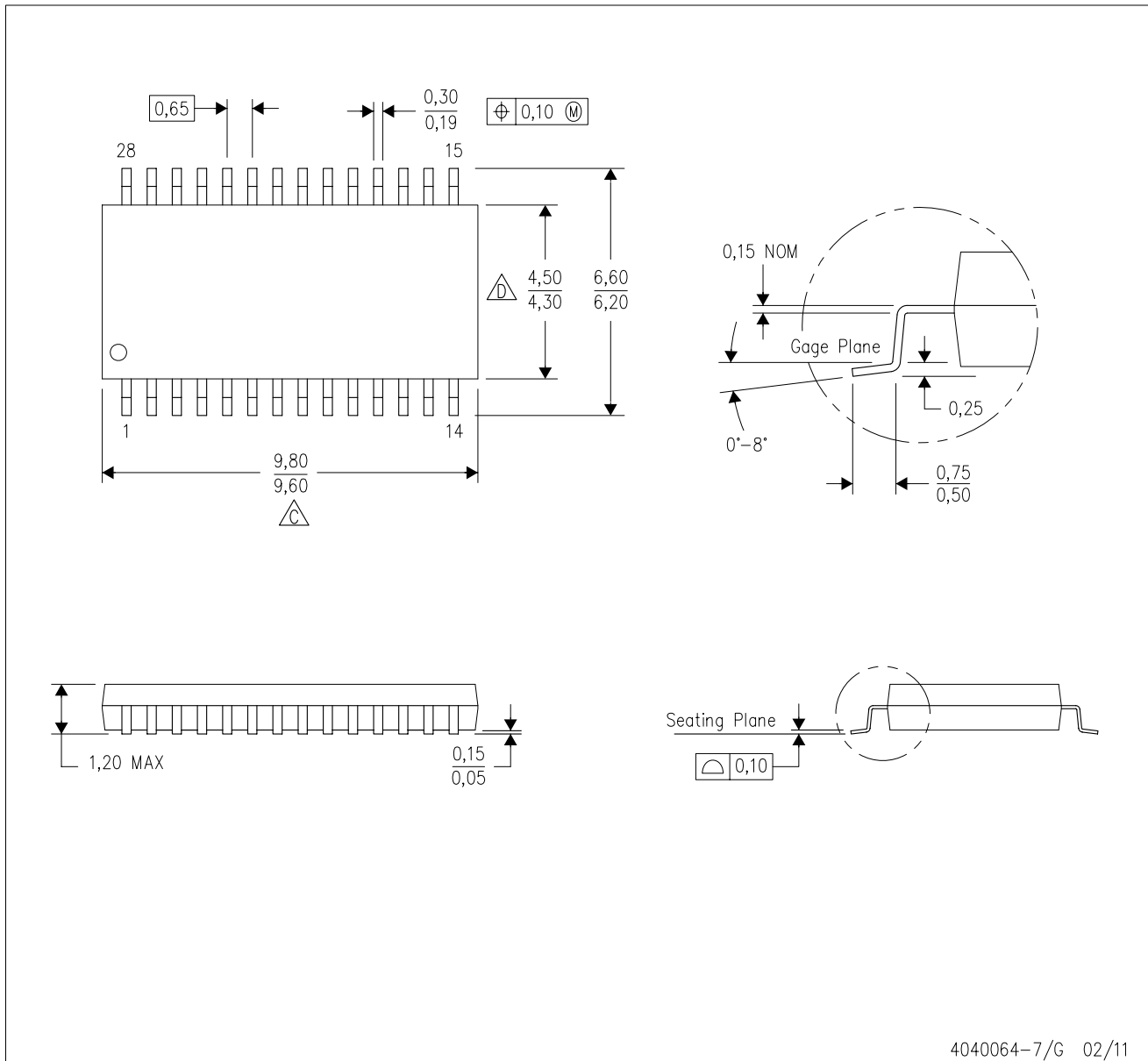
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

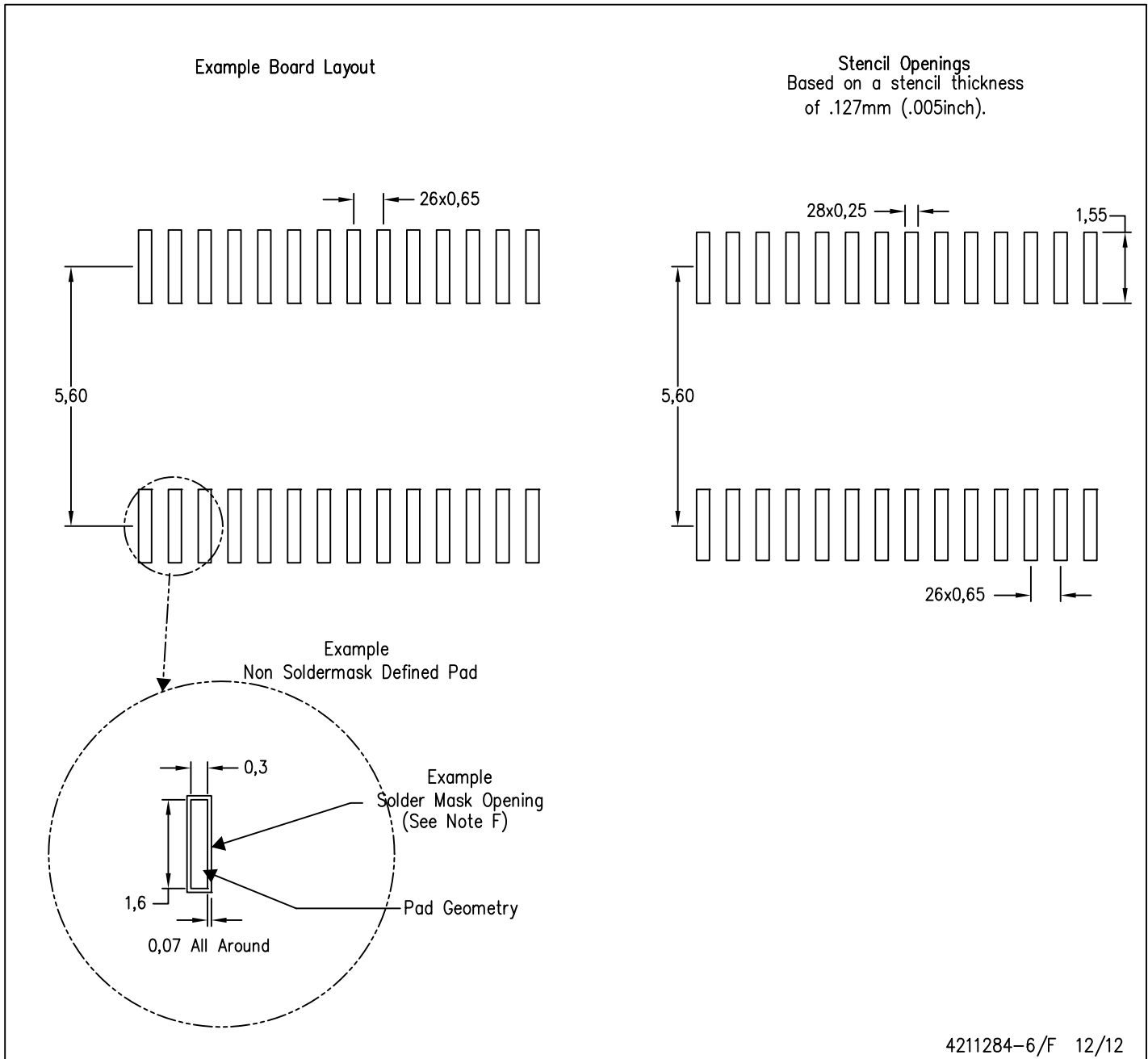


4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

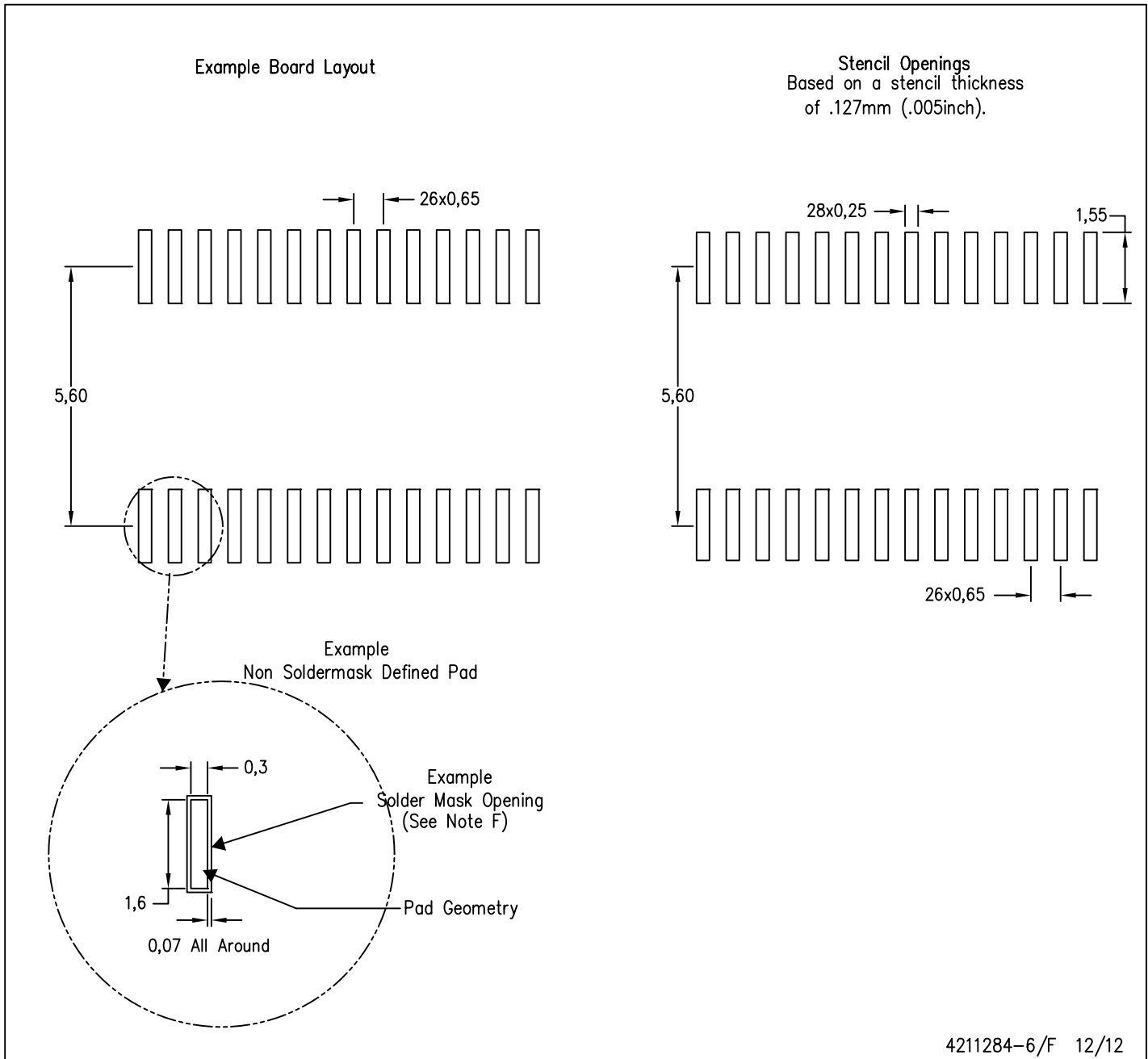
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G28)

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