ADC344x Quad-Channel, 14-Bit, 25-MSPS to 125-MSPS, Analog-to-Digital Converter

1 Features

- Quad Channel
- 14-Bit Resolution
- Single Supply: 1.8 V
- Serial LVDS Interface (SLVDS)
- Flexible Input Clock Buffer with Divide-by-1, -2, -4
- SNR = 72.4 dBFS, SFDR = 87 dBc at f_{IN} = 70 MHz
- Ultra-Low Power Consumption:
  - 98 mW/Ch at 125 MSPS
- Channel Isolation: 105 dB
- Internal Dither and Chopper
- Support for Multi-Chip Synchronization
- Pin-to-Pin Compatible with 12-Bit Version
- Package: VQFN-56 (8 mm × 8 mm)

2 Applications

- Multi-Carrier, Multi-Mode Cellular Base Stations
- Radar and Smart Antenna Arrays
- Munitions Guidance
- Motor Control Feedback
- Network and Vector Analyzers
- Communications Test Equipment
- Nondestructive Testing
- Microwave Receivers
- Software-Defined Radios (SDRs)
- Quadrature and Diversity Radio Receivers

3 Description

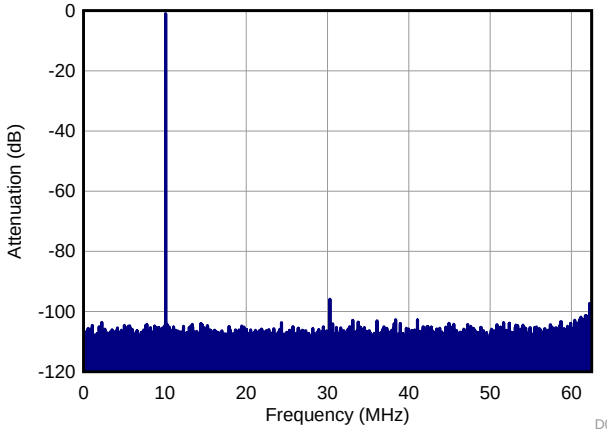
The ADC344x are a high-linearity, ultra-low power, quad-channel, 14-bit, 25-MSPS to 125-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization. The ADC344x family supports serial low-voltage differential signaling (LVDS) and JESD204B interfaces in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 14-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC344x	VQFN (48)	8.00 mm × 8.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Performance at f_S = 125 MSPS, f_{IN} = 10 MHz



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4 Revision History

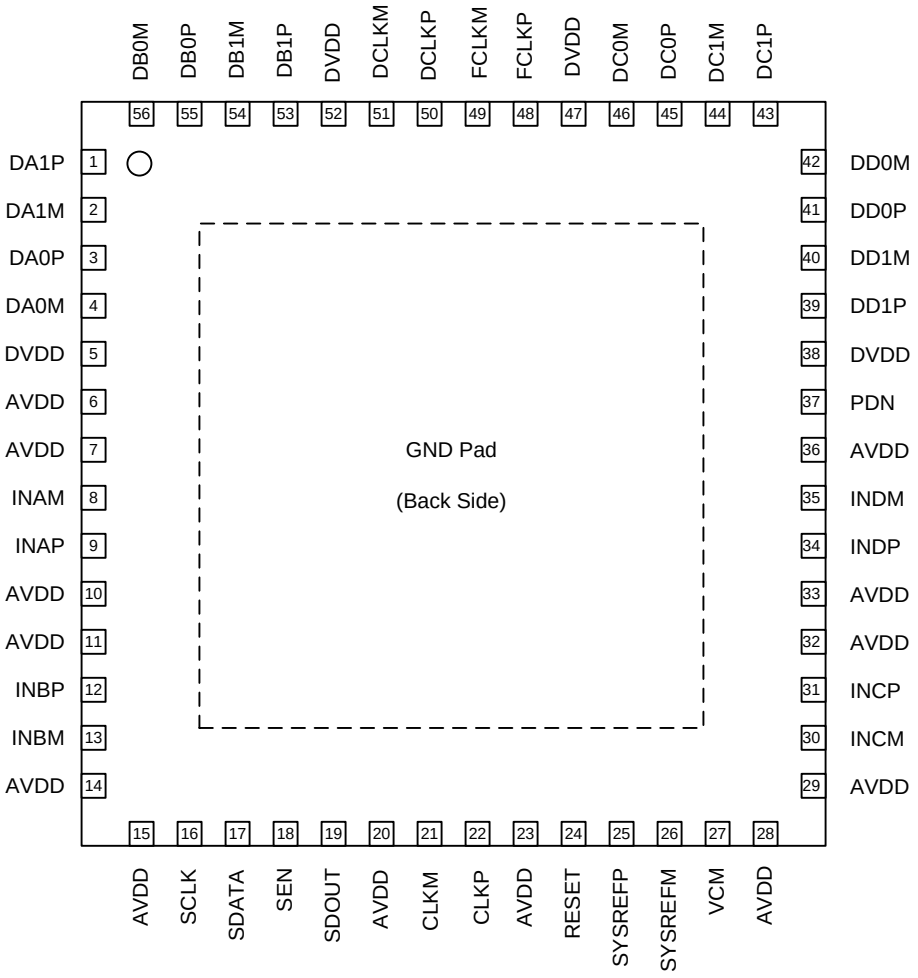
DATE	REVISION	NOTES
July 2014	*	Initial release.

5 Device Comparison Table

INTERFACE	RESOLUTION (Bits)	25 MSPS	50 MSPS	80 MSPS	125 MSPS	160 MSPS
Serial LVDS	12	ADC3421	ADC3422	ADC3423	ADC3424	—
	14	ADC3441	ADC3442	ADC3443	ADC3444	—
JESD204B	12	—	ADC34J22	ADC34J23	ADC34J24	ADC34J25
	14	—	ADC34J42	ADC34J43	ADC34J44	ADC34J45

6 Pin Configuration and Functions

RTQ Package
VQFN-56
(Top View)



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Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	6, 7, 10, 11, 14, 15, 20, 23, 28, 29, 32, 33, 36	I	Analog 1.8-V power supply
CLKM	21	I	Negative differential clock input for the ADC
CLKP	22	I	Positive differential clock input for the ADC
DA0M	4	O	Negative serial LVDS output for channel A0
DA0P	3	O	Positive serial LVDS output for channel A0
DA1M	2	O	Negative serial LVDS output for channel A1
DA1P	1	O	Positive serial LVDS output for channel A1
DB0M	56	O	Negative serial LVDS output for channel B0
DB0P	55	O	Positive serial LVDS output for channel B0
DB1M	54	O	Negative serial LVDS output for channel B1
DB1P	53	O	Positive serial LVDS output for channel B1
DC0M	46	O	Negative serial LVDS output for channel C0
DC0P	45	O	Positive serial LVDS output for channel C0
DC1M	44	O	Negative serial LVDS output for channel C1
DC1P	43	O	Positive serial LVDS output for channel C1
DD0M	42	O	Negative serial LVDS output for channel D0
DD0P	41	O	Positive serial LVDS output for channel D0
DD1M	40	O	Negative serial LVDS output for channel D1
DD1P	39	O	Positive serial LVDS output for channel D1
DCLKM	51	O	Negative bit clock output
DCLKP	50	O	Positive bit clock output
DVDD	5, 38, 47, 52	I	Digital 1.8-V power supply
FCLKM	49	O	Negative frame clock output
FCLKP	48	O	Positive frame clock output
GND	PowerPAD™	I	Ground, 0 V
INAM	8	I	Negative differential analog input for channel A
INAP	9	I	Positive differential analog input for channel A
INBM	13	I	Negative differential analog input for channel B
INBP	12	I	Positive differential analog input for channel B
INCM	30	I	Negative differential analog input for channel C
INCP	31	I	Positive differential analog input for channel C
INDM	35	I	Negative differential analog input for channel D
INDP	34	I	Positive differential analog input for channel D
PDN	37	I	Power-down control. This pin can be configured via the SPI. This pin has an internal 150-kΩ pull-down resistor.
RESET	24	I	Hardware reset; active high. This pin has an internal 150-kΩ pull-down resistor.
SCLK	16	I	Serial interface clock input. This pin has an internal 150-kΩ pull-down resistor.
SDATA	17	I	Serial interface data input. This pin has an internal 150-kΩ pull-down resistor.
SDOUT	19	O	Serial interface data output
SEN	18	I	Serial interface enable; active low. This pin has an internal 150-kΩ pull-up resistor to AVDD.
SYSREFM	26	I	Negative external SYSREF input
SYSREFP	25	I	Positive external SYSREF input
VCM	27	O	Common-mode voltage for analog inputs

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Analog supply voltage range, AVDD		–0.3	2.1	V
Digital supply voltage range, DVDD		–0.3	2.1	V
Voltage applied to input pins:	INAP, INBP, INAM, INBM	–0.3	min (1.9, AVDD + 0.3)	V
	CLKP, CLKM	–0.3	AVDD + 0.3	V
	SYSREFP, SYSREFM	–0.3	AVDD + 0.3	V
	SCLK, SEN, SDATA, RESET, PDN	–0.3	3.9	V
Temperature range	Operating free-air, T_A	–40	85	ºC
	Operating junction, T_J		125	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage range		1.7	1.8	1.9	V
DVDD	Digital supply voltage range		1.7	1.8	1.9	V
ANALOG INPUT						
V_{ID}	Differential input voltage	For input frequencies < 450 MHz		2		V_{PP}
		For input frequencies < 600 MHz		1		V_{PP}
V_{IC}	Input common-mode voltage			VCM ± 0.025		V
CLOCK INPUT						
	Input clock frequency	Sampling clock frequency	10		125(1)	MSPS
	Input clock amplitude (differential)	Sine wave, ac-coupled		1.5		V
		LPECL, ac-coupled		1.6		V
		LVDS, ac-coupled		0.7		V
	Input clock duty cycle			50%		
	Input clock common-mode voltage			0.95		V
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to GND			3.3		pF
R_{LOAD}	Single-ended load resistance			100		Ω

(1) With the clock divider enabled by default for divide-by-1. Maximum sampling clock frequency for the divide-by-4 option is 500 MSPS.

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7.4 Thermal Information

THERMAL METRIC(1)		ADC344x RTQ (VQFN) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	3.4	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	3.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Performance Modes

over operating free-air temperature range (unless otherwise noted)

MODE	REGISTER SETTINGS	DESCRIPTION
Special modes	Registers 139 (bit 3), 239 (bit 3), 439 (bit 3), and 539 (bit 3)	Always write 1 for best performance
Disable dither	Registers 1 (bits 7:0), 134 (bits 5 and 3), 234 (bits 5 and 3), 434 (bits 5 and 3), and 534 (bits 5 and 3)	Disable dither to improve SNR
Disable chopper	Registers 122 (bit 1), 222 (bit 1), 422 (bit 1), and 522 (bit 1)	Disable chopper to shift 1/f noise floor at dc

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7.6 Electrical Characteristics: ADC3441, ADC3442

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER	ADC3441			ADC3442			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
ADC clock frequency			25			50	MSPS
Resolution	14			14			Bits
1.8-V analog supply current		54			71		mA
1.8-V digital supply current		45			56		mA
Total power dissipation		177			228		mW
Global power-down dissipation		5			5		mW
Wake-up time from global power-down		85			85		µs
Standby power-down dissipation		34			35		mW
Wake-up time from standby power-down		35			35		µs

7.7 Electrical Characteristics: ADC3443, ADC3444

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER	ADC3443			ADC3444			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
ADC clock frequency			80			125	MSPS
Resolution	14			14			Bits
1.8-V analog supply current		92			119		mA
1.8-V digital supply current		68			98		mA
Total power dissipation		288			391		mW
Global power-down dissipation		5			5		mW
Wake-up time from global power-down		85			85		us
Standby power-down dissipation		40			43		mW
Wake-up time from standby power-down		35			35		µs

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7.8 Electrical Characteristics: General

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Differential input full-scale				2.0		V_{PP}
r_i	Input resistance	Differential at dc			6.6		kΩ
c_i	Input capacitance	Differential at dc			3.7		pF
$V_{OC(VCM)}$	VCM common-mode voltage output				0.95		V
	VCM output current capability				10		mA
	Input common-mode current	Per analog input pin			1.5		µA/MSPS
	Analog input bandwidth (3 dB)	50-Ω differential source driving 50-Ω termination across INP and INM			540		MHz
DC ACCURACY							
E_O	Offset error			–TBD		TBD	mV
α_{EO}	Temperature coefficient of offset error				TBD		mV/C
$E_{G(REF)}$	Gain error as a result of internal reference inaccuracy alone			–TBD		TBD	%FS
$E_{G(CHAN)}$	Gain error of channel alone				1.5		%FS
$\alpha_{(EGCHAN)}$	Temperature coefficient of $E_{G(CHAN)}$				TBD		Δ%FS/Ch
CHANNEL-TO-CHANNEL ISOLATION							
	Crosstalk(1)	f_{IN} = 10 MHz	Near channel		105		dB
			Far channel		105		dB
		f_{IN} = 100 MHz	Near channel		95		dB
			Far channel		105		dB
		f_{IN} = 200 MHz	Near channel		94		dB
			Far channel		105		dB
		f_{IN} = 230 MHz	Near channel		92		dB
			Far channel		105		dB
		f_{IN} = 300 MHz	Near channel		85		dB
			Far channel		105		dB

(1) Crosstalk is measured with a –1-dBFS input signal on the aggressor channel and no input on the victim channel.

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7.9 AC Performance: ADC3441

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3441 (f_S = 25 MSPS)						UNITS
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio (from 1-MHz offset)	f_{IN} = 10 MHz		73.7			74		dBFS
		f_{IN} = 20 MHz	TBD	73.65			73.9		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	73.65			73.9		
		f_{IN} = 70 MHz		73.5			73.7		
		f_{IN} = 100 MHz		73			73.2		
		f_{IN} = 170 MHz		71.3			71.5		
		f_{IN} = 230 MHz		70.7			70.8		
	Signal-to-noise ratio (full Nyquist band)	f_{IN} = 10 MHz		72.6			72.9		dBFS
		f_{IN} = 20 MHz		72.55			72.8		
		f_{IN} = 20 MHz, T_A = 25°C		72.55			72.8		
		f_{IN} = 70 MHz		72.5			72.7		
		f_{IN} = 100 MHz		72.1			72.3		
		f_{IN} = 170 MHz		70.5			70.7		
		f_{IN} = 230 MHz		69.9			70		
NSD(1)	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–144.7			–145		dBFS/Hz
		f_{IN} = 20 MHz	TBD	–144.6			–144.9		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	–144.6			–144.9		
		f_{IN} = 70 MHz		–144.5			–144.7		
		f_{IN} = 100 MHz		–144			–144.2		
		f_{IN} = 170 MHz		–142.3			–142.5		
		f_{IN} = 230 MHz		–141.7			–141.8		
SINAD(1)	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.6			73.9		dBFS
		f_{IN} = 20 MHz	TBD	73.6			73.7		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	73.6			73.7		
		f_{IN} = 70 MHz		73.4			73.5		
		f_{IN} = 100 MHz		72.9			72.9		
		f_{IN} = 170 MHz		71.1			71.2		
		f_{IN} = 230 MHz		70.4			70.2		
ENOB(1)	Effective number of bits	f_{IN} = 10 MHz		11.9			12		Bits
		f_{IN} = 20 MHz	TBD	11.9			12		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	11.9			12		
		f_{IN} = 70 MHz		11.9			11.9		
		f_{IN} = 100 MHz		11.8			11.8		
		f_{IN} = 170 MHz		11.5			11.5		
		f_{IN} = 230 MHz		11.4			11.4		

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(1) Reported from 1 MHz offset.

AC Performance: ADC3441 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3441 (f_S = 25 MSPS)						UNITS
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		93			90		dBc
		f_{IN} = 20 MHz	TBD	92			89		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	92			89		
		f_{IN} = 70 MHz		90			88		
		f_{IN} = 100 MHz		89			86		
		f_{IN} = 170 MHz		85			83		
		f_{IN} = 230 MHz		83			80		
HD2	Second harmonic distortion	f_{IN} = 10 MHz		99			95		dBc
		f_{IN} = 20 MHz	TBD	95			91		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	95			91		
		f_{IN} = 70 MHz		92			90		
		f_{IN} = 100 MHz		90			87		
		f_{IN} = 170 MHz		87			85		
		f_{IN} = 230 MHz		83			81		
HD3	Third harmonic distortion	f_{IN} = 10 MHz		93			90		dBc
		f_{IN} = 20 MHz	TBD	92			89		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	92			89		
		f_{IN} = 70 MHz		90			88		
		f_{IN} = 100 MHz		89			86		
		f_{IN} = 170 MHz		85			83		
		f_{IN} = 230 MHz		83			80		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		98			97		dBc
		f_{IN} = 20 MHz	TBD	97			95		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	97			95		
		f_{IN} = 70 MHz		96			95		
		f_{IN} = 100 MHz		96			95		
		f_{IN} = 170 MHz		96			94		
		f_{IN} = 230 MHz		94			92		
THD	Total harmonic distortion	f_{IN} = 10 MHz		92			89		dBc
		f_{IN} = 20 MHz	TBD	90			87		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	90			87		
		f_{IN} = 70 MHz		88			86		
		f_{IN} = 100 MHz		87			84		
		f_{IN} = 170 MHz		84			82		
		f_{IN} = 230 MHz		81			78		
IMD3	Third-tone intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		94			95		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		89			88		

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7.10 AC Performance: ADC3442

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3442 (f_S = 50 MSPS)						UNITS
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio (from 1-MHz offset)	f_{IN} = 10 MHz		73.5			73.7		dBFS
		f_{IN} = 20 MHz	TBD	73.4			73.6		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	73.4			73.6		
		f_{IN} = 70 MHz		73			73.2		
		f_{IN} = 100 MHz		72.9			73		
		f_{IN} = 170 MHz		71.6			71.7		
		f_{IN} = 230 MHz		71.2			71.3		
	Signal-to-noise ratio (full Nyquist band)	f_{IN} = 10 MHz		72.7			72.9		
		f_{IN} = 20 MHz		72.7			72.9		
		f_{IN} = 20 MHz, T_A = 25°C		72.7			72.9		
		f_{IN} = 70 MHz		72.3			72.5		
		f_{IN} = 100 MHz		72.2			72.3		
		f_{IN} = 170 MHz		71			71.1		
		f_{IN} = 230 MHz		70.6			70.7		
NSD(1)	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–147.5			–147.7		dBFS/Hz
		f_{IN} = 20 MHz	TBD	–147.4			–147.6		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	–147.4			–147.6		
		f_{IN} = 70 MHz		–147			–147.2		
		f_{IN} = 100 MHz		–146.9			–147		
		f_{IN} = 170 MHz		–145.6			–145.7		
		f_{IN} = 230 MHz		–145.2			–145.3		
SINAD(1)	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.4			73.6		dBFS
		f_{IN} = 20 MHz	TBD	73.3			73.5		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	73.3			73.5		
		f_{IN} = 70 MHz		72.9			73		
		f_{IN} = 100 MHz		72.8			72.8		
		f_{IN} = 170 MHz		71.4			71.4		
		f_{IN} = 230 MHz		70.9			70.6		
ENOB(1)	Effective number of bits	f_{IN} = 10 MHz		11.9			11.9		Bits
		f_{IN} = 20 MHz	TBD	11.9			11.9		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	11.9			11.9		
		f_{IN} = 70 MHz		11.8			11.8		
		f_{IN} = 100 MHz		11.8			11.8		
		f_{IN} = 170 MHz		11.6			11.6		
		f_{IN} = 230 MHz		11.5			11.4		

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(1) Reported from 1 MHz offset.

AC Performance: ADC3442 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3442 (f_S = 50 MSPS)						UNITS
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		90			89		dBc
		f_{IN} = 20 MHz	TBD	90			89		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	90			89		
		f_{IN} = 70 MHz		90			87		
		f_{IN} = 100 MHz		89			87		
		f_{IN} = 170 MHz		86			83		
		f_{IN} = 230 MHz		83			80		
HD2	Second harmonic distortion	f_{IN} = 10 MHz		100			94		dBc
		f_{IN} = 20 MHz	TBD	97			93		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	97			93		
		f_{IN} = 70 MHz		92			89		
		f_{IN} = 100 MHz		92			88		
		f_{IN} = 170 MHz		88			86		
		f_{IN} = 230 MHz		84			80		
HD3	Third harmonic distortion	f_{IN} = 10 MHz		90			89		dBc
		f_{IN} = 20 MHz	TBD	90			89		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	90			89		
		f_{IN} = 70 MHz		90			87		
		f_{IN} = 100 MHz		89			87		
		f_{IN} = 170 MHz		86			83		
		f_{IN} = 230 MHz		83			80		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		100			97		dBc
		f_{IN} = 20 MHz	TBD	100			96		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	100			96		
		f_{IN} = 70 MHz		97			94		
		f_{IN} = 100 MHz		96			94		
		f_{IN} = 170 MHz		96			92		
		f_{IN} = 230 MHz		95			92		
THD	Total harmonic distortion	f_{IN} = 10 MHz		90			88		dBc
		f_{IN} = 20 MHz	TBD	90			88		
		f_{IN} = 20 MHz, T_A = 25°C	TBD	90			88		
		f_{IN} = 70 MHz		88			85		
		f_{IN} = 100 MHz		88			85		
		f_{IN} = 170 MHz		85			82		
		f_{IN} = 230 MHz		81			78		
IMD3	Third-tone intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		93			93		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		91			89		

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7.11 AC Performance: ADC3443

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3443 (f_S = 80 MSPS) DITHER ON MIN	DITHER ON TYP	DITHER ON MAX	DITHER OFF MIN	DITHER OFF TYP	DITHER OFF MAX	UNITS
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio (from 1-MHz offset)	f_{IN} = 10 MHz		73.1			73.4		dBFS
		f_{IN} = 70 MHz	TBD	72.3			72.6		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.3			72.6		
		f_{IN} = 100 MHz		72.2			72.4		
		f_{IN} = 170 MHz		71.4			71.7		
		f_{IN} = 230 MHz		70.7			71		
	Signal-to-noise ratio (full Nyquist band)	f_{IN} = 10 MHz		72.4			72.7		
		f_{IN} = 70 MHz		71.7			72		
		f_{IN} = 70 MHz, T_A = 25°C		71.7			72		
		f_{IN} = 100 MHz		71.6			71.8		
		f_{IN} = 170 MHz		70.8			71.1		
		f_{IN} = 230 MHz		70.2			70.5		
NSD(1)	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–149.1			–149.4		dBFS/Hz
		f_{IN} = 70 MHz	TBD	–148.3			–148.6		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	–148.3			–148.6		
		f_{IN} = 100 MHz		–148.2			–148.4		
		f_{IN} = 170 MHz		–147.4			–147.7		
		f_{IN} = 230 MHz		–146.7			–147		
SINAD(1)	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.1			73.3		dBFS
		f_{IN} = 70 MHz	TBD	72.2			72.4		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.2			72.4		
		f_{IN} = 100 MHz		72.1			72.2		
		f_{IN} = 170 MHz		71.3			71.4		
		f_{IN} = 230 MHz		70.5			70.5		
ENOB(1)	Effective number of bits	f_{IN} = 10 MHz		11.9			11.9		Bits
		f_{IN} = 70 MHz	TBD	11.7			11.7		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	11.7			11.7		
		f_{IN} = 100 MHz		11.7			11.7		
		f_{IN} = 170 MHz		11.6			11.6		
		f_{IN} = 230 MHz		11.4			11.4		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		93			90		dBc
		f_{IN} = 70 MHz	TBD	90			87		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	90			87		
		f_{IN} = 100 MHz		89			86		
		f_{IN} = 170 MHz		87			83		
		f_{IN} = 230 MHz		83			81		

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(1) Reported from 1 MHz offset.

AC Performance: ADC3443 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3443 (f_S = 80 MSPS)						UNITS
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second harmonic distortion	f_{IN} = 10 MHz		101			95		dBc
		f_{IN} = 70 MHz	TBD	97			92		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	97			92		
		f_{IN} = 100 MHz		93			89		
		f_{IN} = 170 MHz		88			85		
		f_{IN} = 230 MHz		83			81		
HD3	Third harmonic distortion	f_{IN} = 10 MHz		93			90		dBc
		f_{IN} = 70 MHz	TBD	90			87		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	90			87		
		f_{IN} = 100 MHz		89			86		
		f_{IN} = 170 MHz		87			83		
		f_{IN} = 230 MHz		86			81		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		99			95		dBc
		f_{IN} = 70 MHz	TBD	97			94		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	97			94		
		f_{IN} = 100 MHz		96			94		
		f_{IN} = 170 MHz		96			94		
		f_{IN} = 230 MHz		96			93		
THD	Total harmonic distortion	f_{IN} = 10 MHz		93			89		dBc
		f_{IN} = 70 MHz	TBD	90			86		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	90			86		
		f_{IN} = 100 MHz		88			85		
		f_{IN} = 170 MHz		85			82		
		f_{IN} = 230 MHz		82			79		
IMD3	Third-tone intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		95			95		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		89			88		

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7.12 AC Performance: ADC3444

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3444 (f_S = 125 MSPS)						UNITS
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio (from 1-MHz offset)	f_{IN} = 10 MHz		72.7			73.1		dBFS
		f_{IN} = 70 MHz	TBD	72.4			72.7		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.4			72.7		
		f_{IN} = 100 MHz		72.1			72.4		
		f_{IN} = 170 MHz		71.3			71.9		
		f_{IN} = 230 MHz		70.8			71.2		
	Signal-to-noise ratio (full Nyquist band)	f_{IN} = 10 MHz		72.3			72.7		
		f_{IN} = 70 MHz		72			72.3		
		f_{IN} = 70 MHz, T_A = 25°C		72			72.3		
		f_{IN} = 100 MHz		71.8			72.1		
		f_{IN} = 170 MHz		71			71.6		
		f_{IN} = 230 MHz		70.5			70.9		
NSD	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–150.7			–151.1		dBFS/Hz
		f_{IN} = 70 MHz	TBD	–150.4			–150.7		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	–150.4			–150.7		
		f_{IN} = 100 MHz		–150.1			–150.4		
		f_{IN} = 170 MHz		–149.3			–149.9		
		f_{IN} = 230 MHz		–148.8			–149.2		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		72.7			73		dBFS
		f_{IN} = 70 MHz	TBD	72.3			72.5		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.3			72.5		
		f_{IN} = 100 MHz		71.9			72.1		
		f_{IN} = 170 MHz		71.1			71.4		
		f_{IN} = 230 MHz		70.4			70.5		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.8			11.8		Bits
		f_{IN} = 70 MHz	TBD	11.7			11.7		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	11.7			11.7		
		f_{IN} = 100 MHz		11.6			11.7		
		f_{IN} = 170 MHz		11.5			11.6		
		f_{IN} = 230 MHz		11.4			11.4		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		93			89		dBc
		f_{IN} = 70 MHz	TBD	87			85		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	87			85		
		f_{IN} = 100 MHz		86			84		
		f_{IN} = 170 MHz		84			81		
		f_{IN} = 230 MHz		82			80		
HD2	Second harmonic distortion	f_{IN} = 10 MHz		100			94		dBc
		f_{IN} = 70 MHz	TBD	96			91		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	96			91		
		f_{IN} = 100 MHz		91			87		
		f_{IN} = 170 MHz		87			85		
		f_{IN} = 230 MHz		83			80		

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AC Performance: ADC3444 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC3444 (f_S = 125 MSPS)						UNITS
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
HD3	Third harmonic distortion	f_{IN} = 10 MHz		93			89		dBc
		f_{IN} = 70 MHz	TBD	87			85		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	87			85		
		f_{IN} = 100 MHz		86			84		
		f_{IN} = 170 MHz		84			81		
		f_{IN} = 230 MHz		82			80		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		98			94		dBc
		f_{IN} = 70 MHz	TBD	97			93		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	97			93		
		f_{IN} = 100 MHz		96			93		
		f_{IN} = 170 MHz		96			92		
		f_{IN} = 230 MHz		96			92		
THD	Total harmonic distortion	f_{IN} = 10 MHz		92			88		dBc
		f_{IN} = 70 MHz	TBD	87			85		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	87			85		
		f_{IN} = 100 MHz		85			83		
		f_{IN} = 170 MHz		83			80		
		f_{IN} = 230 MHz		80			78		
IMD3	Third-tone intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		95			95		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		87			86		

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7.13 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, PDN)							
V_{IH}	High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V_{IL}	Low-level input voltage					0.4	V
I_{IH}	High-level input current	RESET, SDATA, SCLK, PDN	V_{HIGH} = 1.8 V		10		µA
		SEN(1)	V_{HIGH} = 1.8 V		0		µA
I_{IL}	Low-level input current	RESET, SDATA, SCLK, PDN	V_{LOW} = 0 V		0		µA
		SEN	V_{LOW} = 0 V		10		µA
DIGITAL OUTPUTS, CMOS INTERFACE (SDOUT)							
V_{OH}	High-level output voltage			DVDD – 0.1	DVDD		V
V_{OL}	Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS, LVDS INTERFACE							
V_{ODH}	High-level output differential voltage		With an external 100-Ω termination	TBD	350	TBD	mV
V_{ODL}	Low-level output differential voltage		With an external 100-Ω termination	TBD	–350	TBD	mV
V_{OCM}	Output common-mode voltage				1.05		V

(1) SEN has an internal 150-kΩ pull-up resistor to AVDD. Because the pull-up resistor is weak, SEN can also be driven by 1.8-V or 3.3-V CMOS buffers.

7.14 Timing Requirements: General

Typical values are at 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C.

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
t_A	Aperture delay		1.24	1.44	1.64	ns
	Aperture delay matching	Between two channels of the same device		±70		ps
	Variation of aperture delay	Between two devices at the same temperature and supply voltage.		±150		ps
t_J	Aperture jitter			130		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		35	TBD	µs
		Time to valid data after coming out of GLOBAL power-down mode (in this mode, both channels power-down)		85	TBD	µs
	ADC latency(1)	Default latency after reset		TBD		Clock cycles
t_{SU_SYSREF}		Setup time for SYSREF Referenced to input clock rising edge	1000			ps
t_{H_SYSREF}		Hold time for SYSREF Referenced to input clock rising edge	100			ps

(1) Overall latency = ADC latency + t_{PDI}.

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7.15 Timing Requirements: LVDS Output(1)

Typical values are at 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C.

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SU}	Data setup time	Data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM)(2)	TBD	0.42		ns
t_{HO}	Data hold time	Zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid(2)	TBD	0.47		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock (CLKOUTP – CLKOUTM) rising edge cross-over	TBD	TBD	TBD	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock (CLKOUTP – CLKOUTM)		49%		
t_{FALL}, t_{RISE}	Data fall time, Data rise time	Rise time measured from –100 mV to 100 mV *10 MSPS ≤ Sampling frequency ≤ 125 MSPS*		0.11		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100 mV to 100 mV *10 MSPS ≤ Sampling frequency ≤ 125 MSPS*		0.11		ns

(1) Measurements are done with a transmission line of a 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(2) Data valid refers to a logic high of 100 mV and a logic low of –100 mV.

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Table 1. LVDS Timings at Lower Sampling Frequencies: 7x Serialization

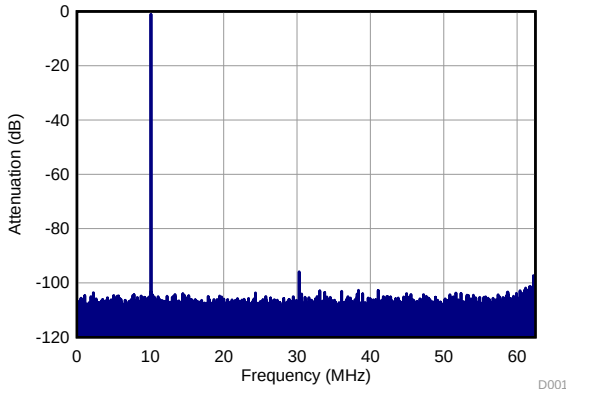
SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns) t_{SU}			HOLD TIME (ns) t_{HO}			CLOCK PROPAGATION DELAY (ns) t_{PDI}		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
25	TBD	2.6		TBD	2.6		TBD	TBD	TBD
40	TBD	1.6		TBD	1.7		TBD	TBD	TBD
50	TBD	1.32		TBD	1.4		TBD	TBD	TBD
60	TBD	1.04		TBD	1.09		TBD	TBD	TBD
80	TBD	0.75		TBD	0.81		TBD	TBD	TBD
100	TBD	0.57		TBD	0.62		TBD	TBD	TBD

Table 2. LVDS Timings at Lower Sampling Frequencies: 14x Serialization

SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns) t_{SU}			HOLD TIME (ns) t_{HO}			CLOCK PROPAGATION DELAY (ns) t_{PDI}		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
25	TBD	1.24		TBD	1.34		TBD	TBD	TBD
40	TBD	0.72		TBD	0.82		TBD	TBD	TBD
50	TBD	0.55		TBD	0.64		TBD	TBD	TBD
60	TBD	0.41		TBD	0.51		TBD	TBD	TBD
80	TBD	0.24		TBD	0.38		TBD	TBD	TBD

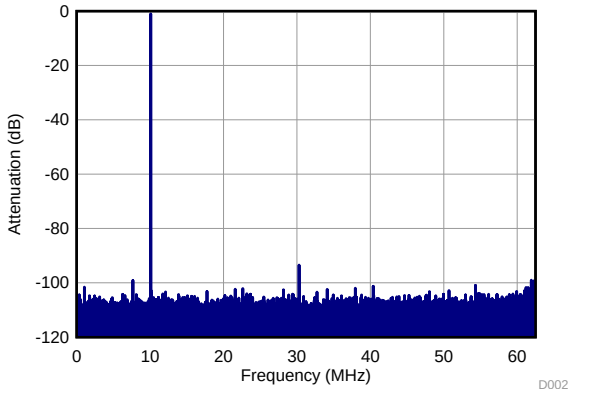
7.16 Typical Characteristics

Typical values are at T_A= 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with 1-MHz offset from dc when chopper disabled, and from f_S / 2 when chopper enabled, unless otherwise noted.



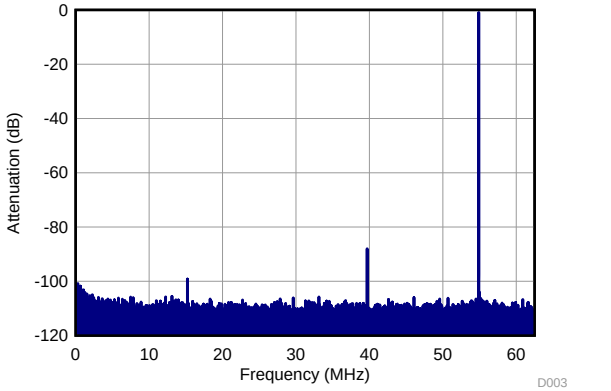
f_S = 125 MSPS SNR = 72.7 dBFS Chopper enabled
f_{IN} = 10 MHz SFDR = 94 dBc

Figure 1. FFT with Dither On



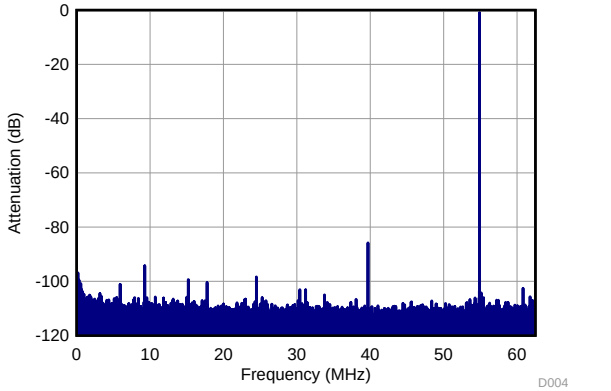
f_S = 125 MSPS SNR = 73.1 dBFS Chopper enabled
f_{IN} = 10 MHz SFDR = 86 dBc

Figure 2. FFT with Dither Off



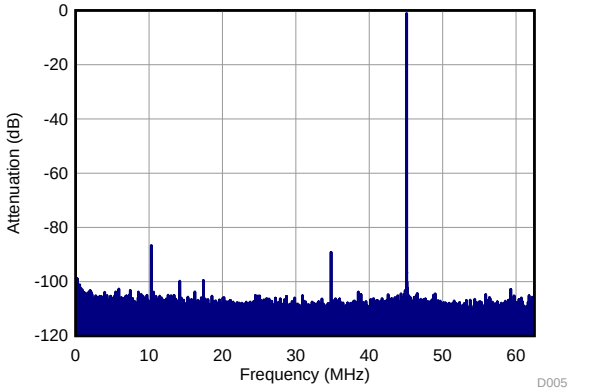
f_S = 125 MSPS SNR = 72.4 dBFS
f_{IN} = 70 MHz SFDR = 87 dBc

Figure 3. FFT with Dither On



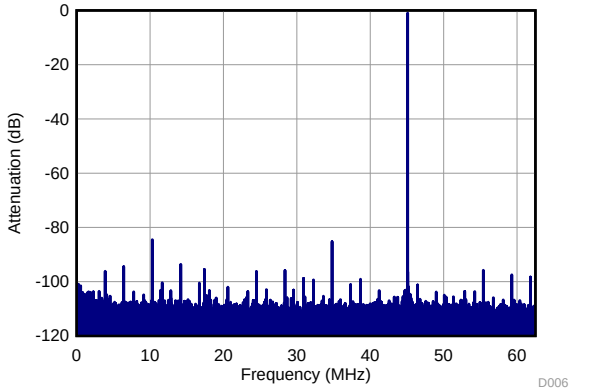
f_S = 125 MSPS SNR = 72.7 dBFS
f_{IN} = 70 MHz SFDR = 85 dBc

Figure 4. FFT with Dither Off



f_S = 125 MSPS SNR = 71.3 dBFS
f_{IN} = 170 MHz SFDR = 85 dBc

Figure 5. FFT with Dither On



f_S = 125 MSPS SNR = 71.9 dBFS
f_{IN} = 170 MHz SFDR = 84 dBc

Figure 6. FFT with Dither Off

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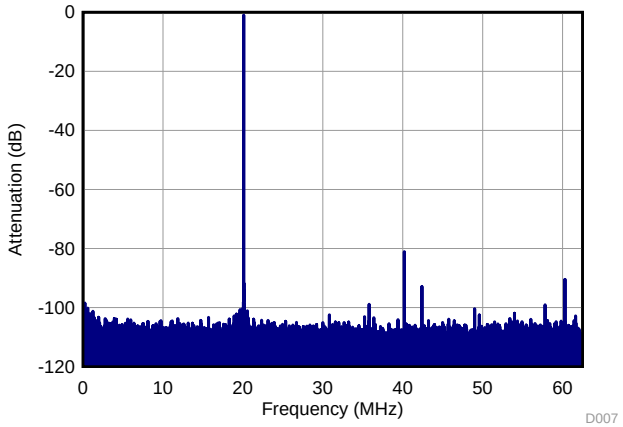
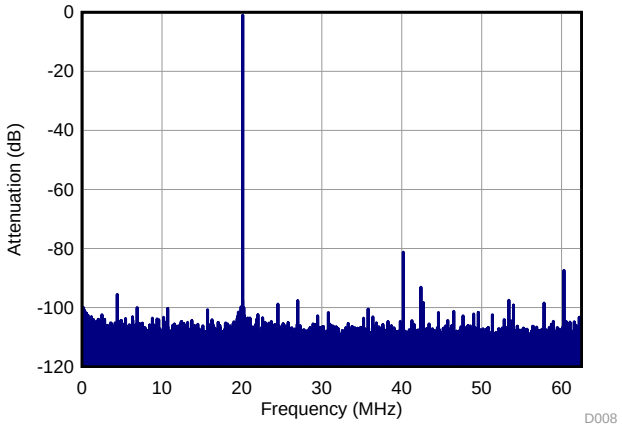
Typical Characteristics (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with 1-MHz offset from dc when chopper disabled, and from f_S / 2 when chopper enabled, unless otherwise noted.



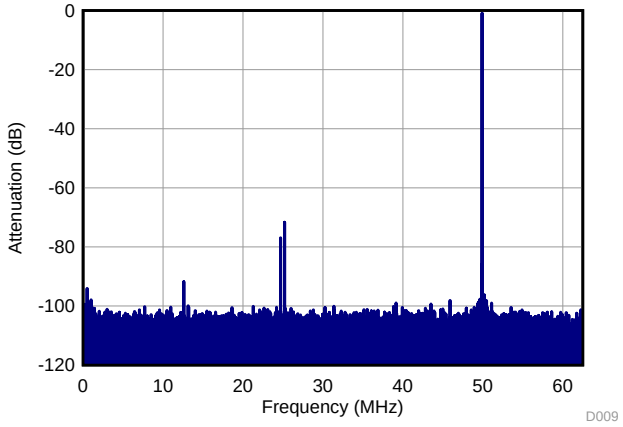
f_S = 125 MSPS SNR = 70.4 dBFS
f_{IN} = 270 MHz SFDR = 80 dBc

Figure 7. FFT with Dither On



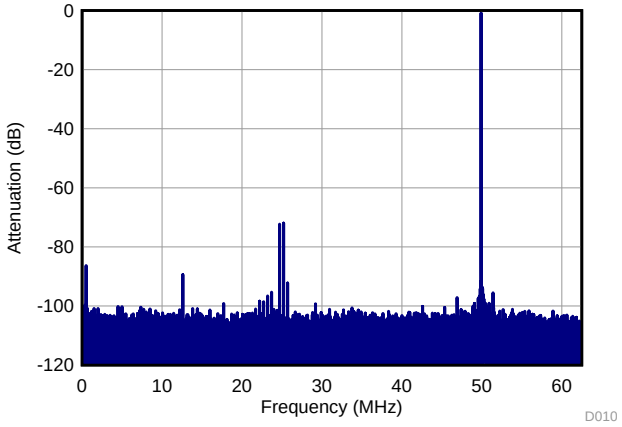
f_S = 125 MSPS SNR = 70.6 dBFS
f_{IN} = 270 MHz SFDR = 80 dBc

Figure 8. FFT with Dither Off



f_S = 125 MSPS SNR = 68.1 dBFS
f_{IN} = 450 MHz SFDR = 71 dBc

Figure 9. FFT with Dither On



f_S = 125 MSPS SNR = 68.3 dBFS
f_{IN} = 450 MHz SFDR = 71 dBc

Figure 10. FFT with Dither Off

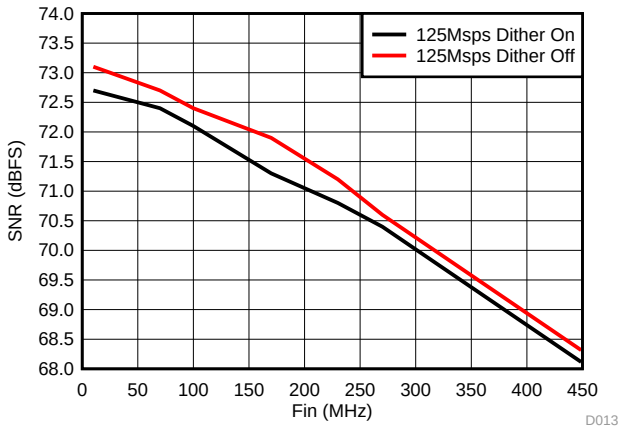


Figure 11. SNR vs Input Frequencies

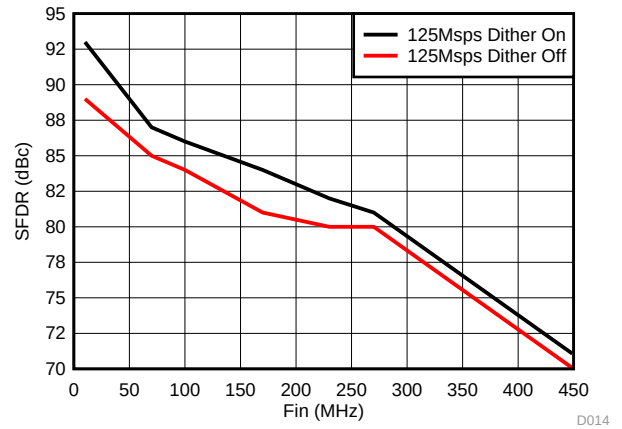


Figure 12. SFDR vs Input Frequencies

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Typical Characteristics (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with 1-MHz offset from dc when chopper disabled, and from f_S / 2 when chopper enabled, unless otherwise noted.

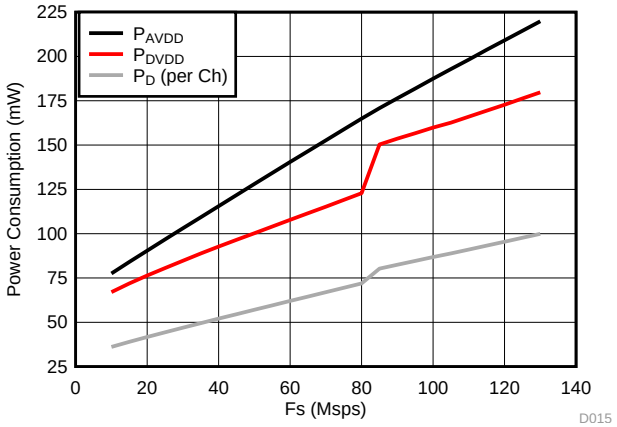
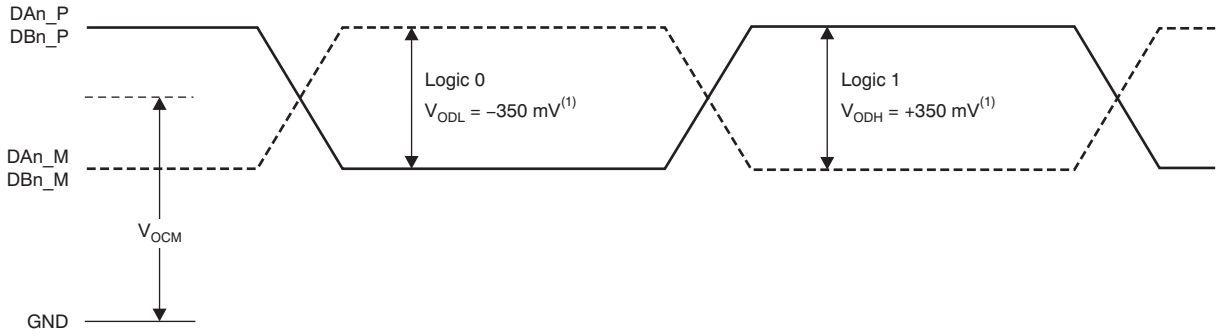


Figure 13. Power Consumption vs Sampling Rate

8 Parameter Measurement Information

8.1 Timing Diagrams



(1) With an external 100-Ω termination.

Figure 14. Serial LVDS Output Voltage Levels

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Timing Diagrams (continued)

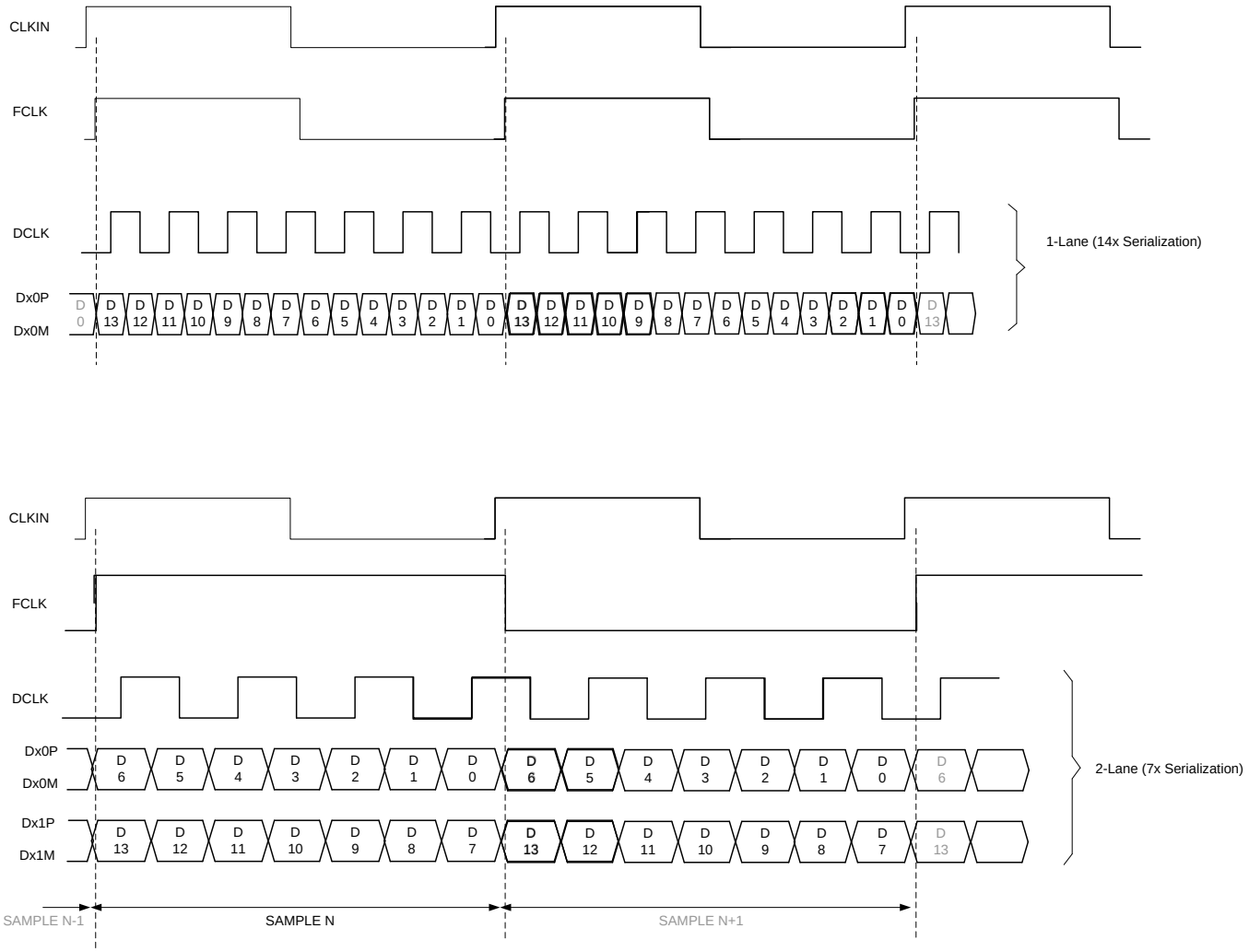

Figure 15. Output Timing Diagram

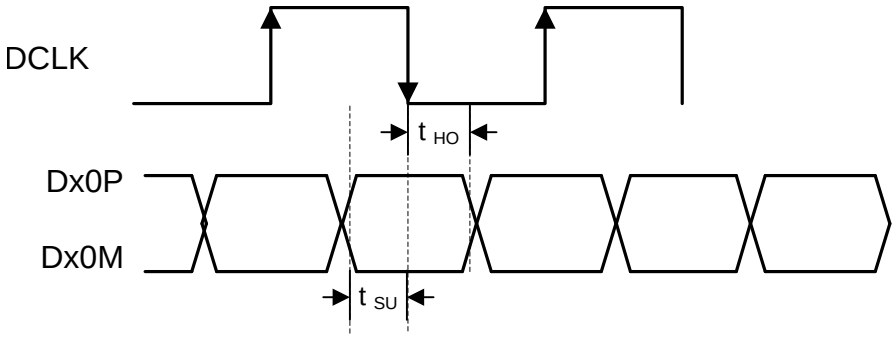

Figure 16. Setup and Hold Time

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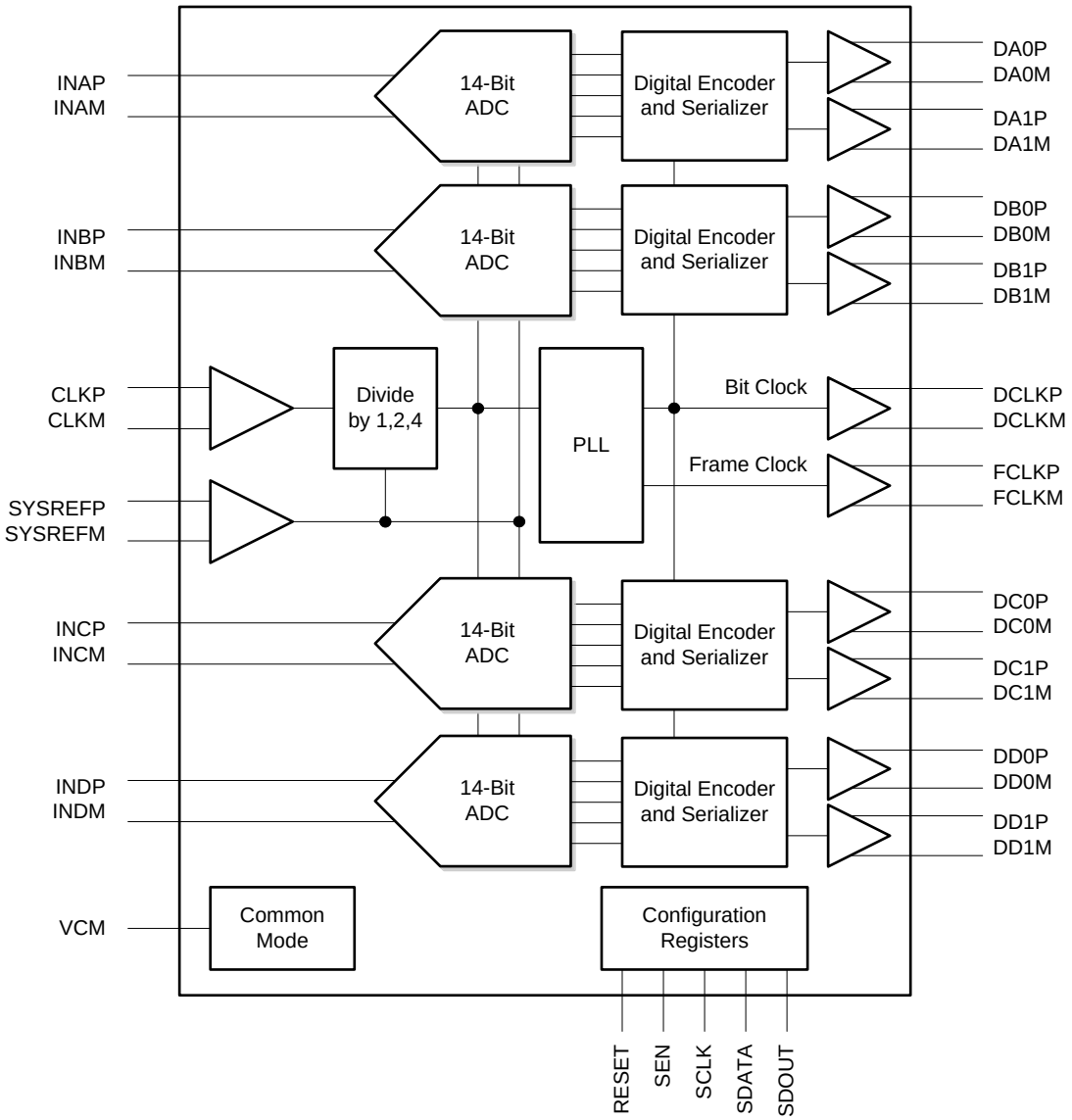
9 Detailed Description

9.1 Overview

The ADC344x are a high-linearity, ultra-low power, quad-channel, 14-bit, 25-MSPS to 125-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization. The ADC344x family supports serial LVDS interface in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 14-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

9.2 Functional Block Diagram



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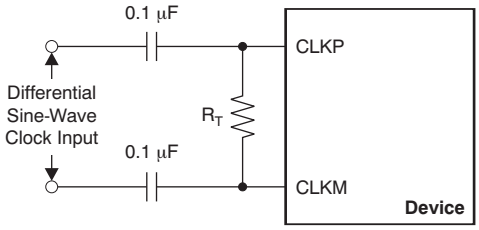
9.3 Feature Description

9.3.1 Analog Inputs

The ADC344x analog signal inputs are designed to be driven differentially. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 540 MHz (50-Ω source driving 50-Ω termination between INP and INM).

9.3.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95 V using internal 5-kΩ resistors. The self-bias clock inputs of the ADC344x can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 17, Figure 18, and Figure 19. See Figure 20 for details regarding the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

Figure 17. Differential Sine-Wave Clock Driving Circuit

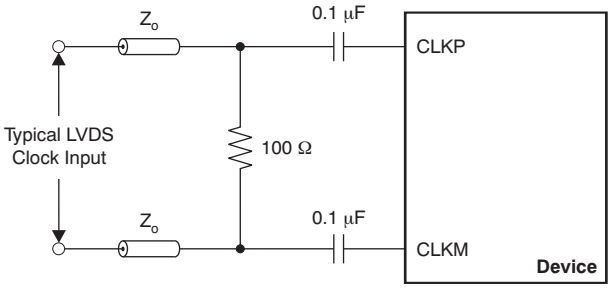


Figure 18. LVDS Clock Driving Circuit

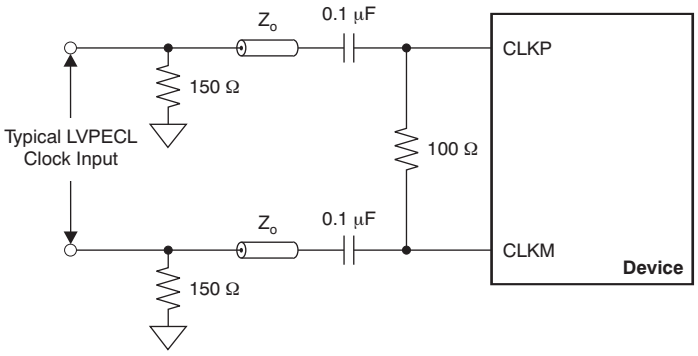
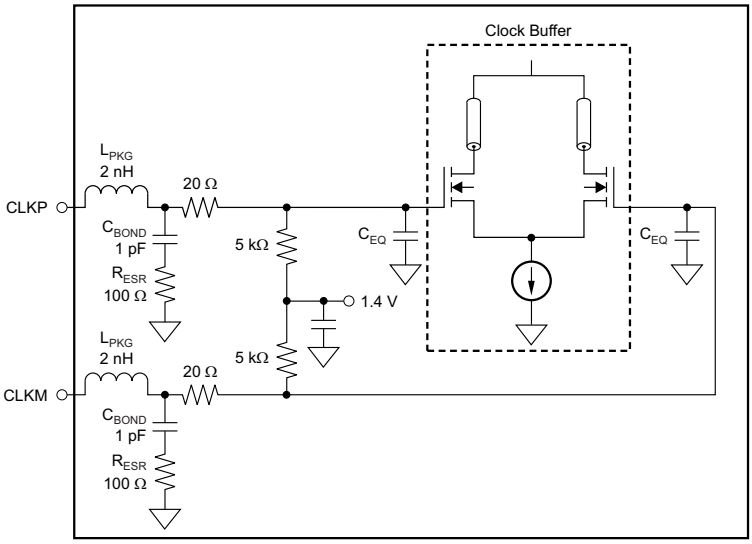


Figure 19. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 20. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 21. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

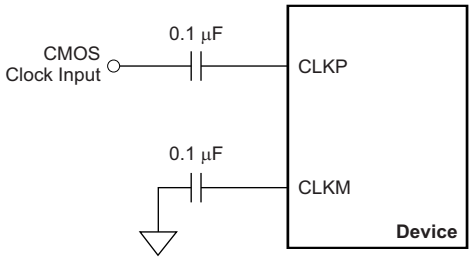


Figure 21. Single-Ended Clock Driving Circuit

9.3.2.1 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors, as shown in Equation 1. Quantization noise (typically 86 dB for a 14-bit ADC) and thermal noise limit SNR at low input frequencies while the clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{-\frac{SNR_{Quantizatoin\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation resulting from sample clock jitter can be calculated with Equation 2.

$$SNR_{Jitter}[dBc] = -20 \cdot \log(2\pi \cdot f_{in} \cdot T_{Jitter}) \quad (2)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (130 fs for the device) which is set by the noise of the clock input buffer and the external clock. T_{Jitter} can be calculated with Equation 3.

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (3)$$

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External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter. The devices have a typical thermal noise of 72.7 dBFS and internal aperture jitter of 130 fs. The SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 22.

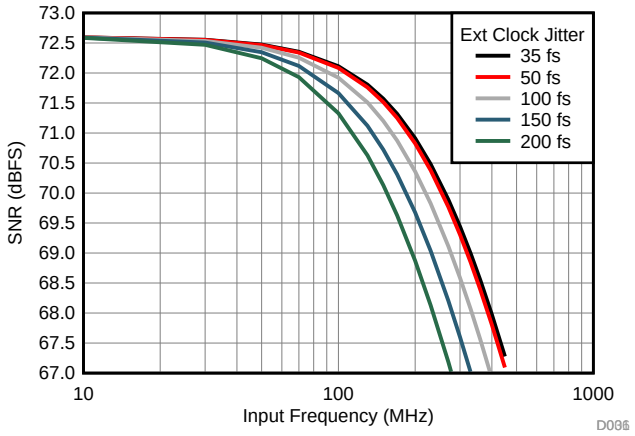

Figure 22. SNR vs Frequency for Different Clock Jitter

9.3.3 Digital Output Interface

The devices offer two different output format options, thus making interfacing to a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC) easy. Each option can be easily programmed using the serial interface, as shown in Table 3. The output interface options are:

- One-wire, 1x frame clock, 14x serialization with the DDR bit clock and
- Two-wire, 1x frame clock, 7x serialization with the DDR bit clock.

Table 3. Interface Rates

INTERFACE OPTIONS	SERIALIZATION	MAXIMUM RECOMMENDED SAMPLING FREQUENCY (MSPS)	BIT CLOCK FREQUENCY (MHz)	FRAME CLOCK FREQUENCY (MHz)	SERIAL DATA RATE PER WIRE (Mbps)
One-wire	14x	80	560	80	1120
Two-wire	7x	125	437.5	62.5	875

9.3.3.1 One-Wire Interface: 14x Serialization

In this interface option, the device outputs the data of each ADC serially on a single LVDS pair (one-wire). The data are available at the rising and falling edges of the bit clock (DDR bit clock). The ADC outputs a new word at the rising edge of every frame clock, starting with the MSB. The data rate is 14x sample frequency (14x serialization).

9.3.3.2 Two-Wire Interface: 7x Serialization

The two-wire interface is recommended for sampling frequencies above 65 MSPS. The output data rate is 6x sample frequency because six data bits are output every clock cycle on each differential pair. Each ADC sample is sent over the two wires with the seven MSBs on Dx1P, Dx1M and the seven LSBs on Dx0P, Dx0M, as shown in Figure 23.

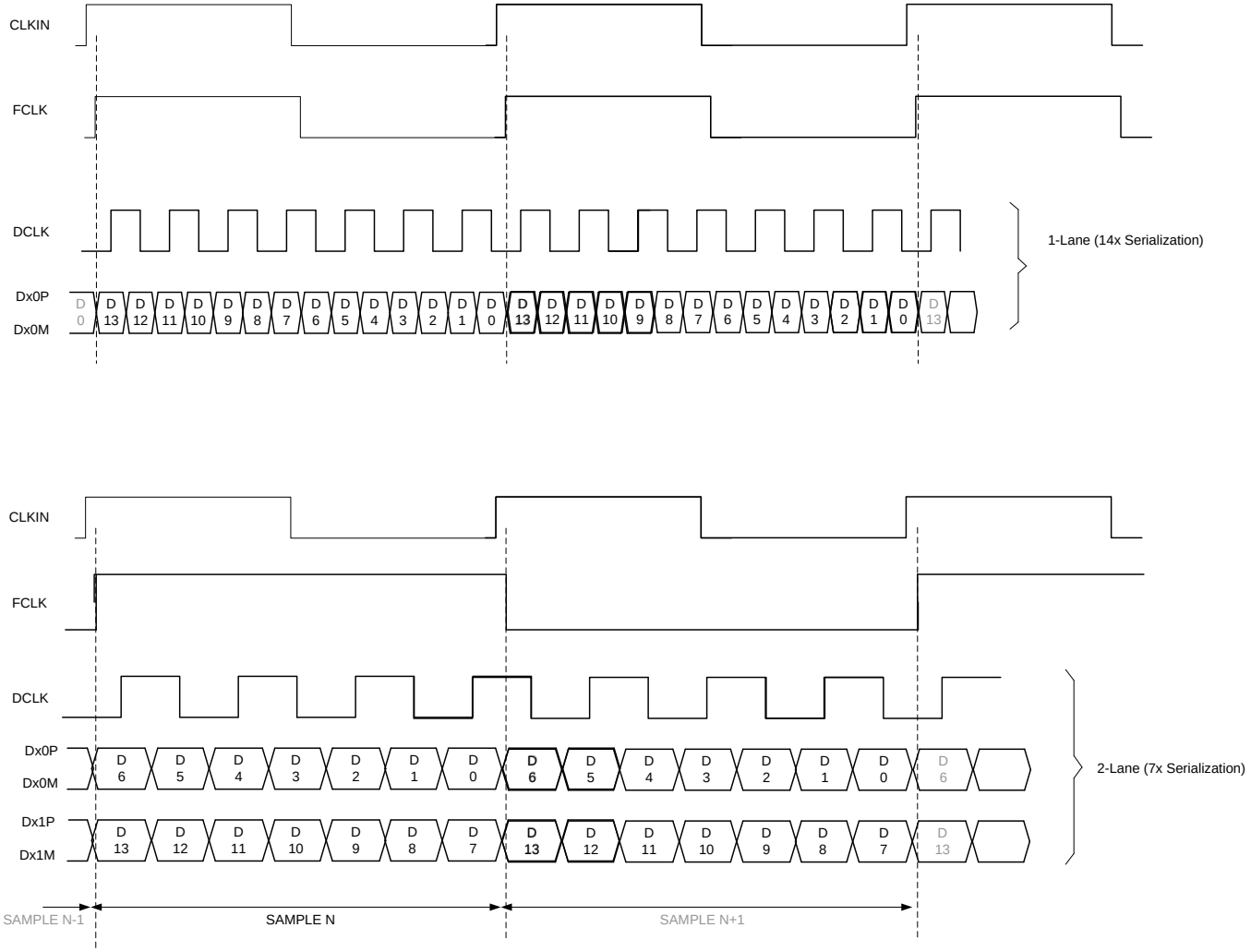

Figure 23. Output Timing Diagram

9.4 Device Functional Modes

9.4.1 Input Clock Divider

The devices are equipped with an internal divider on the clock input. The clock divider allows operation with a faster input clock, thus simplifying the system clock distribution design. The clock divider can be bypassed for operation with a 125-MHz clock while the divide-by-2 option supports a maximum input clock of 250 MHz and the divide-by-4 option provides a maximum input clock frequency of 500 MHz.

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Device Functional Modes (continued)

9.4.2 Chopper Functionality

The devices are equipped with an internal chopper front-end. Enabling the chopper function swaps the ADC noise spectrum by shifting the 1/f noise from dc to f_S / 2. Figure 24 shows the noise spectrum with the chopper off and Figure 25 shows the noise spectrum with the chopper on. This function is especially useful in applications requiring good ac performance at low input frequencies or in dc-coupled applications. The chopper can be enabled via SPI register writes and is recommended for input frequencies below 30 MHz. The chopper function creates a spur at f_S / 2 that must be filtered out digitally.

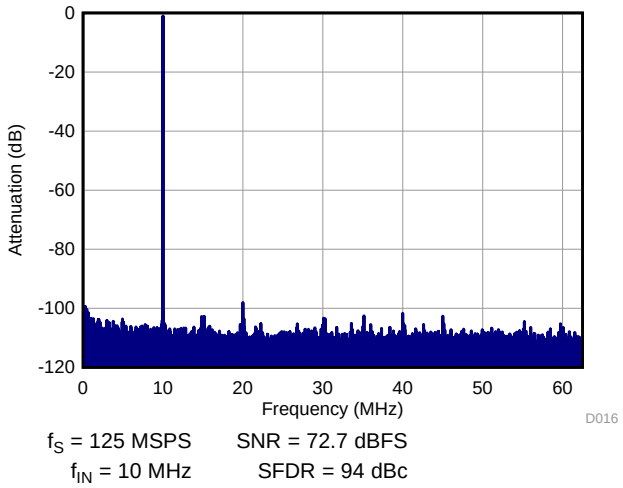

Figure 24. Chopper Off

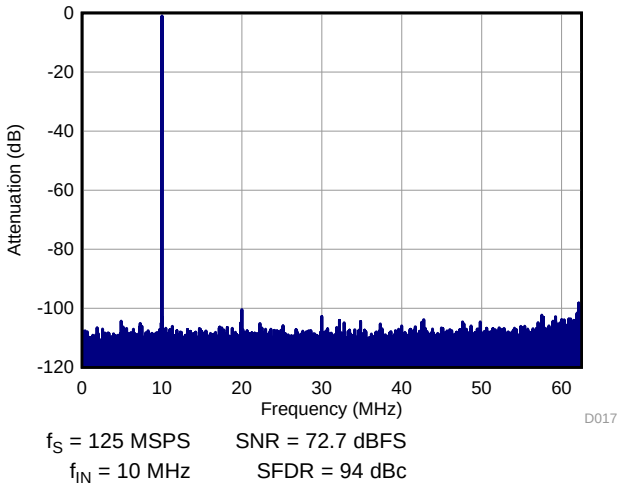

Figure 25. Chopper On

9.4.3 Power-Down Control

The power-down functions of the ADC344x can be controlled either through the parallel control pin (PDN) or through an SPI register setting (see Figure 43, register 15h). The PDN pin can also be configured via SPI to a global power-down or standby functionality, as shown in Table 4.

Table 4. Power-Down Modes

FUNCTION	POWER CONSUMPTION (mW)	WAKE-UP TIME (µs)
Global power-down	5	85
Standby	45	35

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9.4.4 Internal Dither Algorithm

The ADC344x use an internal dither algorithm to achieve high SFDR and a clean spectrum. However, the dither algorithm marginally degrades SNR, creating a trade-off between SNR and SFDR. If desired, the dither algorithm can be turned off by using the DIS DITH CHx registers bits. Figure 26 and Figure 27 show the effect of using dither algorithms.

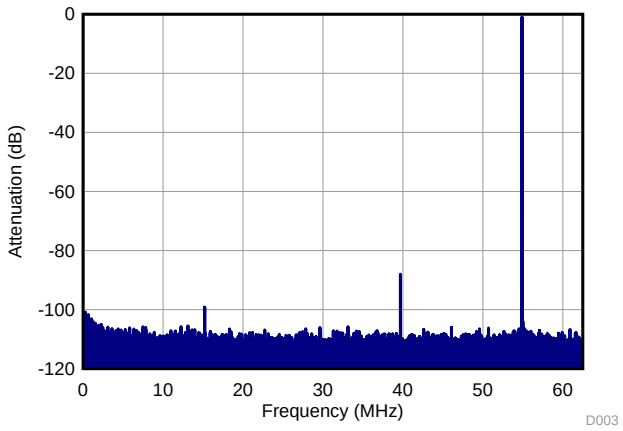

Figure 26. FFT with Dither On

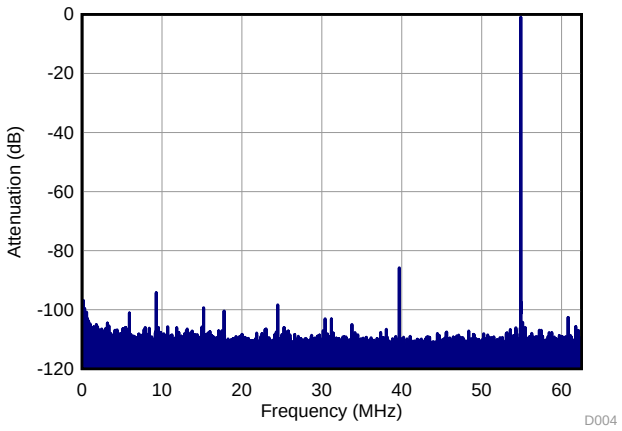

Figure 27. FFT with Dither Off

9.5 Programming

The ADC344x can be configured using a serial programming interface, as described in this section.

9.5.1 Serial Interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

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Programming (continued)

9.5.1.1 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin (of durations greater than 10 ns), as shown in Figure 28. If required, the serial interface registers can be cleared during operation either:

1. Through a hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.5.1.1.1 Serial Register Write

The device internal register can be programmed with these steps:

1. Drive the SEN pin low,
2. Set the R/W bit to 0 (bit A15 of the 16-bit address),
3. Set bit A14 in the address field to 1,
4. Initiate a serial interface cycle by specifying the address of the register (A13 to A0) whose content must be written, and
5. Write the 8-bit data that are latched in on the SCLK rising edge.

Figure 28 and Table 5 show the timing requirements for the serial register write operation.

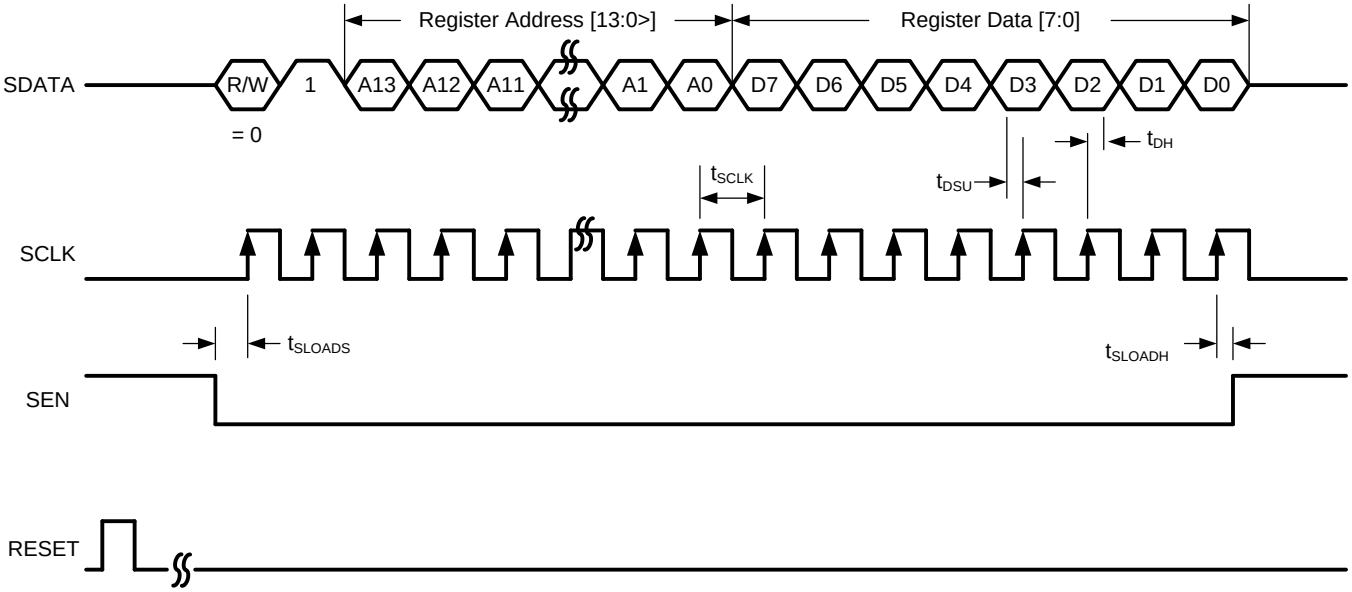

Figure 28. Serial Register Write Timing Diagram

Table 5. Serial Interface Timing(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, and AVDD = DVDD = 1.8 V, unless otherwise noted.

9.5.1.1.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low.
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Set bit A14 in the address field to 1.
4. Initiate a serial interface cycle specifying the address of the register (A13 to A0) whose content must be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK rising edge.
7. To enable register writes, reset the R/W register bit to 0.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 29 shows a timing diagram of the serial register read operation. Data appear on the SDOUT pin at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in Figure 30.

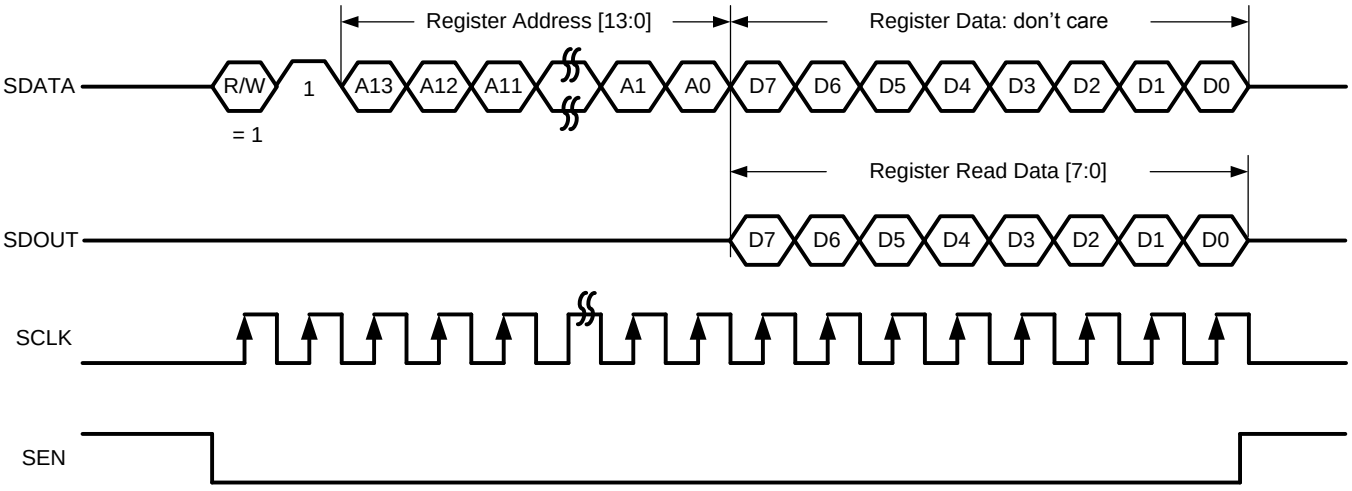

Figure 29. Serial Register Read Timing Diagram

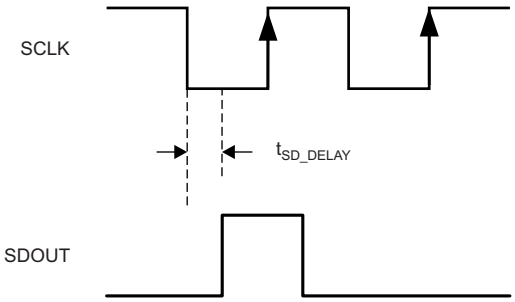

Figure 30. SDOUT Timing Diagram

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9.5.2 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in Figure 31 and Table 6.

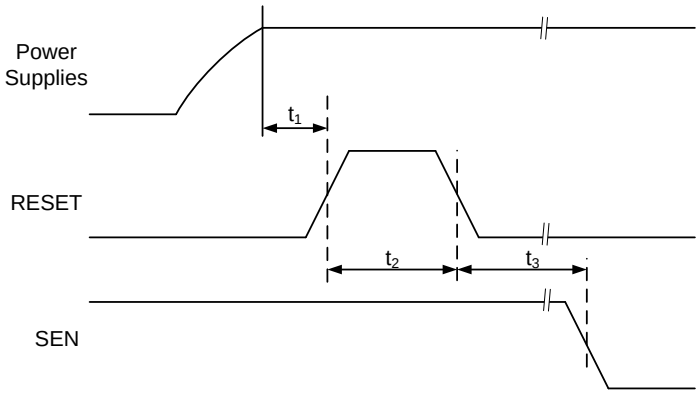

Figure 31. Initialization of Serial Registers after Power-Up

Table 6. Power-Up Timing

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power up to active high RESET pulse	1			ms
t_2	Reset pulse duration	Active high RESET pulse duration	10			ns
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

If required, the serial interface registers can be cleared during operation either:

1. Through hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

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9.6 Register Maps

Table 7. Register Map Summary

REGISTER ADDRESS	REGISTER DATA							
A[13:0] (Hex)	7	6	5	4	3	2	1	0
01	DIS DITH CHA		DIS DITH CHB		DIS DITH CHC		DIS DITH CHD	
03	0	0	0	0	0	0	0	ODD EVEN
04	0	0	0	0	0	0	0	FLIP BITS
05	0	0	0	0	0	0	0	1W-2W
06	0	0	0	0	0	0	TEST PATTERN EN	RESET
07	0	0	0	0	0	0	0	OVR ON LSB
09	0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
0A	0	0	0	0	CHA TEST PATTERN			
0B	CHB TEST PATTERN			0	0	0	0	0
0E	CUSTOM PATTERN[13:6]							
0F	CUSTOM PATTERN[5:0]						0	0
15	0	CHA PDN	CHB PDN	0	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN
25	LVDS SWING							
27	CLK DIV		0	0	0	0	0	0
122	0	0	0	0	0	0	DIS CHOP CHA	0
134	0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
139	0	0	0	0	SP1 CHA	0	0	0
222	0	0	0	0	0	0	DIS CHOP CHD	0
234	0	0	DIS DITH CHD	0	DIS DITH CHD	0	0	0
239	0	0	0	0	SP1 CHD	0	0	0
422	0	0	0	0	0	0	DIS CHOP CHB	0
434	0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0
439	0	0	0	0	SP1 CHB	0	0	0
522	0	0	0	0	0	0	DIS CHOP CHC	0
534	0	0	DIS DITH CHC	0	DIS DITH CHC	0	0	0
539	0	0	0	0	SP1 CHC	0	0	0

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9.6.1 Serial Register Description

Figure 32. Register 01h

7	6	5	4	3	2	1	0
DIS DITH CHA		DIS DITH CHB		DIS DITH CHC		DIS DITH CHD	

Table 8. Register 01h Description

Name	Description
Bits 7:6	**DIS DITH CHA**
	These bits enable or disable the on-chip dither. Control this bit with bits 5 and 3 of register 134h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bits 5:4	**DIS DITH CHB**
	These bits enable or disable the on-chip dither. Control this bit with bits 5 and 3 of register 434h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bits 3:2	**DIS DITH CHC**
	These bits enable or disable the on-chip dither. Control this bit with bits 5 and 3 of register 534h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bits 1:0	**DIS DITH CHD**
	These bits enable or disable the on-chip dither. Control this bit with bits 5 and 3 of register 234h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.

Figure 33. Register 03h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ODD EVEN

Table 9. Register 03h Description

Name	Description
Bits 7:6	**Must write 0**
Bit 0	**ODD EVEN:** Select bit sequence on output lanes. (In 2-wire mode only)
	0 = Bits D0, D1, and D2 appear on lane 0; bits D7, D8, D9 appear on lane 1. 1 = Bits D0, D2, and D4 appear on lane 0; bits D1, D3, and D5 appear on lane 1.

Figure 34. Register 04h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FLIP BITS

Table 10. Register 04h Description

Name	Description
Bits 7:6	**Must write 0**
Bit 0	**FLIP BITS: Flip bits on the output lanes**
	0 = LSB comes out first, sequence is D0, D1, D2, and so forth 1 = MSB comes out first, sequence is D13, D12, D11, and so forth

Figure 35. Register 05h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1W-2W

Table 11. Register 05h Description

Name	Description
Bits 7:6	**Must write 0**
Bit 0	**1W-2W**:
	This bit transmits output data on either one or two wires. 0 = Output data are transmitted on two wires (Dx0P, Dx0M and Dx1P, Dx1M) 1 = Output data are transmitted on one wire (Dx0P, Dx0M). In this mode, the recommended f_S is less than 62.5 MSPS.

Figure 36. Register 06h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TEST PATTERN EN	RESET

Table 12. Register 06h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**TEST PATTERN EN: Enables test pattern selection for the digital outputs**
	0 = Normal output 1 = Test pattern output enabled
Bit 0	**RESET: Software reset applied**
	This bit resets all internal registers to the default values and self-clears to 0.

Figure 37. Register 07h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	OVR ON LSB

Table 13. Register 07h Description

Name	Description
Bits 7:6	**Must write 0**
Bit 0	**OVR ON LSB: OVR information on the LSB bits**
	0 = Output data bit 0 functions as the LSB of the 14-bit data 1 = Output data bit 0 carries the overrange (OVR) information.

Figure 38. Register 09h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ALIGN TEST PATTER	DATA FORMAT

Table 14. Register 09h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**ALIGN TEST PATTER**
	This bit aligns the test patterns across the outputs of both channels. 0 = Test patterns of both channels are free running 1 = Test patterns of both channels are aligned
Bit 0	**DATA FORMAT: Digital output data format**
	0 = Twos complement 1 = offset binary

PRODUCT PREVIEW

Figure 39. Register 0Ah

7	6	5	4	3	2	1	0
CHA TEST PATTERN				CHB TEST PATTERN			

Table 15. Register 0Ah Description

Name	Description
Bits 7:4	**CHA TEST PATTERN**
	These bits control test pattern for channel A after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383. 0110 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 1000 = Deskew pattern: data are 3AAAh. 1010 = PRBS pattern: data are a sequence of pseudo random numbers. 1011 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use
Bits 3:0	**CHB TEST PATTERN**
	These bits control test pattern for channel B after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383. 0110 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 1000 = Deskew pattern: data are 3AAAh. 1010 = PRBS pattern: data are a sequence of pseudo random numbers. 1011 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use

Figure 40. Register 0Bh

7	6	5	4	3	2	1	0
CHC TEST PATTERN				CHD TEST PATTERN			

Table 16. Register 0Bh Description

Name	Description
Bits 7: 4	**CHC TEST PATTERN**
	These bits control test pattern for channel C after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383. 0110 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 1000 = Deskew pattern: data are 3AAAh. 1010 = PRBS pattern: data are a sequence of pseudo random numbers. 1011 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use
Bits 3:0	**CHD TEST PATTERN**
	These bits control test pattern for channel D after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383. 0110 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 1000 = Deskew pattern: data are 3AAAh. 1010 = PRBS pattern: data are a sequence of pseudo random numbers. 1011 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use

Figure 41. Register 0Eh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[13:6]							

Table 17. Register 0Eh Description

Name	Description
Bits 7:0	**CUSTOM PATTERN[13:6]**
	These bits set the 14-bit custom pattern (bits 13:6) for all channels.

Figure 42. Register 0Fh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[5:0]						0	0

Table 18. Register 0Fh Description

Name	Description
Bits 7:2	**CUSTOM PATTERN[5:0]**
	These bits set the 14-bit custom pattern (bits 5:0) for all channels.
Bits 1:0	**Must write 0**

Figure 43. Register 15h

7	6	5	4	3	2	1	0
0	CHA PDN	CHB PDN	0	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN

Table 19. Register 15h Description

Name	Description
Bit 7	**Must write 0**
Bit 6	**CHA PDN**
	0 = Normal operation 1 = Power-down channel A
Bit 5	**CHB PDN**
	0 = Normal operation 1 = Power-down channel B
Bit 4	**Must write 0**
Bit 3	**STANDBY: ADCs of both channels enter standby**
	0 = Normal operation 1 = Standby
Bit 2	**GLOBAL PDN**
	0 = Normal operation 1 = Global power-down
Bit 1	**Must write 0**
Bit 0	**CONFIG PDN PIN:**
	This bit configures the PDN pin as either a global power-down or standby pin. 0 = Logic high voltage on PDN pin sends the device into global power-down 1 = Logic high voltage on PDN pin sends the device into standby

Figure 44. Register 25h

7	6	5	4	3	2	1	0
LVDS SWING							

Table 20. Register 25h Description

Name	Description
Bits 7:0	**LVDS SWING**
	These bits control the swing of the LVDS outputs (including the data output, bit clock, and frame clock).

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Figure 45. Register 27h

7	6	5	4	3	2	1	0
CLK DIV		0	0	0	0	0	0

Table 21. Register 27h Description

Name	Description
Bits 7:6	**CLK DIV: Internal clock divider for the input sampling clock**
	00 = Divide-by-1 01 = Divide-by-1 10 = Divide-by-2 11 = Divide-by-4
Bits 5:0	**Must write 0**

Figure 46. Register 122h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHA	0

Table 22. Register 122h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**DIS CHOP CHA: Disable chopper**
	Set this bit to shift 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
Bit 0	**Must write 0**

Figure 47. Register 134h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0

Table 23. Register 134h Description

Name	Description
Bits 7:6	**Must write 0**
Bit 5	**DIS DITH CHA**
	Set this bit with bits 7 and 6 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bit 4	**Must write 0**
Bit 3	**DIS DITH CHA**
	Set this bit with bits 7 and 6 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bits 2:0	**Must write 0**

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Figure 48. Register 139h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHA	0	0	0

Table 24. Register 139h Description

Name	Description
Bits 7:4	**Must write 0**
Bit D3	**SP1 CHA: Special mode for best performance on channel A**
	Always write 1 after reset.
Bits 2:0	**Must write 0**

Figure 49. Register 222h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHD	0

Table 25. Register 222h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**DIS CHOP CHD: Disable chopper**
	Set this bit to shift 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
Bit 0	**Must write 0**

Figure 50. Register 234h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHD	0	DIS DITH CHD	0	0	0

Table 26. Register 234h Description

Name	Description
Bits 7:6	**Must write 0**
Bit 5	**DIS DITH CHD**
	Set this bit with bits 1 and 0 of register 01h. 00 = Default 11 = Dither is disabled for channel D. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bit 4	**Must write 0**
Bit 3	**DIS DITH CHD**
	Set this bit with bits 1 and 0 of register 01h. 00 = Default 11 = Dither is disabled for channel D. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bits 2:0	**Must write 0**

Figure 51. Register 239h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHD	0	0	0

Table 27. Register 239h Description

Name	Description
Bits 7:4	**Must write 0**
Bit D3	**SP1 CHD: Special mode for best performance on channel D**
	Always write 1 after reset.
Bits 2:0	**Must write 0**

Figure 52. Register 422h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHB	0

Table 28. Register 422h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**DIS CHOP CHB: Disable chopper**
	Set this bit to shift 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
Bit 0	**Must write 0**

Figure 53. Register 434h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0

Table 29. Register 434h Description

Name	Description
Bits 7:6	**Must write 0**
Bit 5	**DIS DITH CHB**
	Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bit 4	**Must write 0**
Bit 3	**DIS DITH CHB**
	Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bits 2:0	**Must write 0**

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Figure 54. Register 439h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHB	0	0	0

Table 30. Register 439h Description

Name	Description
Bits 7:4	**Must write 0**
Bit D3	**SP1 CHB: Special mode for best performance on channel B**
	Always write 1 after reset.
Bits 2:0	**Must write 0**

Figure 55. Register 522h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHC	0

Table 31. Register 522h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**DIS CHOP CHC: Disable chopper**
	Set this bit to shift 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
Bit 0	**Must write 0**

Figure 56. Register 534h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHC	0	DIS DITH CHC	0	0	0

Table 32. Register 534h Description

Name	Description
Bits 7:6	**Must write 0**
Bit 5	**DIS DITH CHC**
	Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel C. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bit 4	**Must write 0**
Bit 3	**DIS DITH CHC**
	Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel C. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bits 2:0	**Must write 0**

Figure 57. Register 539h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHC	0	0	0

Table 33. Register 539h Description

Name	Description
Bits 7:4	**Must write 0**
Bit D3	**SP1 CHC: Special mode for best performance on channel C**
	Always write 1 after reset.
Bits 2:0	**Must write 0**

10 Applications and Implementation

10.1 Application Information

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 250 MHz to achieve good phase and amplitude balances at ADC inputs. While designing the dc driving circuits, the ADC input impedance must be considered. Figure 58 and Figure 59 show the impedance (Z_{in} = R_{in} || C_{in}) across the ADC input pins.

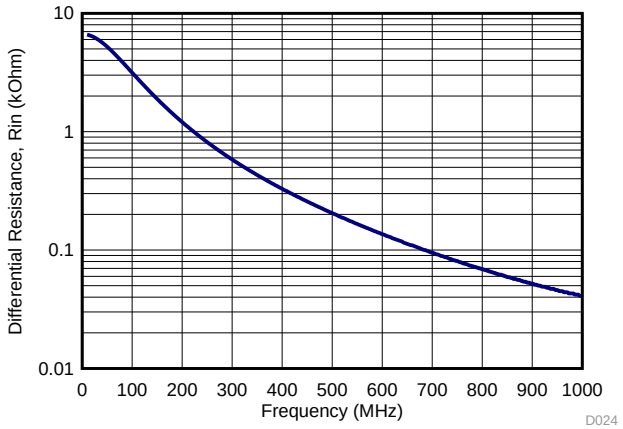

Figure 58. Differential Input Resistance, R_{IN}

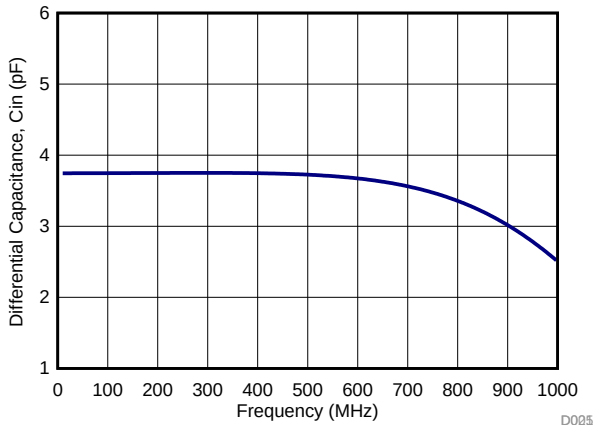

Figure 59. Differential Input Capacitance, C_{IN}

10.2 Typical Applications

10.2.1 Driving Circuit Design: Low Input Frequencies

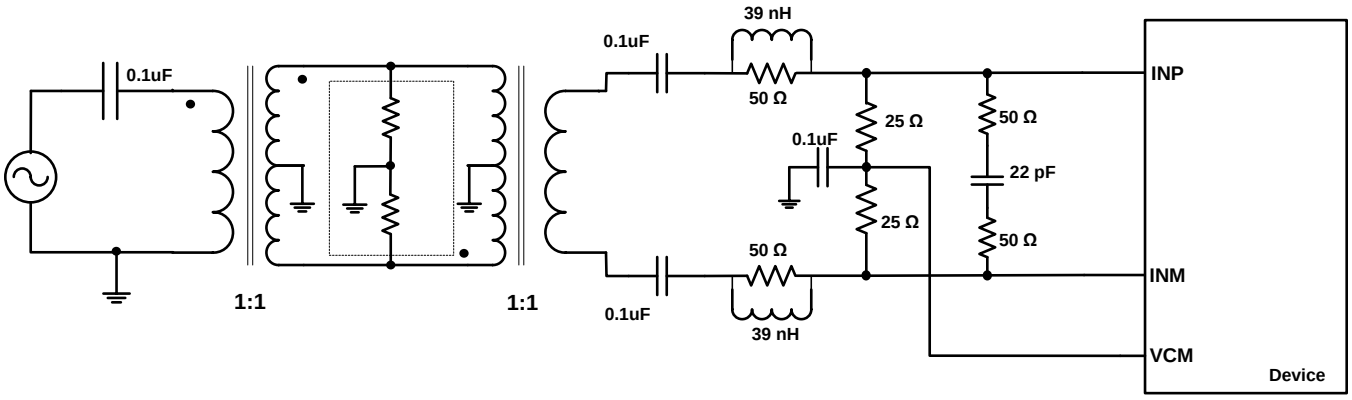

Figure 60. Driving Circuit for Low Input Frequencies

10.2.1.1 Design Requirements

For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitic. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

10.2.1.2 Detailed Design Procedure

A typical application involving using two back-to-back coupled transformers is illustrated in Figure 60. The circuit is optimized for low input frequencies. An external R-C-R filter using 50-Ω resistors and a 22-pF capacitor is used with the series inductor (39 nH), this combination helps absorb the sampling glitches.

Typical Applications (continued)

10.2.1.3 Application Curve

Figure 61 shows the performance obtained by using the circuit shown in Figure 60.

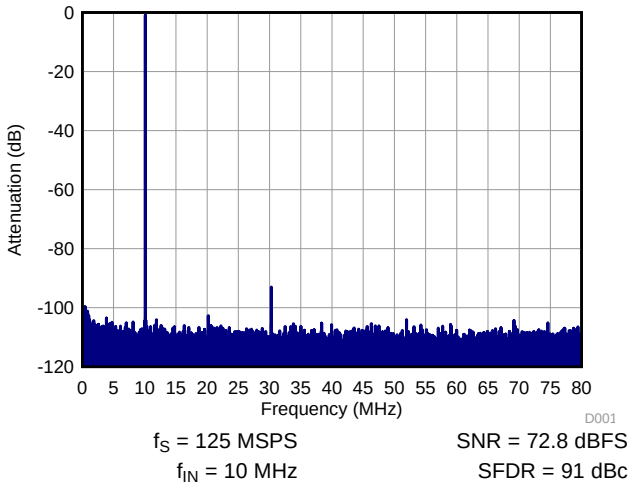

Figure 61. Performance FFT at 10 MHz (Low Input Frequency)

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Typical Applications (continued)

10.2.2 Driving Circuit Design: Input Frequencies Between 100 MHz to 230 MHz

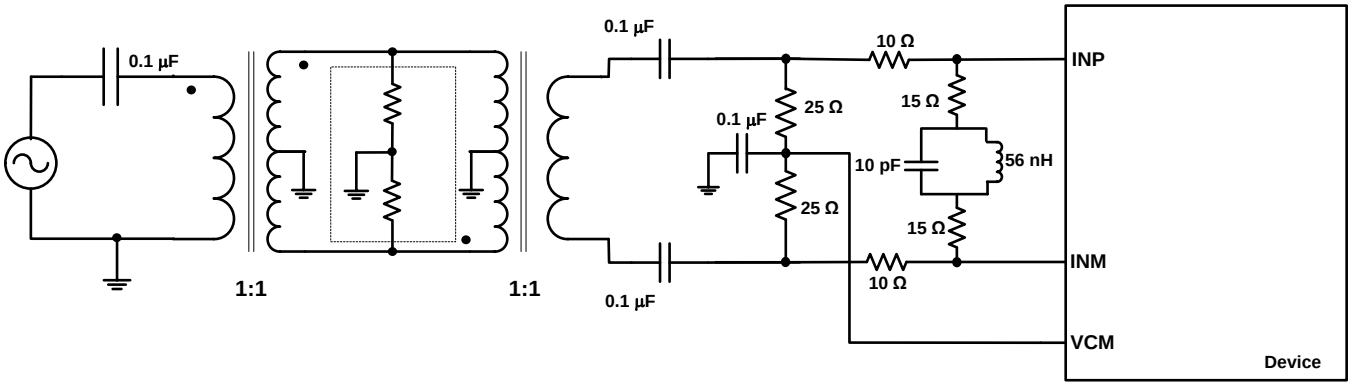


Figure 62. Driving Circuit for Mid-Range Input Frequencies (100 MHz < f_{IN} < 230 MHz)

10.2.2.1 Design Requirements

See the *Design Requirements* section for further details.

10.2.2.2 Detailed Design Procedure

When input frequencies are between 100 MHz to 230 MHz, an R-LC-R circuit can be used to optimize performance, as shown in Figure 62.

10.2.2.3 Application Curve

Figure 63 shows the performance obtained by using the circuit shown in Figure 62.

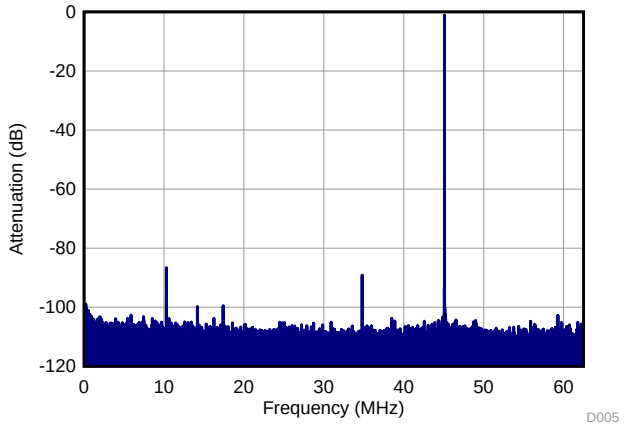


Figure 63. Performance FFT at 170 MHz (Mid Input Frequency)

PRODUCT PREVIEW

Typical Applications (continued)

10.2.3 Driving Circuit Design: Input Frequencies Greater than 230 MHz

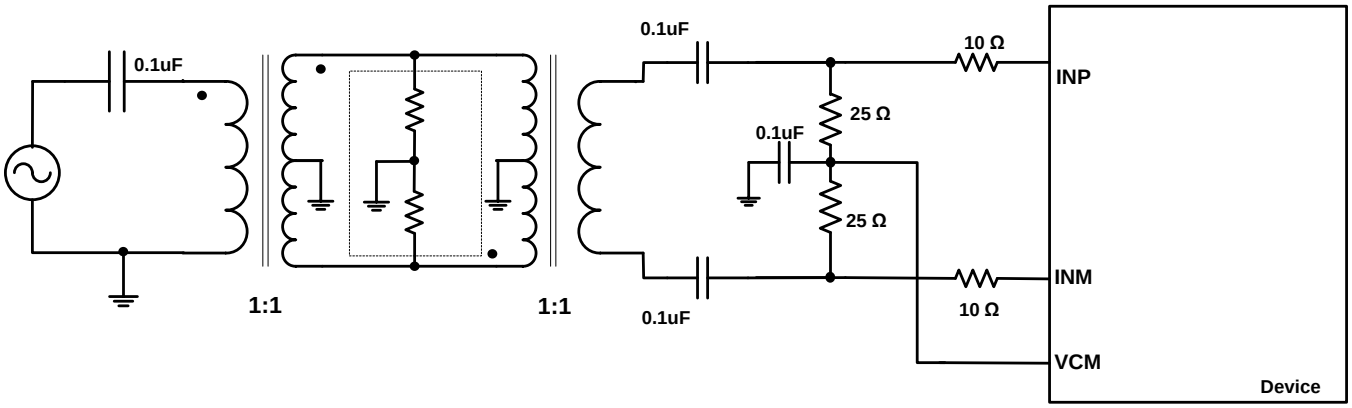


Figure 64. Driving Circuit for High Input Frequencies (f_{IN} > 230 MHz)

10.2.3.1 Design Requirements

See the *Design Requirements* section for further details.

10.2.3.2 Detailed Design Procedure

For high input frequencies (> 230 MHz), using the R-C-R or R-LC-R circuit does not show significant improvement in performance. However, a series resistance of 10 Ω can be used as shown in Figure 64.

10.2.3.3 Application Curve

Figure 65 shows the performance obtained by using the circuit shown in Figure 64.

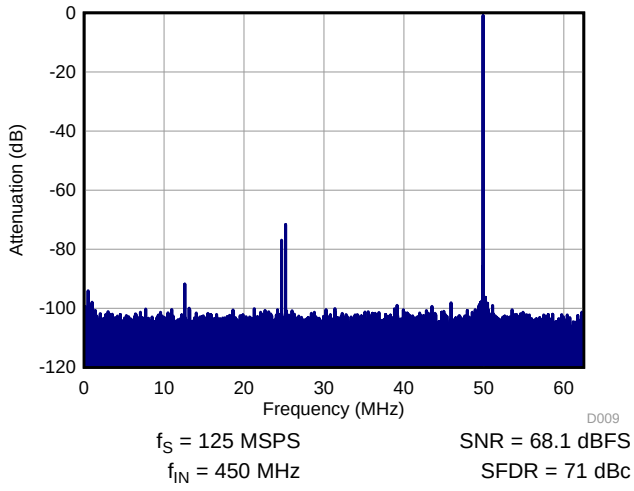


Figure 65. Performance FFT at 450 MHz (High Input Frequency)

11 Power Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD can power up in any order.

PRODUCT PREVIEW

12 Layout

12.1 Layout Guidelines

The ADC344x EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 66. Some important points to remember during laying out the board are:

1. Analog inputs are located on opposite sides of the device pin out to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs should exit the pin out in opposite directions, as shown in the reference layout of Figure 66 as much as possible.
2. In the device pin out, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 66 as much as possible.
3. Digital outputs should be kept away from the analog inputs. When these digital outputs exit the pin out, the digital output traces should not be kept parallel to the analog input traces because this configuration may result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] should be matched in length to avoid skew among outputs.
4. At each power-supply pin (AVDD and DVDD), a 0.1-µF decoupling capacitor should be kept close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

12.2 Layout Example

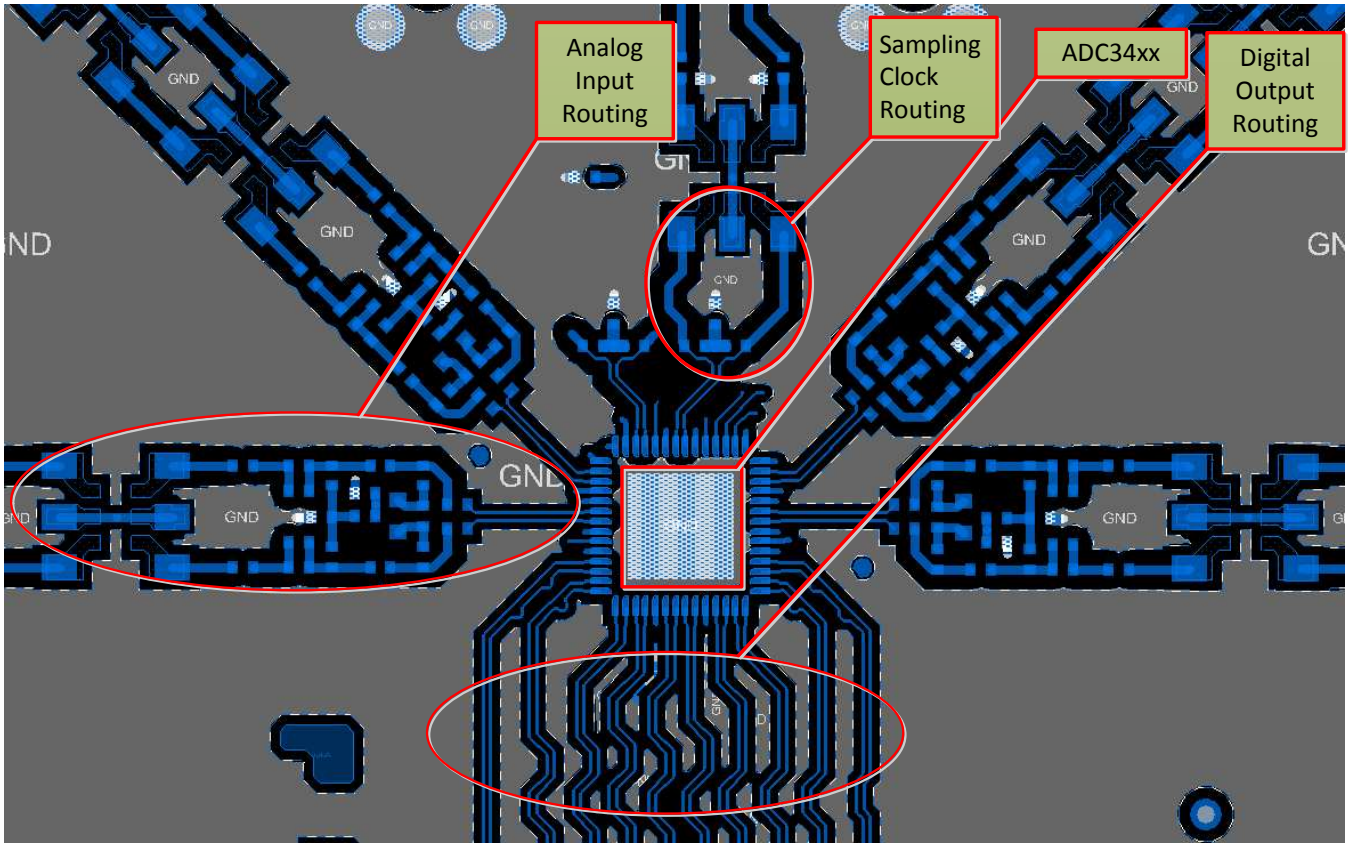


Figure 66. Typical Layout of ADC344x Board

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 34. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADC3441	Click here	Click here	Click here	Click here	Click here
ADC3442	Click here	Click here	Click here	Click here	Click here
ADC3443	Click here	Click here	Click here	Click here	Click here
ADC3444	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

PowerPAD is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC3441IRTQR	PREVIEW	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3441	
ADC3441IRTQT	PREVIEW	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3441	
ADC3442IRTQR	PREVIEW	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3442	
ADC3442IRTQT	PREVIEW	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3442	
ADC3443IRTQR	PREVIEW	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3443	
ADC3443IRTQT	PREVIEW	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3443	
ADC3444IRTQR	PREVIEW	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3444	
ADC3444IRTQT	PREVIEW	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3444	
PADC3444IRTQT	PREVIEW	QFN	RTQ	56	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

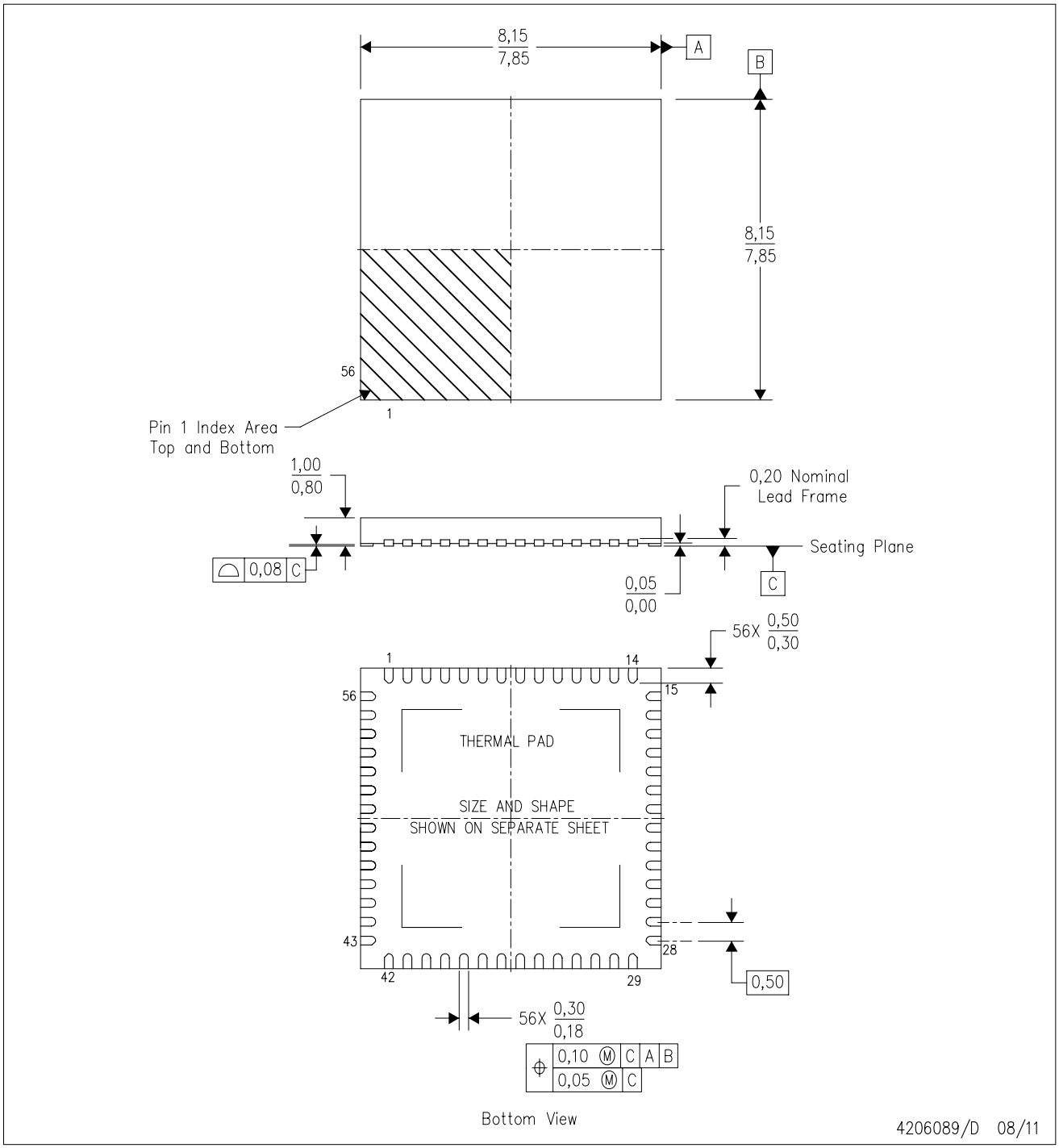
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RTQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220.

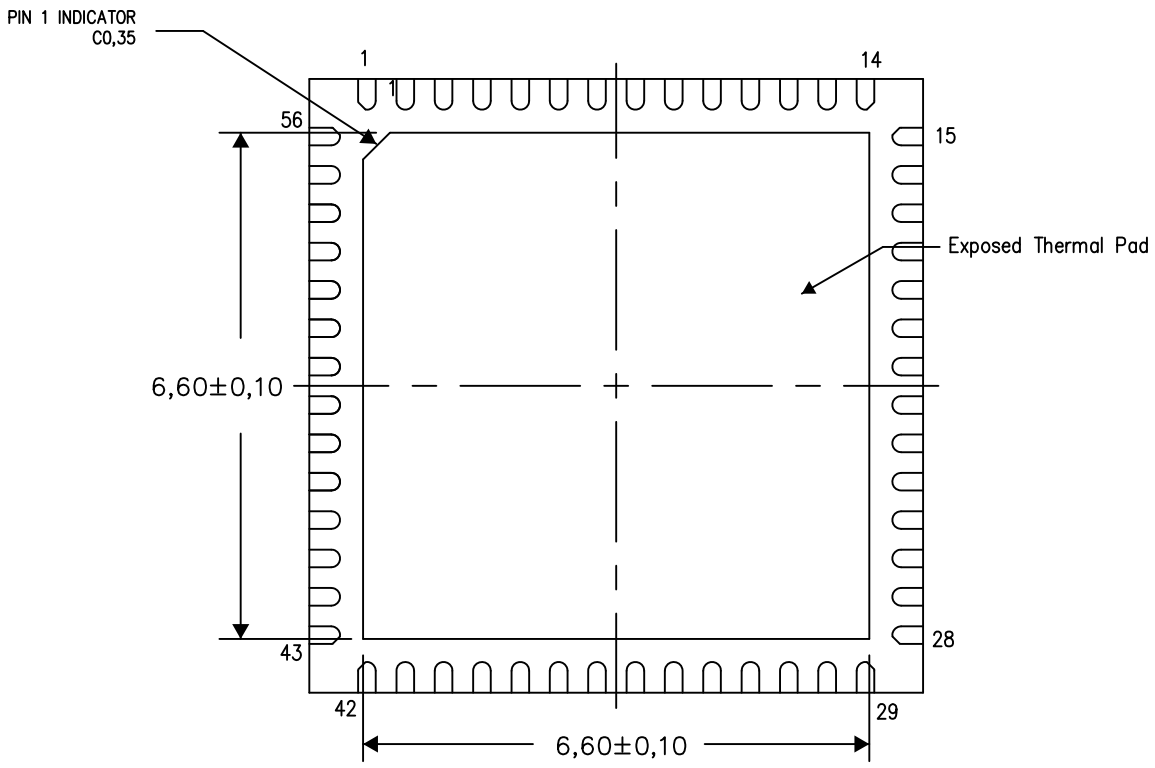
RTQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



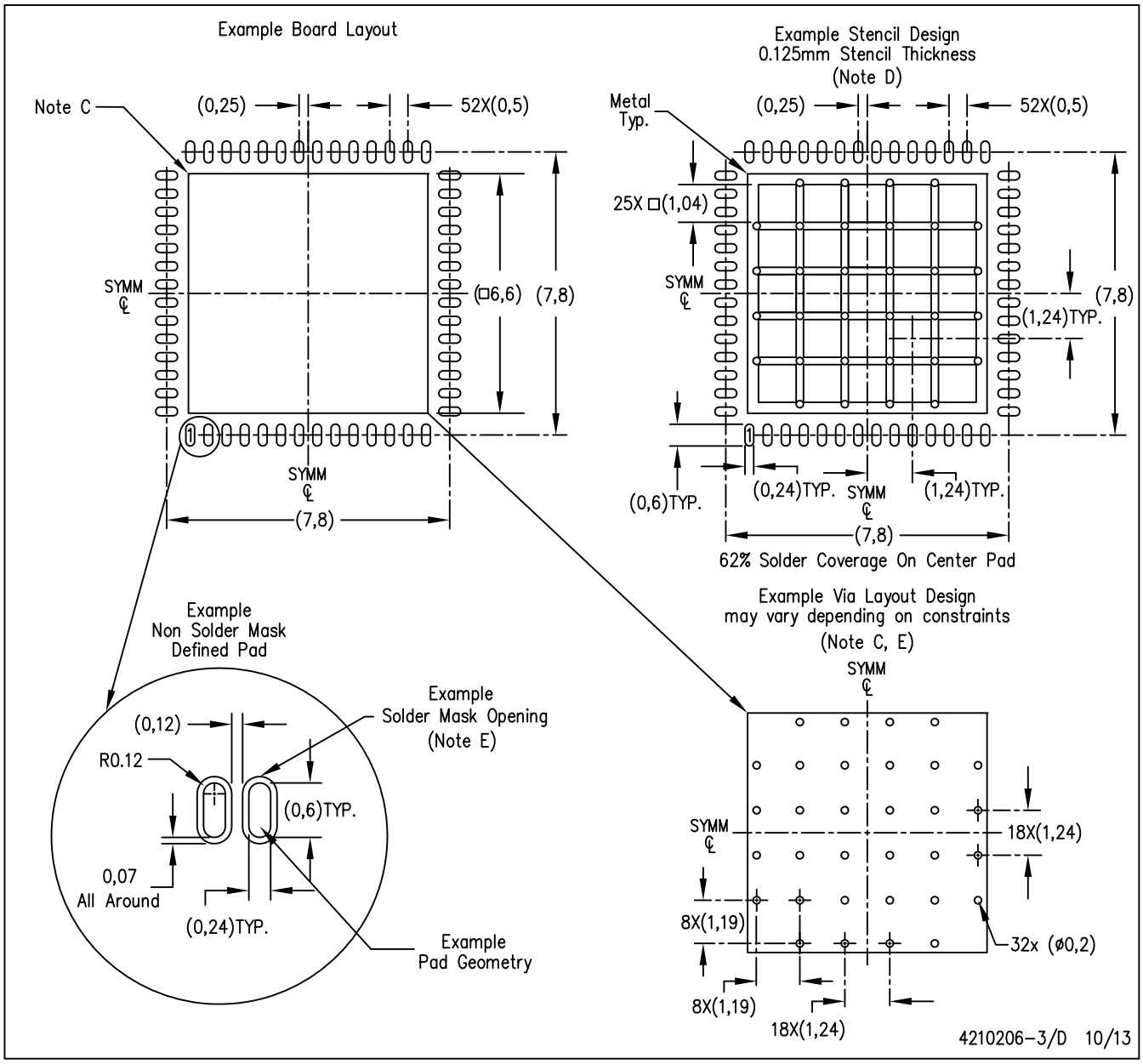
Bottom View

Exposed Thermal Pad Dimensions

4206252–6/Q 03/15

NOTE: All linear dimensions are in millimeters

RTQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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