ADC32J4x Dual-Channel, 14-Bit, 50-MSPS to 160-MSPS, Analog-to-Digital Converters with JESD204B Interface

1 Features

- Dual Channel
- 14-Bit Resolution
- Single Supply: 1.8 V
- Flexible Input Clock Buffer with Divide-by-1, -2, -4
- SNR = 72.2 dBFS, SFDR = 87 dBc at f_{IN} = 70 MHz
- Ultra-Low Power Consumption:
  - 227 mW/Ch at 160 MSPS
- Channel Isolation = 105 dB
- Internal Dither
- JESD204B Serial Interface:
  - Subclass 0, 1, 2 Compliant up to 3.2 Gbps
  - Supports One Lane per ADC up to 160 MSPS
- Support for Multi-Chip Synchronization
- Pin-to-Pin Compatible with 12-Bit Version
- Package: VQFN-48 (7 mm × 7 mm)

2 Applications

- Multi-Carrier, Multi-Mode Cellular Base Stations
- Radar and Smart Antenna Arrays
- Munitions Guidance
- Motor Control Feedback
- Network and Vector Analyzers
- Communications Test Equipment
- Nondestructive Testing
- Microwave Receivers
- Software-Defined Radios (SDRs)
- Quadrature and Diversity Radio Receivers

3 Description

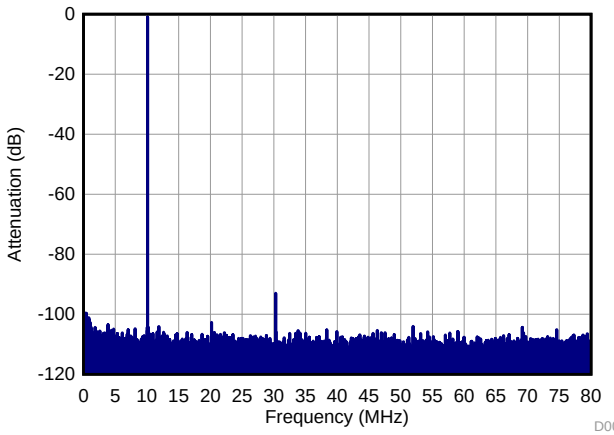
The ADC32J4x are a high-linearity, ultra-low power, dual-channel, 14-bit, 50-MSPS to 160-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. A clock input divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization. The ADC32J4x family supports serial low-voltage differential signaling (LVDS) and JESD204B interfaces in order to reduce the number of interface lines, thus allowing high system integration density. The JESD204B interface is a serial interface, where the data of each ADC are serialized and output over only one differential pair. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock by 20 to derive the bit clock, which is used to serialize the 14-bit data from each channel. The devices support subclass 1 with interface speeds up to 3.2 Gbps.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC32J42	VQFN (48)	7.00 mm × 7.00 mm
ADC32J43		
ADC32J44		
ADC32J45		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Performance at f_S = 160 MSPS, f_{IN} = 10 MHz (SNR = 72.5 dBFS, SFDR = 92 dBc)



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4 Revision History

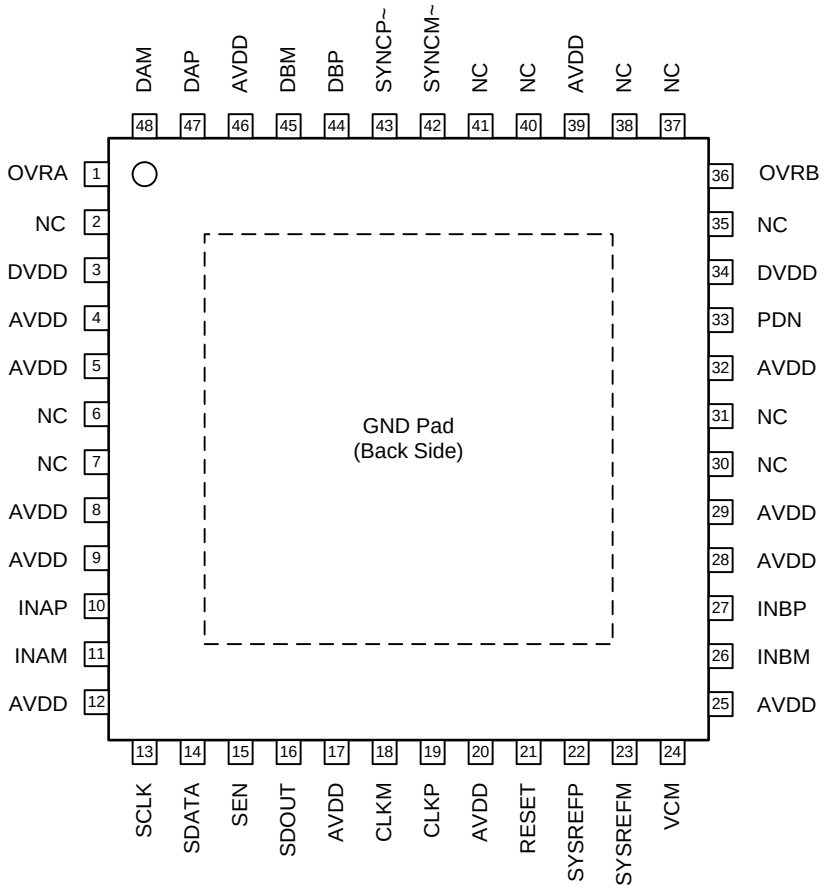
DATE	REVISION	NOTES
May 2014	*	Initial release.

5 Device Comparison Table

INTERFACE	RESOLUTION (Bits)	25 MSPS	50 MSPS	80 MSPS	125 MSPS	160 MSPS
Serial LVDS	12	ADC3221	ADC3222	ADC3223	ADC3224	—
	14	ADC3241	ADC3242	ADC3243	ADC3244	—
JESD204B	12	—	ADC32J22	ADC32J23	ADC32J24	ADC32J2x
	14	—	ADC32J42	ADC32J43	ADC32J44	ADC32J45

6 Pin Configuration and Functions

RGZ Package
VQFN-48
(Top View)



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Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	4, 5, 8, 9, 12, 17, 20, 25, 28, 29, 32, 39, 46	I	Analog 1.8-V power supply
CLKM	18	I	Negative differential clock input for the ADC
CLKP	19	I	Positive differential clock input for the ADC
DAM	48	O	Negative serial JESD204B output for channel A
DAP	47	O	Positive serial JESD204B output for channel A
DBM	45	O	Negative serial JESD204B output for channel B
DBP	44	O	Positive serial JESD204B output for channel B
DVDD	3,34	I	Digital 1.8-V power supply
GND	PowerPAD™	I	Ground, 0 V
INAM	11	I	Negative differential analog input for channel A
INAP	10	I	Positive differential analog input for channel A
INBM	26	I	Negative differential analog input for channel B
INBP	27	I	Positive differential analog input for channel B
NC	2, 6, 7, 30, 31, 35, 37, 38, 40, 41	—	Do not connect
OVRA	1	O	Overrange indicator for channel A
OVRB	36	O	Overrange indicator for channel B
PDN	33	I	Power-down control. This pin has an internal 150-kΩ pull-down resistor.
RESET	21	I	Hardware reset; active high. This pin has an internal 150-kΩ, pull-down resistor.
SCLK	13	I	Serial interface clock input. This pin has an internal 150-kΩ pull-down resistor.
SDATA	14	I	Serial Interface data input. This pin has an internal 150-kΩ pull-down resistor.
SDOUT	16	O	Serial interface data output
SEN	15	I	Serial interface enable. This pin has an internal 150-kΩ pull-up resistor to AVDD.
SYNCM~	42	I	Positive JESD204B synch input
SYNCP~	43	I	Negative JESD204B synch input
SYSREFM	23	I	Negative external SYSREF input
SYSREFP	22	I	Positive external SYSREF input
VCM	24	O	Common-mode voltage output for analog inputs

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Analog supply voltage range, AVDD		–0.3	2.1	V
Digital supply voltage range, DVDD		–0.3	2.1	V
Voltage applied to input pins:	INAP, INBP, INAM, INBM	–0.3	AVDD + 0.3	V
	CLKP, CLKM	–0.3	AVDD + 0.3	V
	SYSREFP, SYSREFM, SYNCP~, SYNCM~	–0.3	AVDD + 0.3	V
	SCLK, SEN, SDATA, RESET, PDN	–0.3	DVDD + 0.3	V
Temperature range	Operating free-air, T_A	–40	85	ºC
	Operating junction, T_J		125	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage range		1.7	1.8	1.9	V
DVDD	Digital supply voltage range		1.7	1.8	1.9	V
ANALOG INPUT						
V_{ID}	Differential input voltage	For input frequencies < 450 MHz		2		V_{PP}
		For input frequencies < 600 MHz		1		V_{PP}
V_{IC}	Input common-mode voltage			VCM ± 0.025		V
CLOCK INPUT						
	Input clock frequency	Sampling clock frequency	25		160(1)	MSPS
	Input clock amplitude (differential)	Sine wave, ac-coupled		1.5		V
		LPECL, ac-coupled		1.6		V
		LVDS, ac-coupled		0.7		V
	Input clock duty cycle			50%		
	Input clock common-mode voltage			0.95		V
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to GND			3.3		pF
R_{LOAD}	Single-ended load resistance			100		Ω

(1) With clock divider enabled for default ‘div by 1’. Maximum sampling clock frequency for ‘div by 4’ option is 640MSPS.

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7.4 Thermal Information

THERMAL METRIC(1)		ADC32J4x RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	3.0	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: ADC32J42, ADC32J43

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, Maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER	ADC32J42 MIN	ADC32J42 TYP	ADC32J42 MAX	ADC32J43 MIN	ADC32J43 TYP	ADC32J43 MAX	UNIT
ADC clock frequency			50			80	MSPS
Resolution	14			14			Bits
1.8-V analog supply current		134			152		mA
1.8-V digital supply current		22			31		mA
Total power dissipation		281			329		mW
Global power-down dissipation		5			5		mW
Wake-up time from global power-down		85			85		us
Standby power-down dissipation		99			105		mW
Wake-up time from standby power-down		35			35		µs

7.6 Electrical Characteristics: ADC32J44, ADC32J45

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, Maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER	ADC32J44 MIN	ADC32J44 TYP	ADC32J44 MAX	ADC32J45 MIN	ADC32J45 TYP	ADC32J45 MAX	UNIT
ADC clock frequency			125			160	MSPS
Resolution	14			14			Bits
1.8-V analog supply current		177			192		mA
1.8-V digital supply current		46			56		mA
Total power dissipation		401			454		mW
Global power-down dissipation		5			5		mW
Wake-up time from global power-down		85			85		us
Standby power-down dissipation		112			118		mW
Wake-up time from standby power-down		35			35		µs

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7.7 Electrical Characteristics: General

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, Maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Differential input full-scale			2.0		V_{PP}
r_i	Input resistance	Differential at dc		6.5		kΩ
c_i	Input capacitance	Differential at dc		5.2		pF
$V_{OC(VCM)}$	VCM common-mode voltage output			0.95		V
	VCM output current capability			10		mA
	Input common-mode current	Per analog input pin		1.5		µA/MSPS
	Analog input bandwidth (3 dB)	50-Ω differential source driving 50-Ω termination across INP and INM		450		MHz
DC ACCURACY						
E_O	Offset error		–TBD		TBD	mV
α_{EO}	Temperature coefficient of offset error			TBD		mV/C
$E_{G(REF)}$	Gain error as a result of internal reference inaccuracy alone		–TBD		TBD	%FS
$E_{G(CHAN)}$	Gain error of channel alone			TBD		%FS
$\alpha_{(EGCHAN)}$	Temperature coefficient of $E_{G(CHAN)}$			TBD		Δ%FS/Ch
CHANNEL-TO-CHANNEL ISOLATION						
	Crosstalk(1)	f_{IN} = 10 MHz		105		dB
		f_{IN} = 100 MHz		105		dB
		f_{IN} = 200 MHz		105		dB
		f_{IN} = 230 MHz		105		dB
		f_{IN} = 300 MHz		105		dB

(1) Crosstalk is measured with a –1-dBFS input signal on aggressor channel and no input on victim channel.

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7.8 AC Performance: ADC32J42

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J42 (f_S = 50 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		73			73.2		dBFS
		f_{IN} = 70 MHz	TBD	72.3			72.5		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.3			72.5		
		f_{IN} = 100 MHz		72.2			72.8		
		f_{IN} = 170 MHz		70.4			70.6		
		f_{IN} = 230 MHz		69.1			69.4		
NSD	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–147			–147.2		dBFS/Hz
		f_{IN} = 70 MHz	TBD	–146.3			–146.5		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	–146.3			–146.5		
		f_{IN} = 100 MHz		–146.2			–146.8		
		f_{IN} = 170 MHz		–144.4			–144.6		
		f_{IN} = 230 MHz		–143.1			–143.4		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73			73.2		dBFS
		f_{IN} = 70 MHz	TBD	72.2			72.3		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.2			72.3		
		f_{IN} = 100 MHz		72.1			72.6		
		f_{IN} = 170 MHz		70.2			70.1		
		f_{IN} = 230 MHz		68.6			68.8		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.8			11.9		Bits
		f_{IN} = 70 MHz	TBD	11.7			11.7		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	11.7			11.7		
		f_{IN} = 100 MHz		11.7			11.8		
		f_{IN} = 170 MHz		11.4			11.4		
		f_{IN} = 230 MHz		11.1			11.1		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		100			95		dBc
		f_{IN} = 70 MHz	TBD	89			87		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	89			87		
		f_{IN} = 100 MHz		88			86		
		f_{IN} = 170 MHz		85			79		
		f_{IN} = 230 MHz		79			77		
HD2	Second harmonic distortion	f_{IN} = 10 MHz		100			98		dBc
		f_{IN} = 70 MHz	TBD	92			90		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	92			90		
		f_{IN} = 100 MHz		92			89		
		f_{IN} = 170 MHz		85			79		
		f_{IN} = 230 MHz		79			77		
HD3	Third harmonic distortion	f_{IN} = 10 MHz		100			95		dBc
		f_{IN} = 70 MHz	TBD	89			87		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	89			87		
		f_{IN} = 100 MHz		88			86		
		f_{IN} = 170 MHz		87			84		
		f_{IN} = 230 MHz		84			81		

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AC Performance: ADC32J42 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J42 (f_S = 50 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		95			93		dBc
		f_{IN} = 70 MHz	TBD	95			95		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	95			95		
		f_{IN} = 100 MHz		96			93		
		f_{IN} = 170 MHz		96			89		
		f_{IN} = 230 MHz		94			91		
THD	Total harmonic distortion	f_{IN} = 10 MHz		98			94		dBc
		f_{IN} = 70 MHz	TBD	88			86		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	88			86		
		f_{IN} = 100 MHz		88			85		
		f_{IN} = 170 MHz		84			79		
		f_{IN} = 230 MHz		79			77		
IMD3	Third-tone intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		93			93		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		91			89		

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7.9 AC Performance: ADC32J43

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J43 (f_S = 80 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		73			73.1		dBFS
		f_{IN} = 70 MHz	TBD	72.7			73.2		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.7			73.2		
		f_{IN} = 100 MHz		72.3			72.6		
		f_{IN} = 170 MHz		70.4			70.6		
		f_{IN} = 230 MHz		69.6			69.9		
NSD	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–149			–149.1		dBFS/Hz
		f_{IN} = 70 MHz	TBD	–148.7			–149.2		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	–148.7			–149.2		
		f_{IN} = 100 MHz		–148.3			–148.6		
		f_{IN} = 170 MHz		–146.4			–146.6		
		f_{IN} = 230 MHz		–145.6			–145.9		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73			73		dBFS
		f_{IN} = 70 MHz	TBD	72.6			73.1		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.6			73.1		
		f_{IN} = 100 MHz		72.2			72.4		
		f_{IN} = 170 MHz		70.2			70.1		
		f_{IN} = 230 MHz		69.1			69.1		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.8			11.8		Bits
		f_{IN} = 70 MHz	TBD	11.8			11.9		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	11.8			11.9		
		f_{IN} = 100 MHz		11.7			11.7		
		f_{IN} = 170 MHz		11.4			11.4		
		f_{IN} = 230 MHz		11.2			11.2		
SFDR	Spurious-free dynamic range	f_{IN}= 10 MHz		95			91		dBc
		f_{IN} = 70 MHz	TBD	91			88		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	91			88		
		f_{IN} = 100 MHz		90			85		
		f_{IN} = 170 MHz		82			80		
		f_{IN} = 230 MHz		78			77		
HD2	Second harmonic distortion	f_{IN} = 10 MHz		101			99		dBc
		f_{IN} = 70 MHz	TBD	96			94		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	96			94		
		f_{IN} = 100 MHz		93			90		
		f_{IN} = 170 MHz		82			80		
		f_{IN} = 230 MHz		78			77		
HD3	Third harmonic distortion	f_{IN} = 10 MHz		95			91		dBc
		f_{IN} = 70 MHz	TBD	91			88		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	91			88		
		f_{IN} = 100 MHz		90			85		
		f_{IN} = 170 MHz		86			83		
		f_{IN} = 230 MHz		84			79		

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AC Performance: ADC32J43 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J43 (f_S = 80 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		97			97		dBc
		f_{IN} = 70 MHz	TBD	91			93		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	91			93		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz		91			86		
		f_{IN} = 230 MHz		90			85		
THD	Total harmonic distortion	f_{IN} = 10 MHz		95			91		dBc
		f_{IN} = 70 MHz	TBD	91			88		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	91			88		
		f_{IN} = 100 MHz		89			85		
		f_{IN} = 170 MHz		82			79		
		f_{IN} = 230 MHz		78			76		
IMD3	Third-tone intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		95			95		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		89			88		

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7.10 AC Performance: ADC32J44

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J44 (f_S = 125 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		73.2			73.6		dBFS
		f_{IN} = 70 MHz	TBD	72.5			73		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.5			73		
		f_{IN} = 100 MHz		72.1			72.2		
		f_{IN} = 170 MHz		70.3			71.1		
		f_{IN} = 230 MHz		69.4			70		
NSD	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–151.2			–151.6		dBFS/Hz
		f_{IN} = 70 MHz	TBD	–150.5			–151		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	–150.5			–151		
		f_{IN} = 100 MHz		–150.1			–150.2		
		f_{IN} = 170 MHz		–148.3			–149.1		
		f_{IN} = 230 MHz		–147.4			–148		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.1			73.4		dBFS
		f_{IN} = 70 MHz	TBD	72.4			72.8		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.4			72.8		
		f_{IN} = 100 MHz		71.9			71.9		
		f_{IN} = 170 MHz		70.1			70.7		
		f_{IN} = 230 MHz		68.8			69.2		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.9			11.9		Bits
		f_{IN} = 70 MHz	TBD	11.7			11.8		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	11.7			11.8		
		f_{IN} = 100 MHz		11.7			11.7		
		f_{IN} = 170 MHz		11.4			11.5		
		f_{IN} = 230 MHz		11.1			11.2		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		90			88		dBc
		f_{IN} = 70 MHz	TBD	88			86		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	88			86		
		f_{IN} = 100 MHz		87			85		
		f_{IN} = 170 MHz		85			82		
		f_{IN} = 230 MHz		77			76		
HD2	Second harmonic distortion	f_{IN} = 10 MHz		91			91		dBc
		f_{IN} = 70 MHz	TBD	90			88		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	90			88		
		f_{IN} = 100 MHz		88			85		
		f_{IN} = 170 MHz		85			82		
		f_{IN} = 230 MHz		77			76		
HD3	Third harmonic distortion	f_{IN} = 10 MHz		90			88		dBc
		f_{IN} = 70 MHz	TBD	88			86		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	88			86		
		f_{IN} = 100 MHz		87			85		
		f_{IN} = 170 MHz		85			83		
		f_{IN} = 230 MHz		82			80		

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AC Performance: ADC32J44 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J44 (f_S = 125 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		95			94		dBc
		f_{IN} = 70 MHz	TBD	95			93		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	95			93		
		f_{IN} = 100 MHz		95			94		
		f_{IN} = 170 MHz		92			87		
		f_{IN} = 230 MHz		92			89		
THD	Total harmonic distortion	f_{IN} = 10 MHz		88			87		dBc
		f_{IN} = 70 MHz	TBD	87			85		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	87			85		
		f_{IN} = 100 MHz		85			83		
		f_{IN} = 170 MHz		83			80		
		f_{IN} = 230 MHz		77			76		
IMD3	Third-tone intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		95			95		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		87			86		

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7.11 AC Performance: ADC32J45

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J45 (f_S = 160 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		72.9			73.1		dBFS
		f_{IN} = 70 MHz	TBD	72.2			72.7		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.2			72.7		
		f_{IN} = 100 MHz		71.6			72		
		f_{IN} = 170 MHz		70.2			70.5		
		f_{IN} = 230 MHz		69.1			69.6		
NSD	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–151.9			–152.1		dBFS/Hz
		f_{IN} = 70 MHz	TBD	–151.2			–151.7		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	–151.2			–151.7		
		f_{IN} = 100 MHz		–150.6			–151		
		f_{IN} = 170 MHz		–149.2			–149.5		
		f_{IN} = 230 MHz		–148.1			–148.6		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		72.8			72.9		dBFS
		f_{IN} = 70 MHz	TBD	72.1			72.4		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	72.1			72.4		
		f_{IN} = 100 MHz		71.4			71.6		
		f_{IN} = 170 MHz		69.9			69.9		
		f_{IN} = 230 MHz		68.6			68.7		
ENOB	Effective number of bits	f_{IN} = 10 MHz		11.8			11.8		Bits
		f_{IN} = 70 MHz	TBD	11.7			11.7		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	11.7			11.7		
		f_{IN} = 100 MHz		11.6			11.6		
		f_{IN} = 170 MHz		11.3			11.3		
		f_{IN} = 230 MHz		11.1			11.1		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		89			84		dBc
		f_{IN} = 70 MHz	TBD	87			83		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	87			83		
		f_{IN} = 100 MHz		85			82		
		f_{IN} = 170 MHz		82			80		
		f_{IN} = 230 MHz		78			76		
HD2	Second harmonic distortion	f_{IN} = 10 MHz		97			95		dBc
		f_{IN} = 70 MHz	TBD	92			87		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	92			87		
		f_{IN} = 100 MHz		88			85		
		f_{IN} = 170 MHz		84			80		
		f_{IN} = 230 MHz		78			76		
HD3	Third harmonic distortion	f_{IN} = 10 MHz		89			84		dBc
		f_{IN} = 70 MHz	TBD	87			83		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	87			83		
		f_{IN} = 100 MHz		85			82		
		f_{IN} = 170 MHz		82			80		
		f_{IN} = 230 MHz		80			78		

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AC Performance: ADC32J45 (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADC32J45 (f_S = 160 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		97			96		dBc
		f_{IN} = 70 MHz	TBD	94			91		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	94			91		
		f_{IN} = 100 MHz		92			90		
		f_{IN} = 170 MHz		93			88		
		f_{IN} = 230 MHz		92			89		
THD	Total harmonic distortion	f_{IN}= 10 MHz		89			85		dBc
		f_{IN} = 70 MHz	TBD	87			83		
		f_{IN} = 70 MHz, T_A = 25°C	TBD	87			83		
		f_{IN} = 100 MHz		84			81		
		f_{IN} = 170 MHz		81			78		
		f_{IN} = 230 MHz		77			75		
IMD3	Third-tone intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2}= 50 MHz		100			100		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		89			88		

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7.12 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = DVDD = 1.8 V and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SEN, SDATA, PDN)(1)						
V_{IH}	High-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels	1.2			V
V_{IL}	Low-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels			0.4	V
I_{IH}	High-level input current	SEN		0		µA
		RESET, SCLK, SDATA, PDN		10		µA
I_{IL}	Low-level input current	SEN		10		µA
		RESET, SCLK, SDATA, PDN		0		µA
DIGITAL INPUTS (SYNCP~, SYNCM~, SYSREFP, SYSREFM)						
V_{IH}	High-level input voltage			1.3		V
V_{IL}	Low-level input voltage			0.5		V
$V_{(CM\_DIG)}$	Common-mode voltage for SYNC~ and SYSREF			0.95		V
DIGITAL OUTPUTS (SDOUT, OVRA, OVRB)						
V_{OH}	High-level output voltage		DVDD – 0.1	DVDD		V
V_{OL}	Low-level output voltage				0.1	V
DIGITAL OUTPUTS (JESD204B Interface: DxP, DxM)(2)						
V_{OH}	High-level output voltage			AVDD		V
V_{OL}	Low-level output voltage			AVDD – 0.4		V
V_{OD}	Output differential voltage			0.4		V
V_{OC}	Output common-mode voltage			AVDD – 0.2		V
	Transmitter short-circuit current	Transmitter pins shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
z_{os}	Single-ended output impedance			50		Ω
	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) RESET, SCLK, SDATA, and PDN pins have 150-kΩ (typical) internal pull-down resistor to ground, while SEN pin has 150-kΩ (typical) pull-up resistor to AVDD.
(2) 50-Ω, single-ended external termination to 1.8 V.

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7.13 Timing Characteristics

Typical values are at 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C. See Figure 25.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLE TIMING CHARACTERISTICS						
	Aperture delay		0.85	1.25	1.65	ns
	Aperture delay matching	Between two channels on the same device		±70		ps
		Between two devices at the same temperature and supply voltage		±150		ps
	Aperture jitter			200		f_S rms
	Wake-up time	Time to valid data after coming out of STANDBY mode		TBD	TBD	µs
		Time to valid data after coming out of global power-down		TBD	TBD	µs
$t_{SU\_SYNC\sim}$	Setup time for SYNC~	Referenced to input clock rising edge	1			ns
$t_{H\_SYNC\sim}$	Hold time for SYNC~	Referenced to input clock rising edge	100			ps
t_{SU_SYSREF}	Setup time for SYSREF	Referenced to input clock rising edge	1			ns
t_{H_SYSREF}	Hold time for SYSREF	Referenced to input clock rising edge	100			ps
CML OUTPUT TIMING CHARACTERISTICS						
	Unit interval		320		1667	ps
	Serial output data rate				3.125	Gbps
	Total jitter	3.125 Gbps (20x mode, f_S = 156.25 MSPS)		0.3		$_{P\text{-}P}$UI
t_R, t_F	Data rise time, data fall time	Rise and fall times measured from 20% to 80%, differential output waveform, 600 Mbps ≤ bit rate ≤ 3.125 Gbps		105		ps

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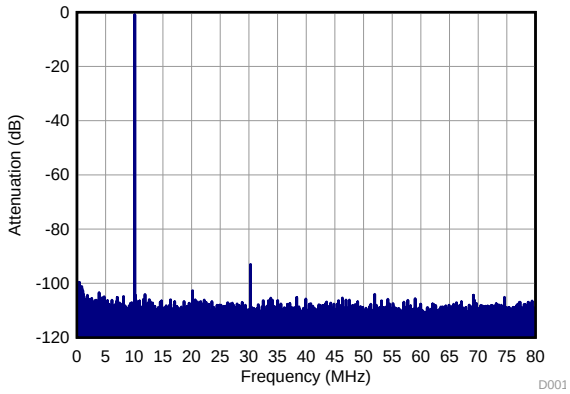
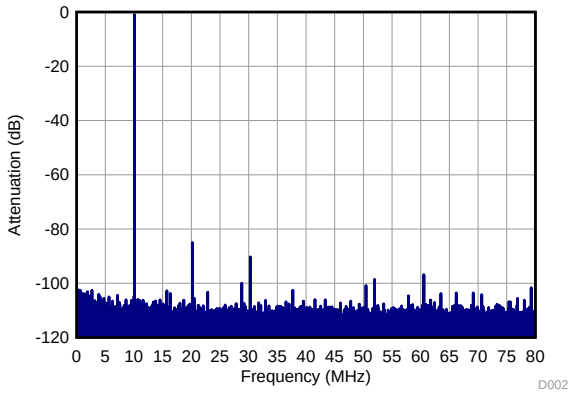
7.14 Typical Characteristics

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



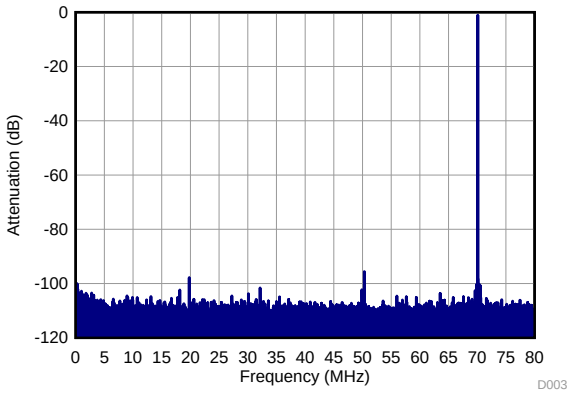
f_S = 160 MSPS SNR = 72.5 dBFS
f_{IN} = 10 MHz SFDR = 92 dBc

Figure 1. FFT with Dither On



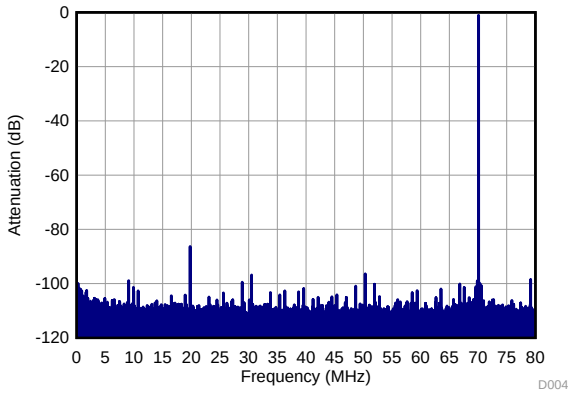
f_S = 160 MSPS SNR = 73.2 dBFS
f_{IN} = 10 MHz SFDR = 84 dBc

Figure 2. FFT with Dither Off



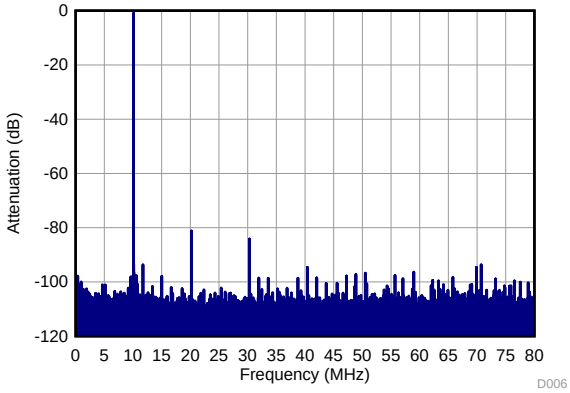
f_S = 160 MSPS SNR = 72 dBFS
f_{IN} = 70 MHz SFDR = 95 dBc

Figure 3. FFT with Dither On



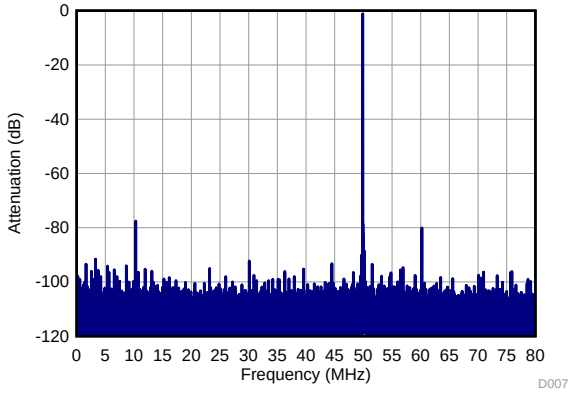
f_S = 160 MSPS SNR = 72.5 dBFS
f_{IN} = 70 MHz SFDR = 85 dBc

Figure 4. FFT with Dither Off



f_S = 160 MSPS SNR = 70 dBFS
f_{IN} = 170 MHz SFDR = 83 dBc

Figure 5. FFT with Dither On



f_S = 160 MSPS SNR = 70.3 dBFS
f_{IN} = 170 MHz SFDR = 80 dBc

Figure 6. FFT with Dither Off

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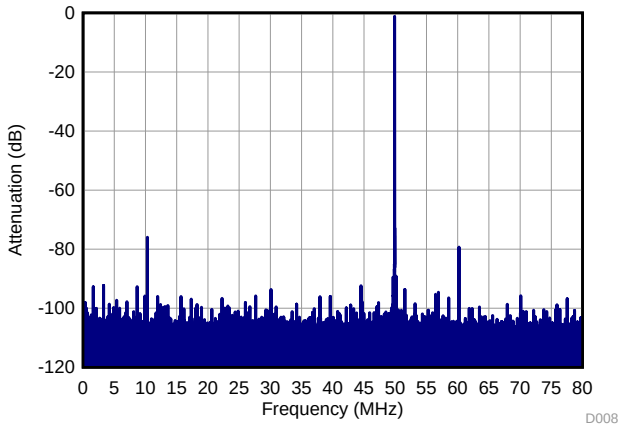
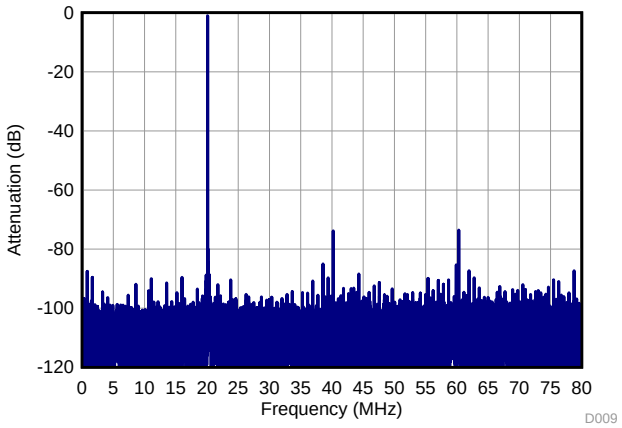
Typical Characteristics (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



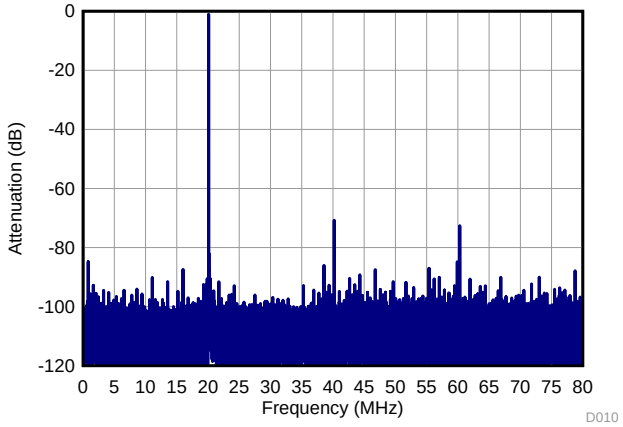
f_S = 160 MSPS SNR = 67.8 dBFS
f_{IN} = 270 MHz SFDR = 76 dBc

Figure 7. FFT with Dither On



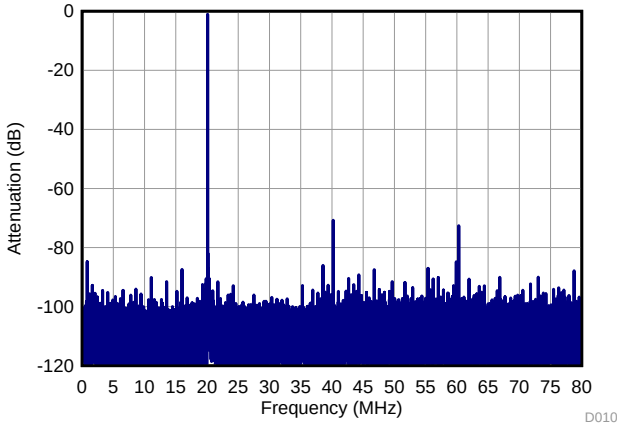
f_S = 160 MSPS SNR = 68.2 dBFS
f_{IN} = 270 MHz SFDR = 75 dBc

Figure 8. FFT with Dither Off



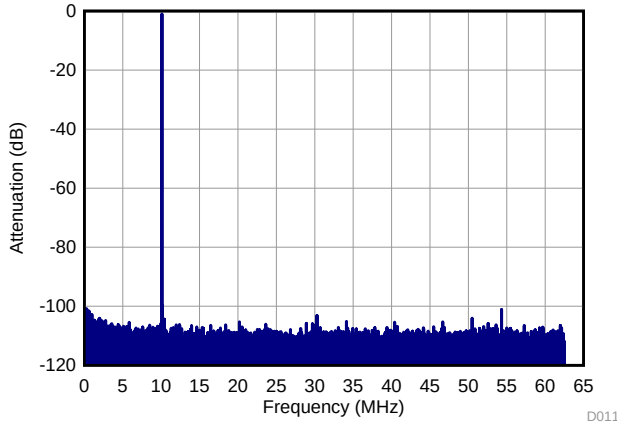
f_S = 160 MSPS SNR = 63.1 dBFS
f_{IN} = 500 MHz SFDR = 73 dBc

Figure 9. FFT with Dither On



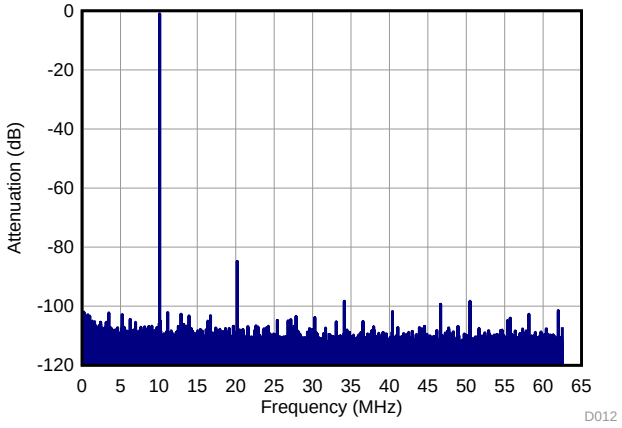
f_S = 160 MSPS SNR = 63.4 dBFS
f_{IN} = 500 MHz SFDR = 70 dBc

Figure 10. FFT with Dither Off



f_S = 125 MSPS SNR = 72.6 dBFS
f_{IN} = 10 MHz SFDR = 100 dBc

Figure 11. FFT with Dither On



f_S = 125 MSPS SNR = 73.3 dBFS
f_{IN} = 10 MHz SFDR = 84 dBc

Figure 12. FFT with Dither Off

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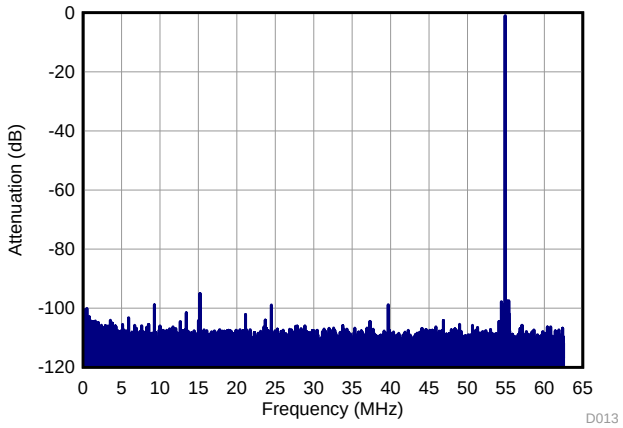
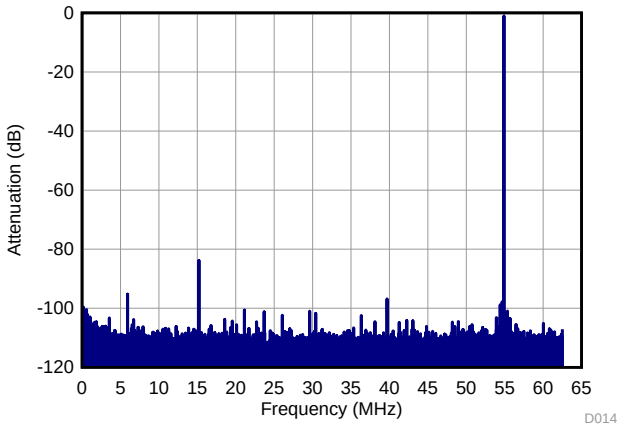
Typical Characteristics (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



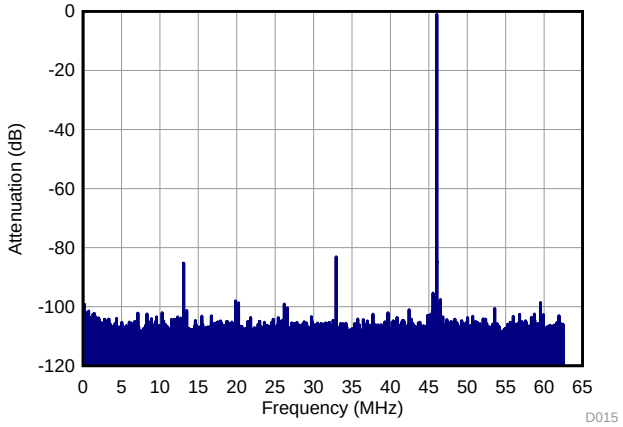
f_S = 125 MSPS SNR = 72.2 dBFS
f_{IN} = 70 MHz SFDR = 94 dBc

Figure 13. FFT with Dither On



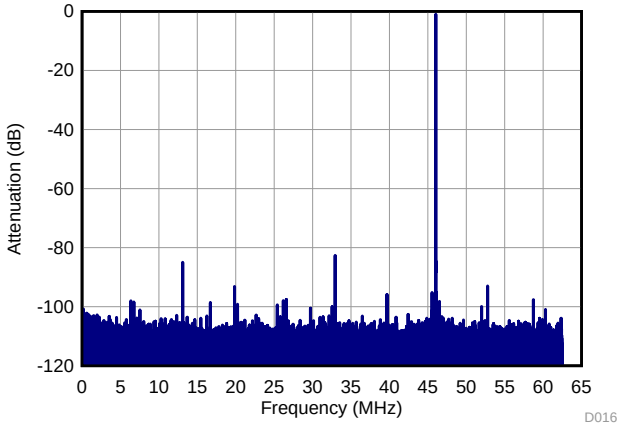
f_S = 125 MSPS SNR = 73 dBFS
f_{IN} = 70 MHz SFDR = 83 dBc

Figure 14. FFT with Dither Off



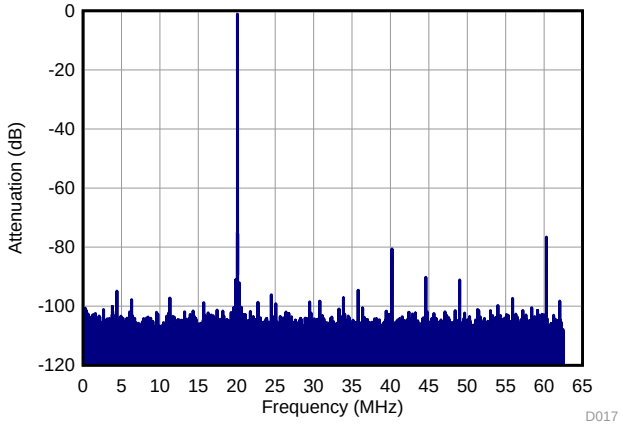
f_S = 125 MSPS SNR = 70.4 dBFS
f_{IN} = 170 MHz SFDR = 82 dBc

Figure 15. FFT with Dither On



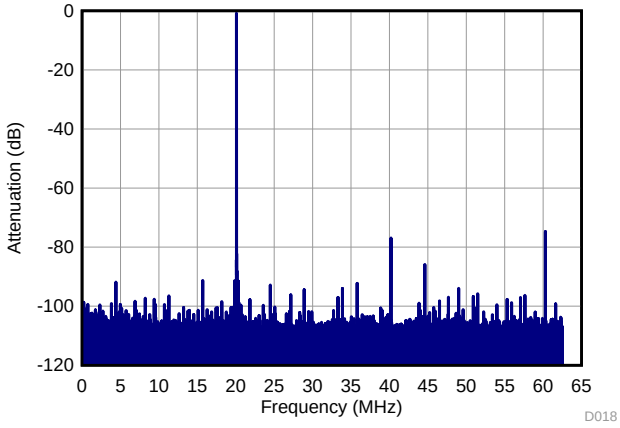
f_S = 125 MSPS SNR = 70.6 dBFS
f_{IN} = 170 MHz SFDR = 81 dBc

Figure 16. FFT with Dither Off



f_S = 125 MSPS SNR = 69 dBFS
f_{IN} = 270 MHz SFDR = 75 dBc

Figure 17. FFT with Dither On



f_S = 125 MSPS SNR = 69.1 dBFS
f_{IN} = 270 MHz SFDR = 74 dBc

Figure 18. FFT with Dither Off

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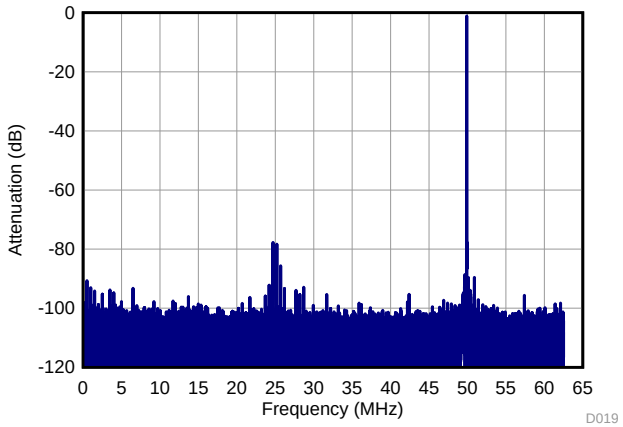
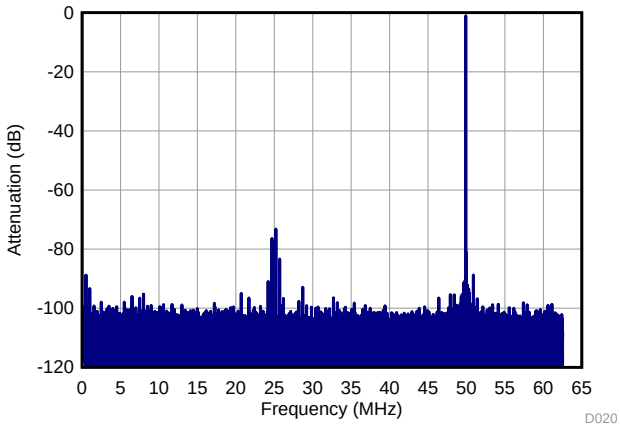
Typical Characteristics (continued)

Typical values are at T_A= 25°C, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.



f_S = 125 MSPS SNR = 65.9 dBFS
f_{IN} = 450 MHz SFDR = 77 dBc

Figure 19. FFT with Dither On



f_S = 125 MSPS SNR = 66 dBFS
f_{IN} = 450 MHz SFDR = 72 dBc

Figure 20. FFT with Dither Off

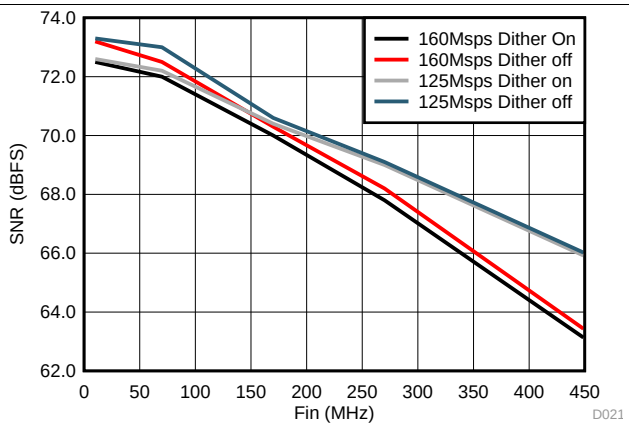


Figure 21. SNR vs Input Frequencies

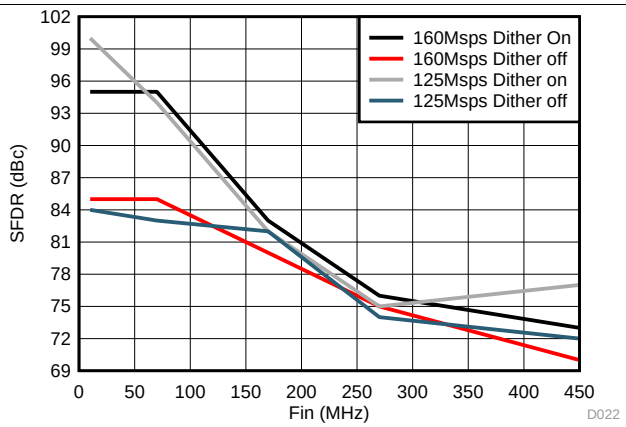


Figure 22. SFDR vs Input Frequencies

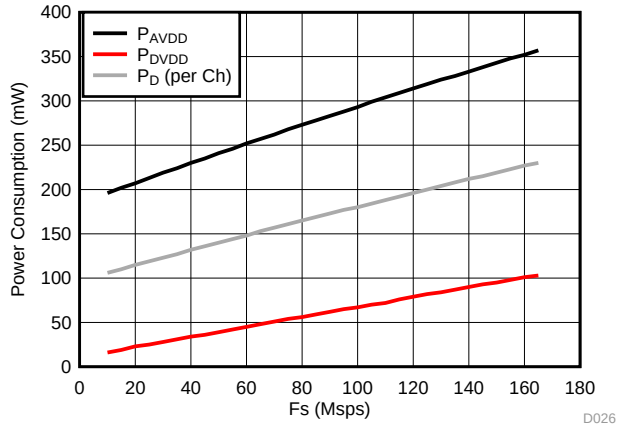


Figure 23. Power Consumption vs Sampling Rate (20x Mode)

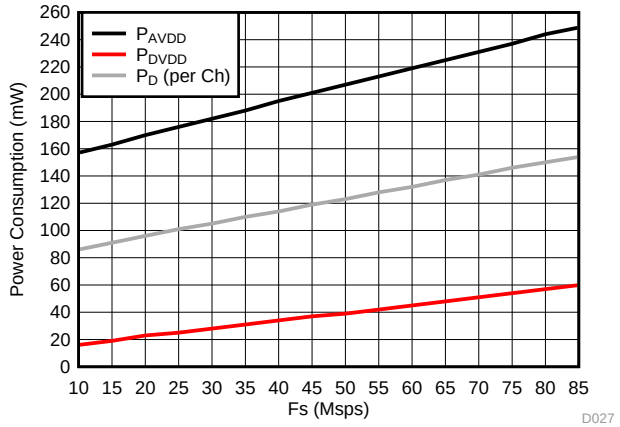


Figure 24. Power Consumption vs Sampling Rate (40x Mode)

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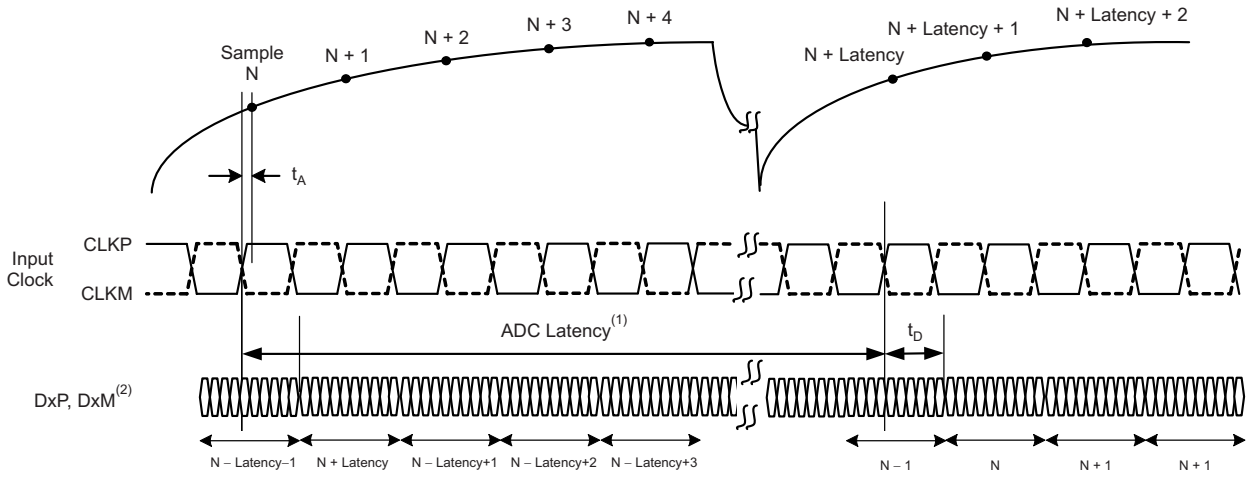
8 Parameter Measurement Information

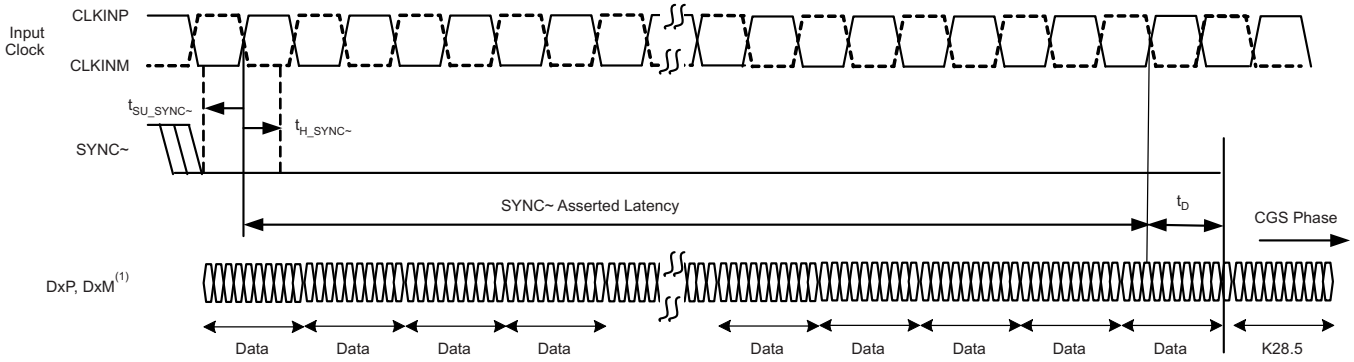
8.1 Timing Diagrams



(1) Overall latency = ADC latency + t_D.

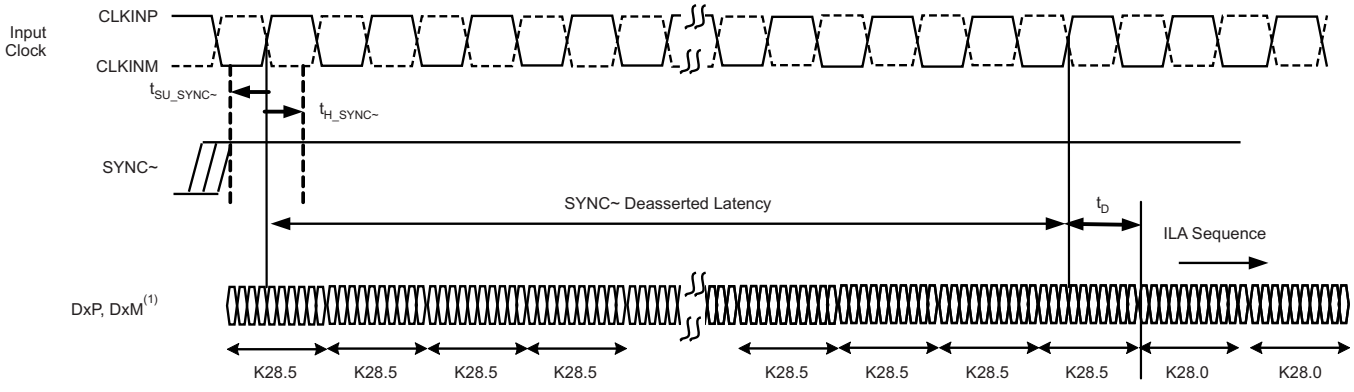
(2) x = A for channel A and B for channel B.

Figure 25. ADC Latency



(1) x = A for channel A and B for channel B.

Figure 26. SYNC~ Latency in CGS Phase (Two-Lane Mode)



(1) x = A for channel A and B for channel B.

Figure 27. SYNC~ Latency in ILAS Phase (Two-Lane Mode)

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Timing Diagrams (continued)

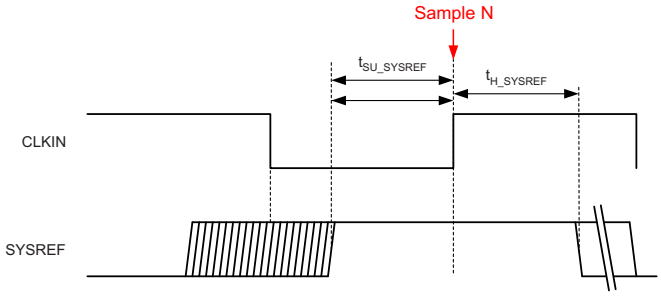

Figure 28. SYSREF Timing (Subclass 1)

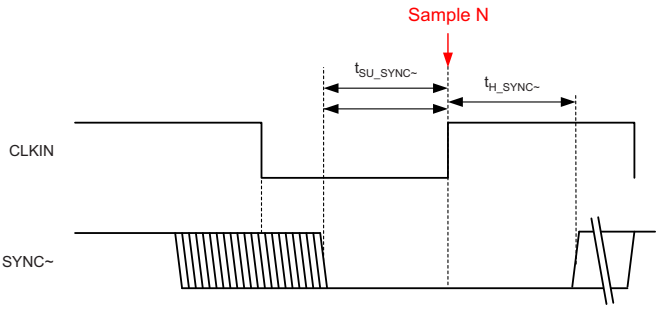

Figure 29. SYNC~ Timing (Subclass 2)

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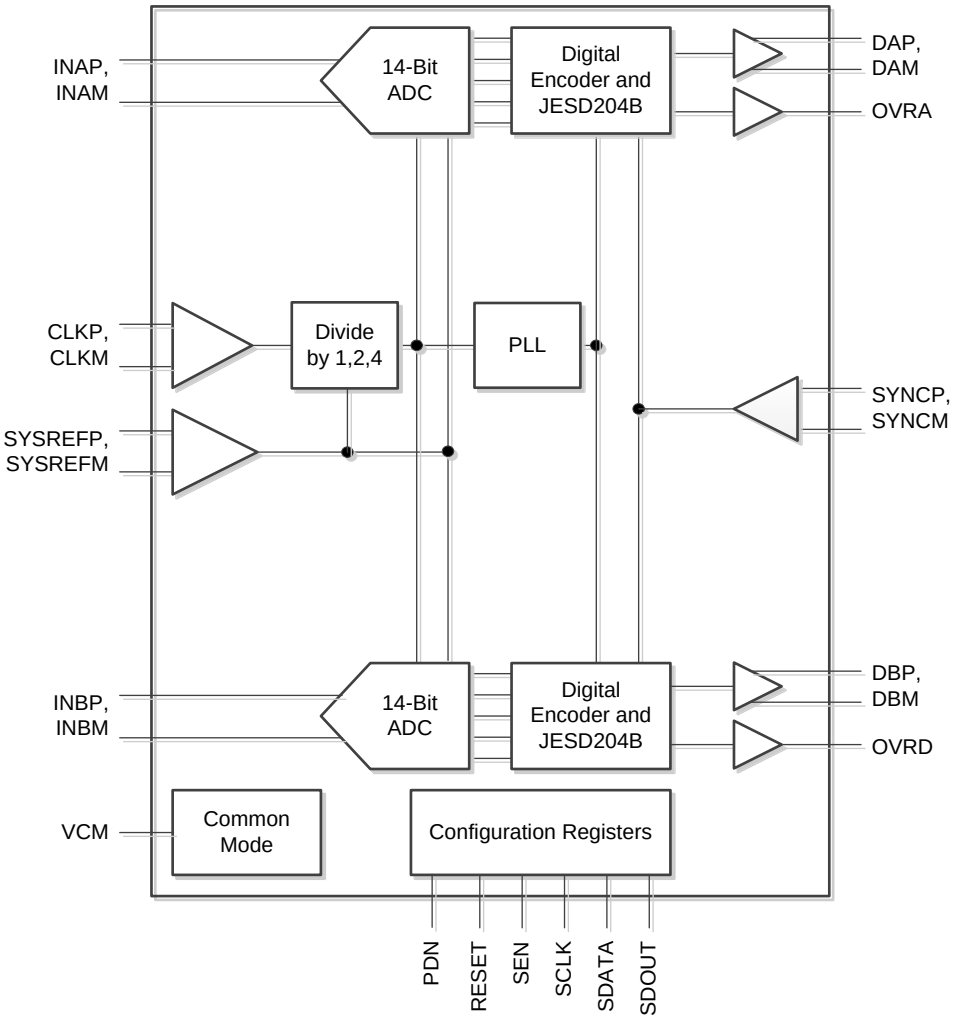
9 Detailed Description

9.1 Overview

The ADC32J4x are a high-linearity, ultra-low power, dual-channel, 14-bit, 50-MSPS to 160-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. A clock input divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization. The ADC32J4x family supports JESD204B interface in order to reduce the number of interface lines, thus allowing for high system integration density. The JESD204B interface is a serial interface, where the data of each ADC are serialized and output over only one differential pair. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock by 20 to derive the bit clock, which is used to serialize the 14-bit data from each channel. The ADC32J4x devices support subclass 1 with interface data rates up to 3.2 Gbps.

9.2 Functional Block Diagram



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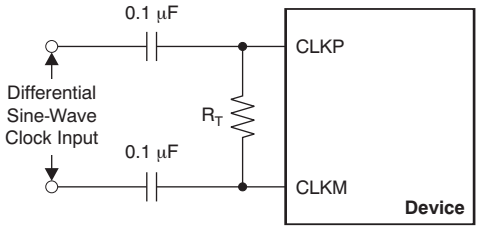
9.3 Feature Description

9.3.1 Analog Inputs

The ADC32J4x analog signal inputs are designed to be driven differentially. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 450 MHz (50-Ω source driving 50-Ω termination between INP and INM).

9.3.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 1.4 V using internal 5-kΩ resistors. The self-bias clock inputs of the ADC32J4x can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 30, Figure 31, and Figure 32. See Figure 33 for details regarding the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

Figure 30. Differential Sine-Wave Clock Driving Circuit

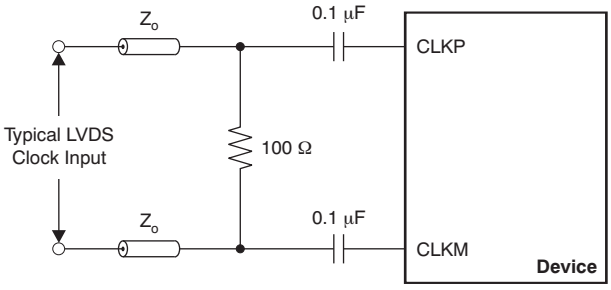


Figure 31. LVDS Clock Driving Circuit

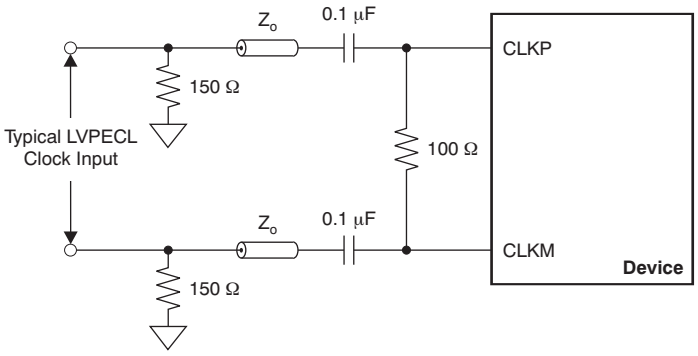


Figure 32. LVPECL Clock Driving Circuit

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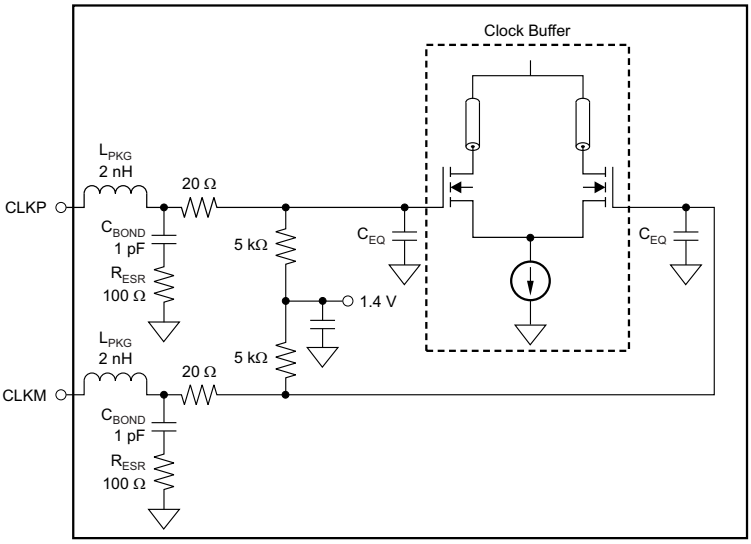

NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 33. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 34. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

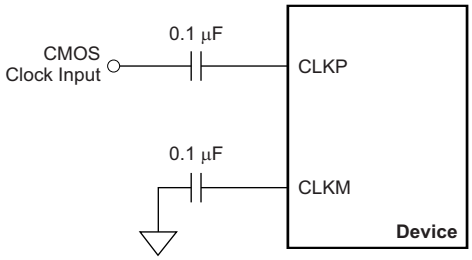

Figure 34. Single-Ended Clock Driving Circuit

9.3.2.1 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors: quantization noise, thermal noise, and jitter noise, as shown in Equation 1. Quantization noise is typically not noticeable in pipeline converters and is 86 dB for a 14-bit ADC. Thermal noise limits SNR at low input frequencies while the clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{-\frac{SNR_{Quantizatoin\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation resulting from sample clock jitter can be calculated with Equation 2:

$$SNR_{Jitter}[dBc] = -20 \cdot \log(2\pi \cdot f_{in} \cdot T_{Jitter}) \quad (2)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (200 fs for the device) which is set by the noise of the clock input buffer and the external clock. T_{Jitter} can be calculated with Equation 3:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (3)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter. The devices have a thermal noise of 73.5 dBFS and internal aperture jitter of 200 fs. The SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 35.

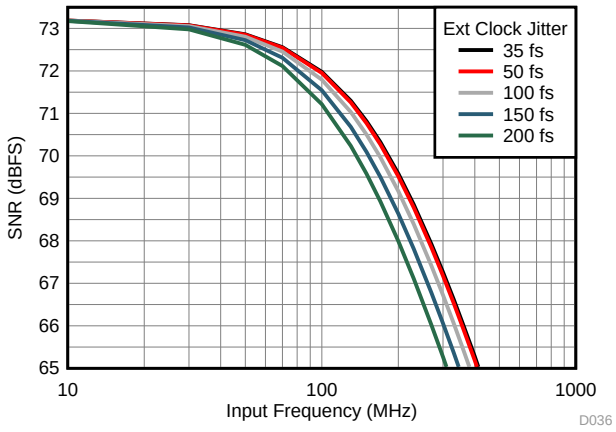

Figure 35. SNR vs Frequency vs Jitter

9.3.2.2 Input Clock Divider

The devices are equipped with an internal divider on the clock input. The divider allows operation with a faster input clock, thus simplifying the system clock distribution design. The clock divider can be bypassed (divide-by-1) for operation with a 160-MHz clock while the divide-by-2 option supports a maximum input clock of 320 MHz and the divide-by-4 option supports a maximum input clock frequency of 640 MHz.

9.3.3 Power-Down Control

The power-down functions of the ADC32J4x can be controlled either through the parallel control pin (PDN) or through an SPI register setting (see Figure 61, register 15h). The PDN pin can also be configured via SPI to a global power-down or standby functionality.

Table 1. Power-Down Modes

FUNCTION	POWER CONSUMPTION (mW)	WAKE-UP TIME (µs)
Global power-down	5	85
Standby	118	35

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9.3.4 Internal Dither Algorithm

The ADC32J4x uses an internal dither algorithm to achieve high SFDR and a clean spectrum. However, the dither algorithm marginally degrades SNR, creating a trade-off between SNR and SFDR. If desired, the dither algorithm can be turned off by using the DIS DITH CHx registers bits. Figure 36 and Figure 37 show the effect of using dither algorithms.

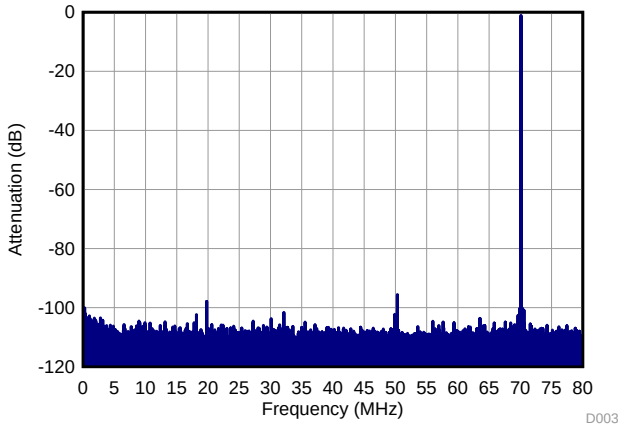

Figure 36. FFT with Dither On

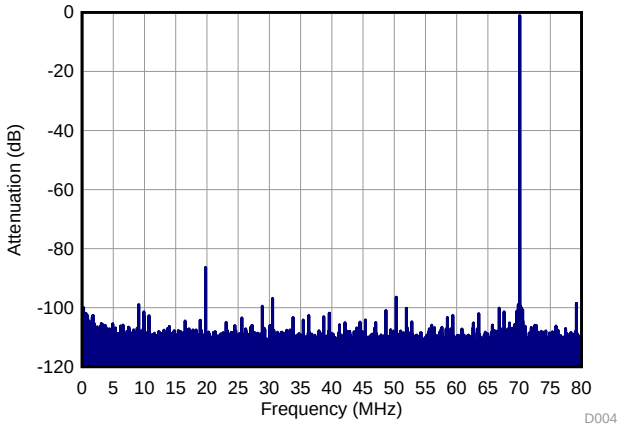

Figure 37. FFT with Dither Off

9.3.5 JESD204B Interface

The ADC32J4x support device subclass 0, 1, and 2 with a maximum output data rate of 3.2 Gbps for each serial transmitter, as shown in Figure 38. The data of each ADC are serialized by 20x using an internal PLL and then transmitted out on one differential pair each. An external SYSREF (subclass 1) or SYNC (subclass 2) signal is used to align all internal clock phases and the local multiframe clock to a specific sampling clock edge. This process allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty.

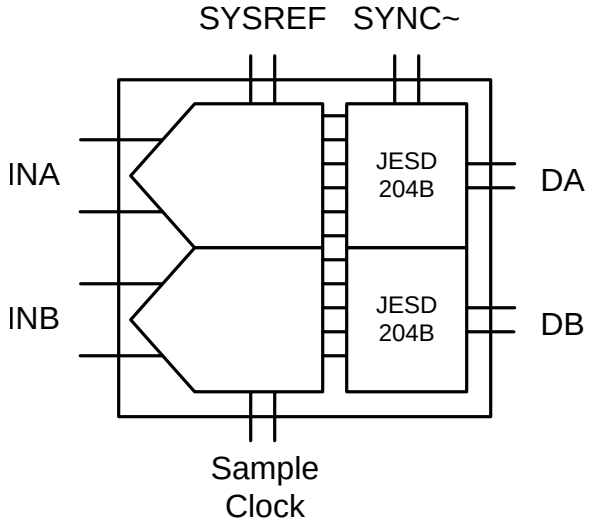

Figure 38. JESD204B Interface

The JESD204B transmitter block consists of the transport layer, the data scrambler, and the link layer, as shown in Figure 39. The transport layer maps the ADC output data into the selected JESD204B frame data format and determines if the ADC output data or test patterns are transmitted. The link layer performs the 8b or 10b data encoding and the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer can be scrambled.

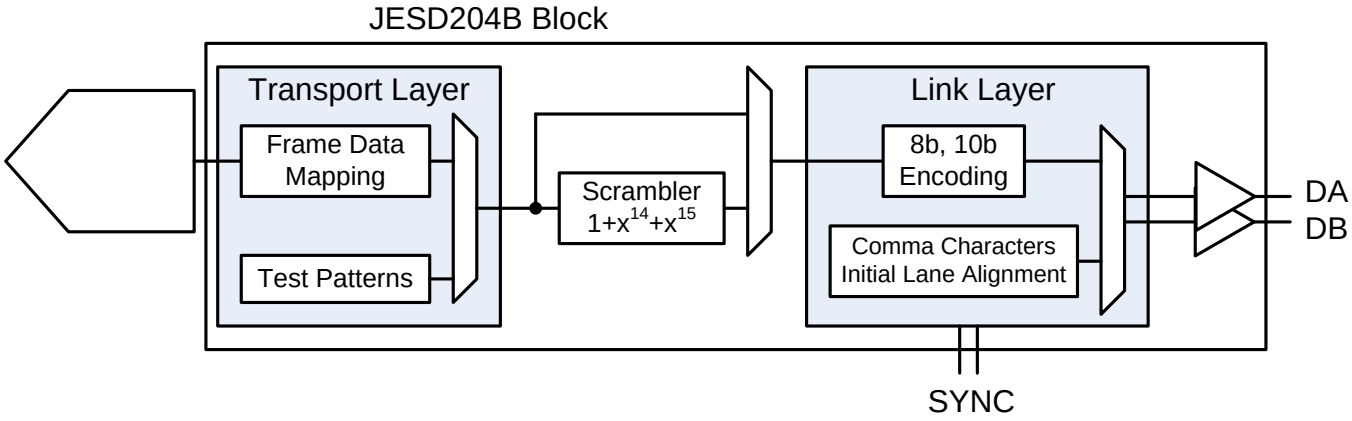

Figure 39. JESD204B Block

9.3.5.1 JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started by the receiving device by asserting the SYNC signal. When a logic high is detected on the SYNC input pins, the ADC32J4x starts transmitting comma (K28.5) characters to establish code group synchronization. When synchronization is complete, the receiving device de-asserts the SYNC signal and the ADC32J4x starts the initial lane alignment sequence with the next local multiframe clock boundary. The ADC32J4x transmits four multiframes, each containing K frames (K is SPI programmable). Each multiframe contains the frame start and end symbols; the second multiframe also contains the JESD204 link configuration data.

9.3.5.2 JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The ADC32J4x supports a clock output, an encoded, and a PRBS (2^{15} – 1) pattern. These patterns can be enabled via SPI register writes and are located in address 26h (bits 7:6).

9.3.5.3 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per link,
- M is the number of converters per device,
- F is the number of octets per frame clock period, and
- S is the number of samples per frame.

Table 2 lists the available JESD204B format and valid range for the ADC32J4x. The ranges are limited by the SERDES line rate and the maximum ADC sample frequency.

Table 2. LMFS Values and Interface Rate

L	M	F	S	MINIMUM ADC SAMPLING RATE (MSPS)	MAXIMUM f_{SERDES} (Mbps)	MAXIMUM ADC SAMPLING RATE (Msps)	MAXIMUM f_{SERDES} (GSPS)	MODE
2	2	2	1	15	300	160	3.2	20x (default)
1	2	4	1	10	400	80	3.2	40x

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The detailed frame assembly for quad-channel mode is shown in Figure 40. The frame assembly configuration can be changed from 20x (default) to 40x by setting the registers listed in Table 3.

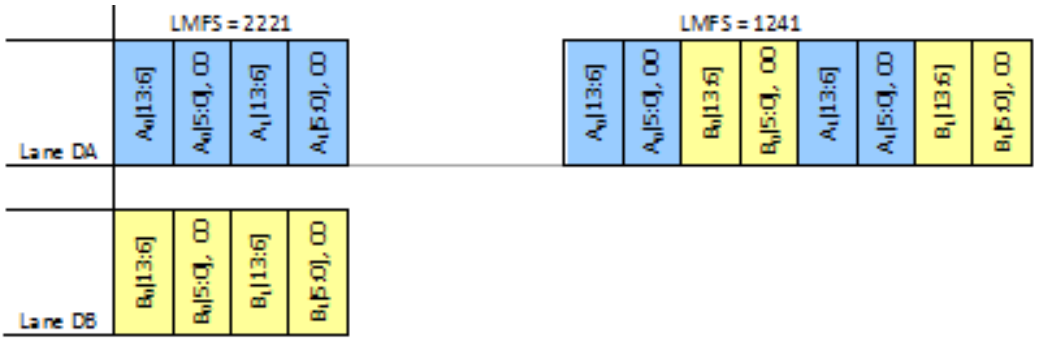

Figure 40. JESD Frame Assembly

Table 3. Configuring 40x Mode

ADDRESS	DATA
2Bh	01h
30h	11h

9.3.5.4 Digital Outputs

The ADC32J4x JESD204B transmitter uses differential CML output drivers. The CML output current is programmable from 5 mA to 20 mA using SPI register settings. The output driver expects to drive a differential 100-Ω load impedance and the termination resistors should be placed as close to the receiver inputs as possible to avoid unwanted reflections and signal distortion. Because the JESD204B employs 8b, 10b encoding, the output data stream is dc-balanced and ac-coupling can be used to avoid the need to match up common-mode voltages between the transmitter and receivers. The termination resistors should be connected to the termination voltage as shown in Figure 41.

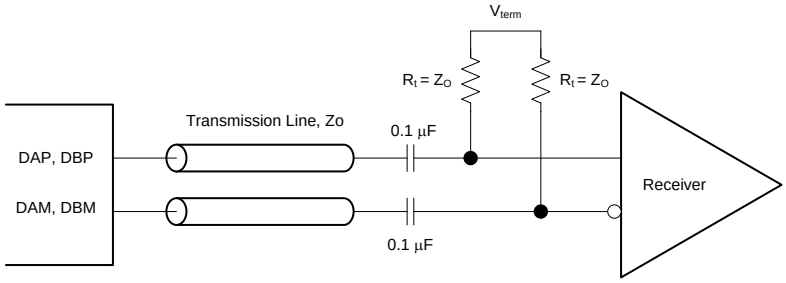

Figure 41. CML Output Connections

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Figure 42 shows the data eye measurements of the device JESD204B transmitter against the JESD204B transmitter mask at 3.125 Gbps (156.25 MSPS, 20x mode), respectively.

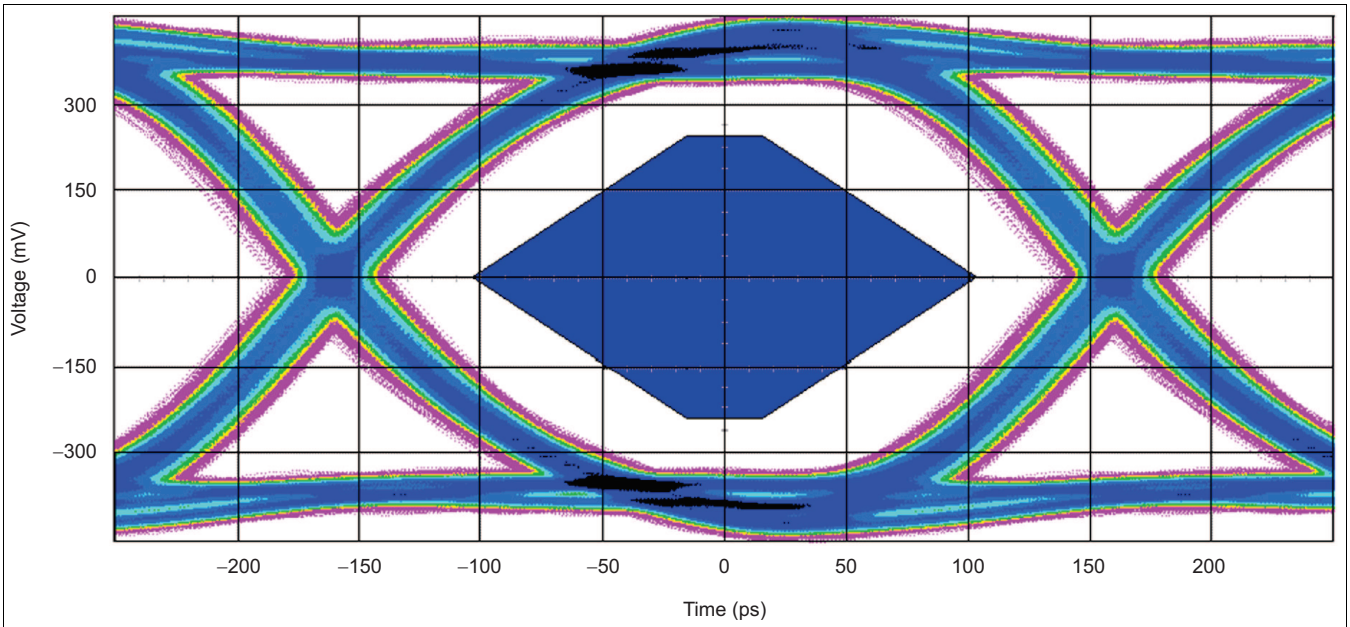

Figure 42. Eye Diagram: 3.125 Gbps

9.4 Device Functional Modes

9.4.1 Digital Gain

The input full-scale amplitude can be selected between 1 V_{PP} to 2 V_{PP} (default is 2 V_{PP}) by choosing the appropriate digital gain setting via an SPI register write. Digital gain provides an option to trade-off SNR for SFDR performance. A larger input full-scale increases SNR performance (2 V_{PP} is recommended for maximum SNR) while reduced input swing typically results in better SFDR performance. Table 4 lists the available digital gain settings.

Table 4. Digital Gain vs Full-Scale Amplitude

DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})
0	2.0
0.5	1.89
1	1.78
1.5	1.68
2	1.59
2.5	1.50
3	1.42
3.5	1.34
4	1.26
4.5	1.19
5	1.12
5.5	1.06
6	1.00

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9.4.2 Overrange Indication

The ADC32J4x provides two different overrange indications. The normal OVR (default) is triggered if the final 14-bit data output exceeds the maximum code value. The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after just nine clock cycles, thus enabling a quicker reaction to an overrange event. By default, the normal overrange indication is output on the OVRA, OVRB pins. The fast OVR indication can be presented on the overrange pins instead by using the SPI register map.

9.5 Programming

The ADC32J4x can be configured using a serial programming interface, as described in this section.

9.5.1 Serial Interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

9.5.1.1 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin (of durations greater than 10 ns), as shown in Figure 43. If required, the serial interface registers can be cleared during operation either:

1. Through a hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.5.1.1.1 Serial Register Write

The device internal register can be programmed with these steps:

1. Drive the SEN pin low,
2. Set the R/W bit to 0 (bit A15 of the 16-bit address),
3. Set bit A14 in the address field to 1,
4. Initiate a serial interface cycle by specifying the address of the register (A13 to A0) whose content must be written, and
5. Write the 8-bit data that are latched in on the SCLK rising edge.

Programming (continued)

Figure 43 and Table 5 show the timing requirements for the serial register write operation.

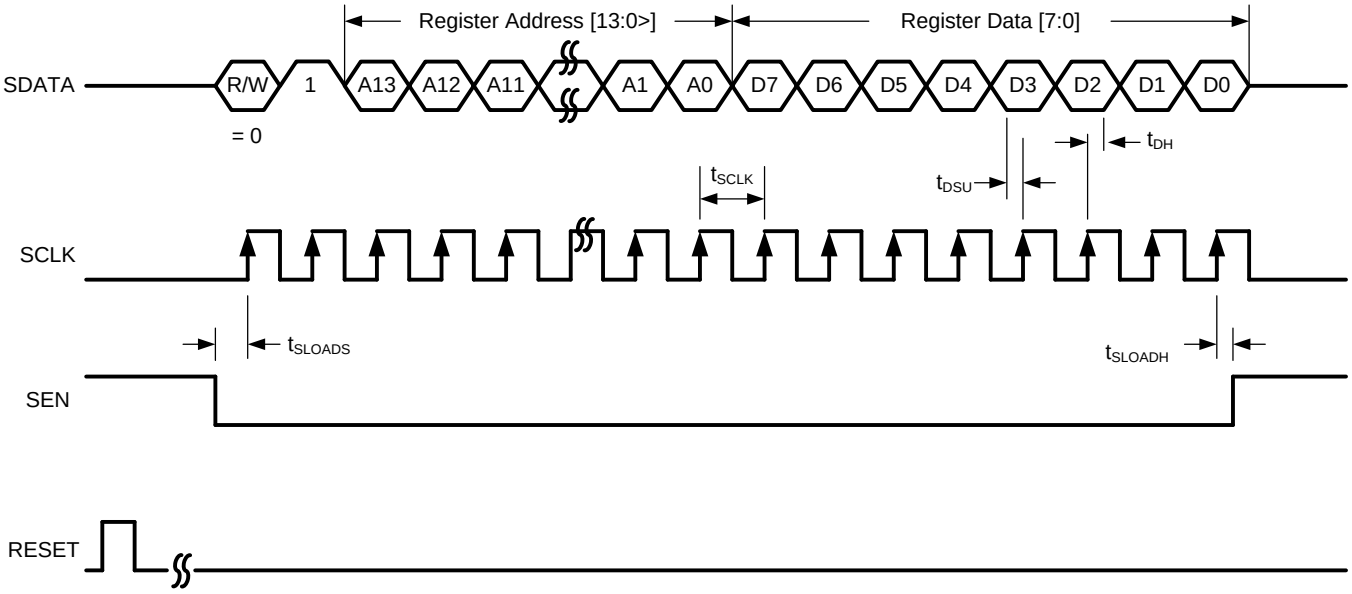

Figure 43. Serial Register Write Timing Diagram

Table 5. Serial Interface Timing(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, and AVDD = DVDD = 1.8 V, unless otherwise noted.

9.5.1.1.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. Given below is the procedure to read contents of serial registers:

1. Drive the SEN pin low.
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Set bit A14 in the address field to 1.
4. Initiate a serial interface cycle specifying the address of the register (A13 to A0) whose content must be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK rising edge.
7. To enable register writes, reset the R/W register bit to 0.

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When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 44 shows a timing diagram of the serial register read operation. Data appear on the SDOUT pin at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in Figure 45.

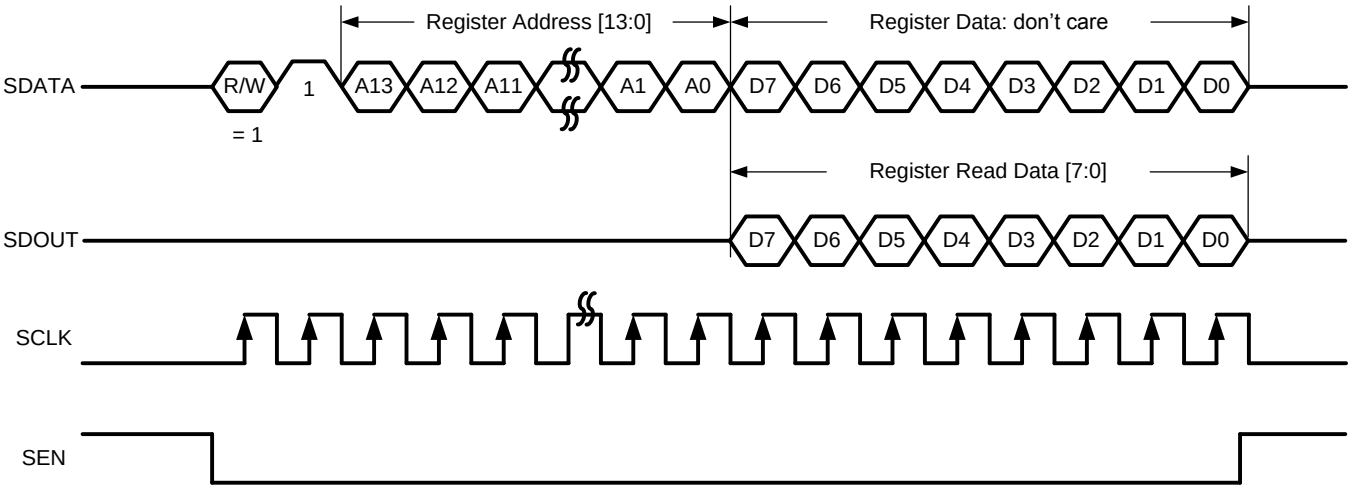

Figure 44. Serial Register Read Timing Diagram

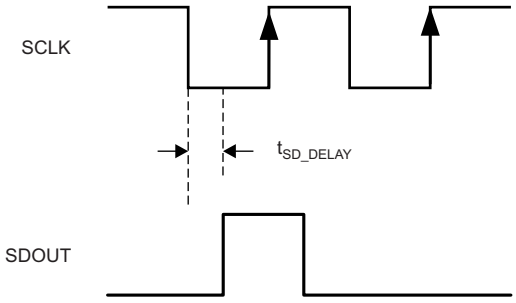

Figure 45. SDOUT Timing Diagram

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9.5.2 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in Figure 46 and Table 6.

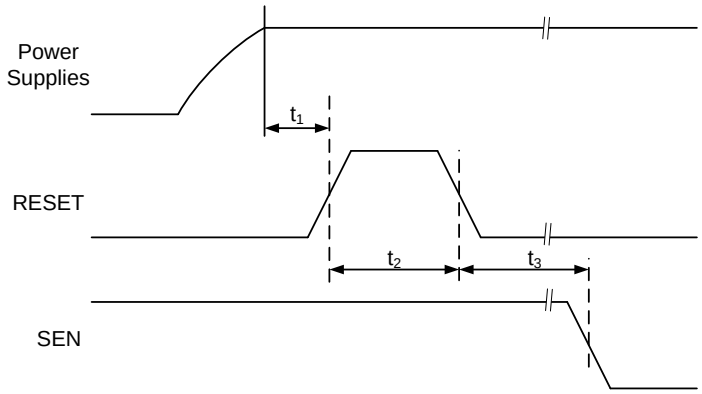

Figure 46. Initialization of Serial Registers after Power-Up

Table 6. Power-Up Timing

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power up to active high RESET pulse	1			ms
t_2	Reset pulse width	Active high RESET pulse width	10		1000	ns
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

If required, the serial interface registers can be cleared during operation either:

1. Through hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.5.3 Start-Up Sequence

After power-up, the sequence described in Table 7 can be used to set up the ADC32J4x for basic operation.

Table 7. Start-Up Settings

STEP	DESCRIPTION	REGISTER ADDRESS AND DATA
1	Supply all supply voltages. There is no required power supply sequence for AVDD and DVDD	—
2	Pulse hardware reset (low to high to low) on pin 24	—
3	Optional configure LMFS of JESD204B interface to LMFS = 1241 (default is LMFS = 2221)	Address 2Bh, data 01h Address 30h, data 11h
4	Pulse SYNC~ from high to low to transmit data from k28.5 sync mode	—

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9.6 Register Maps

Table 8. Register Map Summary

REGISTER ADDRESS	REGISTER DATA							
A[13:0] (Hex)	7	6	5	4	3	2	1	0
01	0	0	DIS DITHER CHA		DIS DITHER CHB		0	0
03	0	0	0	0	0	0	CHA GAINEN	0
04	0	0	0	0	0	0	CHB GAINEN	0
06	0	0	0	0	0	0	TEST PATTERN EN	RESET
07	0	0	0	SPECIAL MODE1 CHA			EN FOVR	0
08	0	0	0	SPECIAL MODE1 CHB			0	0
09	0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
0A	0	0	0	0	CHA TEST PATTERN			
0B	CHB TEST PATTERN				0	0	0	0
0C	0	0	0	0	CHA DIGITAL GAIN			
0D	CHB DIGITAL GAIN				0	0	0	0
0E	CUSTOM PATTERN [13:6]							
0F	CUSTOM PATTERN [5:0]					0	0	0
13	LOW SPEED MODE	0	0	0	0	0	0	0
15	0	CHA PDN	CHB PDN	0	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN
27	CLK DIV		0	0	0	0	0	0
2A	SERDES TEST PATTERN		IDLE SYNC	TRP LAYER TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TXMIT LINKDATA DIS
2B	0	0	0	0	0	0	CTRL K	CTRL F
2F	SCRAMBLE EN	0	0	0	0	0	0	0
30	OCTETS PER FRAME							
31	0	0	0	FRAMES PER MULTIFRAME				
34	SUBCLASSV			0	0	0	0	0
3A	SYNC REG	SYNC REQ EN	0	0	OUTPUT CURRENT SEL			
3B	LINK LAYER TESTMODE SEL [2:0]			LINK LAYER RPAT	0	PULSE DET MODES		
3C	FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	

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Register Maps (continued)

Table 8. Register Map Summary (continued)

REGISTER ADDRESS	REGISTER DATA							
A[13:0] (Hex)	7	6	5	4	3	2	1	0
422	0	0	0	0	0	0	SPECIAL MODE2 CHA	0
434	0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
522	0	0	0	0	0	0	SPECIAL MODE2 CHB	0
534	0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0

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9.6.1 Serial Register Description

Figure 47. Register 01h

7	6	5	4	3	2	1	0
0	0	DIS DITHER CHA		DIS DITHER CHB		0	0

Table 9. Register 01h Description

Name	Description
Bits 7:6	**Must write 0**
Bits 5:4	**DIS DITHER CHA**
	These bits enable or disables the on-chip dither. Control these bits with bits 5 and 3 of register 434h. 00 = Dither enabled 11 = Dither disabled. Improves SNR by 0.4 dB for input frequencies up to 170 MHz.
Bits 3:2	**DIS DITHER CHB**
	These bits enable or disables the on-chip dither. Control these bits with bits 5 and 3 of register 534h. 00 = Dither enabled 11 = Dither disabled. Improves SNR by 0.4 dB for input frequencies up to 170 MHz.
Bits 1:0	**Must write 0**

Figure 48. Register 03h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CHA GAINEN	0

Table 10. Register 03h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**CHA GAINEN: Digital gain enable bit for channel A**
	0 = Digital gain disabled 1 = Digital gain enabled
Bit 0	**Must write 0**

Figure 49. Register 04h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CHB GAINEN	0

Table 11. Register 04h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**CHB GAINEN: Digital gain enable bit for channel B**
	0 = Digital gain disabled 1 = Digital gain enabled
Bit 0	**Must write 0**

Figure 50. Register 06h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TEST PATTERN EN	RESET

Table 12. Register 06h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**TEST PATTERN EN**
	This bit enables the test pattern selection for the digital outputs. 0 = Normal operation 1 = Test pattern output enabled
Bit 0	**RESET: Software reset applied**
	This bit resets all internal registers to the default values and self-clears to 0.

Figure 51. Register 07h

7	6	5	4	3	2	1	0
0	0	0	SPECIAL MODE1 CHA			EN FOVR	0

Table 13. Register 07h Description

Name	Description
Bits 7:5	**Must write 0**
Bits 4:2	**SPECIAL MODE1 CHA**
	010 = For frequencies < 120 MHz 111 = For frequencies > 120 MHz
Bit 1	**EN FOVR**
	0 = Normal OVR on OVRx pins 1 = Enable fast OVR on OVRx pins
Bit 0	**Must write 0**

Figure 52. Register 08h

7	6	5	4	3	2	1	0
0	0	0	SPECIAL MODE1 CHB			0	0

Table 14. Register 08h Description

Name	Description
Bits 7:5	**Must write 0**
Bits 4:2	**SPECIAL MODE1 CHB**
	010 = For frequencies < 120 MHz 111 = For frequencies > 120 MHz
Bits 1:0	**Must write 0**

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Figure 53. Register 09h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT

Table 15. Register 09h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**ALIGN TEST PATTERN**
	This bit aligns test patterns across the outputs of the four channels. 0 = Test patterns of four channels are free running 1 = Test patterns of all 4 channels are aligned
Bit 0	**DATA FORMAT**
	This bit sets the digital output data format. 0 = Twos complement 1 = Offset binary

Figure 54. Register 0Ah

7	6	5	4	3	2	1	0
0	0	0	0	CHA TEST PATTERN			

Table 16. Register 0Ah Description

Name	Description
Bits 7:4	**Must write 0**
Bits 3:0	**CHA TEST PATTERN**
	These bits control the test pattern for channel A after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 10101010101010 and 01010101010101. 0100 = Digital ramp: data increments by 1 LSB every clock cycle from code 0 to 16383. 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 0110 = Deskew pattern: data are 3AAAh. 1000 = PRBS pattern: data are a sequence of pseudo random numbers. 1001 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use

Figure 55. Register 0Bh

7	6	5	4	3	2	1	0
CHB TEST PATTERN				0	0	0	0

Table 17. Register 0Bh Description

Name	Description
Bits 7:4	**CHB TEST PATTERN**
	These bits control the test pattern for channel B after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 10101010101010 and 01010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383. 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 0110 = Deskew pattern: data are 3AAAh. 1000 = PRBS pattern: data are a sequence of pseudo random numbers. 1001 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use
Bits 3:0	**Must write 0**

Figure 56. Register 0Ch

7	6	5	4	3	2	1	0
0	0	0	0	CHA DIGITAL GAIN			

Table 18. Register 0Ch Description

Name	Description
Bits 7:4	**Must write 0**
Bits 3:0	**CHA DIGITAL GAIN**
	These bits set the digital gain for individual channels. For register settings see Table 19.

Table 19. Channel Digital Gain

REGISTER VALUE	DIGITAL GAIN (dB)	MAXIMUM INPUT VOLTAGE (V_{PP})
0000	0	2.0
0001	0.5	1.89
0010	1	1.78
0011	1.5	1.68
0100	2	1.59
0101	2.5	1.50
0110	3	1.42
0111	3.5	1.34
1000	4	1.26
1001	4.5	1.19
1010	5	1.12
1011	5.5	1.06
1100	6	1.00

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Figure 57. Register 0Dh

7	6	5	4	3	2	1	0
CHB DIGITAL GAIN				0	0	0	0

Table 20. Register 0Dh Description

Name	Description
Bits 7:4	**CHB DIGITAL GAIN**
	These bits set the digital gain for the individual channels. For register settings see Table 19.
Bits 3:0	**Must write 0**

Figure 58. Register 0Eh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[13:6]							

Table 21. Register 0Eh Description

Name	Description
Bits 7:0	**CUSTOM PATTERN[13:6]**
	These bits set the custom pattern (13:6) for all channels.

Figure 59. Register 0Fh

7	6	5	4	3	2	1	0
CUSTOM PATTERN (5:0)						0	0

Table 22. Register 0Fh Description

Name	Description
Bits 7:2	**CUSTOM PATTERN[5:0]**
	These bits set the custom pattern (5:0) for all channels.
Bits 1:0	**Must write 0**

Figure 60. Register 13h

7	6	5	4	3	2	1	0
LOW SPEED MODE	0	0	0	0	0	0	0

Table 23. Register 13h Description

Name	Description
Bit 7	**LOW SPEED MODE**
	Use this bit for sampling frequencies < 25 MSPS. 0 = Normal operation 1 = Low-speed mode is enabled
Bits 6:0	**Must write 0**

Figure 61. Register 15h

7	6	5	4	3	2	1	0
0	CHA PDN	CHB PDN	0	STANDBY	GLOBAL PDN	0	PDN PIN DISABLE

Table 24. Register 15h Description

Name	Description
Bit 7	**Must write 0**
Bit 6	**CHA PDN: Power-down channel A**
	0 = Normal operation 1 = Power-down channel A if PDN PIN DISABLE register bit is set
Bit 5	**CHB PDN: Power-down channel B**
	0 = Normal operation 1 = Power-down channel B if PDN PIN DISABLE register bit is set
Bit 4	**Must write 0**
Bit 3	**STANDBY: ADCs of both channels enter standby**
	0 = Normal operation 1 = Standby
Bit 2	**GLOBAL PDN: Global power-down**
	0 = Normal operation 1 = Global power-down
Bit 1	**Must write 0**
Bit 0	**PDN PINDISABLE**
	This bit disables the power-down control from the pin. 0 = Normal operation 1 = Power-down pin is disabled, register settings should be used for power-down operations

Figure 62. Register 27h

7	6	5	4	3	2	1	0
CLK DIV		0	0	0	0	0	0

Table 25. Register 27h Description

Name	Description
Bits 7:6	**CLK DIV: Internal clock divider for the input sample clock**
	00 = Clock divider bypassed 01 = Divide-by-1 10 = Divide-by-2 11 = Divide-by-4
Bits 5:0	**Must write 0**

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Figure 63. Register 2Ah

7	6	5	4	3	2	1	0
SERDES TEST PATTERN		IDLE SYNC	TRP LAYER TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TX LINK CONFIG DATA DIS

Table 26. Register 2Ah Description

Name	Description
Bits 7:6	**SERDES TEST PATTERN**
	00 = Normal operation 01 = Outputs clock pattern: output is 10101010 pattern 10 = Encoded pattern: output is 1111111100000000 11 = PRBS sequence: output is $2^{15} – 1$
Bit 5	**IDLE SYNC**
	This bit sets the output pattern when SYNC is high. 0 = Sync code is k28.5 (0xBCBC) 1 = Sync code is 0xBC50
Bit 4	**TRP LAYER TESTMODE EN**
	This bit generates the long transport layer test pattern mode according to 5.1.6.3 clause of the JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled
Bit 3	**FLIP ADC DATA**
	0 = Normal operation 1 = Output data order is reversed: MSB – LSB
Bit 2	**LANE ALIGN**
	This bit inserts a lane alignment character (K28.3) for the receiver to align to the lane boundary per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts lane alignment characters
Bit 1	**FRAME ALIGN**
	This bit inserts a frame alignment character (K28.7) for the receiver to align to the lane boundary per section 5.3.3.4 of the JESD204B specification. 0 = Normal operation 1 = Inserts frame alignment characters
Bit 0	**TX LINK CONFIG DATA DIS**
	This bit disables sending the initial link alignment (ILA) sequence when SYNC is de-asserted. 0 = Normal operation 1 = ILA disabled

Figure 64. Register 2Bh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CTRL K	CTRL F

Table 27. Register 2Bh Description

Name	Description
Bit 7:2	**Must write 0**
Bit 1	**CTRL K: Enable bit for number of frames per multiframe**
	0 = Default is 9 (20x mode) frames per multiframe 1 = Frames per multiframe can be set in register 31h
Bit 0	**CTRL F: Enable bit for number of octets per frame**
	0 = 20x mode using one lane per ADC (default is F = 2) 1 = Octets per frame can be specified in register 30h

Figure 65. Register 2Fh

7	6	5	4	3	2	1	0
SCRAMBLE EN	0	0	0	0	0	0	0

Table 28. Register 2Fh Description

Name	Description
Bit 7	**SCRAMBLE EN: Scramble enable bit in the JESD204B interface**
	0 = Scrambling disabled 1 = Scrambling enabled
Bit 6:0	**Must write 0**

Figure 66. Register 30h

7	6	5	4	3	2	1	0
OCTETS PER FRAME							

Table 29. Register 30h Description

Name	Description
Bits 7:0	**OCTETS PER FRAME**
	These bits set the number of octets per frame (F). 01 = 20x Serialization: two octets per frame 11 = 40x Serialization: four octets per frame

Figure 67. Register 31h

7	6	5	4	3	2	1	0
0	0	0	FRAMES PER MULTI FRAME				

Table 30. Register 31h Description

Name	Description
Bits 7:5	**Must write 0**
Bits 4:0	**FRAMES PER MULTI FRAME**
	These bits set the number of frames per multiframe. After reset, the default settings for frames per multiframe are: 20x mode: K = 8 For each mode, K should not be set to a lower value.

Figure 68. Register 34h

7	6	5	4	3	2	1	0
SUBCLASSV			0	0	0	0	0

Table 31. Register 34h Description

Name	Description
Bits 7:5	**SUBCLASSV: JESD204B subclass setting**
	000 = Subclass 0 backward compatibility with JESD204A 001 = Subclass 1 deterministic latency using SYSREF signal 010 = Subclass 2 deterministic latency using SYNC detection
Bits 4:0	**Must write 0**

Figure 69. Register 3Ah

7	6	5	4	3	2	1	0
SYNC REQ	SYNC REQ EN	0	0	OUTPUT CURRENT SEL			

Table 32. Register 3Ah Description

Name	Description	
Bit 7	**SYNC REQ**	
	This bit generates a synchronization request only when the SYNC REQ EN register bit is set. 0 = Normal operation 1 = Generates sync request	
Bit 6	**SYNC REQ EN**	
	0 = Sync request is made with the SYNCP~, SYNCM~ pins 1 = Sync request is made with the SYNC REQ register bit	
Bits 5:4	**Must write 0**	
Bits 3:0	**OUTPUT CURRENT SEL: JESD output buffer current selection**	
	0000 = 16 mA 0001 = 15 mA 0010 = 14 mA 0011 = 13 mA 0100 = 20 mA 0101 = 19 mA 0110 = 18 mA 0111 = 17 mA	1000 = 8 mA 1001 = 7 mA 1010 = 6 mA 1011 = 5 mA 1100 = 12 mA 1101 = 11 mA 1110 = 10 mA 1111 = 9 mA

Figure 70. Register 3Bh

7	6	5	4	3	2	1	0
LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		

Table 33. Register 3Bh Description

Name	Description
Bits 7:5	**LINK LAYER TESTMODE**
	These bits generate a pattern according to clause 5.3.3.8.2 of the JESD204B document. 000 = Normal ADC data 001 = D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed frequency jitter pattern) 011 = Repeat initial lane alignment (generates K28.5 character and repeat lane alignment sequences continuously) 100 = 12 octet RPAT jitter pattern
Bit 4	**LINK LAYER RPAT**
	This bit changes the running disparity in the modified RPAT pattern test mode (only when link layer test mode = 100). 0 = Normal operation 1 = Changes disparity
Bit 3	**Must write 0**
Bits 2:0	**PULSE DET MODES**
	These bits select different detection modes for SYSREF (subclass 1) and SYNC (subclass2). For register settings see Table 34.

Table 34. PULSE DET MODES Register Settings

D2	D1	D0	FUNCTIONALITY
0	Don't care	0	Allow all pulses to reset input clock dividers
1	Don't care	0	Do not allow reset of analog clock dividers
Don't care	0 to 1 transition	1	Allow one pulse immediately after the 0 to1 transition to reset the divider

Figure 71. Register 3Ch

7	6	5	4	3	2	1	0
FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILAN SEQ	

Table 35. Register 3Ch Description

Name	Description
Bits 7	**FORCE LMFC COUNT**
	0 = Normal operation 1 = Enables using different starting value for LMFC counter
Bits 6:2	**LMFC COUNT INIT**
	If SYSREF is transmitted to the digital block, the LMFC count resets to 0 and K28.5 stops transmitting when the LMFC count reaches 31. The initial value that the LMFC count resets to can be set using LMFC COUNT INIT. In this manner, the Rx can be synchronized early because the Rx receives the LANE ALIGNMENT SEQUENCE early. The FORCE LMFC COUNT register bit must be enabled.
Bit 1:0	**RELEASE ILAN SEQ**
	These bits delay the lane alignment sequence generation by 0, 1, 2, or 3 multiframes after the code group synchronization. 00 = 0 01 = 1 10 = 2 11 = 3

Figure 72. Register 422h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SPECIAL MODE2 CHA	0

Table 36. Register 422h Description

Name	Description
Bits 7:2	**Must write 0**
Bit 1	**SPECIAL MODE2 CHA**
	Always write 1 for improved HD2 performance.
Bit 0	**Must write 0**

Figure 73. Register 434h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0

Table 37. Register 434h Description

Name	Description
Bits 7:6	**Must write 0**
Bits 5	**DIS DITH CHA**
	Set this bit along with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bit 4	**Must write 0**
Bit 3	**DIS DITH CHA**
	Set this bit along with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bits 2:0	**Must write 0**

Figure 74. Register 522h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SPECIAL MODE2 CHB	0

Table 38. Register 522h Description

Name	Description
Bits 7:2 and	**Must write 0**
Bit 1	**SPECIAL MODE2 CHB**
	Always write 1 for better HD2 performance
Bit 0	**Must write 0**

Figure 75. Register 534

7	6	5	4	3	2	1	0
0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0

Table 39. Register Description

Name	Description
Bits 7:6	**Must write 0**
Bits 5	**DIS DITH CHB**
	Set this bit along with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
Bit 4	**Must write 0**
Bit 3	**DIS DITH CHB**
	Set this bit along with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
	Must write 0

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10 Application and Implementation

10.1 Application Information

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 250 MHz to achieve good phase and amplitude balances at ADC inputs. While designing the dc driving circuits, the ADC input impedance must be considered. Figure 76 and Figure 77 show the impedance (Z_{in} = R_{in} || C_{in}) across the ADC input pins.

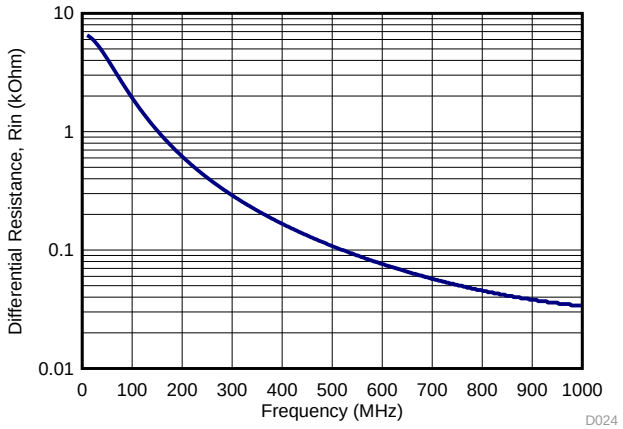


Figure 76. Differential Input Resistance, R_{IN}

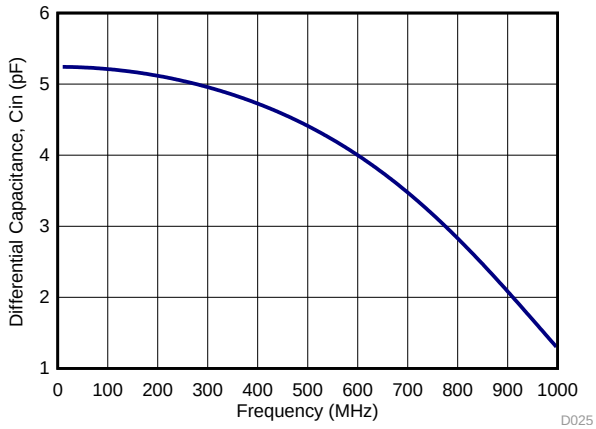


Figure 77. Differential Input Capacitance, C_{IN}

10.2 Typical Applications

10.2.1 Driving Circuit Design: Low Input Frequencies

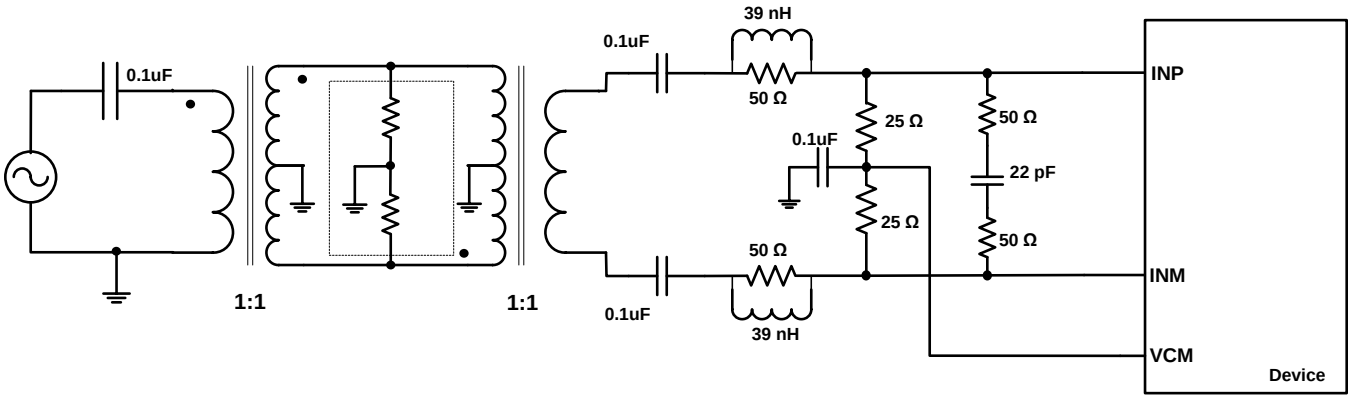


Figure 78. Driving Circuit for Low Input Frequencies

10.2.1.1 Design Requirements

For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitics. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

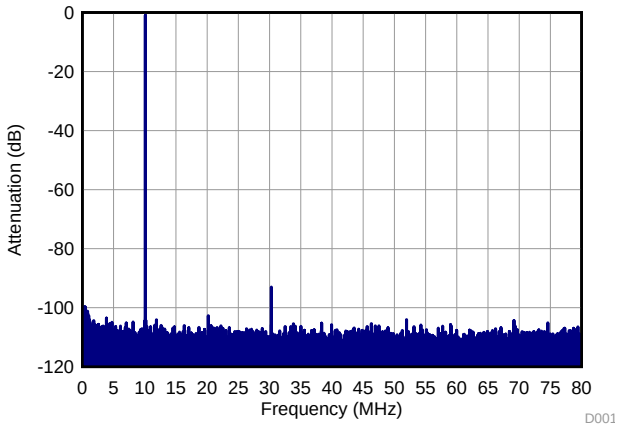
10.2.1.2 Detailed Design Procedure

A typical application using two back-to-back coupled transformers is illustrated in Figure 78. The circuit is optimized for low input frequencies. An external R-C-R filter using 50-Ω resistors and a 22-pF capacitor is used. With the series inductor (39 nH), this combination helps absorb the sampling glitches.

Typical Applications (continued)

10.2.1.3 Application Curves

Figure 79 shows the performance obtained by using the circuit shown in Figure 78.



f_S = 160 MSPS SNR = 72.8 dBFS
f_{IN} = 10 MHz SFDR = 91 dBc

Figure 79. Performance FFT at 10 MHz (Low Input Frequency)

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Typical Applications (continued)

10.2.2 Driving Circuit Design: Input Frequencies Between 100 MHz to 230 MHz

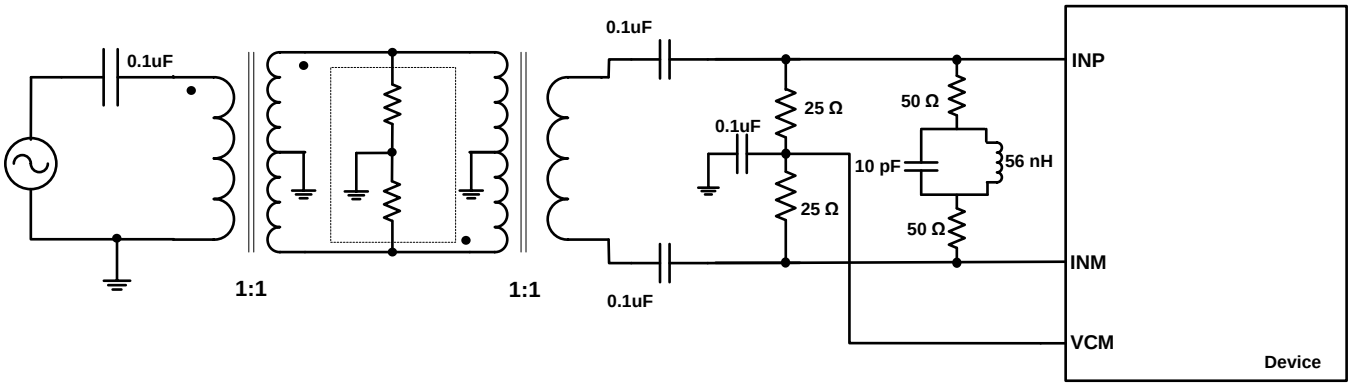


Figure 80. Driving Circuit for Mid-Range Input Frequencies (100 MHz < f_{IN} < 230 MHz)

10.2.2.1 Design Requirements

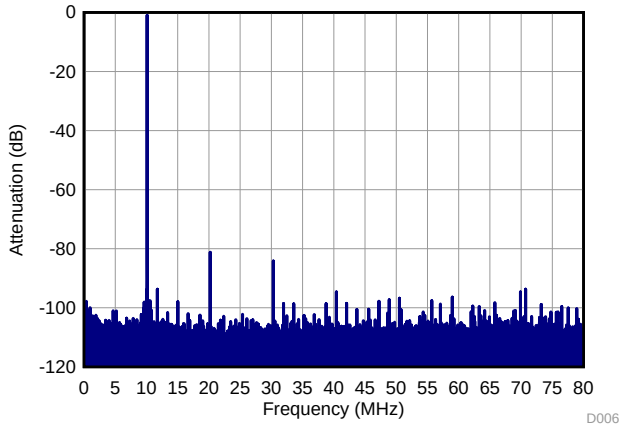
See the *Design Requirements* section for further details.

10.2.2.2 Detailed Design Procedure

When input frequencies are between 100 MHz to 230 MHz, an R-LC-R circuit can be used to optimize performance, as shown in Figure 80.

10.2.2.3 Application Curve

Figure 81 shows the performance obtained by using the circuit shown in Figure 80.



f_S = 160 MSPS SNR = 70.3 dBFS
f_{IN} = 170 MHz SFDR = 81 dBc

Figure 81. Performance FFT at 170 MHz (Mid Input Frequency)

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Typical Applications (continued)

10.2.3 Driving Circuit Design: Input Frequencies Greater than 230 MHz

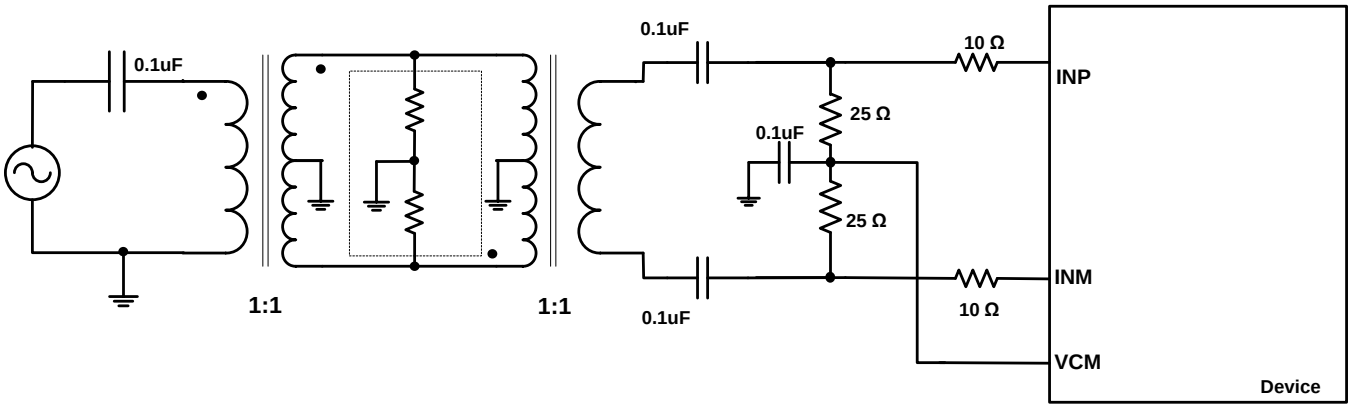

Figure 82. Driving Circuit for High Input Frequencies (f_{IN} > 230 MHz)

10.2.3.1 Design Requirements

See the *Design Requirements* section for further details.

10.2.3.2 Detailed Design Procedure

For high input frequencies (> 230 MHz), using the R-C-R or R-LC-R circuit does not show significant improvement in performance. However, a series resistance of 10 Ω can be used as shown in Figure 82.

10.2.3.3 Application Curve

Figure 83 shows the performance obtained by using the circuit shown in Figure 82.

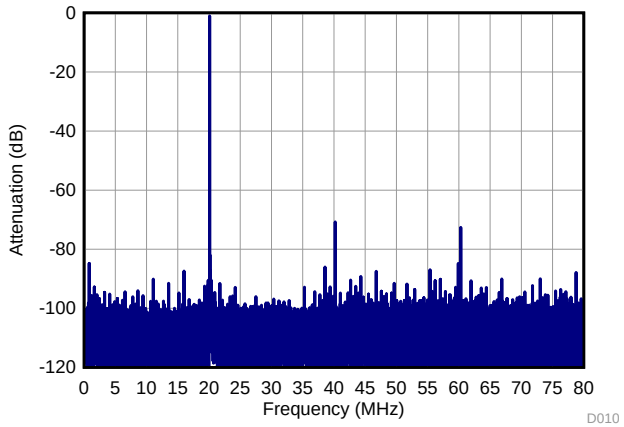

Figure 83. Performance FFT at 500 MHz (High Input Frequency)

11 Power-Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD can power up in any order.

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12 Layout

12.1 Layout Guidelines

The ADC32J4x EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 84. Some important points to remember while laying out the board are:

1. Analog inputs are located on opposite sides of the device pin out to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs should exit the pin out in opposite directions, as shown in the reference layout of Figure 84 as much as possible.
2. In the device pin out, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 84 as much as possible.
3. Digital outputs should be kept away from the analog inputs. When these digital outputs exit the pin out, the digital output traces should not be kept parallel to the analog input traces because this configuration may result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] should be matched in length to avoid skew among outputs.
4. At each power-supply pin (AVDD and DVDD), a 0.1-µF decoupling capacitor should be kept close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

12.2 Layout Example

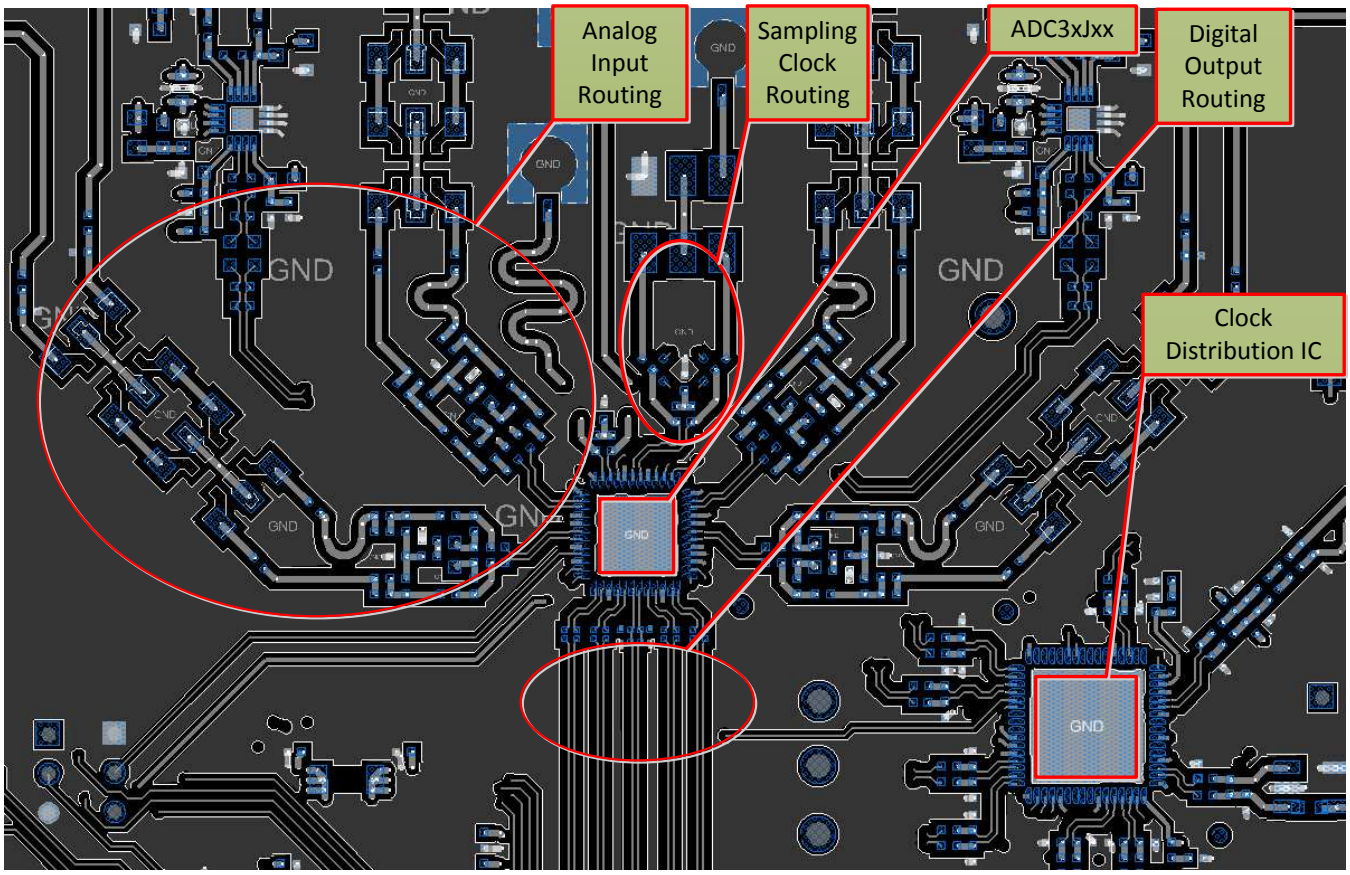


Figure 84. Typical Layout of the ADC32J4x Board

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 40. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADC32J42	Click here	Click here	Click here	Click here	Click here
ADC32J43	Click here	Click here	Click here	Click here	Click here
ADC32J44	Click here	Click here	Click here	Click here	Click here
ADC32J45	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

PowerPAD is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC32J42IRGZR	PREVIEW	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J42	
ADC32J42IRGZT	PREVIEW	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J42	
ADC32J42RGZT	PREVIEW	VQFN	RGZ	48		TBD	Call TI	Call TI	-40 to 85		
ADC32J43IRGZR	PREVIEW	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J43	
ADC32J43IRGZT	PREVIEW	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J43	
ADC32J44IRGZR	PREVIEW	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J44	
ADC32J44IRGZT	PREVIEW	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J44	
ADC32J45IRGZR	PREVIEW	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J45	
ADC32J45IRGZT	PREVIEW	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ32J45	
PADC32J45IRGZT	PREVIEW	VQFN	RGZ	48	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

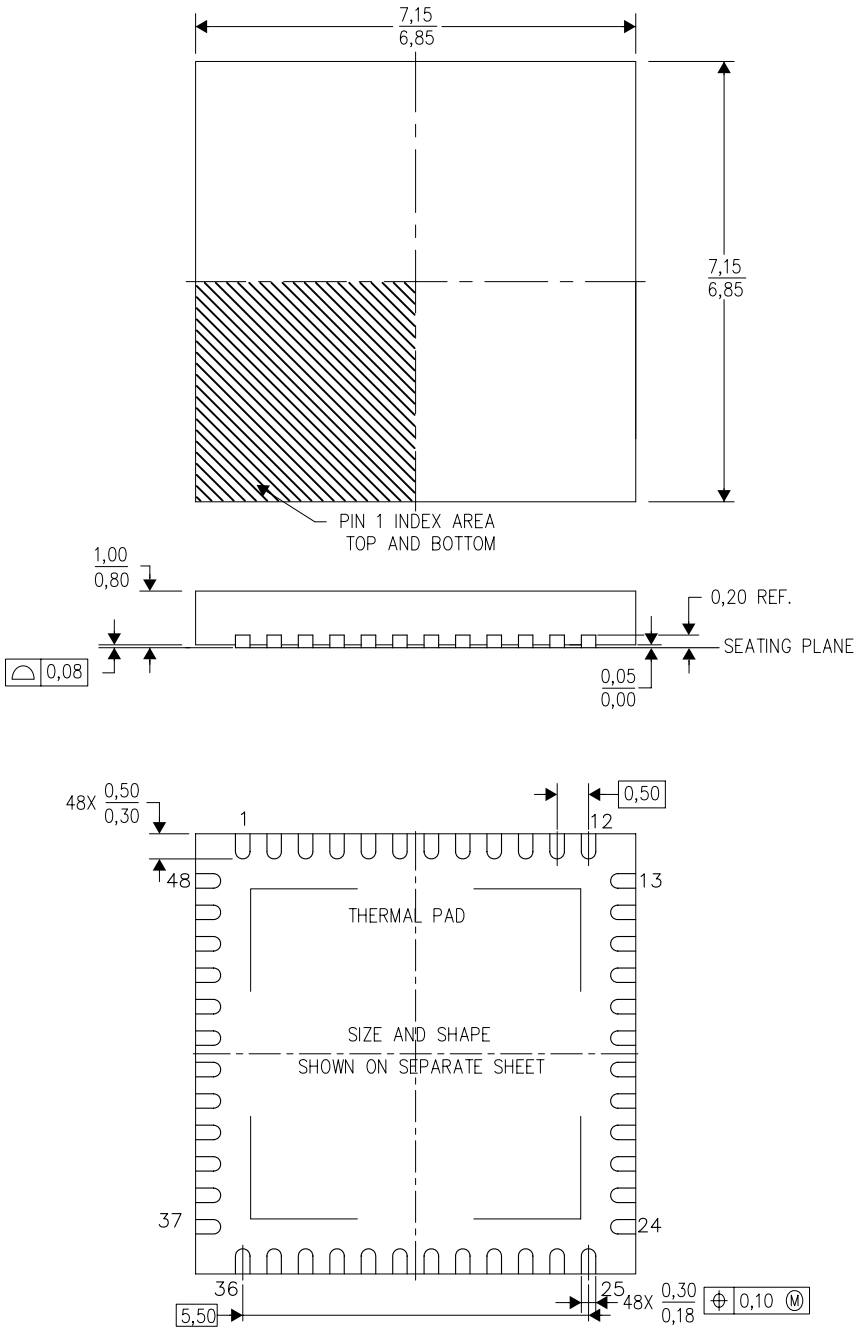
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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