8-Ch, 24-Bit Simultaneous Sampling ADC

Preliminary Technical Data

AD7779

FEATURES

- 8 Channel 24-Bit Simultaneous Sampling ADCs
- Sample Rate Converter (SRC) for coherent sampling
- Adjustable Phase Synchronization
- PGA per Channel (gain 1, 2, 4, 8)
- Low Input Bias Current: 4nA
- Single Ended or True Differential Inputs
- 16ksps Output Data Rate/per channel
- Internal 2.5V reference
- Optimize Power Dissipation & Performance
- Two Power Modes:
  - High Resolution Mode
  - Low Power Mode
- Programmable Output Data Rates & Bandwidth
- Low Latency Sinc3 Filter Path
- Low Resolution SAR ADC for System and Chip Diagnostics

POWER SUPPLY

- Bipolar (±1.65V Supply) or Unipolar (3.3V Supply) Supply
- Digital/IO Supply 1.8V to 3.6V
- Performance Temperature range: –40°C to +105°C
- Functional Temperature range: –40°C to +125°C

PERFORMANCE

- Combined AC & DC Performance
- 112dB SNR/Dynamic Range at 8 kSPS in High precision mode
- -108dB THD
- ±15ppm INL, ±250 uV Offset Error, ±0.1% Gain Error
- ±5 ppm/°C typ Internal Reference TempCo

APPLICATIONS

- Circuit Breakers Applications
- General Purpose Data Acquisition Applications
- EEG Applications
- Industrial Process Control Applications

FUNCTIONAL BLOCK DIAGRAM

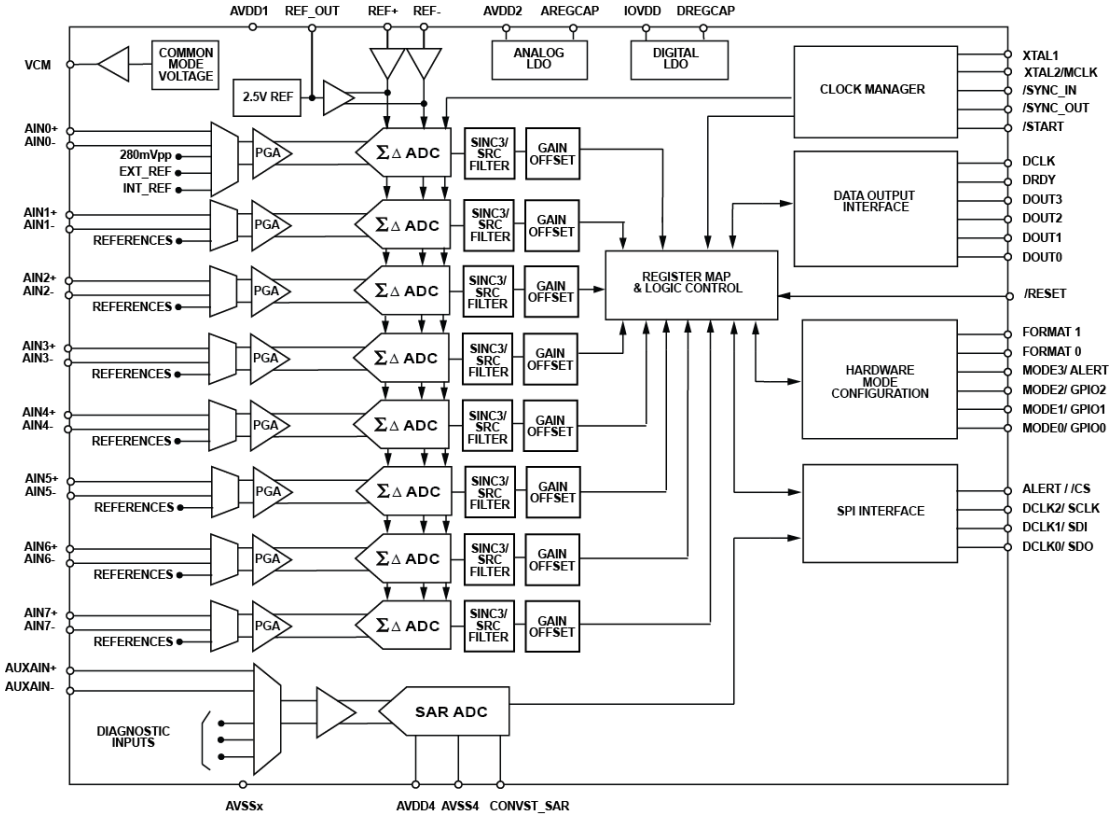

Figure 1 AD7779 Functional Block Diagram

Rev. PrD

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GENERAL DESCRIPTION

The AD7779 is an 8-channel simultaneously sampled, Analog-to-Digital Converter. There are 8 full Sigma Delta ADCs on-chip. The AD7779 provides a high input impedance of 10 MOhms to allow for direct sensor connection. Each input channel has a programmable gain stage catering for gains of 1,2,4,8 to map lower amplitude sensor outputs into the Full Scale ADC input range to maximize the Dynamic Range of the signal chain. The Analog inputs can accept unipolar 0 to 2.5V or true bipolar ±1.25V analog input signals with 3.3V or ±1.65V Analog Supply voltages respectively. The Analog inputs can be configured to accept True Differential or Single-Ended signals to match different sensor output configurations.

Each channel contains an ADC modulator and Sinc 3 low latency digital filter. A Sample Rate Converter (SRC) is provided to allow fine resolution control over the AD7779 Output Data Rate (ODR). This can be used in application where the ODR resolution is required to maintain coherency with 0.01Hz changes in the line frequency. The SRC can be programmed through the SPI interface. The AD7779 implements two different interfaces, Data Output Interface and a SPI control Interface. The ADC Data Output interface is dedicated to transmitting the ADC conversion results from the AD7779 to the processor. The SPI interface is used to write to and read from the AD7779 configuration registers and for the control and reading of data from the SAR ADC. The SPI interface can also be configure to output the sigma delta conversion data.

The AD7779 includes a 12-Bit SAR ADC. This ADC can be used for AD7779 diagnostics without having to decommission one of the Sigma Delta ADC channels dedicated to system measurement functions. With the use of an external multiplexer and signal conditioning, the SAR ADC can be used to validate the Sigma Delta ADC measurements in applications where Functional Safety is required. In addition, the AD7779 offers three GPIOs that can be used to control an external multiplexer, and an internal multiplexer to sense internal nodes.

The AD7779 contains a 2.5V reference and reference buffer. The reference has a temperature co-efficient of 20 ppm/°C max.

The AD7779 offers two modes of operation: High Resolution Mode and Low Power Mode. The High Resolution mode provides higher dynamic range while consuming 13 mW/ch and the Low Power mode consumes just 5 mW/ch at a reduced dynamic range specification.

The specified operating temperature range is -40°C to +105°C, while the part is operational up to +125°C

SPECIFICATIONS

AVDD1x/AVSSx = ±1.65V, 3.3V/AGND, AVDD2 - AVSSx = 2.2 V to 3.6V; IOVDD = 2.3V to 3.6V; DGND = 0V, REF = 2.5 V internal/external, MCLK = 8192 kHz for High Resolution Mode and 4096 kHz for Low Power Mode, ODR = 16 kHz High Resolution (HR) Mode, ODR = 4 kHz Low Power (LP) Mode; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1. Specification Table

Parameter	Test Conditions Comment	Min	Typ	Max	Unit
ANALOG INPUTS					
Differential Input Voltage Range	VREF = (REF+ − REF−)			±VREF/PGA_{GAIN}	V
Single-Ended Input Voltage Range				0 to VREF/ PGA_{GAIN}	V
Common-Mode Input Range		AVSS1 +0.10	(AVDD1−AVSS)/2	AVDD1 – 0.10	V
Absolute AIN Voltage Limits		AVSSx +0.10		AVDD 1– 0.10	
DC Input Current	HP, MCLK=8192 kHz		±4		nA
	LP, MCLK=4096 kHz		±1.5		nA
DC Differential Input current	HP, MCLK=8192 kHz		±1.5		nA
	LP, MCLK=4096 kHz		±0.6		nA
Input Current Drift			TBD		nA/°C
AC Input Capacitance			8		pF
PGA					
Gain Settings			1,2,4,8		
Gain drift			±3		ppm/°C
Bandwidth	Small Signal			6	kHz
	Large Signal HR Mode			4	kHz
	Large Signal LP Mode			1	kHz
REFERENCE					
INTERNAL					
Output Voltage	REF_OUT	−0.2%	2.5	+0.2%	V
Initial Accuracy	T_A = 25°C	−5mV	REF_OUT	+5mV	V
Temperature Coefficient			±5		ppm/°C
Reference Load Current	I_L	−10		+10	mA
DC Power Supply Rejection	(Line Regulation)		95		dB
Load Regulation	$\Delta V_{OUT}/\Delta I_L$		100		µV/mA
Voltage Noise	$e_{N\ p-p}$, 0.1 Hz to 10 Hz		6.8		µVrms
Voltage Noise Density	e_N 1kHz,2.5V Reference		273.5		nV/√Hz
Turn-On Settling Time	100nF		1.5		ms
Long-Term Stability	1000 hours		TBD		ppm
EXTERNAL					
Input Voltage	REFIN = (REF+) – (REF−)	1	2.5V	AVDD1x	V
Buffer Headroom		AVSSx + 0.1		AVDD1x – 0.1	
REF− Input Voltage			AVSSx	AVDD1x–REFx+	V
Average REFx Current	Current per Channel				
	REF BUF DISABLED, HR mode		18		µA/V
	REF BUF PRE-Q, HR mode		200		nA/V
	REF BUF DISABLED, LP mode		4.5		µA/V
	REF BUF PRE-Q, LP mode		100		nA/V
	REF BUF ENABLED		120		nA/V
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+105	°C
Functional	T_{MIN} to T_{MAX}	−40		+125	°C

Parameter	Test Conditions Comment	Min	Typ	Max	Unit
TEMPERTAURE SENSOR					
Accuracy			±2		°C
DIGITAL FILTER RESPONSE (SINC 3)					
Group Delay			See CRC details		
Settling Time			See CRC details		
Pass-Band	−0.1 dB		See CRC details		
	−3 dB		See CRC details		
Decimation Rate	Hi Resolution	128		4095.99	
	Low Power	64		4095.99	
CLOCK SOURCE					
Frequency	High Resolution Mode	TBD		8.192	MHz
	Low Power Mode	TBD		4.096	
Input Low Voltage, V_{IL}	XTAL1			0.4	V
	XTAL2				
Input High Voltage, V_{IH}	XTAL1	TBD			V
	XTAL2				
Duty Cycle		45:55	50:50	55:45	%
Input Current		−10		+10	µA
ΣΔ ADC					
SPEED & PERFORMANCE					
Resolution		24			Bits
Output Data Rate (ODR)	High Resolution Mode			16	kSPS
	Low Power Mode			8	kSPS
No Missing Codes		24			Bits
Noise	Shorted input				
	High Resolution Mode		90		nV/√ Hz
	Low Power Mode		250		nV/√ Hz
AC ACCURACY					
Dynamic Range	Shorted inputs, Gain =1				dB
	16kSPS, High Resolution Mode		108		
	4KSPS, High Resolution Mode		116		
	4KSPS, Low Power Mode		106		
	1KSPS, Low Power Mode		116		
THD	HR		-109		dB
	LP		-105		dB
SINAD	f_{IN} = 60 Hz		106		dB
SFDR			107		dB
IMD	f_A = 50 Hz, f_B = 51 Hz, HR		125		dB
	f_A = 50 Hz, f_B = 51 Hz, LP		105		
DC Power Supply Rejection	AVDD1x = 3.3V		-90		dB
DC Common Mode Rejection Ratio		80			dB
Crosstalk	Up to 2 kHz input. Reference Buffer Full mode		-110		dB
DC ACCURACY					
Integral Nonlinearity	End Point Method		±7	±15	ppm of FSR
Offset Error			±40	±250	µV
Offset Error Drift			±0.5		µV/°C

Parameter	Test Conditions Comment	Min	Typ	Max	Unit
	Versus Time		TBD		nV/1000 hrs
Offset Matching			30		µV
Gain Error	PGA_{GAIN} = 1		±0.1		%FS
Gain Drift vs. Temperature			150		ppm/°C
Gain Matching			±0.1		%
SAR ADC					
SPEED & PERFORMANCE					
Resolution			12		Bits
Analog Input Range		AVSS4+0.1		AVDD4-0.1	V
Analog Input Common Mode Range	AVDD4 = 3.3V, AVSS4 = 0V	AVSS4+0.1	(AVDD4-AVSS4)/2	AVDD4-0.1	V
Analog Input Leakage Current			±10		nA
Throughput			256		kSPS
DC ACCURACY	Differential Mode				
INL			1.5		LSB
DNL	No Missing codes (12 bit)		1		LSB
Offset			0.6		LSB
Gain			12		LSB
TUE	Differential Mode		TBD		LSB
AC PERFORMANCE					
SNR	1 kHz		66		dB
THD	1 kHz		-83		dB
VCM PIN					
Output			(AVDD1−AVSS)/2		V
Load Current	I_L		1		mA
Load Regulation	$\Delta V_{OUT}/\Delta I_L$		12		µV/mA
Short Circuit Current			5		mA
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.65V≤ IOVDD ≤1.95V	0.65×IOVDD			V
	2.3V≤ IOVDD ≤3.6V	0.7× IOVDD			V
Input Low Voltage, V_{INL}	1.65V≤ IOVDD ≤1.95V			0.35× IOVDD	V
	2.3V≤ IOVDD ≤3.6V			0.4	V
Hysteresis[2]			0.2		%
	IOVDD <2.7V		0.1		%
Input Currents		-10		+10	µA
LOGIC OUTPUT (DOUT/$\overline{RDY}$, DCLK, SDOUT, GPIO)					
Output High Voltage, V_{OH}	IOVDD ≥ 3V, I_{SOURCE} = 1mA	0.8× IOVDD			V
	2.3≤IOVDD< 3V, I_{SOURCE} 500µA	0.8× IOVDD			V
	IOVDD <2.3V, I_{SOURCE} = 200µA	0.8× IOVDD			V
Output Low Voltage, V_{OL}	IOVDD ≥3V, I_{SINK} 2mA			0.4	V
	2.3≤IOVDD <3V, I_{SINK} 1mA			0.4	V
	IOVDD < 2.3V, I_{SINK} 100µA			0.4	V
Leakage Current	Floating State	-10		+10	µA
Output Capacitance	Floating State		10		pF
ΣΔ Data Output Coding			2s Comp		
SAR Data Output Coding			Binary		

Parameter	Test Conditions Comment	Min	Typ	Max	Unit
POWER SUPPLIES	All ΣΔ Channels Enabled				
AVDD1x – AVSS		3.0		3.6	V
I_AVDD1x[12]	Reference Buffer Pre-Q , VCM Enable, Internal reference Enable				
	HR		17		mA
	LP		4.5		mA
	Reference Buffer Enable, VCM Enabled, Internal reference Enabled				
	HR		19		mA
	LP		5		mA
	Reference Buffer Disable, VCM disabled, Internal reference Disabled				
	HR		13		mA
	LP		3.5		mA
AVDD2 – AVSS		2.2		3.6	V
I_AVDD2	HR		9		mA
	LP		3.5		mA
AVDD4 – AVSS4		AVDD1x		3.6	
IAVDD4	SAR enable		1.5		mA
	SAR disable		10		mA
AVSS-DGND		-1.8		0	V
IOVDD – DGND		1.8		3.6	V
I_IOVDD	HR		8		mA
	LP		3		mA
Power Dissipation	Internal Buffers bypassed, Internal Reference disable, Internal oscillator disable, SAR disable				
HI Resolution Mode	16ksps			104	mW
Low Power Mode	4ksps			40	mW
Power Down	All ADC's disable		TBD		µw

[1] AVDDx = 3.3V, AVSSx = GND, IOVDD = 1.8V, CMOS clock

[2] Disabling either VCM or Internal Reference would lead to a 40uA current consumption reduction

DOUT TIMING CHARACTERISTISTICS

AVDD1x/AVSSx = ±1.65V, 3.3V/AGND, AVDD2 - AVSSx = 2.2 V to 3.6V; IOVDD = 2.3V to 3.6V; DGND = 0V, REF = 2.5 V internal/external, MCLK = 8192 kHz; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. DOUT Timing Specifications

Parameter[1]	Symbol	Comments	Min	Typ	Max	Unit
MCLK frequency	t1	50:50			8.192	MHz
MCLK High time	t2		60			ns
MCLK Low time	t3		60			ns
DCLK Low time	t4	MCLK/2	2/MCLK – TBD		2/MCLK + TBD	ns
DCLK High time	t5	MCLK/2	2/MCLK – TBD		2/MCLK + TBD	ns
MCLK rising edge to DCLK rising edge	t6		TBD			ns
MCLK rising edge to DCLK falling edge	t7		TBD			ns
DCLK rising edge to $\overline{\text{DRDY}}$ rising edge	t8		TBD			ns
DCLK rising edge to $\overline{\text{DRDY}}$ falling edge	t9		TBD			ns
DOUTx setup time	t10		TBD			ns
DOUTx hold time	t11		TBD			ns

[1] All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$

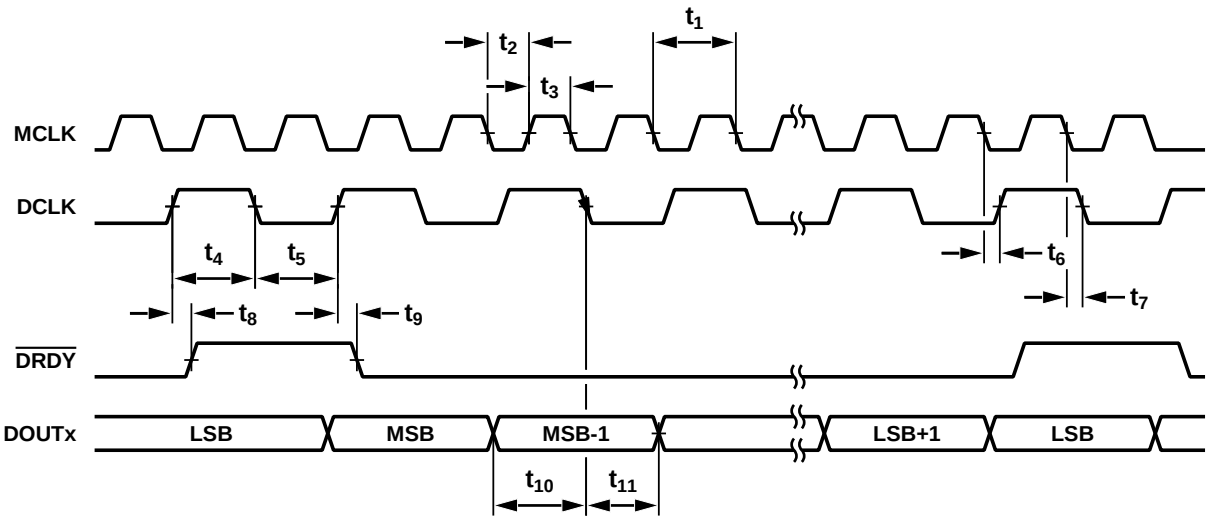


Figure 2. Data Interface timing diagram

SPI TIMING CHARACTERISTISTICS

AVDD1x/AVSSx = ±1.65V, 3.3V/AGND, AVDD2 - AVSSx = 2.2 V to 3.6V; IOVDD = 2.3V to 3.6V; DGND = 0V, REF = 2.5 V internal/external, MCLK = 8192 kHz; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3. SPI Timing Specifications

Parameter[1]	Symbol	Comments	Min	Typ	Max	Unit
SCLK period	t12	50:50			30	MHz
SCLK low time	t13		7			ns
SCLK high time	t14		7			ns
SCLK rising edge to $\overline{CS}$ falling edge	t15		10			ns
$\overline{CS}$ falling edge to SCLK rising edge	t16		10			ns
SCLK rising edge to $\overline{CS}$ rising edge	t17		10			ns
$\overline{CS}$ rising edge to SCLK rising edge	t18		10			ns
Minimum $\overline{CS}$ high time	t19		15			
SDI setup time	t20		5			ns
SDI hold time	t21		5			ns
$\overline{CS}$ falling edge to SDO enable (SPI CPOL = 0)	t22A		10			ns
SCLK falling edge to SDO enable (SPI CPOL = 1)	t22B		5			ns
SDO setup time	t23		10			ns
SDO hold time	t24		10			
$\overline{CS}$ rising edge to SDO disable	t25		10			ns

[1] All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$

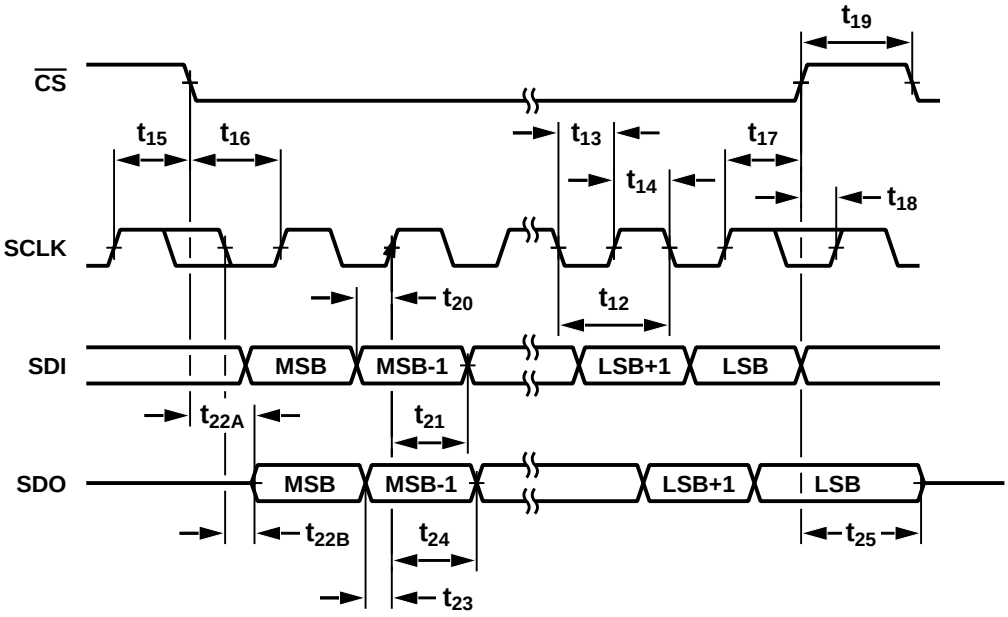


Figure 3. SPI Control Interface

SYNCRONIOZATION PINS AND RESET TIMING CHARACTERISTISTICS

AVDD1x/AVSSx = ±1.65V, 3.3V/AGND, AVDD2 - AVSSx = 2.2 V to 3.6V; IOVDD = 2.3V to 3.6V; DGND = 0V, REF = 2.5 V internal/external, MCLK = 8192 kHz; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4. Timing Specifications

Parameter[1]	Symbol	Comments	Min	Typ	Max	Unit
$\overline{\text{START}}$ Setup time	t26		10			ns
$\overline{\text{START}}$ Hold time	t27		MCLK			ns
MCLK falling edge to $\overline{\text{SYNC\_OUT}}$ falling edge	t28		MCLK			
$\overline{\text{SYNC\_IN}}$ setup time	t29		10			ns
$\overline{\text{SYNC\_IN}}$ hold time	t30		MCLK			
First valid sample	$t_{INIT\_/SYNC\_IN}$	16ksps, HP				ns
First valid sample	$t_{INIT\_/RESET}$	16ksps, HP	320			ns
RESET Hold time	t31		2*MCLK			ns
Start time	t_{POWER_UP}			2		ms

[1] All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$

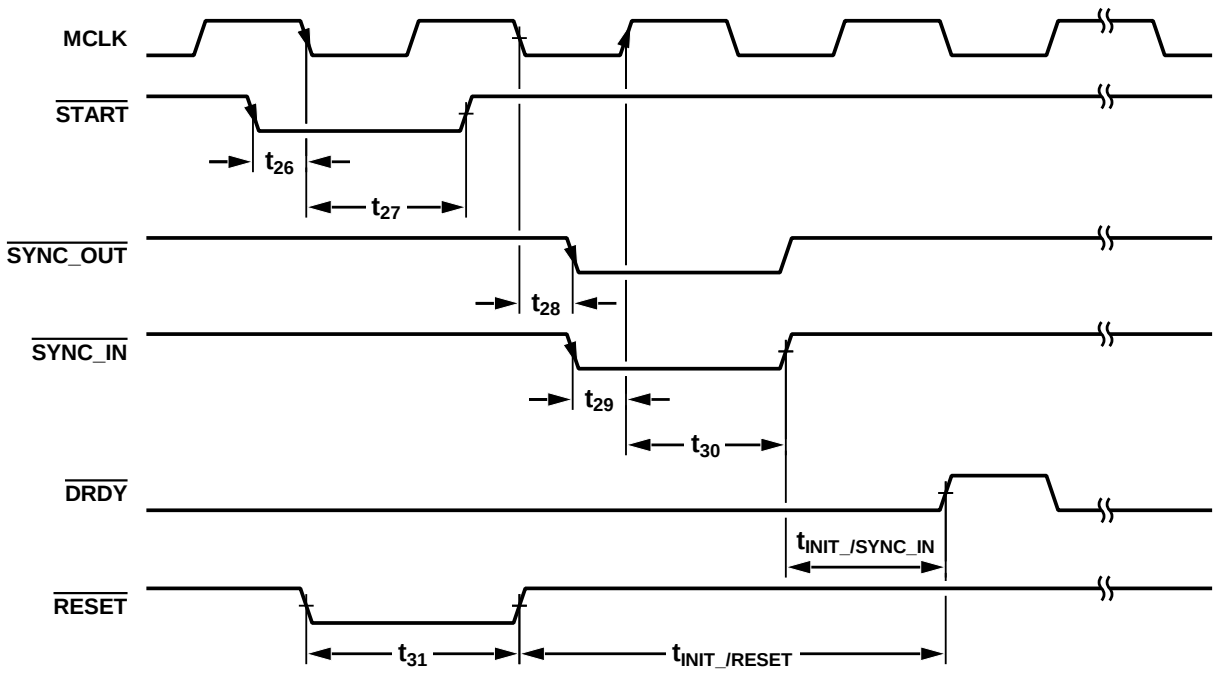


Figure 4. Synchronization pins and reset Control Interface

SAR TIMING CHARACTERISTISTICS

AVDD1x/AVSSx = ±1.65V, 3.3V/AGND, AVDD2 - AVSSx = 2.2 V to 3.6V; IOVDD = 2.3V to 3.6V; DGND = 0V, REF = 2.5 V internal/external, MCLK = 8192 kHz; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5. SAR Timing Specifications

Parameter[1]	Symbol	Comments	Min	Typ	Max	Unit
Conversion time	t_{32}		2.5			us
Acquisition time	t_{33}		500			ns
Delay time	t_{34}		50			ns
Throughput data	t_{35}				256	ksps

[1] All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$

Figure 5. SAR timing diagram

GPIO SCR UPDATE TIMING CHARACTERISTISTICS

AVDD1x/AVSSx = ±1.65V, 3.3V/AGND, AVDD2 - AVSSx = 2.2 V to 3.6V; IOVDD = 2.3V to 3.6V; DGND = 0V, REF = 2.5 V internal/external, MCLK = 8192 kHz; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 6. Timing Specifications

Parameter[1]	Symbol	Comments	Min	Typ	Max	Unit
GPIO2 Setup time	t36		10			ns
GPIO2 Hold time	t37		MCLK			ns
MCLK rising edge to GPIO1 rising edge time	t38		20			ns
GPIO0 setup time	t39		5			ns
GPIO0 hold time	t40		MCLK			ns

[1] All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of IOVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$

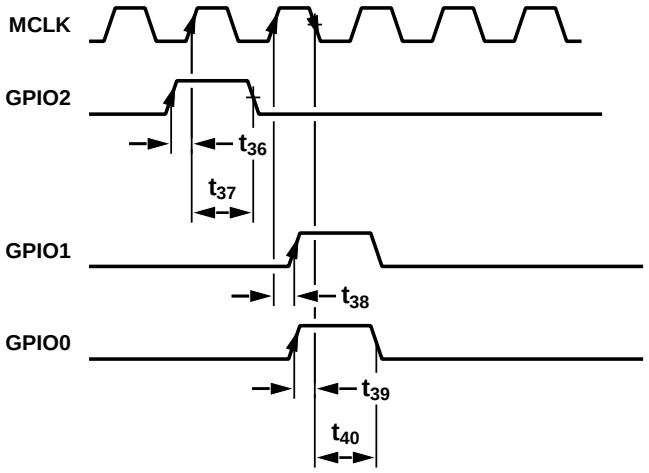


Figure 6. GPIO pin for SRC update

ABSOLUTE MAXIMUM RATINGS

Table 7. Absolute Maximum Ratings

Parameter	Rating
AVDDx to AVSSx	−0.3 V to +3.96V
AVSSx to DGND	−1.98 V to +0.3 V
ARegxCap to AVSSx	−0.3 V to +1.98V
DRegCap to DGND	−0.3 V to +1.98V
IOVDD to DGND	−0.3 V to +3.96V
IOVDD to AVSSx	−0.3 V to +5.94 V
AVSS4 to AVSSx	AVDD1x −0.3 V to +3.96V
Analog Input Voltage	AVSSx− 0.3 V to AVDD1x+0.3 V or +3.96V (whichever is less)
Refx Input Voltage	AVSSx− 0.3 V to AVDD1x+0.3 V or +3.96V (whichever is less)
AUXIN+/AUXIN-	AVSSx− 0.3 V to AVDD4+0.3 V or +3.96V (whichever is less)
Digital Input Voltage to DGND	DGND − 0.3 V to IOVDD + 0.3 V or +3.96V (whichever is less)
Digital Output Voltage to DGND	DGND− 0.3 V to IOVDD + 0.3 V or +3.96V (whichever is less)
XTAL1 to DGND	DGND −0.3 V to DRegCap +0. 3V or +1.98V (whichever is less)
Ain/Digital Input Current	TBD mA
Operating Temperature Range	−40°C to +125°C
Junction Temperature, (T_J maximum)	+150°C
Storage temperature Range	−65°C to +150°C
Reflow soldering	260°C
ESD	2kV
FICDM	
Corner pins (1, 16, 17, 32, 33, 48, 49, 64)	+750V
Others	+500V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 8. Thermal Resistance

Package Type	θ_{ja}	θ_{Jb}	Ψ_{jt}	Ψ_{jb}	UNITS
64-CP-15[1]	30.43		0.13	6.59	°C/W
64-CP-15[2]	22.62	3.17	0.09	3.19	°C/W

1- Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no thermal vias. See JEDEC JESD51.
2- Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 49 thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

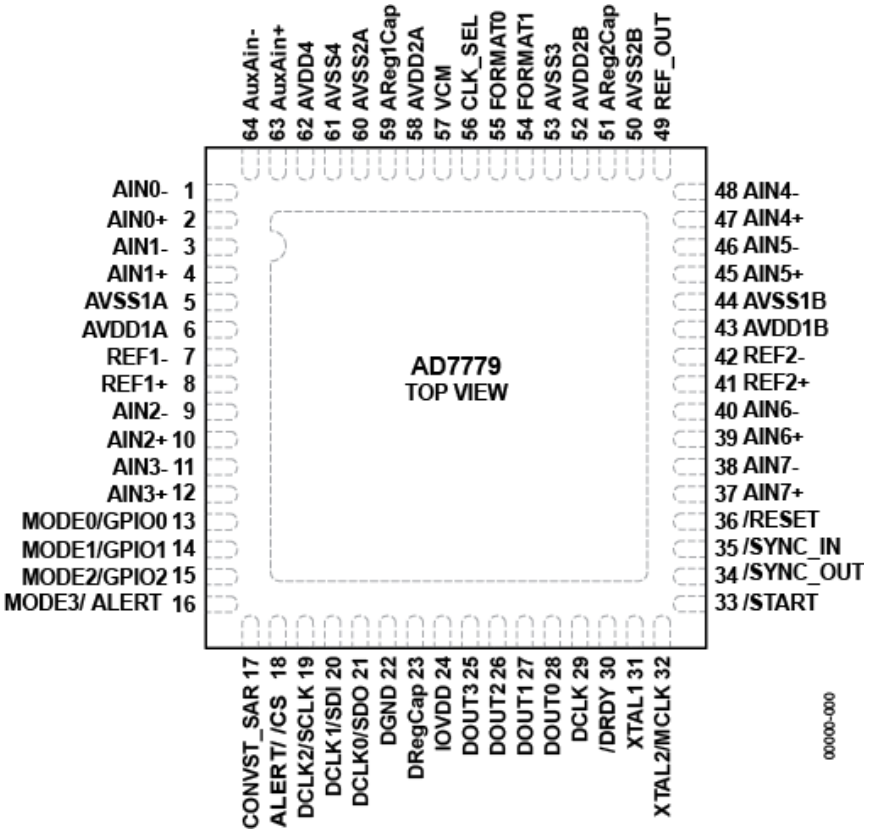


Figure 7. Pin Description

Table 9. Pin Description

Pin No.	Mnemonic	Type	Direction	Description
1	AIN0-	Analog Input	Input	Analog Input Channel 0
2	AIN0+	Analog Input	Input	Analog Input Channel 0
3	AIN1−	Analog Input	Input	Analog Input Channel 1
4	AIN1+	Analog Input	Input	Analog Input Channel 1
5	AVSS1A	Supply	Supply	Negative Front End Analog Supply for Channels 0 to 3, typical −1.65V(Dual Supply), and AGND (Single Supply). Connect all AVSSx pins to the same potential
6	AVDD1A	Supply	Supply	Positive Front End Analog Supply for Channels 0 to 3, typical AVSSx + 3.3V. This pin should be connected together with AVDD1B.
7	REF1−	Reference	Input	Negative Reference Input for Channels 0 to 3, typical AVSSx. Connect all REFx− pins to the same potential
8	REF1+	Reference	Input	Positive Reference Input 1 for Channels 0 to 3, typical REF1− +2.5V
9	AIN2−	Analog Input	Input	Analog Input Channel 2
10	AIN2+	Analog Input	Input	Analog Input Channel 2
11	AIN3−	Analog Input	Input	Analog Input Channel 3
12	AIN3+	Analog Input	Input	Analog Input Channel 3
13	MODE0/GPIO0	Digital I/O	IO	PIN Control Mode: MODE0 input pin, see ***Table 16*** for more details SPI Control Mode: Configurable GPIO0. If this pin is not used, connect to DGND or IOVDD.
14	MODE1/GPIO1	Digital I/O	IO	PIN Control Mode: MODE1 input pin, see ***Table 16*** for more details SPI Control Mode: Configurable GPIO1. If this pin is not used, connect to DGND or IOVDD.
15	MODE2/GPIO2	Digital I/O	IO	PIN Control Mode: MODE2 input pin, see ***Table 16*** for more details SPI Control Mode: Configurable GPIO2. If this pin is not used, connect to DGND or IOVDD.
16	MODE3/ALERT	Digital I/O	IO	PIN Control Mode: MODE3 input pin, see ***Table 16*** for more details SPI Control Mode: Alert Output Pin
17	CONVST_SAR	Digital Input	Input	Pin Control Mode – ΣΔ output interface selection, see **Table *15***for more details SPI Control Mode - SAR Convert Start
18	ALERT/$\overline{CS}$	Digital Input	Input	PIN Control Mode: Alert Output Pin SPI Control Mode: Chip Select
19	DCLK2 / SCLK	Digital Input	Input	PIN Control Mode: DCLK frequency selection, see **Table *14*** for more details SPI Control Mode: SPI Clock.
20	DCLK1 / SDI	Digital Input	Input	PIN Control Mode: DCLK frequency selection, see **Table *14*** for more details SPI Control Mode: SPI Data In. Connect this pin to DGND if the part is configured in Pin Contro Mode with SPI as data output interface
21	DCLK0 / SDO	Digital Output	Output	PIN Control Mode: DCLK frequency selection, see **Table *14*** for more details SPI Control Mode: SPI Data Out
22	DGND	Supply	Supply	Digital ground
23	DREGCAP	Supply	Output	Digital LDO output. Decouple to DGND with 1uF cap
24	IOVDD	Supply	Supply	IO Digital levels and DLDO supply, from 1.8V to 3.6V. IOVDD should not be lower than DRegCap.
25	DOUT3	Digital Output	IO	Data output pin 3. If the part is configured in daisy-chain mode, this pin acts as an input pin, see **Daisy Chain mode** for more details.

Pin No.	Mnemonic	Type	Direction	Description
26	DOUT2	Digital Output	IO	Data output pin 2. If the part is configured in daisy-chain mode, this pin acts as an input pin, see **Daisy Chain mode** for more details.
27	DOUT1	Digital Output	Output	Data output pin 1
28	DOUT0	Digital Output	Output	Data output pin 0
29	DCLK	Digital Output	Output	Data Output Clock
30	$\overline{\text{DRDY}}$	Digital Output	Output	Data Output Ready
31	XTAL1	Clock	Input	XTAL1 input connection, If CMOS is used as a clock source, connect tie this pin to DGND. See Table 13 for more details
32	XTAL2/MCLK	Clock	Input	XTAL2 input connection or CMOS clock, see Table 13 for more details
33	$\overline{\text{START}}$	Digital Input	Input	Synchronization pulse. This pin is used to synchronize internally an external $\overline{\text{START}}$ asynchronous pulse with MCLK. The synchronize signal is shift out by $\overline{\text{SYNC\_OUT}}$ pin.Tie to DGND is not used. See Phase adjustment and Synchronization pins for more details.
34	$\overline{\text{SYNC\_OUT}}$	Digital Output	Input	Synchronization signal. This pin generates a synchronous pulse generated driven by hardware (/START pin) or by software (GENERAL_USER_CONFIG_2 [0]). If this pin is used needs to be wired to $\overline{\text{SYNC\_IN}}$ pin. See Phase adjustment and Synchronization pins for more details.
35	$\overline{\text{SYNC\_IN}}$	Digital Input	Input	$\overline{\text{SYNC\_IN}}$ reset the internal SINC filters. A pulse in this pin is required when phase compensation register are used (CHx_SYNC_OFFSET), or to synchronize multiple devices. See Phase adjustment and Synchronization pins for more details.
36	$\overline{\text{RESET}}$	Digital Input	Input	Asynchronous Reset Pin. Resets all registers to default value. It is recommended to generate a pulse in this pin after the part has been powered-up as slow slew-rate in the supply could generate an incorrect initialization in the digital block.
37	AIN7+	Analog Input	Input	Analog Input Channel 7
38	AIN7–	Analog Input	Input	Analog Input Channel 7
39	AIN6+	Analog Input	Input	Analog Input Channel 6
40	AIN6–	Analog Input	Input	Analog Input Channel 6
41	REF2+	Reference	Input	Positive Reference Input 1 for Channels 4 to 7, recommended value REF2– + 2.5V
42	REF2–	Reference	Input	Negative Reference Input for Channels 4 to 7, typically AVSSx. Connect all REFx– pins to the same potential
43	AVDD1B	Supply	Supply	Positive Front End Analog Supply for Channels 4 to 7. This pin should be connected together with AVDD1A
44	AVSS1B	Supply	Supply	Negative Front End Analog Supply for Channels 4 to 7, typical -1.65V(Dual Supply) or AGND (Single Supply). Connect all AVSSx pins together
45	AIN5+	Analog Input	Input	Analog Input Channel 5
46	AIN5–	Analog Input	Input	Analog Input Channel 5
47	AIN4+	Analog Input	Input	Analog Input Channel 4
48	AIN4–	Analog Input	Input	Analog Input Channel 4
49	REF_OUT	Reference	Output	2.5V Reference Output
50	AVSS2B	Supply	Supply	Negative Analog supply. Connect all AVSSx pins together.
51	AReg2Cap	Supply	Output	Analog LDO output. Decouple to AVSS2 with 1uF cap
52	AVDD2B	Supply	Supply	Positive Analog supply, this pin should be connected together with AVDD2A
53	AVSS3	Supply	Supply	Negative Analog Ground. Connect all AVSSx pins together
54	FORMAT1	Digital Input	Input	Output data frame, see **Table *15*** for more details
55	FORMAT0	Digital Input	Input	Output data frame, see **Table *15*** for more details
56	CLK_SEL	Digital Input	Input	Select Clock Source, see Table 13 for more details

Pin No.	Mnemonic	Type	Direction	Description
57	VCM	Analog Output	Output	Common Mode Voltage Output, (AVDD1−AVSS)/2
58	AVDD2A	Supply	Input	Analog supply, from 2.2V to 3.6V. AVSS2x should not be lower than ARegxCap. AVSS2x should not be lower than ARegxCap.Connected This pin should be connected together with AVDD2B
59	AReg1Cap	Supply	Output	Analog LDO output. Decouple to AVSS with 1uF cap.
60	AVSS2B	Supply	Input	Negative Analog supply. Connect all AVSSx together
61	AVSS4	Supply	Supply	Negative SAR Analog Supply and reference. Connect all AVSSx together
62	AVDD4	Supply	Supply	Positive SAR Analog Supply and Reference source, supply range from AVDD1x to 3.6V
63	AuxAin+	Analog Input	Input	SAR Analog Input Channel
64	AuxAin-	Analog Input	Input	SAR Analog Input Channel

TERMINOLOGY

Common-Mode Rejection Ratio (CMRR)
CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the common-mode voltage of V_{IN+} and V_{IN-} at frequency, f_S.

$$CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is the power at frequency, *f*, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Differential Nonlinearity (DNL) Error
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured for an input typically the input pins are shorted together. The value for dynamic range is expressed in decibels.

Channel to Channel isolation

Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale TBD kHz sine wave signal to all seven nonselected input channels and determining how much that signal is attenuated in the selected channel with a TBD kHz signal. The figure is given worst case across all eight channels for the AD7779

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa and nfb, where m, n = 0,1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb). The AD7779 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Gain Error
The first transition (from 100 … 000 to 100 …001) should occur at a level ½ LSB above nominal negative full scale (−4.0959375 V for the ±2.5 V range). The last transition (from 011 … 110 to 011 … 111) should occur for an analog voltage 1½ LSB below the nominal full scale (+4.0959375 V for the ±2.5V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift

The ratio of the gain error change due to a temperature change of 1°C and the full-scale range (2^N). It is expressed in parts per million.

Least Significant Bit (LSB)
The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (\text{V}) = \frac{V_{INp\text{-}p}}{2^N}$$

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal (including harmonics).

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Zero Error
Zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Zero Error Drift

The ratio of the zero error change due to a temperature change of 1°C and the full scale code range (2^N). It is expressed in parts per million.

THEORY OF OPERATION

The AD7779 is an 8 channel simultaneously sampled, low noise 24-Bit Sigma Delta (ΣΔ) analog-to-Digital Converters (ADC) with integrated digital filtering per channel and sample Rate Converter (SRC).

The AD7779 offers two operation modes, high resolution mode, which offers up to 16ksps, and the low power mode, which offers up to 8ksps. In Low power mode the specifications are guaranteed up to 4ksps, expecting performance degradation at ODRs higher than 4ksps.

Table 10 shows the input referred noise (RTI) against different gain in high performance mode.

Table 10. Input-Referred Noise (μV_{RMS}) for High precision mode

ODR	BW(Hz)	Gain1	Gain2	Gain4	Gain8
16k	5021	7.68	5.62	4.67	4.14
8k	2538	4.18	2.74	2.11	1.84
4k	1273	2.64	1.59	1.12	0.94
2k	636.75	1.82	1.05	0.70	0.57
1k	318.5	1.27	0.73	0.48	0.38

The AD7779 employs a ΣΔ conversion technique to convert the analog input signal into an equivalent digital word. The overview of ΣΔ is that the modulator samples the input waveform and outputs an equivalent digital word at the input clock frequency, f_{CLKIN}.

Due to the high oversampling rate this spreads the quantization noise from 0 to $f_{CLKIN}/2$ (in the case of the AD7779 the f_{CLKIN} relates to the external clock), and therefore the noise energy contained in the band of interest is reduced Figure 8 a. To further reduce the quantization noise, a high order modulator is employed to shape the noise spectrum so that most of the noise energy is shifted out of the band of interest Figure 8 b. The digital filter that follows the modulator removed the large out-of-band quantization noise Figure 8 c.

Further information on the basics as well as more advanced concepts of ΣΔ ADCs are available on www.analog.com, search for MT-022 and MT-023.

Digital filtering has certain advantages over analog filtering. Since digital filtering occurs after the A/D conversion process, it can remove noise injected during the conversion. Analog filtering cannot remove noise injected during conversion.

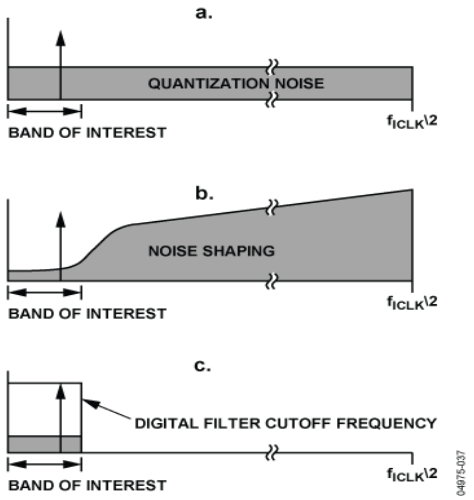


Figure 8. ΣΔ ADC Operation A, B, C, (Linear scale x- axis)

ANALOG INPUTS

The AD7779 can be operated in bipolar or unipolar modes accepting True Differential, Pseudo-differential or Single Ended input signals, as shown in Figure 9.

Table 11 summarizes the maximum differential input signal and dynamic range for the different input modes

Table 11. Input signal modes

Input Signal Mode	PGA GAIN	Maximum Differential signal	Maximum Dynamic Range
True Differential	ALL	$\pm\frac{V_{REF}}{PGA_{GAIN}}$	5Vpkpk
Pseudo-differential	x1	±AVDD1x − 0.1V − VCM or ±AVSSx + 0.1V + VCM (whichever is less)	2x AVDD1x − 0.1V − VCM or 2x AVSSx + 0.1V + VCM
	X2, x4, x8	$\pm\frac{V_{REF}}{PGA_{GAIN}}$	5Vpkpk
Single Ended	ALL	$\frac{V_{REF}}{PGA_{GAIN}}$	2.5pkpk

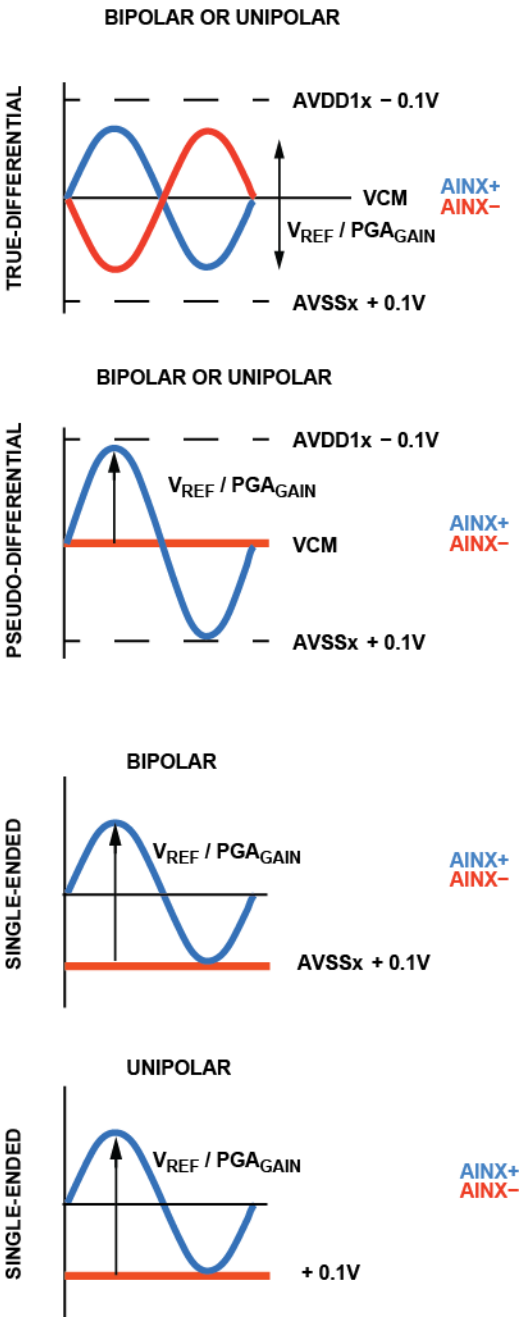


Figure 9 ΣΔ ADC Input Signal Configuration

The input signal common mode is not limited, but the absolute input signal voltage in any AINx pin should be kept between AVSSx + 100mV and AVDD1x – 100mV, otherwise the input signal linearity will be degraded and if exceed the absolute maximum signal rating could damage the part.

Figure 10 shows the maximum and minimum voltage common range at different PGA gains for maximum differential input voltage

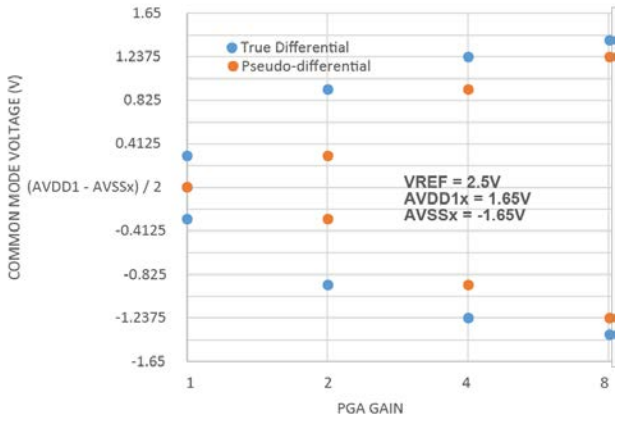


Figure 10. Maximum Common Mode voltage Range for maximum differentail input signal

The AD7779 provides a common mode voltage pin (AVDD1–AVSS)/2, at the VCM pin for single supply, pseudo-differential, or True Differential input configurations.

TRANSFER FUNCTION

The AD7779 can use up to a +3.6V reference, typical 2.5V, and convert the differential voltage between the analog inputs (AIN+ and AIN–) into a digital output. The ADC will convert the voltage difference between the analog input pins (AINx+ – AINx–) into a digital code on the output. The 24-bit conversion result is in MSB first in twos complement format, as shown in **Table 12** and *Figure 11*.

Table 12. Output Codes and Ideal Input Voltages for PGA x1

Description	Analog Input (IN+ – IN–) REF = 2.5 V	Digital Output Code Twos Complement (Hex)
FS – 1 LSB	+2.499999702V	0x7FFFFF
Midscale + 1 LSB	+298nV	0x000001
Midscale	0 V	0x000000
Midscale – 1 LSB	– 298nV	0xFFFFFF
–FS + 1 LSB	–2.499999702V	0x800001
–FS	– 2.5 V	0x800000

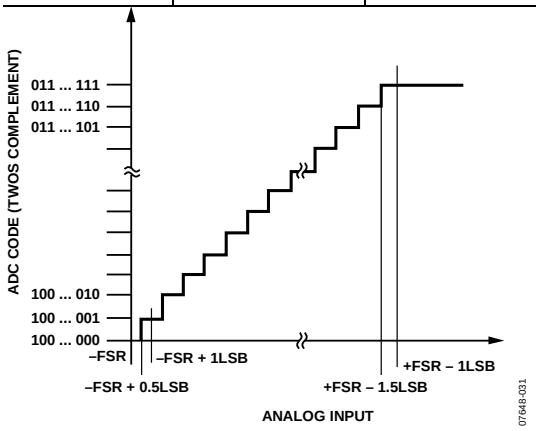


Figure 11. Transfer function

CORE SIGNAL CHAIN

Each ΣΔ ADC channel on the AD7779 has an identical signal path from the analog input pins to the digital output pins. Figure 12 gives a top-level implementation of this. Prior to each ΣΔ ADC there is PGA used to map sensor outputs into the ADC inputs, providing low input current in DC (2nA common and 100pF differential) and 8pF input impedance in AC. and configurable gains of 1,2,4,8. Each ADC channel has its own sigma delta modulator, which oversamples the analog input and passes the digital representation to the digital filter block. The data is filtered, scaled for gain and offset and then output on the data interface.

In addition, to minimize power consumption, the channels can be disabled individually.

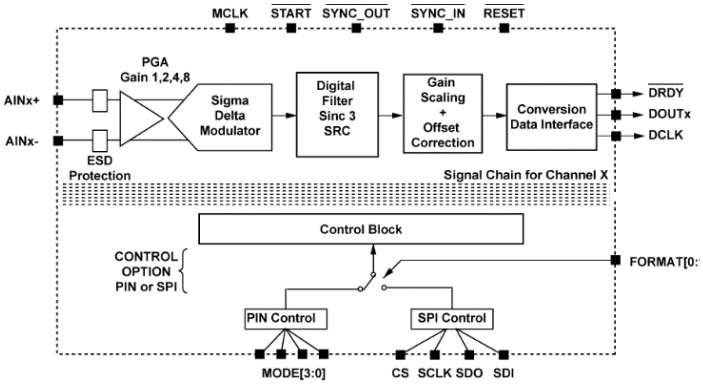


Figure 12. AD7779 Top Level Core Signal Chain

CAPACITIVE PGA

Each ΣΔ ADC has a dedicated Programmable Gain Amplifier offering gain ranges of 1,2,4,8. This PGA reduces the need for an external input buffer and allows the user to gain up small sensor signals to use the full dynamic range of the AD7779.

The PGA will maximize the signal chain dynamic range for small sensor output signals.

The AD7779 uses chopping of the PGA to minimize offset and offset drift in the input amplifier. For the AD7779 the chopping frequency is set to 64 KHz for the high resolution mode and 16 kHz for the Low Power mode, see AN-1131 for more details. The chopping tone is attenuated by the SINC filter.

The capacitive PGA common voltage mode does not depend on the gain, and could be any value as far as the input signal voltage is within AVSSx + 100mV to AVDD1x – 100mV. See Figure 10 for maximum common mode voltage at maximum differential input signals.

The impedance of a capacitive PGA should be analyzed independently for AC and DC. In DC the common leakage current is 4nA typ, with a differential input current of 1.5nA typical.

In AC the impedance is a 8pF capacitor.

INTERNAL REFERENCE AND REFERENCE BUFFERS

The AD7779 integrates a 2.5V, 20 ppm, voltage reference that is disabled at power-up, the buffered reference is available at pin 49, and offers up to 10mA continuous current.

The AD7779 could be used with an external reference connected between REFx+ and REFx– pins. Recommended reference voltage sources for the AD7779 include the ADR44X, ADR45xx family of voltage references, these are low noise, high accuracy voltage references.

If the part in sonfigured in SPI control mode, and the internal reference is used, it is recommended to route externally the REF_OUT pin to REFx+ pins to minimize internal coupled noise. In this case, the part should be configured to use the reference as external.

The internal reference buffers can be operated in three different modes,

1. Buffer Enabled, in this mode the buffer is fully enable, minimizing the current requirements from the external references. Note that the buffer output voltage headroom is ±100mV from the rails.

2. Buffer Bypassed – The external reference is directly connected to the ADC reference caps. In this mode the reference should be able to provide enough current to correctly charge the internal ADC reference caps. In this mode of operation, a degradation in crosstalk is expected as the ADC channels are not isolated from each other

3. Buffer Pre-charged, this is the default operation mode. It is a hybrid mode where the internal reference buffers are connected during the initial acquisition time to pre-charge internal ADC reference caps. During the final phase of the acquisition the reference is connected directly to the ADC caps. This mode has some benefits compared with previous modes,

1- Minimize the reference current requirements.
2- Reduce the noise contribution from the internal reference buffers.

In this mode the headroom/footroom of the buffer reference should not be considered as the reference sets the final voltage in the ADC reference caps.

INTEGRATED LDO'S

The AD7779 has 3 internal LDO's to regulate internal supplies, two LDOs for the analog block and one LDO for the digital core. The internal LDOs requires an external 1µF decoupling capacitor in DRegCap, AReg1Cap and AReg2Cap pins. The LDO slew rate could potentially be low, as depends of the main supply slew rate, it is recommended to generate a hardware reset, pulsing the RESET pin, at power-up.

CLOCKING AND SAMPLING

The AD7779 includes eight ΣΔ ADC cores. Each of these ADCs receive the same master clock signal. The AD7779 requires an

external MCLK frequency of 8192 kHz for High Resolution Mode and 4096 kHz for Low Power Mode, which is internally divided by 4 in high performance mode and by 8 in low power mode to produce the mod_mclk signal used as the modulator sampling clock for the ADCs. The MCLK can be decreased to accommodate lower output data rates, if the minimum ODR selected by the SINC filter is not low enough.
If the external clock is lower than 250kHz, In SPI Control Mode the CLK_QUAL_DIS bit should be set.

The AD7779 integrates an internal oscillator clock that it is used to initialize the internal registers at power-up. The CLK SEL pin defines the external clock used after initialization, see Table 13.

Table 13. Clock Sources

CLK SEL	Clock source	Connection
0	CMOS	Input to XTAL2/MCLK. IOVDD logic level. XTAL1 must be tie to DGND
1	Xtal	Connected between XTAL1 and XTAL2.

The MCLK signal is used to generate the DCLK output signal which is used to clock the ΣΔ Conversion data off the AD7779, as shown in Figure 13.

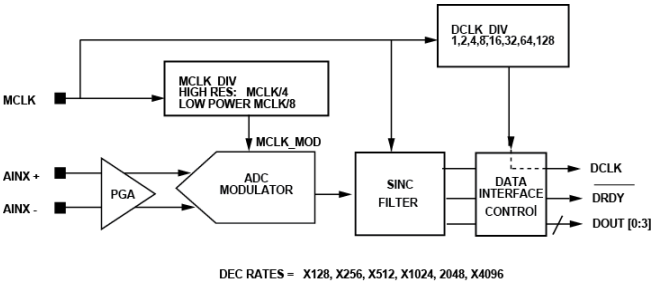


Figure 13 Clock generation on the AD7779

SYNCHRONIZATION PINS

The AD7779 synchronization pin, $\overline{\text{SYNC\_IN}}$, has two different purposes,

1- Reset the SINC filter to guarantee that the phase compensation is applied correctly, CHx_SYNC_OFFSET registers

2- Synchronize multiple devices

In both cases, the synchronization (internal SINC filter reset) is applied by generating a pulse on the $\overline{\text{SYNC\_IN}}$ pin. The pulse in this pin must be synchronous with MCLK.

If the controller/processor cannot generate a synchronous pulse, there are two different ways to achieve this,

1- By applying an asynchronous pulse on the $\overline{\text{START}}$ pin, which is then internally synchronized with the external MCLK clock, and the resultant synchronous signal is output on the $\overline{\text{SYNC_OUT}}$pin.

2- Trigger the $\overline{\text{SYNC\_OUT}}$ internally. When the AD7779 is configured in SPI control mode, toggling the GEN_USER_CONFIG_2[0] bit will generate a synchronous pulse that is output on $\overline{\text{SYNC\_OUT}}$.pin.

The $\overline{\text{SYNC\_IN}}$ and $\overline{\text{SYNC_OUT}}$pins must be externally connected if internal synchronization is used.

If multiple AD7779 needs to be synchronized, the $\overline{\text{SYNC\_OUT}}$ pin of one device can be connected to multiple parts. This synchronization method requires the use of a common MCLK signal for all the AD7779 connected, as shown in Figure 14.

If $\overline{\text{START}}$ pin is not used, tie to DGND.

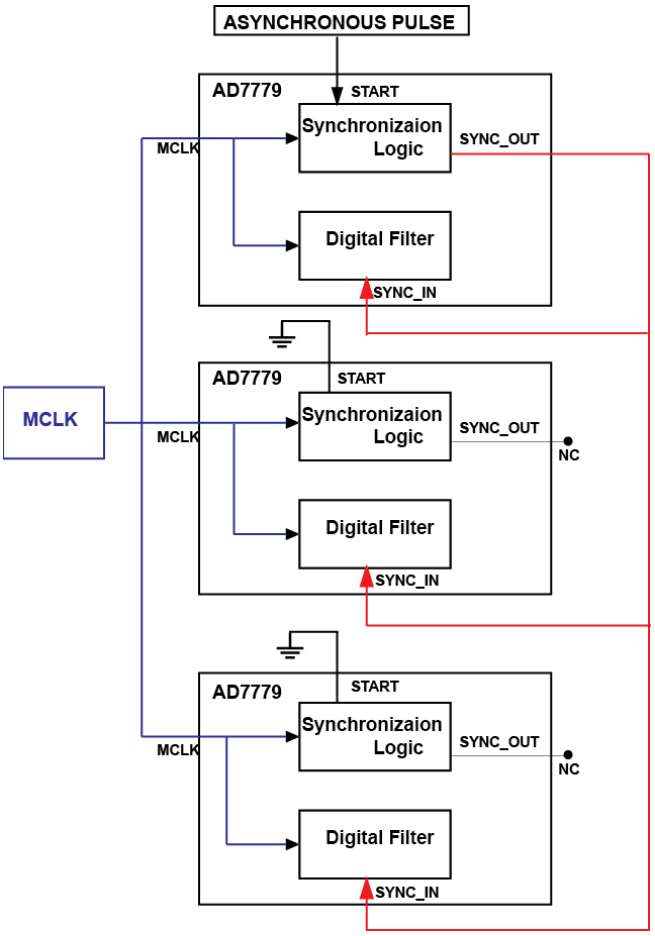


Figure 14. Multiple AD7779 SYNC

DIGITAL FILTERING

The AD7779 offers a low latency SINC3 filter. Most precision ΣΔ ADCs use SINC filters – the SINC filter offers a low latency path for applications looking at low BW signals, for example in control loops or where application specific post processing is required. The digital filter adds notches at multiples of the sampling frequency .

The digital filter implements three main notches, one at the maximum ODR, 16 kHz or 8kHz, depending on the power

mode and another two at the Output Data Rate frequency selected to stop noise aliasing into the passband.

Figure 15 shows typical filter transfer function for High precision and low power mode using a decimation rate of 256 samples.

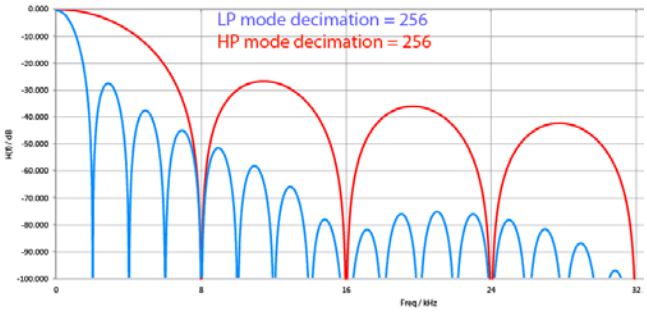


Figure 15. SINC 3 frequency response

The sample rate converter featured allows for fine tune of the decimation rate even for not integer multiples of the decimation rate, 2^n. See Sample Rate Converter (SRC) section for more details on filter profiles for non-integer decimation rates.

CONTROLLING THE AD7779

The AD7779 can be controlled using either of the following methods

- PIN control mode
- SPI control mode

Pin control mode allows the AD7779 to be hardwired to predefined settings that offer a subset of the over-all functionality of the AD7779. In this mode, the sample rate converter and diagnostic features or extended errors source are not available.

Controlling the AD7779 over the SPI interface allows the user access to the full monitoring, diagnostic and ΣΔ control functionality. The SPI control offers additional functionality such as offset, gain and phase correction per channel in addition to access to the flexible Sample Rate Converter to achieve a coherent sampling.

See **Table *15*** for more details about different configurations.

PIN CONTROL

In pin Control Mode, the AD7779 gets configured at power-up based on the Mode pins level, MODE 0, MODE1, MODE2, MODE3. These four pins are used to set the following functions on the AD7779: Mode of operation, Decimation Rate/ODR, PGA Gain and Reference source.

The number of DOUT lines enabled and the number of clocks required for the ΣΔ data transfer is determined by the logic level of the, CONV_START, FORMAT 0 and FORMAT 1 pins. When configured in pin control mode the DCLK2, DCLK1 and DCLK0 pins are used to select the sigma-delta output interface and to control the DCLK divide function, which will be a submultiple of MCLK, as shown in **Table *14***. The DCLK div function sets the frequency of the data output interface DCLK signal. DCLK minimum frequency depends on the decimation rate and operation mode. See

for more details about minimum DCLK frequency.

All the pins that define the AD7779 configuration mode are re-evaluated every time $\overline{\text{SYNC\_IN}}$ pin is pulsed.

Typical connection diagram for pin control mode is shown in Figure 16.

Table 14. DCLK select for PIN Control Mode

DCLK2 / SCLK	DCLK1/ SDI	DCLK0 / SDO	MCLK divide
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Due to the limited number of Mode pins and number of options available, the PGA gain control has been grouped into blocks of 4, and the output data rate is selected to the maximum defined by the decimation rate, ODR (kHz)= 2048 /decimation for High Precision and 512/decimation in low power mode. ***Table 16*** shows available pre-defined configuration.

Depending on the mode selected, the part is configured to use external or internal reference.

Table 15 Format of Data Interface

CONV_START	Format 1	Format 0	Control Mode	Data output mode
1	0	0	PIN Control	SPI Output
	0	1	PIN Control	SPI Output
	1	1	PIN Control	SPI Output
	1	1	SPI Control	Defined in register 0x014
0	0	0	PIN Control	DOUT0 – Channel [0:1] DOUT1 – Channel [2:3] DOUT2 – Channel [4:5] DOUT3 – Channel [6:7]
	0	1	PIN Control	DOUT0 – Channel [3:0] DOUT1 – Channel [7:4]
	1	0	PIN Control	DOUT0 – Channel [7:0]
	1	1	SPI Control	Defined in register 0x014

Table 16. Pin Mode options

MODE3	MODE2	MODE1	MODE0	DECIMATION RATE	POWER MODE	PGA Gain Channels 0 to 3	PGA Gain Channels 4 to 7	REF
0	0	0	0	1024	High Resolution	1	1	Ext
0	0	0	1	512	High Resolution	1	1	Ext
0	0	1	0	256	High Resolution	1	1	Ext
0	0	1	1	128	High Resolution	1	1	Ext
0	1	0	0	256	High Resolution	1	2	Ext
0	1	0	1	512	High Resolution	1	4	Ext
0	1	1	0	256	High Resolution	1	4	Ext
0	1	1	1	128	High Resolution	1	4	Ext
1	0	0	0	512	High Resolution	1	1	Int
1	0	0	1	256	High Resolution	1	1	Int
1	0	1	0	128	High Resolution	1	1	Int
1	0	1	1	512	Low power	1	1	Ext
1	1	0	0	256	Low power	1	1	Ext
1	1	0	1	128	Low power	1	1	Ext
1	1	1	0	128	Low power	1	1	Int
1	1	1	1	256	Low power	1	1	Int

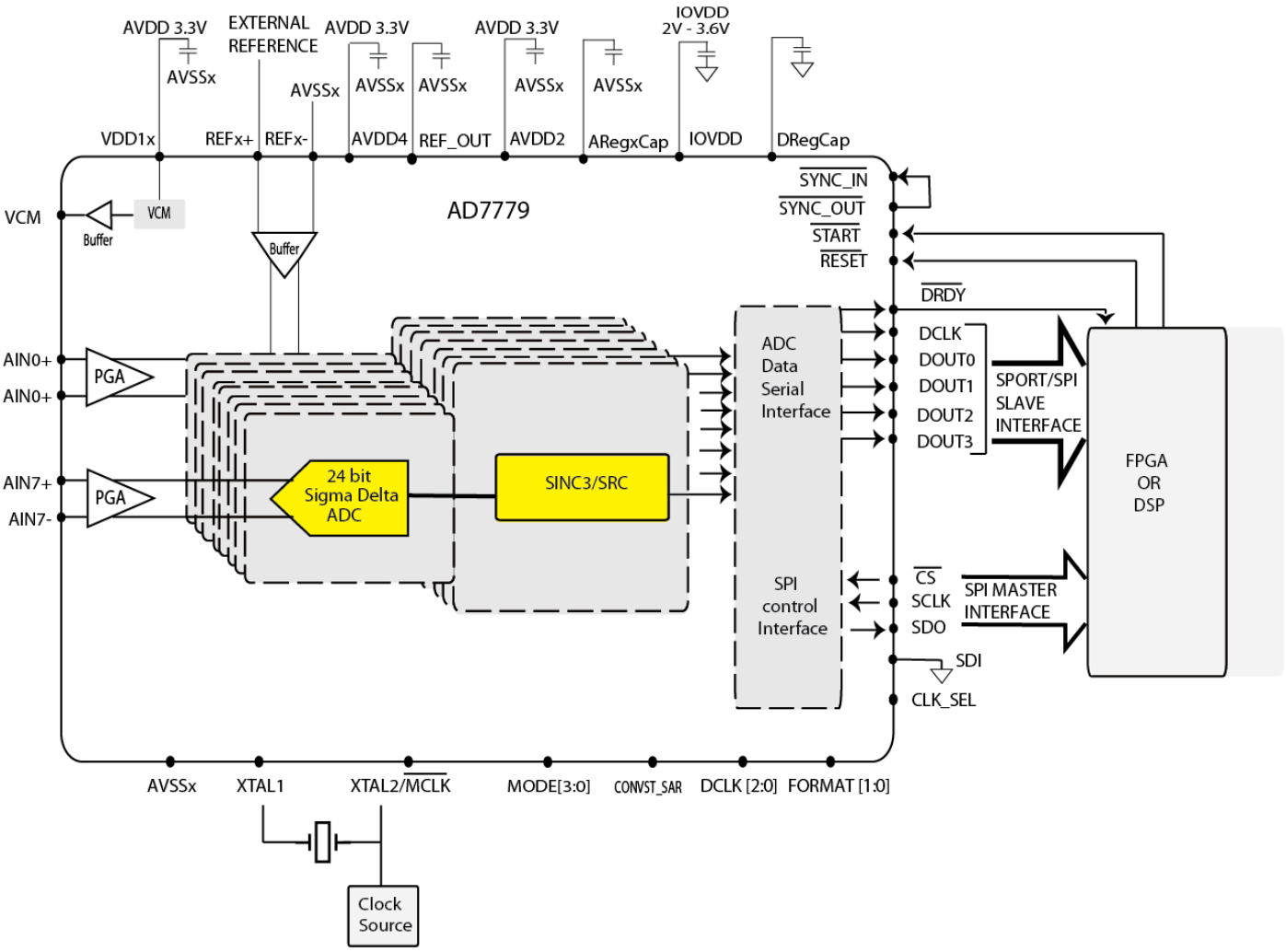


Figure 16. AD7779 PIN mode connection diagram

SPI CONTROL

The second option for control and monitoring the AD7779 is via the SPI interface. This option allows access to the full functionality on the AD7779, including the access to the SAR converter, phase synchronization, offset and gain adjustment, diagnostics and the sample rate converter (SRC). To use the SPI control set the FORMAT 0 and FORMAT 1 bits to a logic high.

Typical connection diagram is shown in Figure 17.

The SPI interface of the AD7779 is an independent path for the control and monitoring functions of the AD7779.
In this mode, the SPI interface can also be used to read the ΣΔ conversation data.

Functionality Available in SPI Mode

SPI control of the AD7779 offers the super set of the functions and diagnostics to the user. ***Table 17*** highlights the functionality and diagnostics offered when in SPI control mode.

Offset and Gain Correction

Offset and gain registers are available for system calibration. The Gain register is pre-programmed during final production for PGA gain of 1, but can be overwritten with a new value if required.

Gain register is 24 bits long split across three registers, CHx_GAIN_UPPER_BYTE, CHx_GAIN_MID_BYTE and CHx_GAIN_LOWER_BYTE, which set the gain on per channel basis.

The gain value is relative to 0x555555 which represents a gain of 1.

The offset register is 24-bit long which is spreed across 3 byte registers, CHx_OFFSET_UPPER_BYTE, CHx_OFFSET_MID_BYTE and CHx_OFFSET_LOWER_BYTE. The default value is 0x000000 at power-up. The offset should be programmed as a 2's complement signed 24 bit number.
The value programmed in the register is multiplied by 3/4 LSBs and subtracted to the modulator results.

As an example of calibration, the offset measured is −200LSB (both AINx pins connected to the same potential), and the FS code (AINx+ − AINx− = VREF) is 0x7E0000

The offset should be compensate by 200LSB, the offset registers should be programmed with a value of 200*(-3/4) = -−150 -> 0xFFFFFF – 0x96 + 1 = 0xFFFF70

CHx_OFFSET_UPPER_BYTE = 0xFF

CHx_OFFSET_MID_BYTE = 0xFF

CHx_OFFSET_LOWER_BYTE. = 0x70

The gain needs to be adjusted by a factor of $\frac{0x7FFFFF}{0x7E0000} = 1.0158$ the register value should be 0x555555x1.0158 = 0x56B015

CHx_GAIN_UPPER_BYTE = 0x56

CHx_GAIN_MID_BYTE = 0xB0

CHx_GAIN_LOWER_BYTE = 0x15

Note that the gain correction is applied after the offset correction so make sure that the gain is set as 1 before calibrate, otherwise the offset will be multiplied by the gain.

Table 17. SPI Control functionality

Global Control Functions	**Per Channel Functions**
Mode of Operation: High Resolution/Low Power	PGA gain
Output Data Rate: Sample Rate Converter (SRC)	ΣΔ Channel Power-Down
VCM buffer power down	Phase delay: SYNC phase offset per channel
Reference: Internal/External	Calibration of offset
Ref Buffers mode: enable, pre-charged or bypassed	Calibration of gain
Reference buffer disable	ΣΔ Input Signal Mux
SAR Diagnostic Mux	Channel error register
SAR power down	PGA gain
GPIO write/read	ΣΔ Channel Power-Down
SPI SAR conversion readback	Phase delay: SYNC phase offset per channel
SDO and DOUT drive strength	
Internal LDO bypassed	
CRC Protection: enable or disable	
SPI slave mode – read ΣΔ results	
DOUT mode	
DCLK Division	

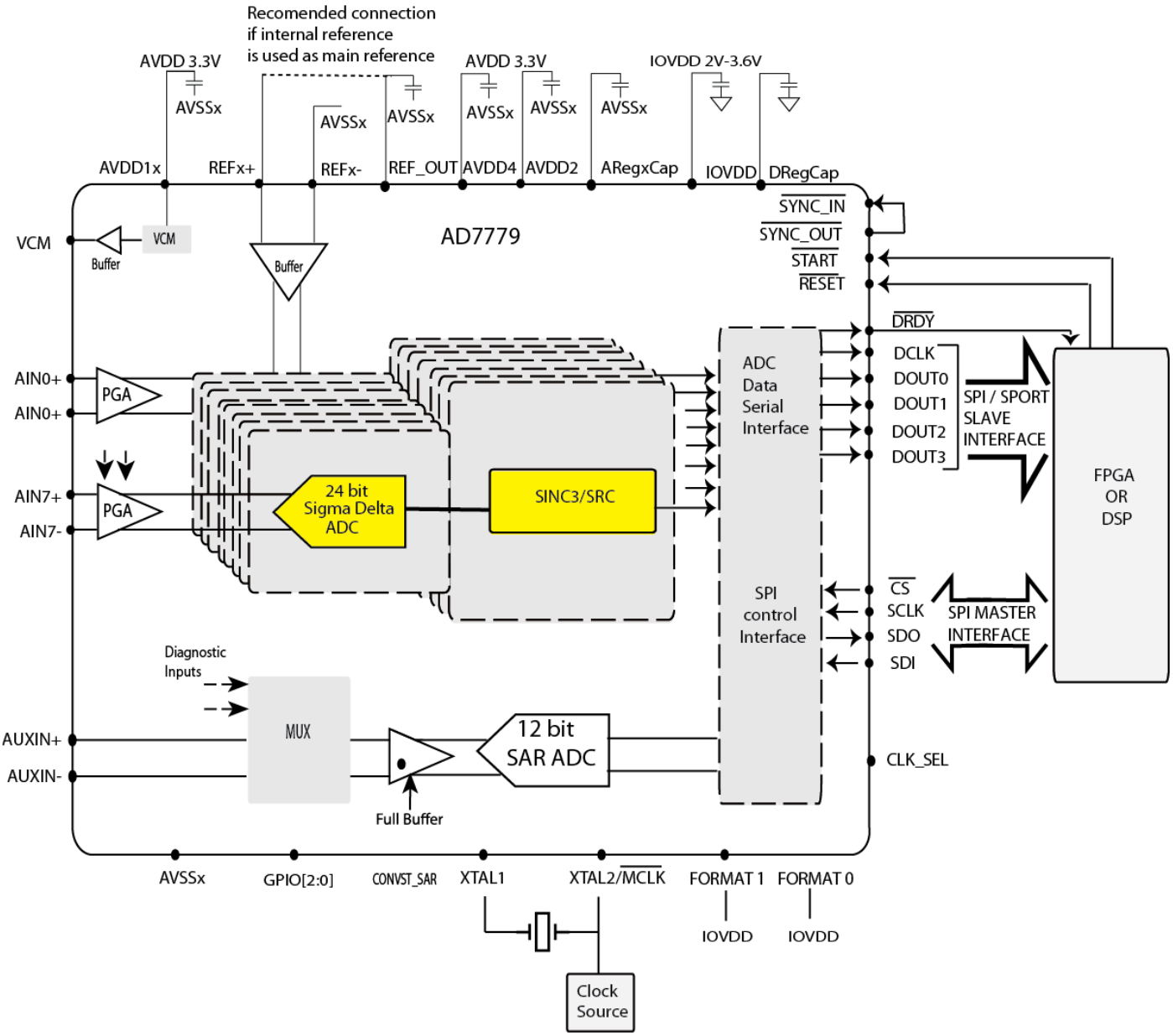


Figure 17. AD7779 SPI mode connection diagram

Phase adjustment

The AD7779 phase delay can be adjusted to compensate for phase mismatches between channels due to sensors or signal channel phase errors prior to the AD7779. This phase adjustment can be achieved by programming register CHx_SYNC_OFFSET. This will delay by a certain numbers of modulator clocks, mod_CLKs the SYNC signal to initiate the digital filter for each ΣΔ ADCs individually.

The phase adjustment register is read during the SYNC_IN pulse, consequently any further change on the register will have no effect unless a pulse in SYNC_IN is generated, see Synchronization pins to get more details about how to generate a pulse in SYNC_IN pin.

The phase offset register is multiplied internally by a factor that depends on the decimation rate, as shown in Table 18

Table 18. Phase adjustment versus decimation rate

Decimation Rate	Phase adjustment multiples of mod_mclk
<=255	x1
<=511	x2
<=1023	x4
<=2047	x8
<=4095	x16

The maximum phase delay cannot be equal or higher than the decimation rate, if this is the case, the offset value will be coerce internally to the decimation rate value.

As an example, the phase mismatch between CH0 and CH1 is 5degrees, and the ODR is 5ksps in HP mode.

In this case, the decimation ration is 2048kHz / 5kHz = 409.6, which means that the offset register value is multiplied internally by x2.

Assuming an input signal of 50Hz, the number of mod_mclk pulses required to sample a full period is 2048kHz/50Hz = 40960 -> 360°/40960 = 8.78e-3°.

If we require a 5degreed delay the number of mod_mclk delays should 569, as the offset register is multiplied by x2, the final offset register value should be 569/2 = 0x11C.

In the case that the programmed value is higher than the decimation factor, which means that the part will internally coerce the offset to 409, resulting in a phase compensation of 409*8.78e-3° = 3.59°.

PGA gain

The PGA gain can be selected individually by selecting appropriately CHx_CONFIG[7:6] register bits as shown in Table 19.

Table 19. PGA gain

CHx_CONFIG[7:6]	Gain
00	X1
01	X2
10	X4
11	X8

DECIMATION

The decimation defines the sampling frequency as,

HP = MCLK / (4*decimation)

LP = MCLK/(8*decimation)

Refer to Sample Rate Converter (SRC) of more details.

GPIO pins

If the AD7779 operates in SPI mode, the Mode 0-2 pins operate as GPIO pins, as shown in Figure 18. The GPIO pins can be configured as inputs or outputs in any order.

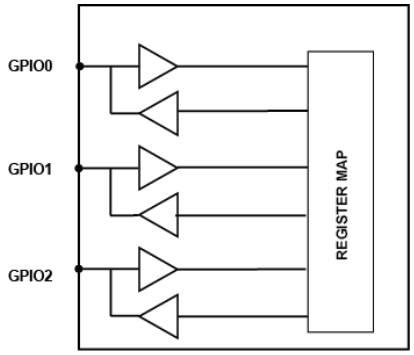


Figure 18 GPIO functionality

Configuration control and read back of the GPIO pins are dealt with by registers GPIO_CONFIG [2:0](0 = input, 1 = output) and GPIO_DATA. Amongst other uses, the GPIO can control an external mux connected to the auxiliary inputs of the SAR ADC. This can be used to verify the results on the sigma delta ADC's.

In addition, those pins can be used to externally trigger a new decimation rate. Refer to Sample Rate Converter (SRC) for more details about this functionality.

Sigma Delta Reference Configuration

The AD7779 can operate with internal or external references, in addition for diagnostic purpose; the analog supply can be used as a reference, as shown in Table 20.

Table 20. S-D References

ADC_MUX_ CONFIG[7:6]	Channel 0 - 3	Channel 4 - 7
00	REF1+ / REF1−	REF2+ / REF2−
01	INTERNAL	INTERNAL
10	AVDD1A/AVSS1A	AVDD1B/AVSS1B
11	REF1− / REF1+	REF2− / REF2+

Reference buffer operation is described in Table 21

Table 21. Reference Buffer operation modes

Operation Mode	REFx+	REFx–
Enable	BUFFER_CONFIG_1[4] = 1, BUFFER_CONFIG_2[7] = 0	BUFFER_CONFIG_1[3] = 1; BUFFER_CONFIG_2[6] = 0
Pre-Charge	BUFFER_CONFIG_1[4] = 1, BUFFER_CONFIG_2[7] = 1	BUFFER_CONFIG_1[3] = 1; BUFFER_CONFIG_2[6] = 1
Disable	BUFFER_CONFIG_1[4] = 0	BUFFER_CONFIG_1[3] = 0

The selected reference and buffer operation mode affect all channels.

If the AD7779 is operated with the internal reference, it is recommended to externally connect the REF_OUT pin to the REFx+ pins, and select the external reference operation mode.

Power modes

The AD7779 offers different power modes to improve the power efficiency – High Resolution and Low Power Mode, which can be controlled thru GENERAL_USER_CONFIG1[6]. To further reduce the power the following blocks can be disabled indipendenly as described in Table 22

.

Table 22. Additional disable power-down blocks

Block	Register	Notes
VCM	GENERAL_USER_CONFIG1[5]	Enable by default
Reference buffer	BUFFER_CONFIG_1[4:3]	
Internal reference buffer	GENERAL_USER_CONFIG1[4]	Disable by default
Sigma delta channel	CH_DISABLE[7:0]	All channels enable
SAR	GENERAL_USER_CONFIG1[3]	Disable by default
Internal oscillator	GENERAL_USER_CONFIG1[2]	Enable by default

DIGITAL SPI INTERFACE

The serial interface on the AD7779 consists of four signals: $\overline{CS}$, SDI, SCLK and SDO, typical connection is shown in Figure 19.

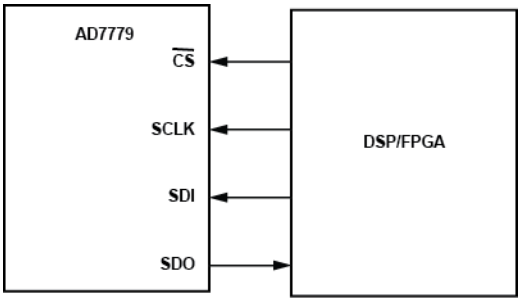


Figure 19 SPI Control Interface, AD7779 is SPI slave, FPGA/DSP is master

The SPI interfaces operates in MODE 0 and MODE 3, CPOL = 0, CPHA = 0 (Mode 0) or CPOL = 1, CPHA = 1 (Mode 3).

In Pin Control Mode, the SDI can be used to readback the SD results, depending on the levels of CONV_START, FORMAT 0 and FORMAT 1 pins, as described in **Table *15***.

In SPI control Mode, the SPI interface is used to transfer data into the on chip registers, while the SDO can be used to read-back data from the on chip registers, read the SAR or ΣΔ conversions results, depending on the selected operation mode.

The SDO data source in SPI control mode is defined by registers GENERAL_USER_CONFIG2 and GENERAL_USER_CONFIG3 as described in Table 23

Table 23. SPI operation mode in SPI control Mode

GENERAL_USER_CONFIG2[5]	GENERAL_USER_CONFIG3[4]	Mode
0	0	SPI Read/Write Register Mode
0	1	ΣΔ Data Mode
1	X	SAR Mode

In SPI control mode, there are four different levels of I/O strength on the SDO pin, which can be selected in GENERAL_USER_CONFIG2[4:3], as described in Table 24.

Table 24. SDO strength

GENERAL_USER_CONFIG2[4:3]		Mode
0	0	Normal
0	1	Strong
1	0	Weak
1	1	Extra Strong

SCLK is the serial clock input for the device, all data transfers (on either SDO or SDI) occur with respect to this SCLK signal.

SPI CRC- CHECKSUM PROTECTION (SPI Control Mode)

The AD7779 has a checksum mode, which can be used to improve SPI interface robustness in SPI control Mode. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the CRC_ERR bit is set in the Error register. However, to ensure that the register write was successful, the register should be read back and checksum verified.

For CRC checksum calculations, the following polynomial is always used: $x^8 + x^2 + x + 1$. See SPI Control Mode Checksum for more details.

SPI Read/Write Register Mode (SPI control mode)

The AD7779 has on board registers to configure and control the device. The basic data frame, with CRC disabled, on the SDI line during the transfer consists of a R/$\overline{W}$ bit (1= Read, 0= Write), 7 bit register address, 8 bits of data, as shown in Figure 20.

The AD7779 registers have 7-bit address'- the 7-bit register address on the SDI line is used to select the register for the read/write function. The 7-bit register address follows the R/$\overline{W}$ bit in the SDI data. The 8 bits on the SDI line following the 7-bit register address is the data to be written to the selected register if the SPI transfer is a write transfer. Data on the SDI line is clocked into the AD7779 on the rising edge of SCLK, as shown in Figure 3.

The SPI interface can operate in multiple of 8-bits, ie. In SPI control mode, if the SDO pin is used to readback the data from the internal register or the SAR ADC, the data frame is 16-bits wide (CRC disable), as shown in Figure 20, or 24-bits wide (CRC enable), as shown in Figure 21. In this case for example, the controller can generate one frame of 16-bits/24-bits (w and w/o CRC) or 2/3 frames of 8-bits (w and w/o CRC) When the SDO line is used to readback the data from the SD channels, 64-bits should be readback from the controller, in this case the controller can generate a frame of 64-bits, 2x32-bits, 4x16bits, or 8x8-bits..

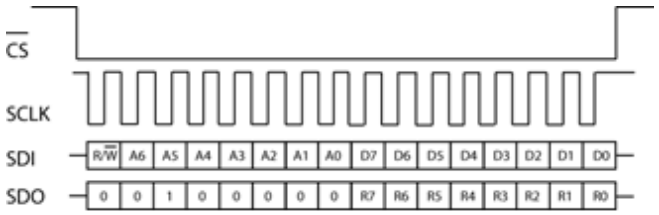


Figure 20 16 Bit SPI Transfer – CRC disabled

The Data on the SDO line during the SPI transfer contains the 8 bit 0010 0000 header and 8 bits of register data in the case of a READ (R) operation and 8 zero's in the case of a $\overline{\text{WRITE}}$ ($\overline{\text{W}}$) SPI transfer. In the case of a Read (R) SPI, transfer this 8 bits of data will contain the contents of the register whose address corresponds to that of the 7-bit address on the SDI line during this SPI read transfer. Data is clocked out of the AD7779 on the SCLK falling edge.

Enabling the SPI_CRC_ERR_EN will result in a CRC check sum being performed on all the READ/$\overline{\text{WRITE}}$ operations. When SPI_CRC_ERR_EN is enabled an 8-bit CRC word is appended to all data write/read operations. When CRC is enabled a minimum of frame length of 24 SCLKs is required on SPI transfers. The 24 bits of Data on the SDO line consists of 8-bit header 0010 0000, 8 bits of data and 8 bit CRC, see Figure 21.

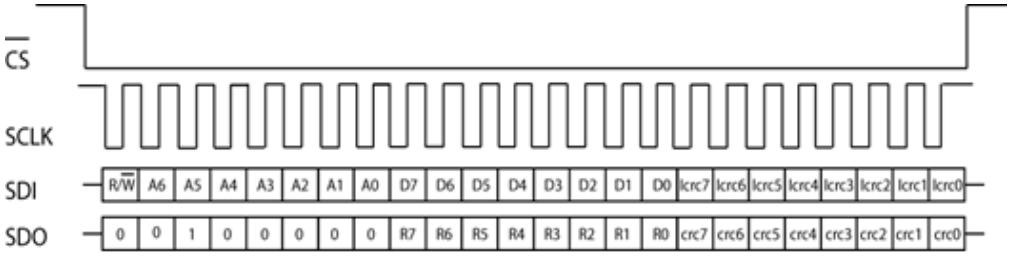


Figure 21 24 Bit SPI transfer CRC enabled

SPI SAR Diagnostic mode (SPI Control Mode)

Setting bit 5 in the GENERAL_USER_CONFIG2 register configures the SDO line to shift out data form the SAR ADC conversions, as described in Table 23.

In this mode, the AD7779 internal registers can be written to but any readback command will be ignored as the SDO data frame is dedicated to shift out the conversion results from the SAR ADC.

To exit this mode of operation reset bit 5 in the GENERAL_USER_CONFIG2 register.

The Data on the SDO line during the SPI transfer contains a 4-bit 0010 header and 12 bits of SAR conversion result.

The data frame consist of 16- or 24- bits data depending on SPI_CRC_ERR_EN bit that enables the CRC checksum, as shown in Figure 22

As per the SPI Read/Write Register Mode the SDI line contains the R/$\overline{W}$ bit, 7 bit register address, 8 bits of data and an eight bit CRC (if enable). To avoid unwanted writes to the internal register, it is recommended to send a readback command, ie. 0x8000, to the part, which will be ignored as the SDO pin is used to shift-out the content of the SAR ADC.

for more details about the frame format.

The SDO pin data can be readback in any multiple of 8-bits, ie. 64-bits, 2x32-bits, 4x16bits, or 8x8-bits.

ΣΔ DATA ADC mode

In PIN control mode, the SPI interface can be used to readback the SD conversions as described in **Table *15***.
In SPI control mode, the SPI interface can be enabled by setting GENERAL_USER_CONFIG3[4], as described in Table 23.
In SPI control mode, the AD7779 internal register can be written to but any readback command will be ignored as the SDO data frame is dedicated to shifting out the conversion results from the ΣΔ ADCs. To avoid unwanted writes to the internal register, it is recommended to send a readback command, ie. 0x8000, to the part, which will be ignored as the SDO pin is used to shift-out the content of the SD ADC.

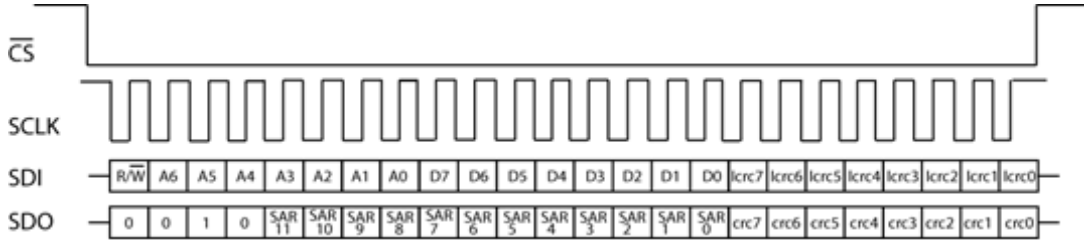


Figure 22 SAR ADC/Diagnostic Mode CRC enabled

AD7779 DIAGNOSTIC & MONITORING

SELF-DIAGNOSTICS ERROR

The AD7779 includes self diagnostic features to guarantee the correct operation. If an error is detected, the ALERT pin is pulled high to generate an external interruption to the controller.
In addition, the header of the ΣΔ output data contain a bit used to inform the controller of the error called Chip Error. See ADC CONVERSION OUTPUT: HEADER & data

In addition, both ALERT pin and Chip error bit are automatically cleared if the error is no longer present.

There are different sources of errors that are detailed below. In PIN control code, it is not possible to check the error source, and some source of error are not enable. In SPI control mode, the source of error can be checked by reading the appropriate register bit.

The STATUS_REGx register bits identify the register that had been generated the error, as summarized in Table 25.

Table 25. Register Error Source

Bit Name	Register Source
ERR_LOC_GEN2	GEN_ERR_REG_2
ERR_LOC_GEN1	GEN_ERR_REG_1
ERR_LOC_CH7	CH7_ERR_REG
ERR_LOC_CH6	CH6_ERR_REG
ERR_LOC_CH5	CH5_ERR_REG
ERR_LOC_CH4	CH4_ERR_REG
ERR_LOC_CH3	CH3_ERR_REG
ERR_LOC_CH2	CH2_ERR_REG
ERR_LOC_CH1	CH1_ERR_REG
ERR_LOC_CH0	CH0_ERR_REG
ERR_LOC_SAT_CH6_7	CH6_7_SAT_ERR
ERR_LOC_SAT_CH4_5	CH4_5_SAT_ERR
ERR_LOC_SAT_CH2_3	CH2_3_SAT_ERR
ERR_LOC_SAT_CH0_1	CH0_1_SAT_ERR

In addition STATUS_REG_x has a bit that indicates if any internal error has been trigger, similar to the CHIP ERROR bit added to the SD header. The bit is clear if the error is no longer present and the register is readback.

The INIT_COMPLETE bit in the STATUS_REG_3 indicates that the part has been initialized correctly.

GENERAL ERRORS

MCLK switch error (SPI Control Mode)

After power up the AD7779 initiates a clocking handover sequence to pass clocking control to the external oscillator, or CMOS clock. In SPI mode, if an error occurs in the handover the EXT_MCLK_SWITCH_ERR bit is set in the general error register, GEN_ERROR_REG2. A reset is required if this event occurs.

If EXT_MCLK_SWITCH_ERR is set then the part is operating off the internal oscillator.
To use the external clock, set the CLK_QUAL_DIS bit. This will clear the error bit also.

RESET Detection

The AD7779 general error register contains a reset_detected bit. This bit is asserted if a reset pulse is applied to the AD7779 and is cleared by reading the general error register. This bit indicates that the POR has initialized correctly the part. In addition, this pin can be used to detect an unexpected device reset or glitch on the reset pin. To reset this error signal in SPI mode - toggling the /SYNC_IN pin or reading from the general error register, GEN_ERROR_REG2. In Pin Control Mode - the signal is reset by toggling the /SYNC_IN pin.

Internal LDO Status

The AD7779 has 3 internal LDO's to regulate internal analog and digital supply rails. The LDO's have internal power supply monitors. Internal comparators monitor and flag errors with these supplies once they pass a predetermined limit.

ALDO1_PSM_ERR, ALDO2_PSM_ERR, and DLDO_PSM_ERR bits indicate a LDO malfunction.

The internal analog and digital voltage monitors can be disable by selecting appropriately the LDO PSM test EN bits .

The SAR ADC can be used to verify the error.

The internal monitors can be manually trigger to check if the detector works correctly, by settling appropriately the bits on LDO_PSM_TRIP_TEST_EN.

ROM and MEMMAP CRC

If an error is found at power-up during the ROM verification, or the internal memory map is corrupted, the AD7779 generates an error, setting MEMMAP_CRC_ERR or ROM_CRC_ERR, depending on the source of the error.

The checker can be disable by clearing bits MEMMAP_CRC_TEST_EN and ROM_CRC_TEST_EN

The part needs to be reset if any of this error triggers.

ΣΔ ADC ERRORS

REFERENCE DETECT (SPI Control Mode)

In SPI control mode, the AD7779 includes on-chip circuitry to to detect if there is a valid reference for conversions or

calibrations when the user selects an external reference as the reference source. If the voltage between the selected REFx+ and REFx– pins goes below 0.3 V, or either the REFx+ or REFx– inputs are open circuit, the AD7779 detects that it no longer has a valid reference CHx_ERR_REF_DET can be interrogated to identify the affected channel, which will clear the bit register if the error is no longer present. The voltage detector can be disable by clearing REF_DET_TEST_EN bit.
The sigma-delta ADC diagnostic or the SAR ADC can be used to verify the error.

Over and Under voltage

The AD7779 includes on chip over/under voltage circuitry on each analog input pin. When the voltage on an analog input pin goes above the specified limit, an alert is flagged.
If an under voltage event occurs the Ain_UV bit is set.

CHx_ERR_AINM_UV, CHx_ERR_AINM_OV, CHx_ERR_AINP_UV, and CHx_ERR_AINP_OV bits can be readback to verify the affected channel input, which will clear the bit register if the error is no longer present.
The over voltage and under voltage detection can be disable independently by clearing AINM_UV_TEST_EN, AINM_OV_TEST_EN, AINP_UV_TEST_EN or AINP_OV_TEST_EN bits.

The input voltage can be checked independently with the SAR ADC.

Modulator Saturation

The AD7779 includes modulator saturation detection on each of the sigma delta ADC's. If 20 consecutive codes for the modulator are either all 1's or 0's this will be flagged as a modulator saturation event.
Reading the CHx_ERR_MOD_SAT will clear the bit if the error has corrected itself.

The detection can be disable by clearing MOD_SAT_TEST_EN bit.

Filter Saturation

TheAD7779 includes digital filter saturation detection on each ΣΔ ADC channel. This will indicate that the filter output is out of bounds. Reading the CHx_ERR_FILTER_SAT bit will clear the bit if the error has corrected itself.

The detection can be disable by clearing FILTER_SAT_TEST_EN bit.

Output saturated

An output Saturation event can occur when gain and offset calibration causes the output from the digital filter to clip at either +Full-scale or –Full-scale, this output will not wrap. Reading the CHx_ERR_OUTPUT_SAT bit will clear the bit if the error has corrected itself.

The detection can be disable by clearing OUTPUT_SAT_TEST_EN bit.

SPI Transmission errors (SPI Control Mode)

All SPI errors are cleared after reading GEN_ERR_REG_1 which contains the SPI errors.

CRC Checksum error

If the CRC checksum is enable by setting SPI_CRC_TEST_EN bit, an error bit, SPI_CRC_ERR, is raised if the CRC message does not match the message computed by the AD7779 internal CRC block. If the CRC message does not match the internally computed message, the register is not updated.

SCLK Counter

If the number of clocks generated by the controller is not multiple of 8 after /CS is pulled high, an error bit is raised, SPI_CLK_COUNT_ERR.

The SCLK counter can be disable by setting SPI_CLK_COUNT_TEST_EN bit.

Invalid Read

When an invalid register is trying to readback, the SPI_INVALID_READ_ERR bit is set.

The invalid readback address detection can be disable by setting SPI_INVALID_READ_TEST_EN bit.

Invalid Write

When an invalid register is trying to write, the SPI_INVALID_WRITE_ERR bit is set.

The invalid write address detection can be disable by setting SPI_INVALID_WRITE_TEST_EN bit.

MONITORING USING THE AD7779 SAR ADC (SPI CONTROL MODE)

The AD7779 contains an on-chip SAR ADC for chip diagnostics, system diagnostics, or measurement verification. The SAR ADC is a 12-Bit ADC. The AVDD4, AVSS4 operate in complete independence of the ΣΔADC Supplies and therefore can be used for chip diagnostics in systems where functional safety is important. The reference for the SAR conversion process the reference is taken from the SAR ADC supply voltage (AVDD4-AVSS4) and therefore the SAR analog input range is from AVSS4 to AVDD4.

The SAR ADC will have a maximum throughput rate of 256 kSPS. The SAR_CONVST pin is used to initiate a conversion on the SAR ADC. The maximum allowable frequency of this SAR_CONVST pin is 256 kHz.

The SAR ADC is only available in SPI control mode. To read conversion results from the SAR ADC requires to set SAR_DIAG_MODE_EN bit. Once this bit is set all subsequent SPI reads will be from the SAR ADC register, as shown in Figure 24.

To minimize the effects of the SAR conversion process on the precision Sigma Delta conversions the SAR_CONVST signal can be internally synchronized with the Sigma Delta clock by clearing CONVST_MOD_ALIGN_DIS bit. This synchronization time is factored into the max SAR conversion time with synchronization enabled.

In addition, the SAR_CONVST pin implements a de-glitcher circuit to avoid false triggers due to noise or other spurious signals. The de-glictcher can be enable by clearing CONVST_DEGLITCH_DIS.

Prior to the SAR ADC, the AD7779 contains an internal multiplexer. This multiplexer can be configured over the SPI interface to set the inputs to the SAR ADC to be either internal circuit nodes in the case of diagnostics or select the external AUX_IN+ and AUX_IN- pins.

Along with converting external voltages, the SAR ADC can be used to monitor the internal nodes on the AVDD, IOVDD and DGND pins, and can monitor the DLDO and ALDO outputs. Some voltages are internally attenuated by 6, and the resulting voltage is applied to the SAR ADC, as shown in Table 26. This is useful because variations in the power supply voltage can be monitored.

The input multiplexer of the SAR is controlled by the GLOBAL_MUX_CONFIG register and the different inputs available are described in Table 26.

The SAR ADC also contains an ADC driver amplifier, as shown in Figure 23. This amplifier will settle the SAR input to 12-Bit accuracy within the tacq time. This driver amplifier will help to minimize the kick back from the SAR converter to the diagnostic/SAR_Mux input circuit nodes.

The Auxiliary inputs, AUX_IN+ and AUX_IN-, can be used to validate the Sigma Delta measurements. While operating in SPI mode the AD7779 will have 3 available GPIO ports controlled via the SPI interface.

The GPIO pins can be used to control an external dual 8:1 multiplexer which in turn is used to sample the 8 sigma delta channels. This diagnostic can be used in applications where functional safety is required. This can aid with removing the need for a secondary external ADC to validate primary measurements on the sigma delta channels.

Table 26. SAR Mux Inputs

SAR Input	Signal+	Signal–	Attenuation ÷6
0	AUX_IN+	AUX_IN-	No
1	Vbe	AVSSx	No
2	REF1+	REF1–	No
3	REF2+	REF2–	No
4	REF_OUT	AVSS1B	No
5	VCM	AVSS1A	No
6	AReg1Cap	AVSS1A	Yes
7	AReg2Cap	AVSS1B	Yes
8	DREGCAP	DGND	Yes
9	AVDD1A	AVSS1A	Yes
10	AVDD1B	AVSS1B	Yes
11	AVDD2A	AVSS1A	Yes
12	AVDD2B	AVSS1B	Yes
13	IOVDD	DGND	Yes
14	AVDD4	AVSS4	No
15	DGND	AVSS1A	Yes
16	DGND	AVSS1B	Yes
17	DGND	AVSS4	Yes
18	AVDD4	AVSS4	Yes
19	REF1P	AVSS1A	No
20	REF2P	AVSS1B	No
21	AVSS4	AVDD4	Yes

Temperature Sensor

The internal die temperature can be measured with an error of ±2°C. The Vbe is proportional to the temperature measured referred to 25°C

$$Temperature\ (°C) = \frac{Vbe - 0.6V}{2mV}$$

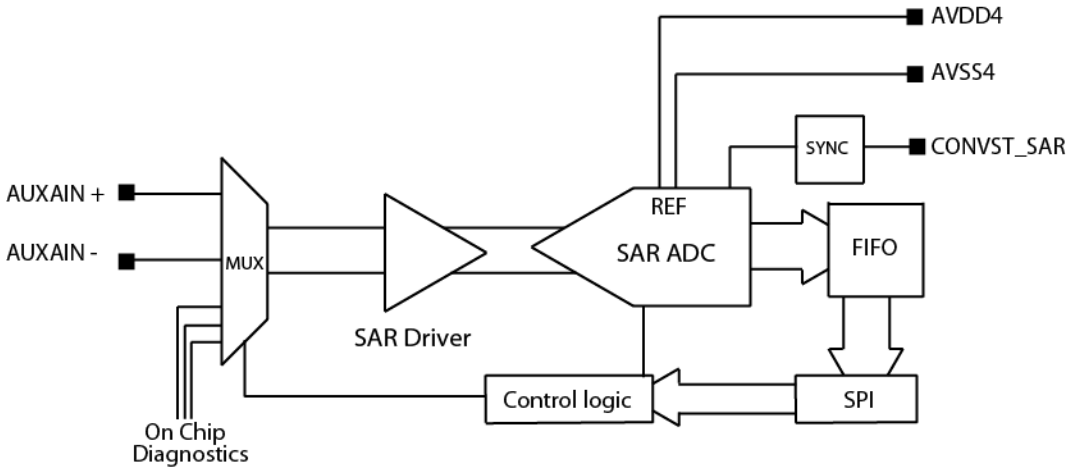


Figure 23 SAR_ADC Configuration and Control

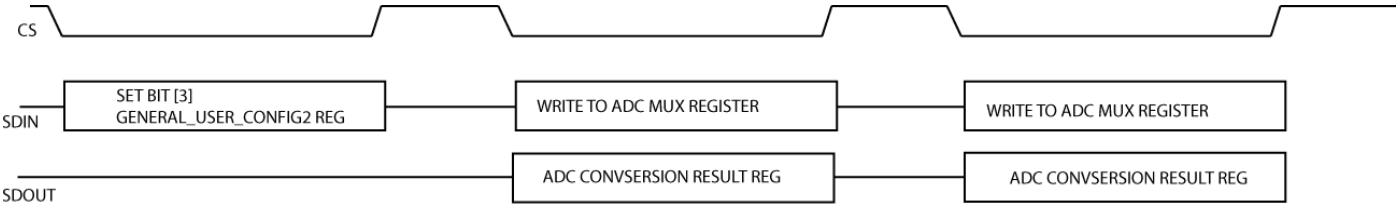


Figure 24 Configuring the AD7779 to operate the SPI to read from the SAR ADC

ΣΔ ADC DIAGNOSTIC (SPI CONTROL MODE)

The AD7779 SD ADC Diagnostic functions are accessible through the SPI interface. The internal mux placed before the PGA has different inputs allowing to select a zero scale, positive full-scale or negative full-scale input to the ΣΔ ADC, which can be converted to verify the correct operation of the ΣΔ ADC channel.

The diagnostic input mux is shared across all the ΣΔ channels. Depending on the diagnostic selected the ΣΔ ADC reference should be connected to a different reference source to guarantee that the conversion will be within measurable range. In addition, the ΣΔ mux of channel 0 is internally connected to the SAR input mux.

There are two different ways to enable the diagnostic mux,

1- Setting CHx_RX bit

This bit will enable the input SD mux. The multiplexer inputs are described in Table 27.

The reference used during the conversions are controlled by REF_MUX_CTRL bits

2- Setting CHx_REF_MONITOR

This bit has the same effect that enabling the CHx_RX bit and select as main reference VDD1x-AVSSx supplies.

If the AINx+/– pin is connected to AVSSx, the input range is outside range (AVSSx + 100mV) so results may differ slightly than expected value.

The inputs can be used alternatively to calibrate gain and offset errors.

Table 27. ΣΔ diagnostic

Input	Voltages	Recommended Voltage Reference	Notes/Result
0	Floating		
1	SAR mux input	Internal/External	Only available in Channel 0
2	280mV differential signal	Internal/External	PGA gain calibration
3	External reference +/–	External	Positive Full Scale
4	External reference –/+	External	Negative Full Scale
5	External Reference –/–	External	Zero Scale
6	Internal reference +/–	Internal	Positive Full Scale
7	Internal Reference –/+	Internal	Negative Full Scale
8	Internal Reference –/–	Internal	Zero Scale
9	External Reference +/+	External	Zero Scale

AD7779 SD OUTPUT DATA

ADC CONVERSION OUTPUT: HEADER & DATA

The AD7779 sigma-delta conversion results are output on the DOUT0 to DOUT3 pins or over the SPI depending on the selected interface. If the DOUTx Interface is selected, the AD7770 acts as master in the transmission, while in SPI interface the controller is the master.

Independently of the interface selected to readback the SD conversion, the /DRDY signal generates the end of conversion. When the SPI is used to readback the SD conversion, if a new conversion is completed (/DRDY low) before the previous conversion had been readback, the results from previous conversion will be overwritten and consequently previous conversion corrupted.

For each channel the with is of 32-bits length, 8-bits for the header and 24-bits for sigma-delta conversion, as shown in Figure 25

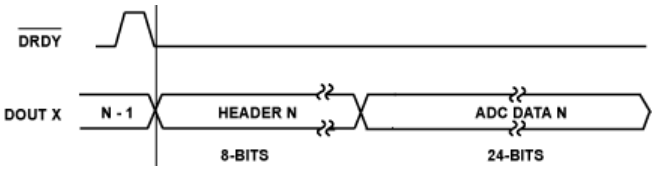


Figure 25. ADC Output: 8 Bit Header + 24 Bit Conversion Data

In PIN control mode, the header is fixed to CRC while in SPI mode, ca be selected between CRC or error headers.

CRC header

This is the header generated in PIN control mode or in SPI mode if DOUT_HEADER_FORMAT is set.

As shown in Figure 26, the header consists of a chip error bit, 3-bits for the ADC channel, as shown in Table *28*, and 4-bits for CRC.

The Chip error bit is set high if an error has been detected in any channel, as explained in GENERAL ERRORS section. The Chip Error remains '1' until the error disappears.

Figure 26. CRC header

Chip Error	Ch no.	Ch no.	Ch no.	CRC	CRC	CRC	CRC

Table 28. Channel ID

	CH ID2	CH ID 1	CHID 0
CH0	0	0	0
CH1	0	0	1
CH2	0	1	0
CH3	0	1	1
CH4	1	0	0
CH5	1	0	1
CH6	1	1	0
CH7	1	1	1

The CRC generated is 8-bit long; the CRC 4 MSBs are placed on the header for the first channel in the pairing and the 4 LSBs on the header of the second channel in the pairing, as shown below

CH2 header,

CE	0	1	0	CRC7	CRC6	CRC5	CRC4

CH3 header

CE	0	1	1	CRC3	CRC2	CRC1	CRC0

If a channel is disabled, the 24-bit output data for this channel is 0x000000

ERROR Header (SPI Control Mode)

In SPI control mode, the default header can be replaced by an error header. If the SD conversion is readback thru the SPI interface, the CRC should be disable by clearing the SPI_CRC_TEST_EN bit. In case of the DOUTx interface is uses, the DOUT_HEADER_FORMAT bit should be clear. The error header provides information of common error sources specific for each channel as shown in Table 29. Modulator and filter errors are indicated even if the checker for this error has been specifically disable as described in ΣΔ ADC ERRORS.

*Table 29. S*tatus Header output

Bit	Name	Description
7	CHIP_ERROR	It is set HI if any of the enabled diagnostic functions have detected an error External Clock not detected, Memory Map bit flip, Internal CRC error. Not Channel specific.
6:4	CH ID [2:0]	Indicates which ADC channel the following conversion data came from, see Table *28*
3	Reset Detected	This bit indicates if a reset condition has occurred. Not channel specific
2	MODULATOR SATURATE	Indicates that the modulator has outputted 20 consecutive 0's or 1's
1	FILTER SATURATE	Indicates that the filter output is out of bounds.
0	AIN_OV_UVERROR	Indicates that there has been an AINx+ over/under voltage condition on the inputs

SAMPLE RATE CONVERTER (SRC) (SPI CONTROL

MODE)

The AD7779 implements a patented featured called Sample Rate Converter on each ΣΔ channel which allows to configure the output data rate to any desired value including non-integers values. The SRC achieves fine resolution control over the ΣΔ ADC ODR. In applications where the ODR needs to change based on changes in the input signal in order to maintain sampling coherency the SRC can be used to provide this fine control over the ODR. For example in Power Quality Applications to achieve the highest classification standard, Class A, it is required to be able to maintain coherency for 0.01 Hz changes in the input power line. The SRC can be used to achieve this sampling frequency accuracy.

In the Pin Control mode, the ODR is fixed as per the predefined pin control options consequently a non-integer numbers cannot be selected, as shown in **Table *15***.

In order to set the ODR the user may have to program up to four registers depending on the decimation value, 2 registers to program the integer value N(effective decimation rate) and 2 registers to program the decimal value, IF(interpolation factor).

The integer value registers are SCR_N_MSB[3:0] and SCR_N_LSB[7:0].

The decimal part value registers are SCR_IF_MSB[7:0] and SCR_IF_LSB[7:0].

As an example, if an output data rate of 2.8 kHz is required, which equates to,

HP = 2048 / 2.8 = 731.428

LP = 512 / 2.8 = 182.857

The register values for the HP mode are,

731d = 0x2DB

SCR_N_MSB[3:0] = 0x02

SCR_N_LSB[7:0] = 0xDB

0.428d -> 0.428x2^16=28049d = 0x6D91

SCR_IF_MSB[7:0] = 0x6D

SCR_IF_LSB[7:0] = 0x91

The ODR can be updated on the fly but new ODR will be effective in 3 conversion cycles of the ΣΔ ADCs. This guarantee a smooth transition with no conversion results out of range.

There are two different ways to change the ODR, once a new value is written in the SRC registers, by software or by hardware, depending on the SRC_UPDATE[7].

If the SCR_LOAD_SOURCE bit is '0', the new ODR value is updated by setting the SRC_LOAD_UPDATE bit to '1'.

The bit needs to held high for at least two MLCK period, and should be returned to '0' before attempting another update.

If the SRC_LOAD_SOURCE is '1' the ODR will be controlled externally by the GPIO0 pin.

A pulse should be applied in GPIO2 pin, which is then internally synchronized with the external MCLK clock, and the resultant synchronous signal is output on the GPIO1 pin.

The GPIO1 and GPIO0 pins must be externally connected.

If multiple AD7779 needs to be synchronized, the GPIO1 pin of one device can be connected to multiple parts. This synchronization method requires the use of a common MCLK signal for all the AD7779 connected, as shown in Figure 27

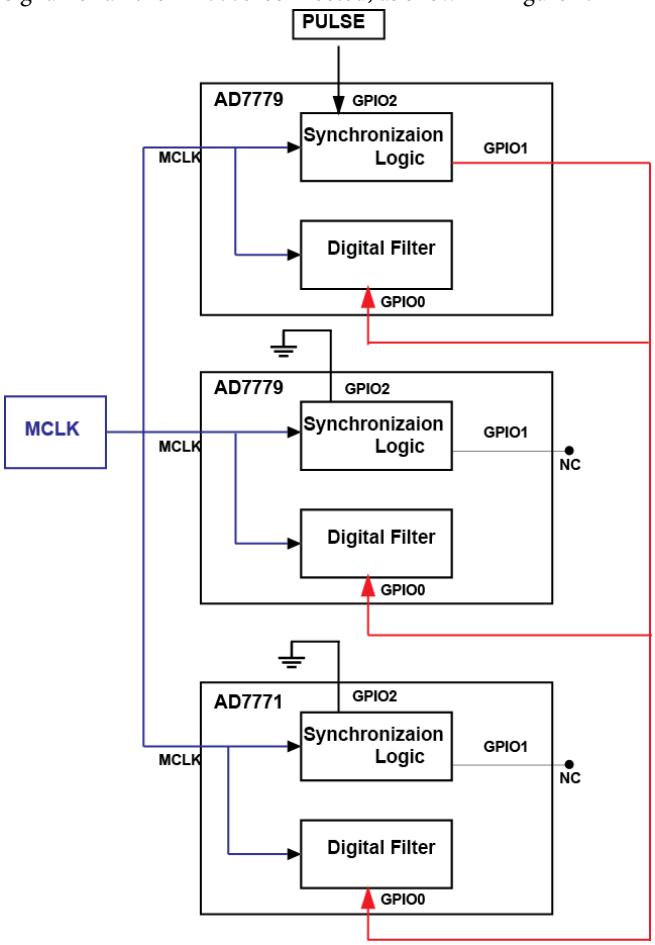


Figure 27. Hardware ODR update

Maximum ODR Configuration

Table ***30*** and Table 31 show the maximum output data rate achievable and the minimum DCLK frequency required for a given DOUT pin configuration. In SPI mode, the DCLK divide is set using the Data Format register, see DOUT3-DOUT0 Data Interface.

In Pin control mode the DCLK divide is selected using the unused SDI, SCLK, SDO pins. See ***Table 16*** for DCLK divide settings in Pin mode.

Table 30.High Resolution mode

Dec Rate	ODR KSPS	1 DOUT Min DCLK (kHz)	2 DOUT Min DCLK (kHz)	4 DOUT Min DCLK (kHz)
4095	0.500122	128	64	32

2048	1	256	128	64
1024	2	512	256	128
512	4	1024	512	256
256	8	2048	1024	512
128	16	4096	2048	1024

Table 31. Low Power Mode

Dec Rate	ODR KSPS	1 DOUT Min DCLK (kHz)	2 DOUT Min DCLK (kHz)	4 DOUT Min DCLK (kHz)
2048	0.25	64	32	16
1024	0.5	128	64	32
512	1	256	128	64
256	2	512	256	128
128	4	1024	512	256

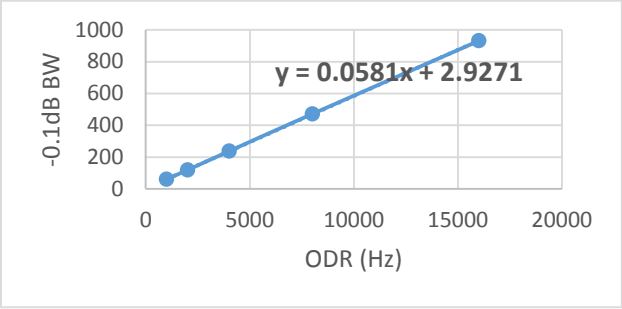
SRC Bandwidth

The new SINC filter architecture allows selecting a non-integer value as output data rate. This versatility means that the filter notches need to be adjusted dynamically, 2 notches at variable frequency, and one fixed notch to remove PGA chopping tone. Consequently the traditional formula for −0.1dB and −3dB bandwidth needs to be adjusted depending on the selected decimation rate.

The bandwidth transfer function is not linear but could be approximated by using a linear function.

Figure 28and Figure 29 shows the bandwidth for −0.1dB and −3dB bandwidth. In low power mode the offset needs to be divided by four, ie. ODR = 1k, -0.1dB point is,

$$BW = 0.0581 \times 1000 + \frac{2.9271}{4} = 59Hz$$



DATA OUTPUT INTERFACE

The SD output data interface is defined by /CONV_SAR, FORMAT0 and FORMAT1 pins in Pin Control Mode at power-up. FORMAT pins cannot be changed dynamically. ***Table 16*** shows the available options for PIN control mode. If the part is configured in SPI control mode, the register SPI_SLAVE_MODE_EN will enable the SPI interface to transmit the ΣΔ ADC conversion results, as shown in Table 23.

Figure 28. –0.1dB correction factor

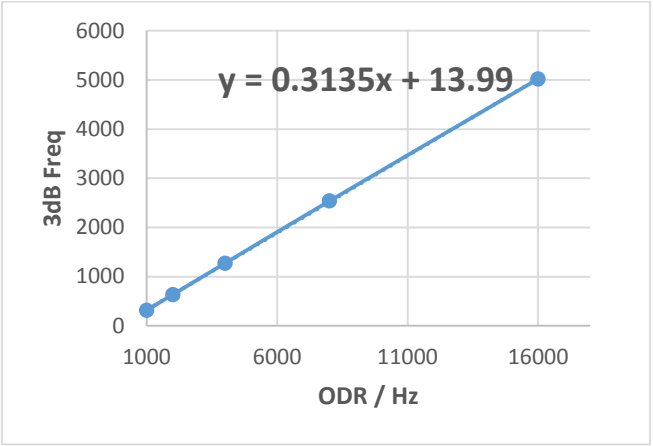


Figure 29. –3dB correction factor

SRC group delay

The group delay depends on the selected ODR and power mode, and it is defined by the following equation,

$$Group\ delay = \frac{PM + SRC\_N}{SRC\_N \times ODR}$$

Where, SRC_N is the natural value of the programmed ODR.

ODR is the programmed output data rate. PM is a value that depends on the power mode, 64 for HR and 32 for LP.

Settling Time

The settling time is the defined by the contribution of all the internal stages, filter delay and block calibration.

The filter delay is defined as 3/ODR. In some extreme cases, as an external pulse applied, this value could go up to 4/ODR.

The calibration delay is defined as,

HR mode: $62\ x\ t_{MCLK}$

With a maximum error of $2\ x\ t_{MCLK}$

LP mode: $121\ x\ t_{MCLK}$

With a maximum error of $4\ x\ t_{MCLK}$

where,

T_{MCLK} is the modulator period, 488ns in HR and 1.9us in LP.

DOUT3-DOUT0 Data Interface

Stand-alone mode

In this mode the AD7779 interface acts as a master. There are 3 different DOUT configurations, configurable through the FORMAT pins in Pin control mode, as shown in Figure 30, or via DOUT_FORMAT[7:6] register in SPI control mode, as described in Table 32.

Table 32. Dout channels

DOUT _FORMAT	Number of DOUT lines enabled	Associated Channels
00	4 DOUTs Enabled	DOUT0 – CH0 – CH1
		DOUT1 – CH2 – CH3
		DOUT2 – CH4 – CH5
		DOUT3 – CH6 – CH7
01	2 DOUTs Enabled	DOUT0 – CH0 – CH1-CH2-CH3
		DOUT1 – CH4 – CH5-CH6-CH7
10	1 DOUT Enabled	DOUT0 - CH0 – CH1-CH2-CH3– CH4 – CH5-CH6-CH7

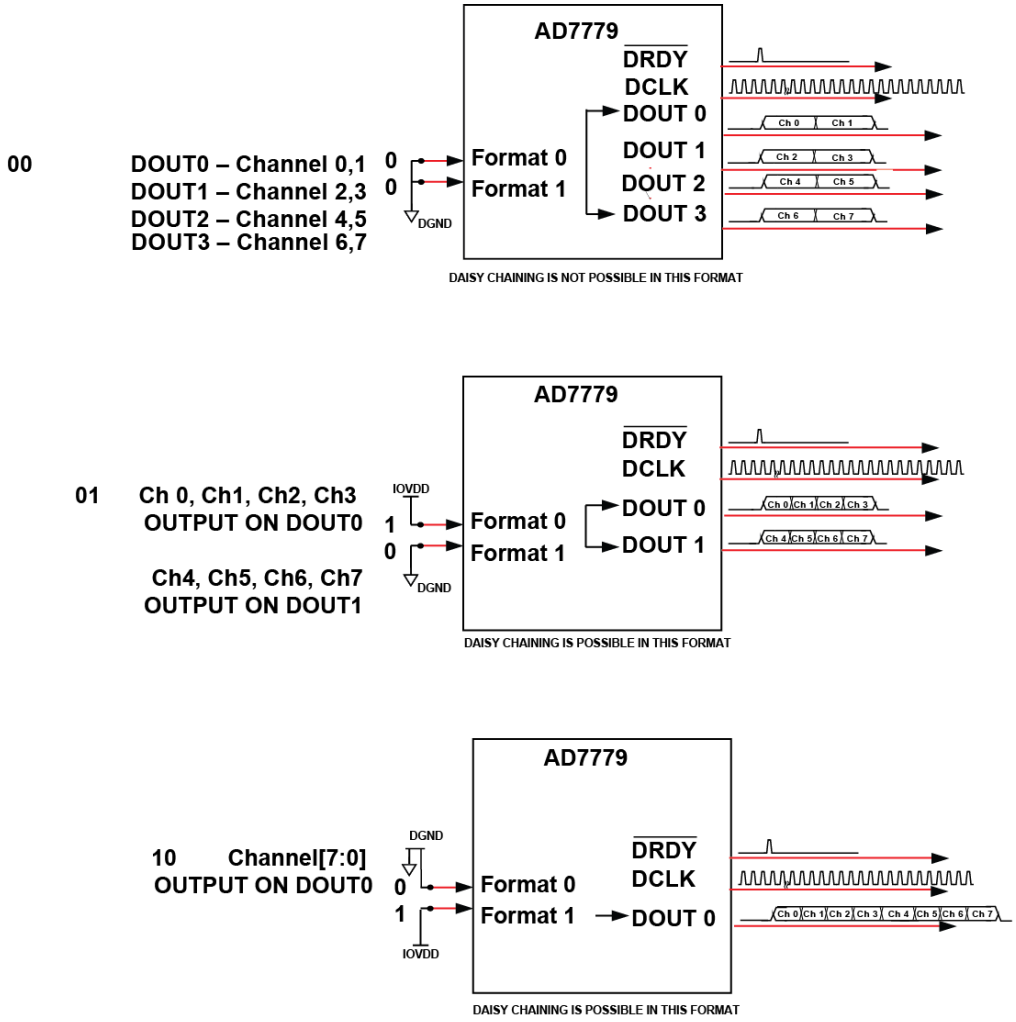


Figure 30. Format Pin configuration

The DCLK frequency should be selected in such a way that the data is completely shifted out before a new conversion is completed, otherwise previous conversion will be overwritten and consequently transmission corrupted. The minimum DCLK frequency is defined by the decimation rate, and the lines enable on the DOUT3-DOUT0 Data Interface,

$DCLK_{MIN\_RATIO}$ < decimation / (8 * CHANNELS_PER_DOUT)

As example, operating in Master Interface Mode, DOUT mode 2, each Doutx will shift out four channels, and assuming a maximum output rate in HR mode, decimation = 128

$DCLK_{MIN\_RATIO}$ < 128/8 * 4 = 4

If the DCLKMIN_RATIO is selected above the minimum necessary, a logic '0' will be continuously transmitted until a new sample is available

Figure 31, Figure 32, and Figure 33 show expected data output for different DOUT output modes.

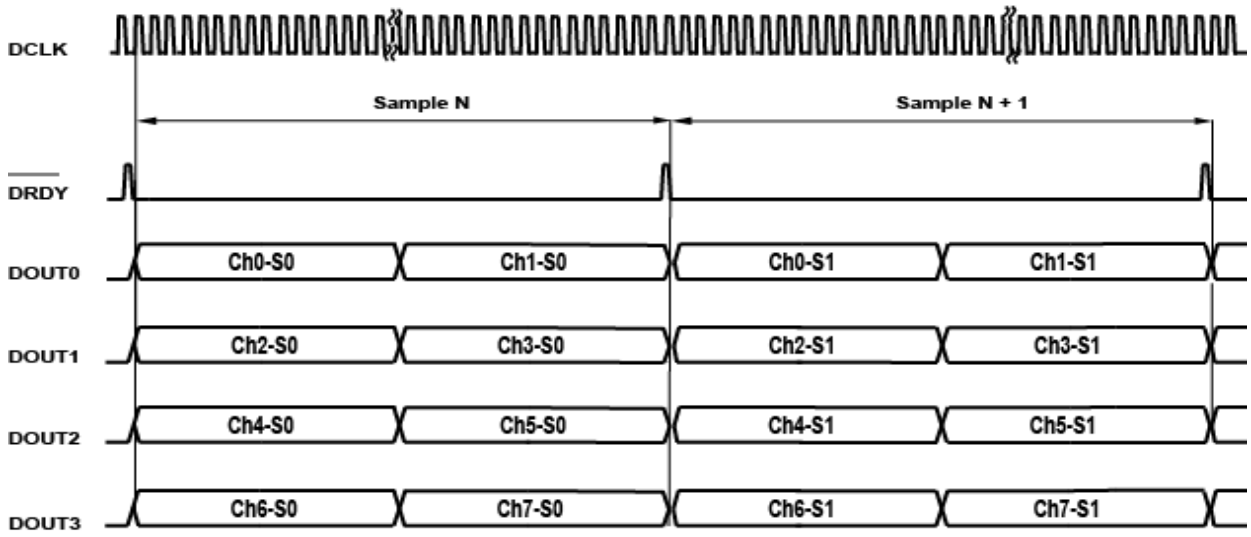


Figure 31 FORMAT [00] Each DOUT outputs 2 ADC conversions, maximum data rate (S0= Sample 0; S1= Sample1)

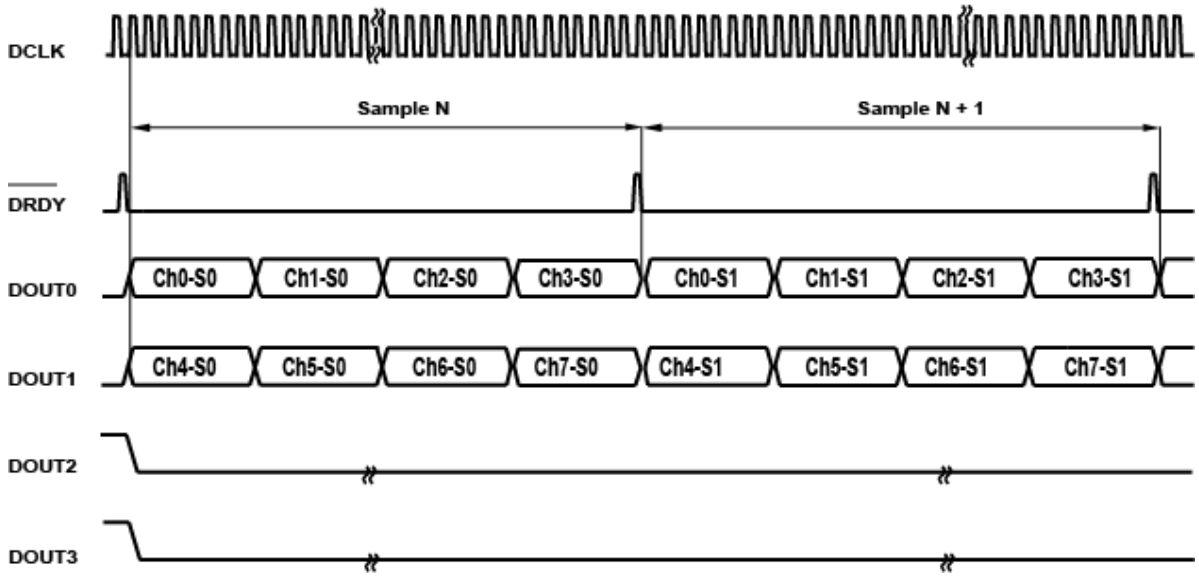


Figure 32 FORMAT [01] Ch0-3 share DOUT0, and Ch4-7 share DOUT1, maximum data rate (S0= Sample 0; S1= Sample1)

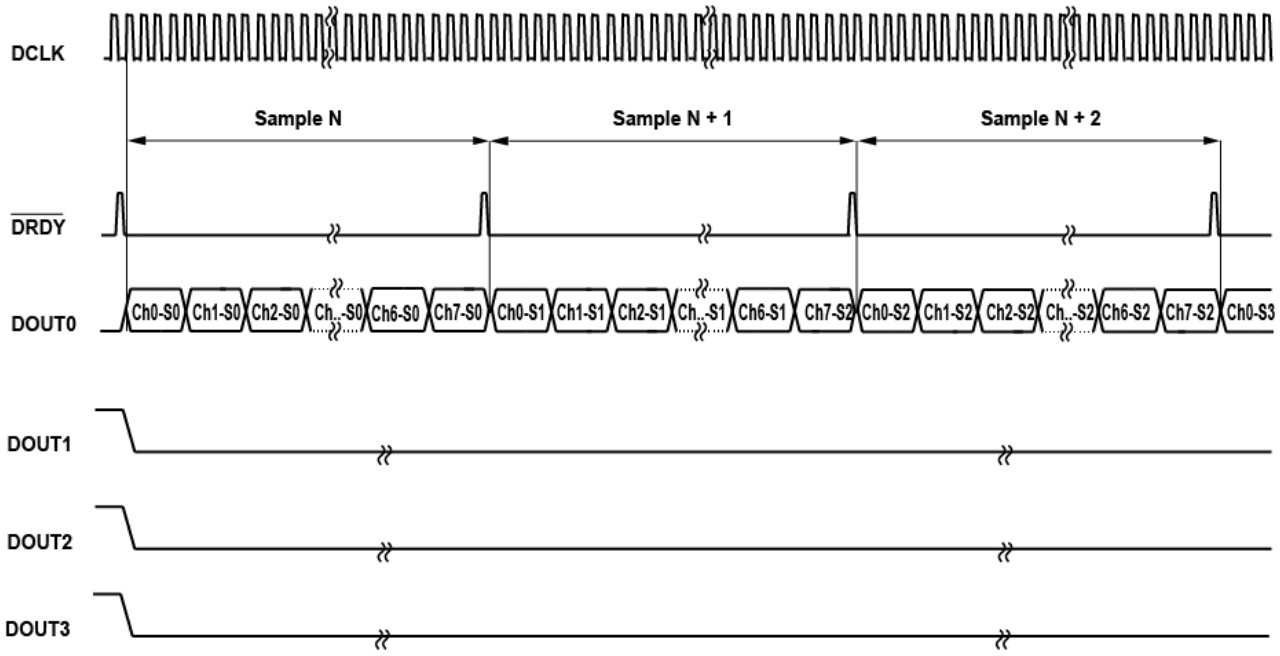


Figure 33 FORMAT [10] Ch0-7 output on DOUT0 only, maximum data rate (S0= Sample 0; S1= Sample1)

If the AD7779 operates in SPI Control mode, it is possible to adjust the DOUTx strength, which can be selected in DOUT_DRIVE_STR bits, as described in Table 33.

Table 33. DOUTx strength

GENERAL_USER_CONFIG2[4:3]		Mode
0	0	Normal
0	1	Strong
1	0	Weak
1	1	Extra Strong

Daisy Chain mode

Daisy chaining devices allows numerous devices to use the same data interface lines by cascading the outputs of multiple ADCs from separate AD7779 devices. In Daisy Chain configuration only one ADC device has direct connection between the data interface and the digital host. For AD7779 Daisy Chain capability is implemented by cascading DOUT0 and DOUT1 through a number of devices, or just using DOUT0, this depends on the selected DOUT mode. The ability to daisy chain devices and the limit on the number of devices that can be handled by the chain is dependent on the selected DOUT mode and Decimation Rate employed.

When operating in Daisy Chain Mode it is required that all AD7779 devices in the chain are correctly synchronized, please refer to Synchronization pins for additional info.

This feature is especially useful for reducing component count and wiring connections, for example, in isolated multi-converter applications or for systems with a limited interfacing capacity.

For daisy-chain operation, there are two different configurations possible as described in Table 34.

Table 34. Dout modes daisy-chain

DOUT MODES	Associated Channels
01	DOUT0 – CH0 – CH1-CH2-CH3
	DOUT1 – CH4 – CH5-CH6-CH7
	DOUT2 – DIN0
	DOUT3 – DIN1
10	DOUT0 - CH0 – CH1-CH2-CH3– CH4 – CH5-CH6-CH7
	DOUT2 – DIN0

In this mode, DOUT2 and DOUT3 acts as input pins Figure 34 shows the example of using the DOUT 10 mode. In this case, the DOUT0 pins of the AD7779 devices are cascaded to the DOUT2 pins of the next device in the chain. Data read-back is analogous to clocking a shift register where data is clocked on the rising edge of DCLK.

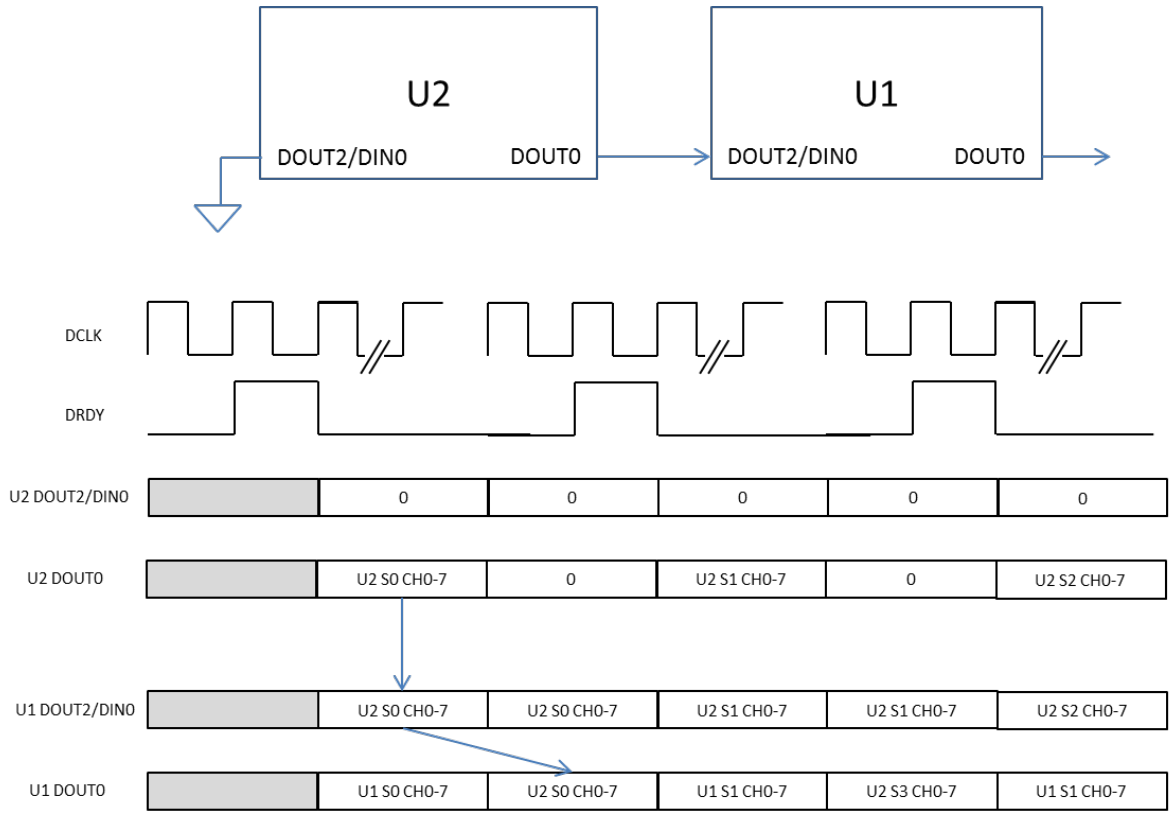


Figure 34. Daisy chain connection mode [10]

The $DCLK_{MIN\_RATIO}$ in defined by the number of devices connected, the decimation rate and the number of channels enabled. As an example, assuming mode 01, 3 devices connected and 256 decimation rate,

$DCLK_{MIN\_RATIO}$ < decimation / (8 * DEVICES*(DOUT_CHANNELS)^2)

$DCLK_{MIN\_RATIO}$ < 256 / ((8^2) * 3) = 1.3 => 1

SPI Interface

The SPI interfaces gives the flexibility to read the conversion from the sigma-delta ADC where the processor or ucontroller is the master.

When a new conversion is completed, the $\overline{DRDY}$ signal is toggled to indicate that data can be accessed. When $\overline{DRDY}$ toggles, the internal channel counter is reset and the next SPI read will be from Channel 0 again. Conversely, after the last Channel data is read all succeeding reads before the next $\overline{DRDY}$ signal will be from Ch7-LSB

The SPI operates in multiples of 8 bits frame; Figure 35 shows a readback example in 16 bits frames, while Figure 36 shows a readbakc in 24-bits frame.

Figure 35. SD 16 bits frame

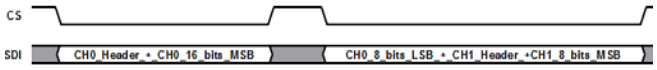


Figure 36. SD 24 bits frame

If the part is configured in SPI control mode, the AD7779 will generate a software reset if the SDI is sample high for 64 consecutive clocks. To avoid a reset, and unwanted register writes, it is recommended to transfer a 0x8000 command, which generates readback command that will be ignored by the part as explained in ΣΔ DATA ADC mode.

HOW TO CALCULATE THE CRC CHECKSUM

The AD7779 implements two different CRC checksum generators, one for the sigma-delta results and another for the SPI control mode.

The AD7779 uses a CRC polynomial to calculate the CRC Check Sum value. The 8-bit CRC polynomial used is $x^8 + x^2 + x + 1$.

The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An XOR (exclusive OR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

As an example of CRC calculation for a 12-bit data is as follow,

Data	0	1	1	0	0	1	0	0	1	1	1	0
Polynomial		1	0	0	0	0	0	1	1			
			1	0	0	1	0	1	0	1	1	0
			1	0	0	0	0	0	1	1		
CRC					0	1	0	1	1	1	1	0

Sigma-delta CRC checksum

The CRC message is calculated internally by the AD7779 on ADC pairs. The CRC is calculated using the ADC output data from two ADC's and bits 7:4 from the header. Therefore, 56-bits are used to calculate the 8-bit CRC. This CRC is split between the two channel headers. CRC data cover channel pairings as follows CH 0&1, 2&3, 4&5, 6&7.

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 1s.

The CRC is calculated from 56-bits across two consecutive/pairing channels, 0-1, 2-3, 4-5, 6-7. The 56-bits consist of the Chip Error, the 3-bits for the first ADC pairing channel and the 24 bits of data of each pairing channel. An example for the second pairing channel CH2&CH3,

56 bits = Chip Error + 3 ADC channel bits (010) + 24 data bit CH2 + Chip Error + 3 ADC channel bits (011) + 24 data bits CH3

SPI Control Mode Checksum

The CRC message is calculated internally by the AD7779. The data transferred to the AD7779 should uses the W/R bit, 7 bits address and 8 bits data for the CRC calculation.

The CRC calculated and appended to the data that it is shift out uses 0010 0000 header and 8 bits data for register readback, and the 0010 header and 12 bits SAR conversion data for SAR readback transfers.

REGISTER SUMMARY: AD7779 MEMORY MAP (AD7779_MEMMAP_DS)

Table 35. AD7779_memmap_DS Register Summary

Address	Name	Description	Reset	Access
0x00	CH0_CONFIG	Channel 0 Configuration.	0x00	R/W
0x01	CH1_CONFIG	Channel 1 Configuration.	0x00	R/W
0x02	CH2_CONFIG	Channel 2 Configuration.	0x00	R/W
0x03	CH3_CONFIG	Channel 3 Configuration.	0x00	R/W
0x04	CH4_CONFIG	Channel 4 Configuration.	0x00	R/W
0x05	CH5_CONFIG	Channel 5 Configuration.	0x00	R/W
0x06	CH6_CONFIG	Channel 6 Configuration.	0x00	R/W
0x07	CH7_CONFIG	Channel 7 Configuration.	0x00	R/W
0x08	CH_DISABLE	Disable clocks to ADC channel.	0x00	R/W
0x09	CH0_SYNC_OFFSET	Channel 0 SYNC Offset.	0x00	R/W
0x0A	CH1_SYNC_OFFSET	Channel 1 SYNC Offset.	0x00	R/W
0x0B	CH2_SYNC_OFFSET	Channel 2 SYNC Offset.	0x00	R/W
0x0C	CH3_SYNC_OFFSET	Channel 3 SYNC Offset.	0x00	R/W
0x0D	CH4_SYNC_OFFSET	Channel 4 SYNC Offset.	0x00	R/W
0x0E	CH5_SYNC_OFFSET	Channel 5 SYNC Offset.	0x00	R/W
0x0F	CH6_SYNC_OFFSET	Channel 6 SYNC Offset.	0x00	R/W
0x10	CH7_SYNC_OFFSET	Channel 7 SYNC Offset.	0x00	R/W
0x11	GENERAL_USER_CONFIG_1	General User Config 1.	0x2C	R/W
0x12	GENERAL_USER_CONFIG_2	General User Config 2.	0x09	R/W
0x13	GENERAL_USER_CONFIG_3	General User Config 3.	0x80	R/W
0x14	DOUT_FORMAT	Data out format.	0x20	R/W
0x15	ADC_MUX_CONFIG	Main ADC meter and reference Mux control.	0x00	R/W
0x16	GLOBAL_MUX_CONFIG	Global diagnostics mux.	0x00	R/W
0x17	GPIO_CONFIG	GPIO config.	0x00	R/W
0x18	GPIO_DATA	GPIO Data.	0x00	R/W
0x19	BUFFER_CONFIG_1	Buffer Config 1.	0x38	R/W
0x1A	BUFFER_CONFIG_2	Buffer Config 2.	0xC0	R/W
0x1C	CH0_OFFSET_UPPER_BYTE	Channel 0 offset upper byte.	0x00	R/W
0x1D	CH0_OFFSET_MID_BYTE	Channel 0 offset middle byte.	0x00	R/W
0x1E	CH0_OFFSET_LOWER_BYTE	Channel 0 offset lower byte.	0x00	R/W
0x1F	CH0_GAIN_UPPER_BYTE	Channel 0 gain upper byte.	0x00	R/W
0x20	CH0_GAIN_MID_BYTE	Channel 0 gain middle byte.	0x00	R/W
0x21	CH0_GAIN_LOWER_BYTE	Channel 0 gain lower byte.	0x00	R/W
0x22	CH1_OFFSET_UPPER_BYTE	Channel 1 offset upper byte.	0x00	R/W
0x23	CH1_OFFSET_MID_BYTE	Channel 1 offset middle byte.	0x00	R/W
0x24	CH1_OFFSET_LOWER_BYTE	Channel 1 offset lower byte.	0x00	R/W
0x25	CH1_GAIN_UPPER_BYTE	Channel 1 gain upper byte.	0x00	R/W
0x26	CH1_GAIN_MID_BYTE	Channel 1 gain middle byte.	0x00	R/W
0x27	CH1_GAIN_LOWER_BYTE	Channel 1 gain lower byte.	0x00	R/W

Address	Name	Description	Reset	Access
0x28	CH2_OFFSET_UPPER_BYTE	Channel 2 offset upper byte.	0x00	R/W
0x29	CH2_OFFSET_MID_BYTE	Channel 2 offset middle byte.	0x00	R/W
0x2A	CH2_OFFSET_LOWER_BYTE	Channel 2 offset lower byte.	0x00	R/W
0x2B	CH2_GAIN_UPPER_BYTE	Channel 2 gain upper byte.	0x00	R/W
0x2C	CH2_GAIN_MID_BYTE	Channel 2 gain middle byte.	0x00	R/W
0x2D	CH2_GAIN_LOWER_BYTE	Channel 2 gain lower byte.	0x00	R/W
0x2E	CH3_OFFSET_UPPER_BYTE	Channel 3 offset upper byte.	0x00	R/W
0x2F	CH3_OFFSET_MID_BYTE	Channel 3 offset middle byte.	0x00	R/W
0x30	CH3_OFFSET_LOWER_BYTE	Channel 3 offset lower byte.	0x00	R/W
0x31	CH3_GAIN_UPPER_BYTE	Channel 3 gain upper byte.	0x00	R/W
0x32	CH3_GAIN_MID_BYTE	Channel 3 gain middle byte.	0x00	R/W
0x33	CH3_GAIN_LOWER_BYTE	Channel 3 gain lower byte.	0x00	R/W
0x34	CH4_OFFSET_UPPER_BYTE	Channel 4 offset upper byte.	0x00	R/W
0x35	CH4_OFFSET_MID_BYTE	Channel 4 offset middle byte.	0x00	R/W
0x36	CH4_OFFSET_LOWER_BYTE	Channel 4 offset lower byte.	0x00	R/W
0x37	CH4_GAIN_UPPER_BYTE	Channel 4 gain upper byte.	0x00	R/W
0x38	CH4_GAIN_MID_BYTE	Channel 4 gain middle byte.	0x00	R/W
0x39	CH4_GAIN_LOWER_BYTE	Channel 4 gain lower byte.	0x00	R/W
0x3A	CH5_OFFSET_UPPER_BYTE	Channel 5 offset upper byte.	0x00	R/W
0x3B	CH5_OFFSET_MID_BYTE	Channel 5 offset middle byte.	0x00	R/W
0x3C	CH5_OFFSET_LOWER_BYTE	Channel 5 offset lower byte.	0x00	R/W
0x3D	CH5_GAIN_UPPER_BYTE	Channel 5 gain upper byte.	0x00	R/W
0x3E	CH5_GAIN_MID_BYTE	Channel 5 gain middle byte.	0x00	R/W
0x3F	CH5_GAIN_LOWER_BYTE	Channel 5 gain lower byte.	0x00	R/W
0x40	CH6_OFFSET_UPPER_BYTE	Channel 6 offset upper byte.	0x00	R/W
0x41	CH6_OFFSET_MID_BYTE	Channel 6 offset middle byte.	0x00	R/W
0x42	CH6_OFFSET_LOWER_BYTE	Channel 6 offset lower byte.	0x00	R/W
0x43	CH6_GAIN_UPPER_BYTE	Channel 6 gain upper byte.	0x00	R/W
0x44	CH6_GAIN_MID_BYTE	Channel 6 gain middle byte.	0x00	R/W
0x45	CH6_GAIN_LOWER_BYTE	Channel 6 gain lower byte.	0x00	R/W
0x46	CH7_OFFSET_UPPER_BYTE	Channel 7 offset upper byte.	0x00	R/W
0x47	CH7_OFFSET_MID_BYTE	Channel 7 offset middle byte.	0x00	R/W
0x48	CH7_OFFSET_LOWER_BYTE	Channel 7 offset lower byte.	0x00	R/W
0x49	CH7_GAIN_UPPER_BYTE	Channel 7 gain upper byte.	0x00	R/W
0x4A	CH7_GAIN_MID_BYTE	Channel 7 gain middle byte.	0x00	R/W
0x4B	CH7_GAIN_LOWER_BYTE	Channel 7 gain lower byte.	0x00	R/W
0x4C	CH0_ERR_REG	Channel 0 Status Register.	0x00	R
0x4D	CH1_ERR_REG	Channel 1 Status Register.	0x00	R
0x4E	CH2_ERR_REG	Channel 2 Status Register.	0x00	R
0x4F	CH3_ERR_REG	Channel 3 Status Register.	0x00	R
0x50	CH4_ERR_REG	Channel 4 Status Register.	0x00	R

Address	Name	Description	Reset	Access
0x51	CH5_ERR_REG	Channel 5 Status Register.	0x00	R
0x52	CH6_ERR_REG	Channel 6 Status Register.	0x00	R
0x53	CH7_ERR_REG	Channel 7 Status Register.	0x00	R
0x54	CH0_1_SAT_ERR	Channel 0/1 DSP errors.	0x00	R
0x55	CH2_3_SAT_ERR	Channel 2/3 DSP errors.	0x00	R
0x56	CH4_5_SAT_ERR	Channel 4/5 DSP errors.	0x00	R
0x57	CH6_7_SAT_ERR	Channel 6/7 DSP errors.	0x00	R
0x58	CHX_ERR_REG_EN	Channel 0-7 Error Reg Enable.	0xFE	R/W
0x59	GEN_ERR_REG_1	General Errors Register 1.	0x00	R
0x5A	GEN_ERR_REG_1_EN	General Errors Register 1 Enable.	0x3E	R/W
0x5B	GEN_ERR_REG_2	General Errors Register 2.	0x00	R
0x5C	GEN_ERR_REG_2_EN	General Errors Register 2 Enable.	0x3C	R/W
0x5D	STATUS_REG_1	Error Status Register 1.	0x00	R
0x5E	STATUS_REG_2	Error Status Register 2.	0x00	R
0x5F	STATUS_REG_3	Error Status Register 3.	0x00	R
0x60	SRC_N_MSB	Decimation Rate (N) MSB.	0x00	R/W
0x61	SRC_N_LSB	Decimation Rate (N) LSB.	0x80	R/W
0x62	SRC_IF_MSB	Decimation Rate (IF) MSB.	0x00	R/W
0x63	SRC_IF_LSB	Decimation Rate (IF) LSB.	0x00	R/W
0x64	SRC_UPDATE	SRC load source and load update.	0x00	R/W

REGISTER DETAILS: AD7779 MEMORY MAP (AD7779_MEMMAP_DS)

CHANNEL 0 CONFIGURATION REGISTER

Address: 0x00, Reset: 0x00, Name: CH0_CONFIG

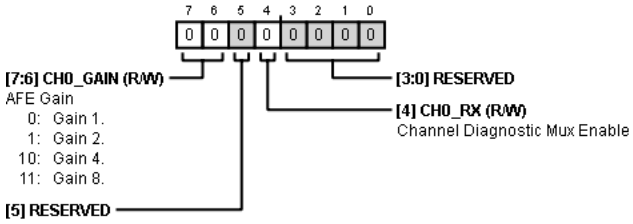


Table 36. Bit descriptions for CH0_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH0_GAIN		AFE Gain	0x0	R/W
		0	Gain 1.		
		1	Gain 2.		
		10	Gain 4.		
		11	Gain 8.		
4	CH0_RX		Channel Diagnostic Mux Enable	0x0	R/W

CHANNEL 1 CONFIGURATION REGISTER

Address: 0x01, Reset: 0x00, Name: CH1_CONFIG

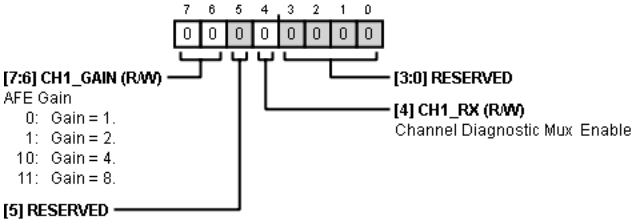


Table 37. Bit descriptions for CH1_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH1_GAIN		AFE Gain	0x0	R/W
		0	Gain = 1.		
		1	Gain = 2.		
		10	Gain = 4.		
		11	Gain = 8.		
4	CH1_RX		Channel Diagnostic Mux Enable	0x0	R/W

CHANNEL 2 CONFIGURATION REGISTER

Address: 0x02, Reset: 0x00, Name: CH2_CONFIG

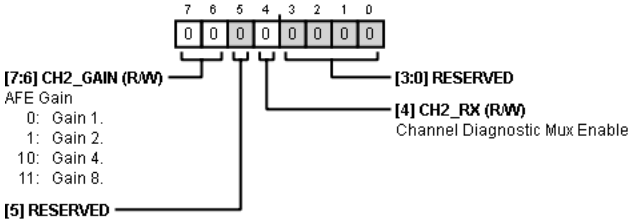


Table 38. Bit descriptions for CH2_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH2_GAIN		AFE Gain	0x0	R/W
		0	Gain 1.		
		1	Gain 2.		
		10	Gain 4.		
		11	Gain 8.		
4	CH2_RX		Channel Diagnostic Mux Enable	0x0	R/W

CHANNEL 3 CONFIGURATION REGISTER

Address: 0x03, Reset: 0x00, Name: CH3_CONFIG

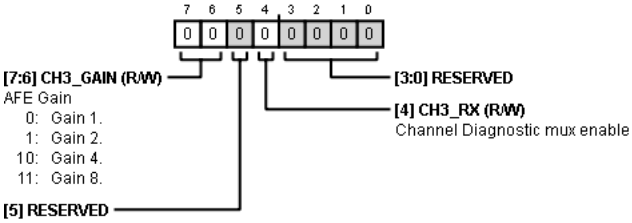


Table 39. Bit descriptions for CH3_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH3_GAIN		AFE Gain	0x0	R/W
		0	Gain 1.		
		1	Gain 2.		
		10	Gain 4.		
		11	Gain 8.		
4	CH3_RX		Channel Diagnostic mux enable	0x0	R/W

CHANNEL 4 CONFIGURATION REGISTER

Address: 0x04, Reset: 0x00, Name: CH4_CONFIG

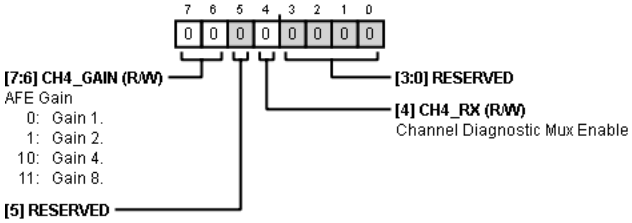


Table 40. Bit descriptions for CH4_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH4_GAIN		AFE Gain	0x0	R/W
		0	Gain 1.		
		1	Gain 2.		
		10	Gain 4.		
		11	Gain 8.		
4	CH4_RX		Channel Diagnostic Mux Enable	0x0	R/W

CHANNEL 5 CONFIGURATION REGISTER

Address: 0x05, Reset: 0x00, Name: CH5_CONFIG

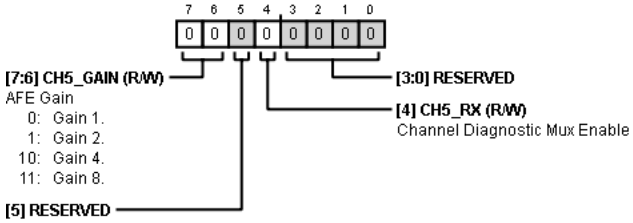


Table 41. Bit descriptions for CH5_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH5_GAIN		AFE Gain	0x0	R/W
		0	Gain 1.		
		1	Gain 2.		
		10	Gain 4.		
		11	Gain 8.		
4	CH5_RX		Channel Diagnostic Mux Enable	0x0	R/W

CHANNEL 6 CONFIGURATION REGISTER

Address: 0x06, Reset: 0x00, Name: CH6_CONFIG

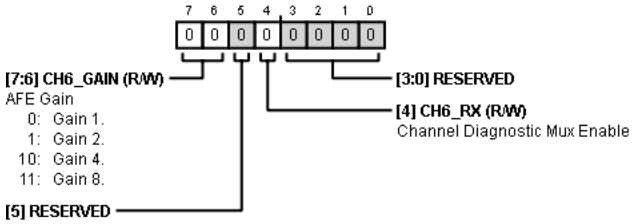


Table 42. Bit descriptions for CH6_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH6_GAIN		AFE Gain	0x0	R/W
		0	Gain 1.		
		1	Gain 2.		
		10	Gain 4.		
		11	Gain 8.		
4	CH6_RX		Channel Diagnostic Mux Enable	0x0	R/W

CHANNEL 7 CONFIGURATION REGISTER

Address: 0x07, Reset: 0x00, Name: CH7_CONFIG

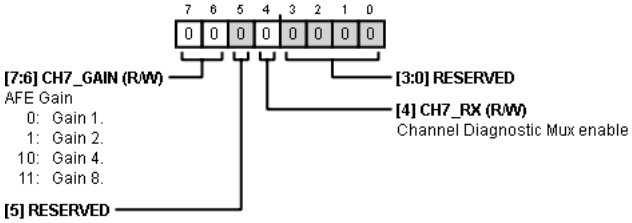


Table 43. Bit descriptions for CH7_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	CH7_GAIN		AFE Gain	0x0	R/W
		0	Gain 1.		
		1	Gain 2.		
		10	Gain 4.		
		11	Gain 8.		
4	CH7_RX		Channel Diagnostic Mux enable	0x0	R/W

DISABLE CLOCKS TO ADC CHANNEL REGISTER

Address: 0x08, Reset: 0x00, Name: CH_DISABLE

.

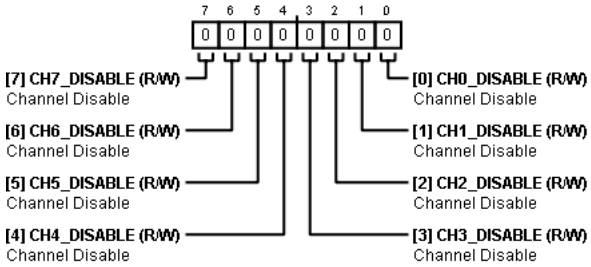


Table 44. Bit descriptions for CH_DISABLE

Bits	Bit Name	Settings	Description	Reset	Access
7	CH7_DISABLE		Channel Disable. Channel 7. 0-Enabled, 1-Standby	0x0	R/W
6	CH6_DISABLE		Channel Disable. Channel 6. 0-Enabled, 1-Standby	0x0	R/W
5	CH5_DISABLE		Channel Disable. Channel 5. 0-Enabled, 1-Standby	0x0	R/W
4	CH4_DISABLE		Channel Disable. Channel 4. 0-Enabled, 1-Standby	0x0	R/W
3	CH3_DISABLE		Channel Disable. Channel 3. 0-Enabled, 1-Standby	0x0	R/W
2	CH2_DISABLE		Channel Disable. Channel 2. 0-Enabled, 1-Standby	0x0	R/W
1	CH1_DISABLE		Channel Disable. Channel 1. 0-Enabled, 1-Standby	0x0	R/W
0	CH0_DISABLE		Channel Disable. Channel 0. 0-Enabled, 1-Standby	0x0	R/W

CHANNEL 0 SYNC OFFSET REGISTER

Address: 0x09, Reset: 0x00, Name: CH0_SYNC_OFFSET

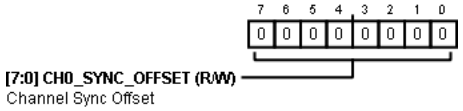


Table 45. Bit descriptions for CH0_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 1 SYNC OFFSET REGISTER

Address: 0x0A, Reset: 0x00, Name: CH1_SYNC_OFFSET

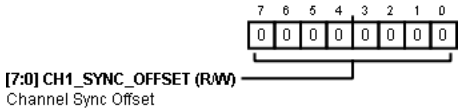


Table 46. Bit descriptions for CH1_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 2 SYNC OFFSET REGISTER

Address: 0x0B, Reset: 0x00, Name: CH2_SYNC_OFFSET

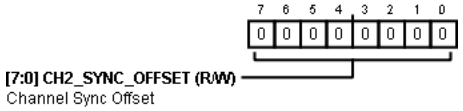


Table 47. Bit descriptions for CH2_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 3 SYNC OFFSET REGISTER

Address: 0x0C, Reset: 0x00, Name: CH3_SYNC_OFFSET

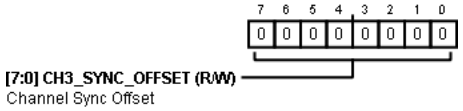


Table 48. Bit descriptions for CH3_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 4 SYNC OFFSET REGISTER

Address: 0x0D, Reset: 0x00, Name: CH4_SYNC_OFFSET

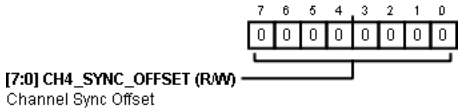


Table 49. Bit descriptions for CH4_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 5 SYNC OFFSET REGISTER

Address: 0x0E, Reset: 0x00, Name: CH5_SYNC_OFFSET

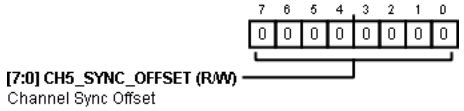


Table 50. Bit descriptions for CH5_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 6 SYNC OFFSET REGISTER

Address: 0x0F, Reset: 0x00, Name: CH6_SYNC_OFFSET

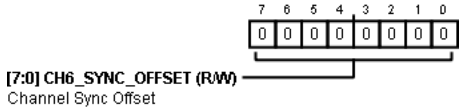


Table 51. Bit descriptions for CH6_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

CHANNEL 7 SYNC OFFSET REGISTER

Address: 0x10, Reset: 0x00, Name: CH7_SYNC_OFFSET

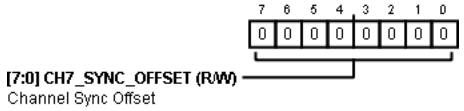


Table 52. Bit descriptions for CH7_SYNC_OFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_SYNC_OFFSET		Channel Sync Offset	0x0	R/W

GENERAL USER CONFIG 1 REGISTER

Address: 0x11, Reset: 0x2C, Name: GENERAL_USER_CONFIG_1

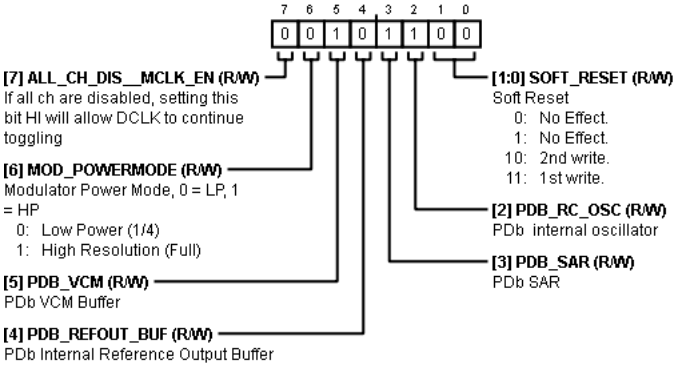


Table 53. Bit descriptions for GENERAL_USER_CONFIG_1

Bits	Bit Name	Settings	Description	Reset	Access
7	ALL_CH_DIS__MCLK_EN		If all ch are disabled, setting this bit HI will allow DCLK to continue toggling. If all ch are disabled, setting this bit HI will allow DCLK to continue toggling	0x0	R/W
6	MOD_POWERMODE		Modulator Power Mode, 0 = LP, 1 = HP. Modulator Power Mode	0x0	R/W
		0	Low Power (1/4) Low Power (1/4)		
		1	High Resolution (Full)		
5	PDB_VCM		PDb VCM Buffer. PDb Internal Reference Output Buffer	0x1	R/W
4	PDB_REFOUT_BUF		PDb Internal Reference Output Buffer. PDb Internal Reference Output Buffer	0x0	R/W
3	PDB_SAR		PDb SAR. PDb SAR	0x1	R/W
2	PDB_RC_OSC		PDb internal oscillator. PDb signal for internal oscillator .	0x1	R/W
[1:0]	SOFT_RESET		Soft Reset. Soft Reset - First 11 and then 10 needs to be sent this this register 00 - No effect 01 - No effect 10 - 2nd write 11 - 1st write 2'b0 - No Effect 2'b1 - No Effect 2'b10 - 2nd write 2'b11 - 1st write	0x0	R/W
		0	No Effect.		
		1	No Effect.		
		10	2nd write.		
		11	1st write.		

GENERAL USER CONFIG 2 REGISTER

Address: 0x12, Reset: 0x09, Name: GENERAL_USER_CONFIG_2

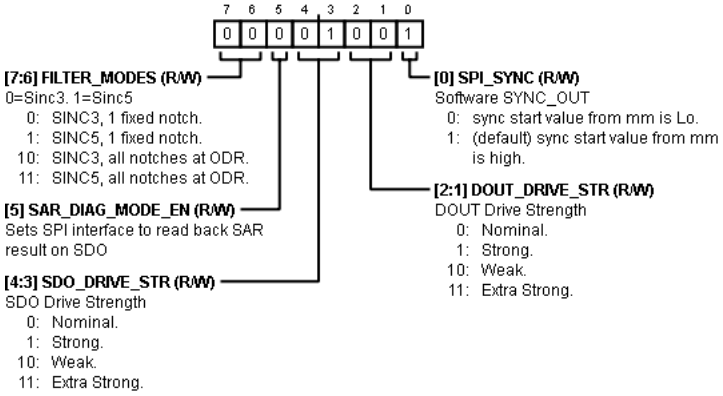


Table 54. Bit descriptions for GENERAL_USER_CONFIG_2

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	FILTER_MODES	0	SINC3, 1 fixed notch. uj	0x0	R/W
		10	SINC3, all notches at ODR.		
5	SAR_DIAG_MODE_EN		Sets SPI interface to read back SAR result on SDO. Sets SPI interface to read back SAR result on SDO	0x0	R/W
[4:3]	SDO_DRIVE_STR		SDO Drive Strength. SDO Drive Strength - 00 - Nominal 01 - Strong 10 - Weak 11 - Extra Strong 2'b0 - Nominal 2'b1 - Strong 2'b10 - Weak 2'b11 - Extra Strong	0x1	R/W
		0	Nominal.		
		1	Strong.		
		10	Weak.		
		11	Extra Strong.		
[2:1]	DOUT_DRIVE_STR		DOUT Drive Strength. DOUT Drive Strength - 00 - Nominal 01 - Strong 10 - Weak 11 - Extra Strong 2'b0 - Nominal 2'b1 - Strong 2'b10 - Weak 2'b11 - Extra Strong	0x0	R/W
		0	Nominal.		
		1	Strong.		
		10	Weak.		
		11	Extra Strong.		
0	SPI_SYNC		Software SYNC_OUT. Control SYNC reset This signal is ANDed with the value on STARTb pin in the control module. 0 - sync start value from mm is LO 1(default) - sync start value from mm is HI 1'b0 - sync start value from mm is Lo 1'b1 - (default) sync start value from mm is high	0x1	R/W
		0	sync start value from mm is Lo.		
		1	(default) sync start value from mm is high.		

GENERAL USER CONFIG 3 REGISTER

Address: 0x13, Reset: 0x80, Name: GENERAL_USER_CONFIG_3

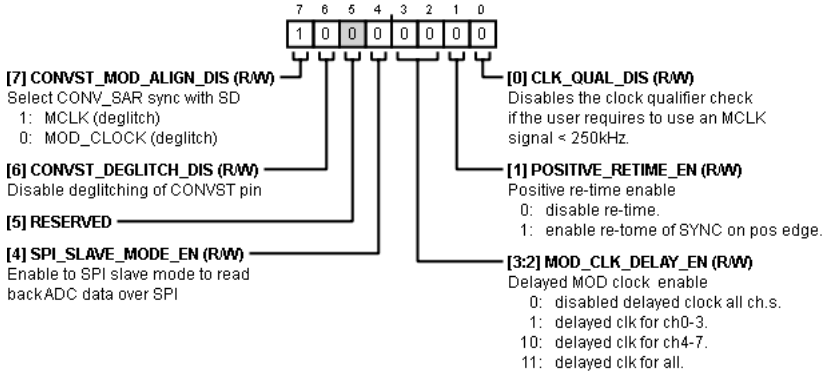


Table 55. Bit descriptions for GENERAL_USER_CONFIG_3

Bits	Bit Name	Settings	Description	Reset	Access
7	CONVST_MOD_ALIGN_DIS		Select CONV_SAR sync with SD. Select the deglitch method If deglitching is enabled, the following clocks can be selected 0: MOD_CLOCK 1: MCLK 1'b0 - MOD_CLOCK (deglitch) 1'b1 - MCLK (deglitch	0x1	R/W
		1	MCLK (deglitch)		
		0	MOD_CLOCK (deglitch)		
6	CONVST_DEGLITCH_DIS		Disable deglitching of CONVST pin. Disable deglitching of CONVST pin Disable the deglitching of CONVST pin used for SAR	0x0	R/W
4	SPI_SLAVE_MODE_EN		Enable to SPI slave mode to read back ADC data over SPI. Enable to SPI slave mode to read back ADC data over SPI Allows read back of the 8 ADC channel results over the SPI interface	0x0	R/W
[3:2]	MOD_CLK_DELAY_EN		Delayed MOD clock enable. Delayed MOD clock enable 00 - Disable delayed clock for all channels 01 - Enable delayed clock for channels 0-3 10 - Enable delayed clock for channels 4-7 11 - Enable delayed clock for all channels 2'b0 - disabled delayed clock all ch.s 2'b1 - delayed clk for ch0-3 2'b10 - delayed clk for ch4-7 2'b11 - delayed clk for all	0x0	R/W
		0	disabled delayed clock all ch.s.		
		1	delayed clk for ch0-3.		
		10	delayed clk for ch4-7.		
		11	delayed clk for all.		

Bits	Bit Name	Settings	Description	Reset	Access
1	POSITIVE_RETIME_EN		Positive re-time enable. Positive re-time enable - 0 - disable re-time. 1 - Enable re-time of SYNC on positive edge of clock. Sync's STARTb on first device and sends to SYNC_INb of all devices (including first device) 1'b0 - disable re-time 1'b1 - enable re-tome of SYNC on pos edge	0x0	R/W
		0	disable re-time.		
		1	enable re-tome of SYNC on pos edge.		
0	CLK_QUAL_DIS		Disables the clock qualifier check if the user requires to use an MCLK signal < 250kHz. Disables the clock qualifier check if the user requires to use an MCLK signal < 250kHz.	0x0	R/W

DATA OUT FORMAT REGISTER

Address: 0x14, Reset: 0x20, Name: DOUT_FORMAT

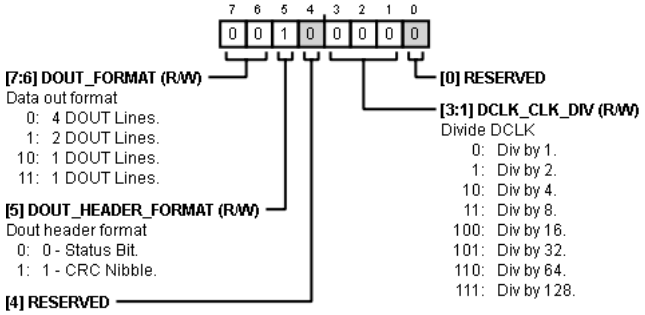


Table 56. Bit descriptions for DOUT_FORMAT

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DOUT_FORMAT		Data out format. Data out format 00 - 4 DOUT lines. CH0,1 - DOUT0, CH2,3 - DOUT1... 01 - 2 DOUT lines. CH0,1,2,3 - DOUT0.... 10 - 1 DOUT line. CH0,1,2,3,4,5,6,7. 11 - 1 DOUT line. CH0,1,2,3,4,5,6,7. Daisy chaining is automatically enabled when DOUT_FORMAT!=00 2'b0 - 4 DOUT Lines 2'b1 - 2 DOUT Lines 2'b10 - 1 DOUT Lines 2'b11 - 1 DOUT Lines	0x0	R/W
		0	4 DOUT Lines.		
		1	2 DOUT Lines.		
		10	1 DOUT Lines.		
		11	1 DOUT Lines.		
5	DOUT_HEADER_FORMAT		Dout header format. 1'b0 - 0 - Status Bit 1'b1 - 1 - CRC Nibble	0x1	R/W
		0	0 - Status Bit.		
		1	1 - CRC Nibble.		
[3:1]	DCLK_CLK_DIV		Divide DCLK. Divide DCLK 3'b0 - Div by 1 3'b1 - Div by 2 3'b10 - Div by 4 3'b11 - Div by 8 3'b101 - Div by 32 3'b110 - Div by 64 3'b111 - Div by 128	0x0	R/W
		0	Div by 1.		
		1	Div by 2.		
		10	Div by 4.		

Bits	Bit Name	Settings	Description	Reset	Access
		11	Div by 8.		
		100	Div by 16.		
		101	Div by 32.		
		110	Div by 64.		
		111	Div by 128.		

MAIN ADC METER AND REFERENCE MUX CONTROL REGISTER

Address: 0x15, Reset: 0x00, Name: ADC_MUX_CONFIG

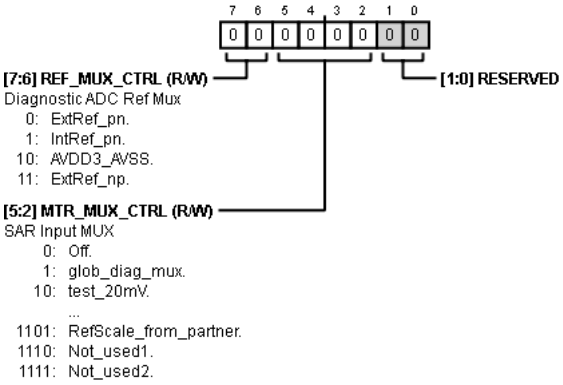


Table 57. Bit descriptions for ADC_MUX_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	REF_MUX_CTRL		Diagnostic ADC Ref Mux	0x0	R/W
		0	ExtRef_pn.		
		1	IntRef_pn.		
		10	AVDD3_AVSS.		
		11	ExtRef_np.		
[5:2]	MTR_MUX_CTRL		SAR Input MUX	0x0	R/W
		0	Off.		
		1	glob_diag_mux.		
		10	test_280mV.		
		11	ExtRef_pn.		
		100	ExtRef_np.		
		101	ExtRef_nn.		
		110	IntRef_pn.		
		111	IntRef_np.		
		1000	IntRef_nn.		
		1001	ExtRef_pp.		

GLOBAL DIAGNOSTICS MUX REGISTER

Address: 0x16, Reset: 0x00, Name: GLOBAL_MUX_CONFIG

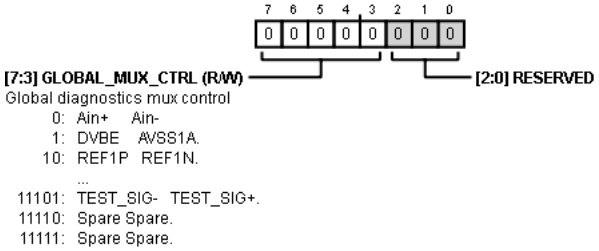


Table 58. Bit descriptions for GLOBAL_MUX_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	GLOBAL_MUX_CTRL		Global diagnostics mux control	0x0	R/W
		0	Ain+ Ain-		
		1	DVBE AVSS1A.		
		10	REF1P REF1N.		
		11	REF2P REF2N.		
		100	REF_OUT AVSS1B.		
		101	VCM AVSS1.		
		110	AVDD1P8_1 AVSS1A.		
		111	AVDD1P8_2 AVSS1B.		
		1000	DVDD DGND.		
		1001	AVDD1A AVSS1A.		
		1010	AVDD1B AVSS1B.		
		1011	AVDD2A AVSS2A.		
		1100	AVDD2B AVSS2B.		
		1101	IOVDD_DGND.		
		1110	AVDD4 AVSS4.		
		1111	DGND AVSS1A.		
		10000	DGND AVSS1B.		
		10001	DGND AVSS4.		
		10010	AVDD4** AVSS4**		
		10011	REF1P AVSS1A.		
		10100	REF2P AVSS1B.		
		10101	AVSS4 AVDD4.		

GPIO CONFIG REGISTER

Address: 0x17, Reset: 0x00, Name: GPIO_CONFIG

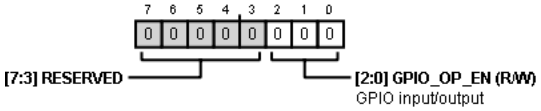


Table 59. Bit descriptions for GPIO_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[2:0]	GPIO_OP_EN		GPIO input/output. GPIO configuration Register: This register is used to configure GPIO pins 0,1,2. Setting bits 2:0 configures the GPIO pins as Inputs or Outputs. 0- Inputs 1- Outputs Register 0x18 is used to read and write data from the GPIO pins	0x0	R/W

GPIO DATA REGISTER

Address: 0x18, Reset: 0x00, Name: GPIO_DATA

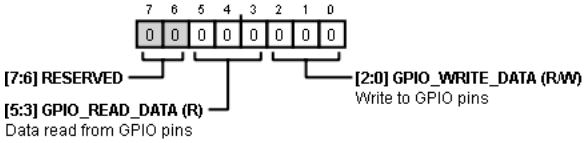


Table 60. Bit descriptions for GPIO_DATA

Bits	Bit Name	Settings	Description	Reset	Access
[5:3]	GPIO_READ_DATA		Data read from GPIO pins. GPIO read. When the GPIO's are set to input mode bit 5:3 are used to read the value set on them. Bit 5:3 corrospond to GPIO pins 2:0	0x0	R
[2:0]	GPIO_WRITE_DATA		Write to GPIO pins. GPIO write value. Setting bits 2:0 sets the value of the GPIO pins 2:0 when they are set up in output mode.	0x0	R/W

BUFFER CONFIG 1 REGISTER

Address: 0x19, Reset: 0x38, Name: BUFFER_CONFIG_1

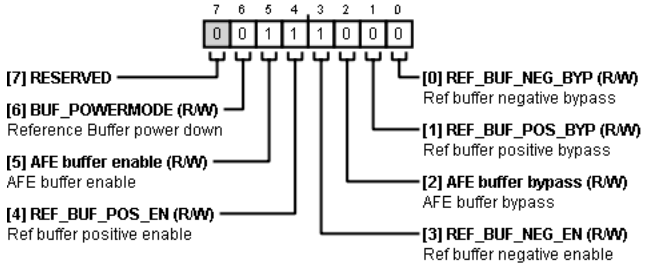


Table 61. Bit descriptions for BUFFER_CONFIG_1

Bits	Bit Name	Settings	Description	Reset	Access
6	BUF_POWERMODE		Reference Buffer power down. Buffer power - 0 - 1/4x buffer power (default) 1 - Full buffer power	0x0	R/W
5	AFE buffer enable		AFE buffer enable. AFE buffer enable	0x1	R/W
4	REF_BUF_POS_EN		Ref buffer positive enable. Ref buffer positive enable	0x1	R/W
3	REF_BUF_NEG_EN		Ref buffer negative enable. Ref buffer negative enable	0x1	R/W
2	AFE buffer bypass		AFE buffer bypass. AFE buffer bypass	0x0	R/W
1	REF_BUF_POS_BYP		Ref buffer positive bypass. Ref buffer positive bypass	0x0	R/W
0	REF_BUF_NEG_BYP		Ref buffer negative bypass. Ref buffer negative bypass	0x0	R/W

BUFFER CONFIG 2 REGISTER

Address: 0x1A, Reset: 0xC0, Name: BUFFER_CONFIG_2

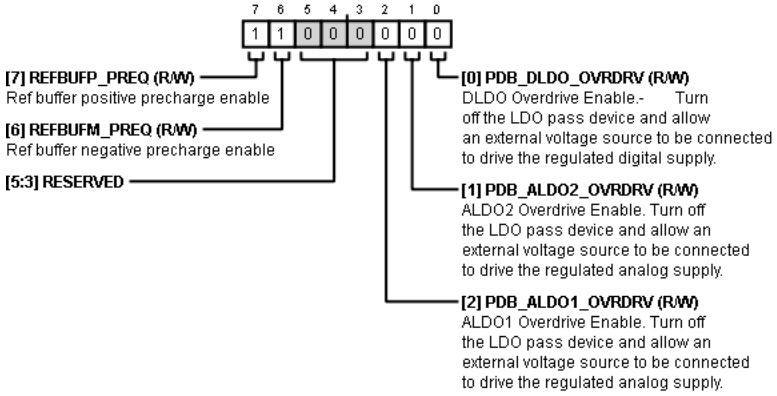


Table 62. Bit descriptions for BUFFER_CONFIG_2

Bits	Bit Name	Settings	Description	Reset	Access
7	REFBUFP_PREQ		Ref buffer positive precharge enable. Ref buffer positive precharge enable	0x1	R/W
6	REFBUFM_PREQ		Ref buffer negative precharge enable. Ref buffer negative precharge enable	0x1	R/W
2	PDB_ALDO1_OVRDRV		ALDO1 Overdrive Enable. Turn off the LDO pass device and allow an external voltage source to be connected to drive the regulated analog supply. ALDO1 Overdrive Enable Turn off the LDO pass device and allow an external voltage source to be connected to drive the regulated analog supply. 0 - LDO pass device is turned off, 1 - LDO pass device is turned on - The voltage source should be connected before the LDO output is turned off.	0x0	R/W
1	PDB_ALDO2_OVRDRV		ALDO2 Overdrive Enable. Turn off the LDO pass device and allow an external voltage source to be connected to drive the regulated analog supply. ALDO2 Overdrive Enable Turn off the LDO pass device and allow an external voltage source to be connected to drive the regulated analog supply. 0 - LDO pass device is turned off, 1 - LDO pass device is turned on The voltage source should be connected before the LDO output is turned off.	0x0	R/W
0	PDB_DLDO_OVRDRV		DLDO Overdrive Enable.- Turn off the LDO pass device and allow an external voltage source to be connected to drive the regulated digital supply. DLDO Overdrive Enable.-Turn off the LDO pass device and allow an external voltage source to be connected to drive the regulated analog supply. Turn off the LDO pass device and allow an external voltage source to be connected to drive the regulated analog supply. 0 - LDO pass device is turned off, 1 - LDO pass device is turned on The voltage source should be connected before the LDO output is turned off.	0x0	R/W

CHANNEL 0 OFFSET UPPER BYTE REGISTER

Address: 0x1C, Reset: 0x00, Name: CH0_OFFSET_UPPER_BYTE

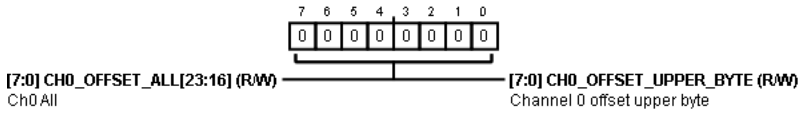


Table 63. Bit descriptions for CH0_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_OFFSET_UPPER_BYTE		Channel 0 offset upper byte	0x0	R/W
[7:0]	CH0_OFFSET_ALL[23:16]		Ch0 All	0x0	R/W

CHANNEL 0 OFFSET MIDDLE BYTE REGISTER

Address: 0x1D, Reset: 0x00, Name: CH0_OFFSET_MID_BYTE

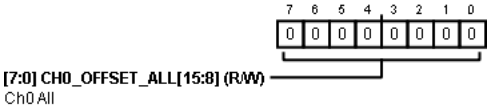


Table 64. Bit descriptions for CH0_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_OFFSET_ALL[15:8]		Ch0 All	0x0	R/W

CHANNEL 0 OFFSET LOWER BYTE REGISTER

Address: 0x1E, Reset: 0x00, Name: CH0_OFFSET_LOWER_BYTE

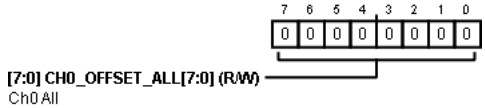


Table 65. Bit descriptions for CH0_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_OFFSET_ALL[7:0]		Ch0 All	0x0	R/W

CHANNEL 0 GAIN UPPER BYTE REGISTER

Address: 0x1F, Reset: 0x00, Name: CH0_GAIN_UPPER_BYTE

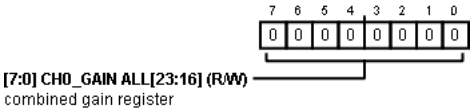


Table 66. Bit descriptions for CH0_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_GAIN ALL[23:16]		combined gain register	0x0	R/W

CHANNEL 0 GAIN MIDDLE BYTE REGISTER

Address: 0x20, Reset: 0x00, Name: CH0_GAIN_MID_BYTE

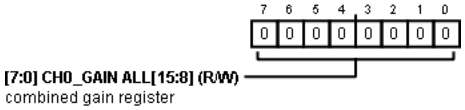


Table 67. Bit descriptions for CH0_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_GAIN ALL[15:8]		combined gain register	0x0	R/W

CHANNEL 0 GAIN LOWER BYTE REGISTER

Address: 0x21, Reset: 0x00, Name: CH0_GAIN_LOWER_BYTE

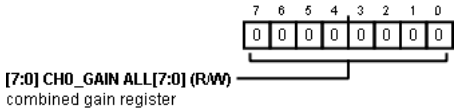


Table 68. Bit descriptions for CH0_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH0_GAIN ALL[7:0]		combined gain register	0x0	R/W

CHANNEL 1 OFFSET UPPER BYTE REGISTER

Address: 0x22, Reset: 0x00, Name: CH1_OFFSET_UPPER_BYTE

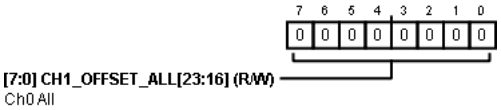


Table 69. Bit descriptions for CH1_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_OFFSET_ALL[23:16]		Ch0 All	0x0	R/W

CHANNEL 1 OFFSET MIDDLE BYTE REGISTER

Address: 0x23, Reset: 0x00, Name: CH1_OFFSET_MID_BYTE

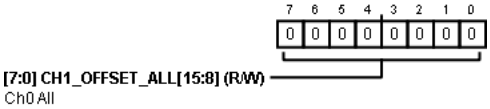


Table 70. Bit descriptions for CH1_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_OFFSET_ALL[15:8]		Ch0 All	0x0	R/W

CHANNEL 1 OFFSET LOWER BYTE REGISTER

Address: 0x24, Reset: 0x00, Name: CH1_OFFSET_LOWER_BYTE

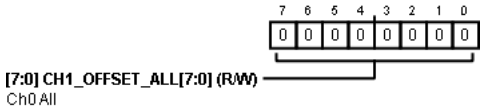


Table 71. Bit descriptions for CH1_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_OFFSET_ALL[7:0]		Ch0 All	0x0	R/W

CHANNEL 1 GAIN UPPER BYTE REGISTER

Address: 0x25, Reset: 0x00, Name: CH1_GAIN_UPPER_BYTE

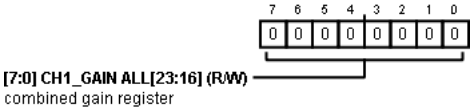


Table 72. Bit descriptions for CH1_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_GAIN ALL[23:16]		combined gain register	0x0	R/W

CHANNEL 1 GAIN MIDDLE BYTE REGISTER

Address: 0x26, Reset: 0x00, Name: CH1_GAIN_MID_BYTE

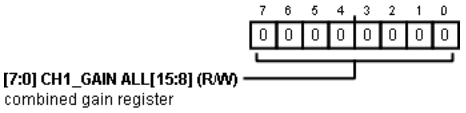


Table 73. Bit descriptions for CH1_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_GAIN ALL[15:8]		combined gain register	0x0	R/W

CHANNEL 1 GAIN LOWER BYTE REGISTER

Address: 0x27, Reset: 0x00, Name: CH1_GAIN_LOWER_BYTE

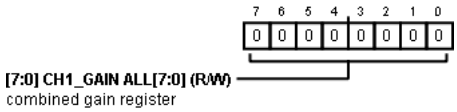


Table 74. Bit descriptions for CH1_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH1_GAIN ALL[7:0]		combined gain register	0x0	R/W

CHANNEL 2 OFFSET UPPER BYTE REGISTER

Address: 0x28, Reset: 0x00, Name: CH2_OFFSET_UPPER_BYTE

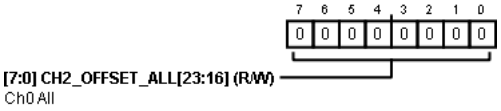


Table 75. Bit descriptions for CH2_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_OFFSET_ALL[23:16]		Ch0 All	0x0	R/W

CHANNEL 2 OFFSET MIDDLE BYTE REGISTER

Address: 0x29, Reset: 0x00, Name: CH2_OFFSET_MID_BYTE

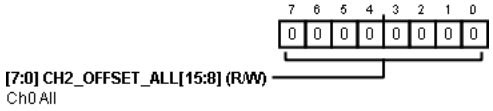


Table 76. Bit descriptions for CH2_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_OFFSET_ALL[15:8]		Ch0 All	0x0	R/W

CHANNEL 2 OFFSET LOWER BYTE REGISTER

Address: 0x2A, Reset: 0x00, Name: CH2_OFFSET_LOWER_BYTE

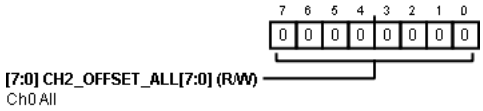


Table 77. Bit descriptions for CH2_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_OFFSET_ALL[7:0]		Ch0 All	0x0	R/W

CHANNEL 2 GAIN UPPER BYTE REGISTER

Address: 0x2B, Reset: 0x00, Name: CH2_GAIN_UPPER_BYTE

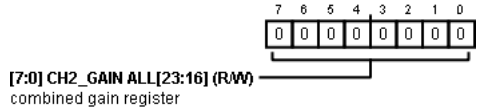


Table 78. Bit descriptions for CH2_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_GAIN ALL[23:16]		combined gain register	0x0	R/W

CHANNEL 2 GAIN MIDDLE BYTE REGISTER

Address: 0x2C, Reset: 0x00, Name: CH2_GAIN_MID_BYTE

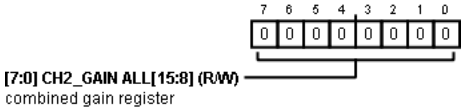


Table 79. Bit descriptions for CH2_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_GAIN ALL[15:8]		combined gain register	0x0	R/W

CHANNEL 2 GAIN LOWER BYTE REGISTER

Address: 0x2D, Reset: 0x00, Name: CH2_GAIN_LOWER_BYTE

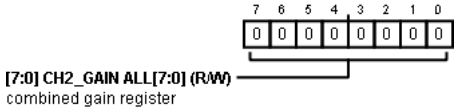


Table 80. Bit descriptions for CH2_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH2_GAIN ALL[7:0]		combined gain register	0x0	R/W

CHANNEL 3 OFFSET UPPER BYTE REGISTER

Address: 0x2E, Reset: 0x00, Name: CH3_OFFSET_UPPER_BYTE

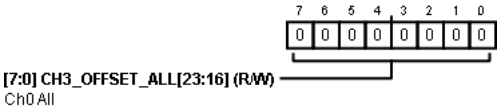


Table 81. Bit descriptions for CH3_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_OFFSET_ALL[23:16]		Ch0 All	0x0	R/W

CHANNEL 3 OFFSET MIDDLE BYTE REGISTER

Address: 0x2F, Reset: 0x00, Name: CH3_OFFSET_MID_BYTE

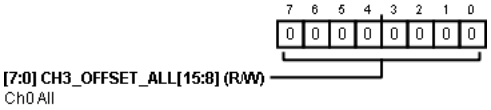


Table 82. Bit descriptions for CH3_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_OFFSET_ALL[15:8]		Ch0 All	0x0	R/W

CHANNEL 3 OFFSET LOWER BYTE REGISTER

Address: 0x30, Reset: 0x00, Name: CH3_OFFSET_LOWER_BYTE

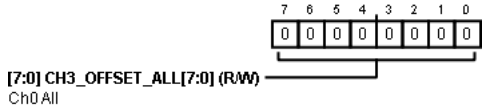


Table 83. Bit descriptions for CH3_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_OFFSET_ALL[7:0]		Ch0 All	0x0	R/W

CHANNEL 3 GAIN UPPER BYTE REGISTER

Address: 0x31, Reset: 0x00, Name: CH3_GAIN_UPPER_BYTE

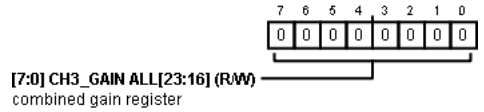


Table 84. Bit descriptions for CH3_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_GAIN ALL[23:16]		combined gain register	0x0	R/W

CHANNEL 3 GAIN MIDDLE BYTE REGISTER

Address: 0x32, Reset: 0x00, Name: CH3_GAIN_MID_BYTE

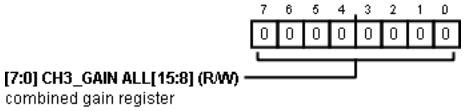


Table 85. Bit descriptions for CH3_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_GAIN ALL[15:8]		combined gain register	0x0	R/W

CHANNEL 3 GAIN LOWER BYTE REGISTER

Address: 0x33, Reset: 0x00, Name: CH3_GAIN_LOWER_BYTE

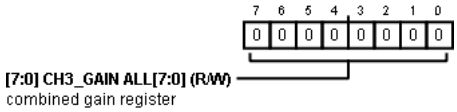


Table 86. Bit descriptions for CH3_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH3_GAIN ALL[7:0]		combined gain register	0x0	R/W

CHANNEL 4 OFFSET UPPER BYTE REGISTER

Address: 0x34, Reset: 0x00, Name: CH4_OFFSET_UPPER_BYTE

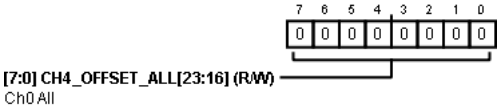


Table 87. Bit descriptions for CH4_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_OFFSET_ALL[23:16]		Ch0 All	0x0	R/W

CHANNEL 4 OFFSET MIDDLE BYTE REGISTER

Address: 0x35, Reset: 0x00, Name: CH4_OFFSET_MID_BYTE

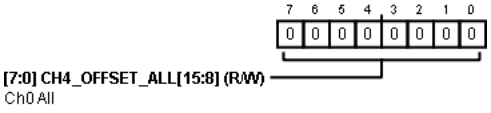


Table 88. Bit descriptions for CH4_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_OFFSET_ALL[15:8]		Ch0 All	0x0	R/W

CHANNEL 4 OFFSET LOWER BYTE REGISTER

Address: 0x36, Reset: 0x00, Name: CH4_OFFSET_LOWER_BYTE

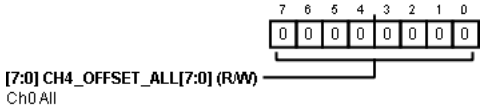


Table 89. Bit descriptions for CH4_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_OFFSET_ALL[7:0]		Ch0 All	0x0	R/W

CHANNEL 4 GAIN UPPER BYTE REGISTER

Address: 0x37, Reset: 0x00, Name: CH4_GAIN_UPPER_BYTE

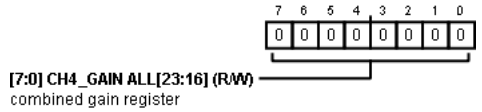


Table 90. Bit descriptions for CH4_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_GAIN ALL[23:16]		combined gain register	0x0	R/W

CHANNEL 4 GAIN MIDDLE BYTE REGISTER

Address: 0x38, Reset: 0x00, Name: CH4_GAIN_MID_BYTE

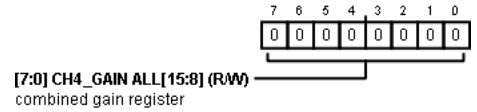


Table 91. Bit descriptions for CH4_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_GAIN ALL[15:8]		combined gain register	0x0	R/W

CHANNEL 4 GAIN LOWER BYTE REGISTER

Address: 0x39, Reset: 0x00, Name: CH4_GAIN_LOWER_BYTE

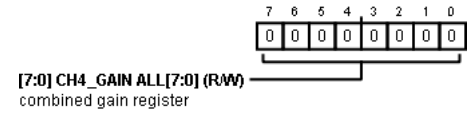


Table 92. Bit descriptions for CH4_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH4_GAIN ALL[7:0]		combined gain register	0x0	R/W

CHANNEL 5 OFFSET UPPER BYTE REGISTER

Address: 0x3A, Reset: 0x00, Name: CH5_OFFSET_UPPER_BYTE

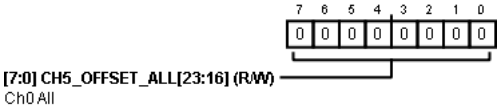


Table 93. Bit descriptions for CH5_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_OFFSET_ALL[23:16]		Ch0 All	0x0	R/W

CHANNEL 5 OFFSET MIDDLE BYTE REGISTER

Address: 0x3B, Reset: 0x00, Name: CH5_OFFSET_MID_BYTE

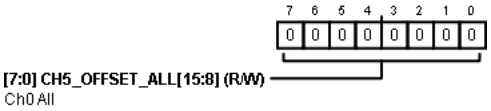


Table 94. Bit descriptions for CH5_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_OFFSET_ALL[15:8]		Ch0 All	0x0	R/W

CHANNEL 5 OFFSET LOWER BYTE REGISTER

Address: 0x3C, Reset: 0x00, Name: CH5_OFFSET_LOWER_BYTE

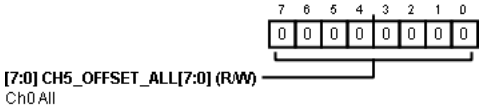


Table 95. Bit descriptions for CH5_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_OFFSET_ALL[7:0]		Ch0 All	0x0	R/W

CHANNEL 5 GAIN UPPER BYTE REGISTER

Address: 0x3D, Reset: 0x00, Name: CH5_GAIN_UPPER_BYTE

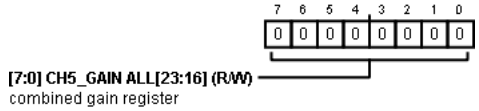


Table 96. Bit descriptions for CH5_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_GAIN ALL[23:16]		combined gain register	0x0	R/W

CHANNEL 5 GAIN MIDDLE BYTE REGISTER

Address: 0x3E, Reset: 0x00, Name: CH5_GAIN_MID_BYTE

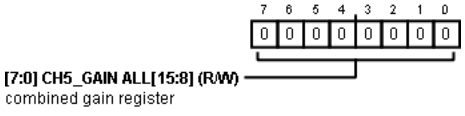


Table 97. Bit descriptions for CH5_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_GAIN ALL[15:8]		combined gain register	0x0	R/W

CHANNEL 5 GAIN LOWER BYTE REGISTER

Address: 0x3F, Reset: 0x00, Name: CH5_GAIN_LOWER_BYTE

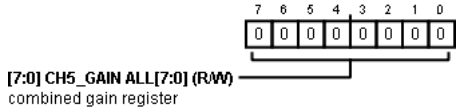


Table 98. Bit descriptions for CH5_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH5_GAIN ALL[7:0]		combined gain register	0x0	R/W

CHANNEL 6 OFFSET UPPER BYTE REGISTER

Address: 0x40, Reset: 0x00, Name: CH6_OFFSET_UPPER_BYTE

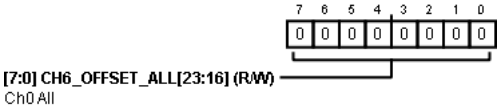


Table 99. Bit descriptions for CH6_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_OFFSET_ALL[23:16]		Ch0 All	0x0	R/W

CHANNEL 6 OFFSET MIDDLE BYTE REGISTER

Address: 0x41, Reset: 0x00, Name: CH6_OFFSET_MID_BYTE

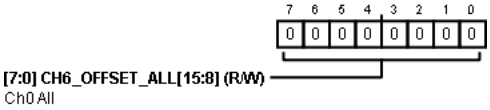


Table 100. Bit descriptions for CH6_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_OFFSET_ALL[15:8]		Ch0 All	0x0	R/W

CHANNEL 6 OFFSET LOWER BYTE REGISTER

Address: 0x42, Reset: 0x00, Name: CH6_OFFSET_LOWER_BYTE

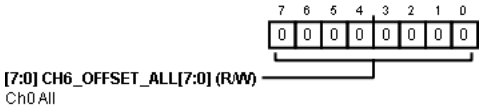


Table 101. Bit descriptions for CH6_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_OFFSET_ALL[7:0]		Ch0 All	0x0	R/W

CHANNEL 6 GAIN UPPER BYTE REGISTER

Address: 0x43, Reset: 0x00, Name: CH6_GAIN_UPPER_BYTE

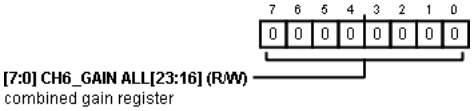


Table 102. Bit descriptions for CH6_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_GAIN ALL[23:16]		combined gain register	0x0	R/W

CHANNEL 6 GAIN MIDDLE BYTE REGISTER

Address: 0x44, Reset: 0x00, Name: CH6_GAIN_MID_BYTE

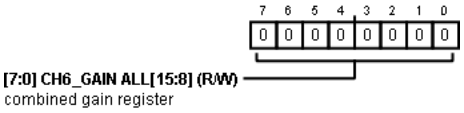


Table 103. Bit descriptions for CH6_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_GAIN ALL[15:8]		combined gain register	0x0	R/W

CHANNEL 6 GAIN LOWER BYTE REGISTER

Address: 0x45, Reset: 0x00, Name: CH6_GAIN_LOWER_BYTE

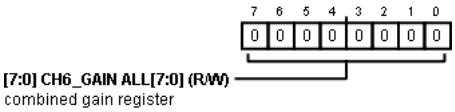


Table 104. Bit descriptions for CH6_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH6_GAIN ALL[7:0]		combined gain register	0x0	R/W

CHANNEL 7 OFFSET UPPER BYTE REGISTER

Address: 0x46, Reset: 0x00, Name: CH7_OFFSET_UPPER_BYTE

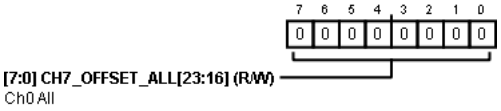


Table 105. Bit descriptions for CH7_OFFSET_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_OFFSET_ALL[23:16]		Ch0 All	0x0	R/W

CHANNEL 7 OFFSET MIDDLE BYTE REGISTER

Address: 0x47, Reset: 0x00, Name: CH7_OFFSET_MID_BYTE

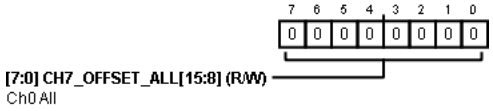


Table 106. Bit descriptions for CH7_OFFSET_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_OFFSET_ALL[15:8]		Ch0 All	0x0	R/W

CHANNEL 7 OFFSET LOWER BYTE REGISTER

Address: 0x48, Reset: 0x00, Name: CH7_OFFSET_LOWER_BYTE

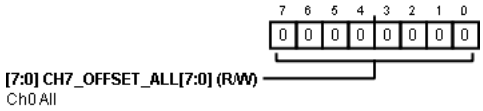


Table 107. Bit descriptions for CH7_OFFSET_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_OFFSET_ALL[7:0]		Ch0 All	0x0	R/W

CHANNEL 7 GAIN UPPER BYTE REGISTER

Address: 0x49, Reset: 0x00, Name: CH7_GAIN_UPPER_BYTE

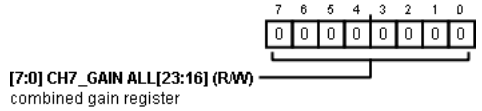


Table 108. Bit descriptions for CH7_GAIN_UPPER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_GAIN ALL[23:16]		combined gain register	0x0	R/W

CHANNEL 7 GAIN MIDDLE BYTE REGISTER

Address: 0x4A, Reset: 0x00, Name: CH7_GAIN_MID_BYTE

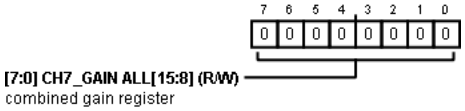


Table 109. Bit descriptions for CH7_GAIN_MID_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_GAIN ALL[15:8]		combined gain register	0x0	R/W

CHANNEL 7 GAIN LOWER BYTE REGISTER

Address: 0x4B, Reset: 0x00, Name: CH7_GAIN_LOWER_BYTE

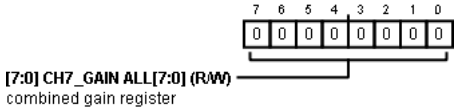


Table 110. Bit descriptions for CH7_GAIN_LOWER_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CH7_GAIN ALL[7:0]		combined gain register	0x0	R/W

CHANNEL 0 STATUS REGISTER

Address: 0x4C, Reset: 0x00, Name: CH0_ERR_REG

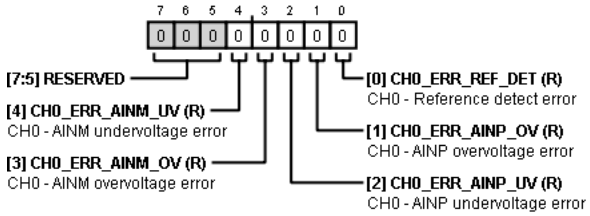


Table 111. Bit descriptions for CH0_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
4	CH0_ERR_AINM_UV		CH0 - AINM undervoltage error	0x0	R
3	CH0_ERR_AINM_OV		CH0 - AINM overvoltage error	0x0	R
2	CH0_ERR_AINP_UV		CH0 - AINP undervoltage error	0x0	R
1	CH0_ERR_AINP_OV		CH0 - AINP overvoltage error	0x0	R
0	CH0_ERR_REF_DET		CH0 - Reference detect error	0x0	R

CHANNEL 1 STATUS REGISTER

Address: 0x4D, Reset: 0x00, Name: CH1_ERR_REG

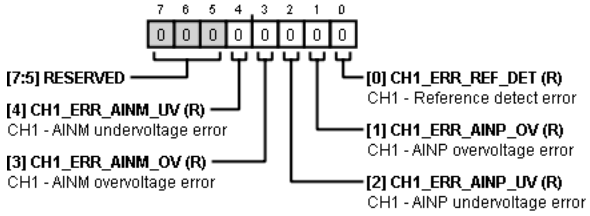


Table 112. Bit descriptions for CH1_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
4	CH1_ERR_AINM_UV		CH1 - AINM undervoltage error	0x0	R
3	CH1_ERR_AINM_OV		CH1 - AINM overvoltage error	0x0	R
2	CH1_ERR_AINP_UV		CH1 - AINP undervoltage error	0x0	R
1	CH1_ERR_AINP_OV		CH1 - AINP overvoltage error	0x0	R
0	CH1_ERR_REF_DET		CH1 - Reference detect error	0x0	R

CHANNEL 2 STATUS REGISTER

Address: 0x4E, Reset: 0x00, Name: CH2_ERR_REG

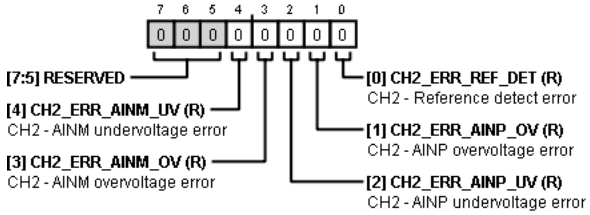


Table 113. Bit descriptions for CH2_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
4	CH2_ERR_AINM_UV		CH2 - AINM undervoltage error	0x0	R
3	CH2_ERR_AINM_OV		CH2 - AINM overvoltage error	0x0	R
2	CH2_ERR_AINP_UV		CH2 - AINP undervoltage error	0x0	R
1	CH2_ERR_AINP_OV		CH2 - AINP overvoltage error	0x0	R
0	CH2_ERR_REF_DET		CH2 - Reference detect error	0x0	R

CHANNEL 3 STATUS REGISTER

Address: 0x4F, Reset: 0x00, Name: CH3_ERR_REG

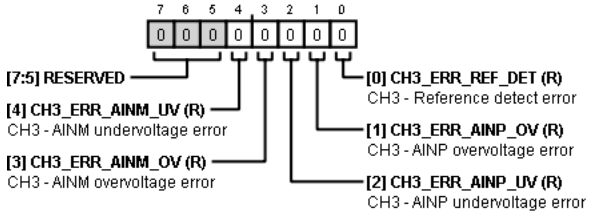


Table 114. Bit descriptions for CH3_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
4	CH3_ERR_AINM_UV		CH3 - AINM undervoltage error	0x0	R
3	CH3_ERR_AINM_OV		CH3 - AINM overvoltage error	0x0	R
2	CH3_ERR_AINP_UV		CH3 - AINP undervoltage error	0x0	R
1	CH3_ERR_AINP_OV		CH3 - AINP overvoltage error	0x0	R
0	CH3_ERR_REF_DET		CH3 - Reference detect error	0x0	R

CHANNEL 4 STATUS REGISTER

Address: 0x50, Reset: 0x00, Name: CH4_ERR_REG

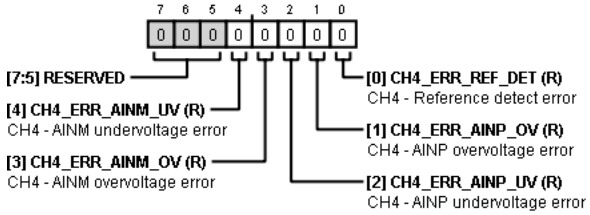


Table 115. Bit descriptions for CH4_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
4	CH4_ERR_AINM_UV		CH4 - AINM undervoltage error	0x0	R
3	CH4_ERR_AINM_OV		CH4 - AINM overvoltage error	0x0	R
2	CH4_ERR_AINP_UV		CH4 - AINP undervoltage error	0x0	R
1	CH4_ERR_AINP_OV		CH4 - AINP overvoltage error	0x0	R
0	CH4_ERR_REF_DET		CH4 - Reference detect error	0x0	R

CHANNEL 5 STATUS REGISTER

Address: 0x51, Reset: 0x00, Name: CH5_ERR_REG

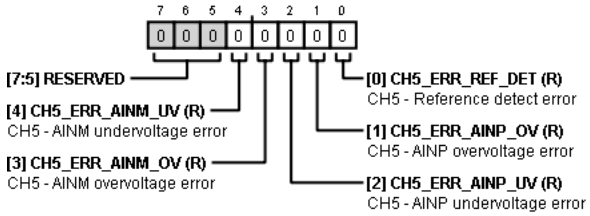


Table 116. Bit descriptions for CH5_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
4	CH5_ERR_AINM_UV		CH5 - AINM undervoltage error	0x0	R
3	CH5_ERR_AINM_OV		CH5 - AINM overvoltage error	0x0	R
2	CH5_ERR_AINP_UV		CH5 - AINP undervoltage error	0x0	R
1	CH5_ERR_AINP_OV		CH5 - AINP overvoltage error	0x0	R
0	CH5_ERR_REF_DET		CH5 - Reference detect error	0x0	R

CHANNEL 6 STATUS REGISTER

Address: 0x52, Reset: 0x00, Name: CH6_ERR_REG

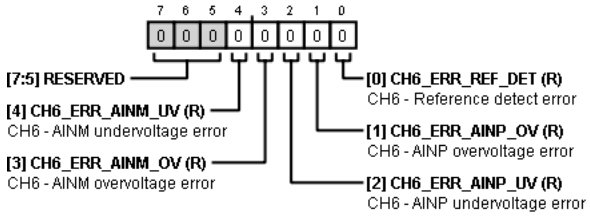


Table 117. Bit descriptions for CH6_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
4	CH6_ERR_AINM_UV		CH6 - AINM undervoltage error	0x0	R
3	CH6_ERR_AINM_OV		CH6 - AINM overvoltage error	0x0	R
2	CH6_ERR_AINP_UV		CH6 - AINP undervoltage error	0x0	R
1	CH6_ERR_AINP_OV		CH6 - AINP overvoltage error	0x0	R
0	CH6_ERR_REF_DET		CH6 - Reference detect error	0x0	R

CHANNEL 7 STATUS REGISTER

Address: 0x53, Reset: 0x00, Name: CH7_ERR_REG

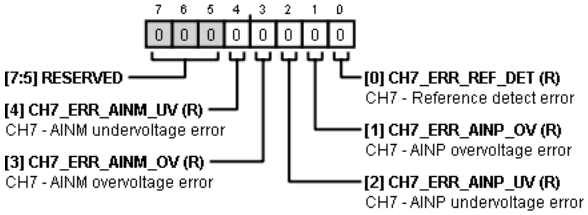


Table 118. Bit descriptions for CH7_ERR_REG

Bits	Bit Name	Settings	Description	Reset	Access
4	CH7_ERR_AINM_UV		CH7 - AINM undervoltage error	0x0	R
3	CH7_ERR_AINM_OV		CH7 - AINM overvoltage error	0x0	R
2	CH7_ERR_AINP_UV		CH7 - AINP undervoltage error	0x0	R
1	CH7_ERR_AINP_OV		CH7 - AINP overvoltage error	0x0	R
0	CH7_ERR_REF_DET		CH7 - Reference detect error	0x0	R

CHANNEL 0/1 DSP ERRORS REGISTER

Address: 0x54, Reset: 0x00, Name: CH0_1_SAT_ERR

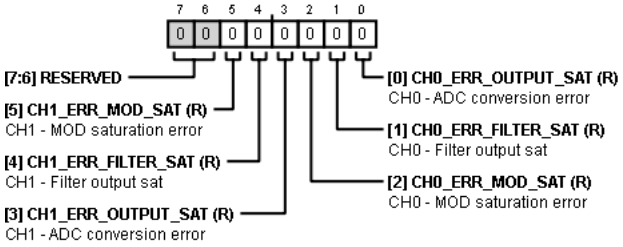


Table 119. Bit descriptions for CH0_1_SAT_ERR

Bits	Bit Name	Settings	Description	Reset	Access
5	CH1_ERR_MOD_SAT		CH1 - MOD saturation error. Modulator output saturation: If the modulator output is 20 consecutive 1's or 0's this bit will be set to indicate a modulator saturation event	0x0	R
4	CH1_ERR_FILTER_SAT		CH1 - Filter output sat. ADC filter output saturation: this bit will indicate if the filter is saturated after gain and offset correction is applied to the signal	0x0	R
3	CH1_ERR_OUTPUT_SAT		CH1 - ADC conversion error. ADC conversion error detected cannot be turned off Conversion errors occurs for following 2 cases: 1: Conversion result is clamped at positive full scale 2: Conversion result is clamped at negative full scale	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
2	CH0_ERR_MOD_SAT		CH0 - MOD saturation error. Modulator output saturation: If the modulator output is 20 consecutive 1's or 0's this bit will be set to indicate a modulator saturation event	0x0	R
1	CH0_ERR_FILTER_SAT		CH0 - Filter output sat. ADC filter output saturation: this bit will indicate if the filter is saturated after gain and offset correction is applied to the signal	0x0	R
0	CH0_ERR_OUTPUT_SAT		CH0 - ADC conversion error. ADC conversion error detected cannot be turned off Conversion errors occurs for following 2 cases: 1: Conversion result is clamped at positive full scale 2: Conversion result is clamped at negative full scale	0x0	R

CHANNEL 2/3 DSP ERRORS REGISTER

Address: 0x55, Reset: 0x00, Name: CH2_3_SAT_ERR

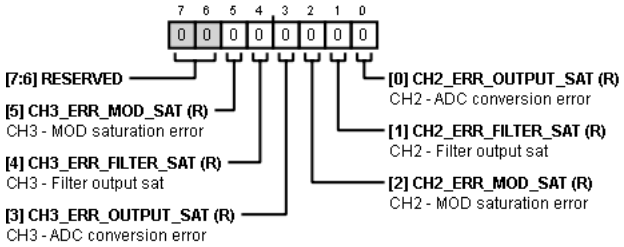


Table 120. Bit descriptions for CH2_3_SAT_ERR

Bits	Bit Name	Settings	Description	Reset	Access
5	CH3_ERR_MOD_SAT		CH3 - MOD saturation error. Modulator output saturation: If the modulator output is 20 consecutive 1's or 0's this bit will be set to indicate a modulator saturation event	0x0	R
4	CH3_ERR_FILTER_SAT		CH3 - Filter output sat. ADC filter output saturation: this bit will indicate if the filter is saturated after gain and offset correction is applied to the signal	0x0	R
3	CH3_ERR_OUTPUT_SAT		CH3 - ADC conversion error. ADC conversion error detected cannot be turned off Conversion errors occurs for following 2 cases: 1: Conversion result is clamped at positive full scale 2: Conversion result is clamped at negative full scale	0x0	R
2	CH2_ERR_MOD_SAT		CH2 - MOD saturation error. Modulator output saturation: If the modulator output is 20 consecutive 1's or 0's this bit will be set to indicate a modulator saturation event	0x0	R
1	CH2_ERR_FILTER_SAT		CH2 - Filter output sat. ADC filter output saturation: this bit will indicate if the filter is saturated after gain and offset correction is applied to the signal	0x0	R
0	CH2_ERR_OUTPUT_SAT		CH2 - ADC conversion error. ADC conversion error detected cannot be turned off Conversion errors occurs for following 2 cases: 1: Conversion result is clamped at positive full scale 2: Conversion result is clamped at negative full scale	0x0	R

CHANNEL 4/5 DSP ERRORS REGISTER

Address: 0x56, Reset: 0x00, Name: CH4_5_SAT_ERR

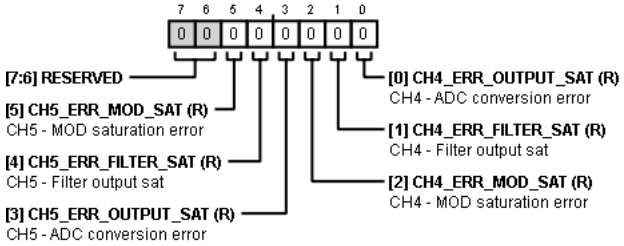


Table 121. Bit descriptions for CH4_5_SAT_ERR

Bits	Bit Name	Settings	Description	Reset	Access
5	CH5_ERR_MOD_SAT		CH5 - MOD saturation error. Modulator output saturation: If the modulator output is 20 consecutive 1's or 0's this bit will be set to indicate a modulator saturation event	0x0	R
4	CH5_ERR_FILTER_SAT		CH5 - Filter output sat. ADC filter output saturation: this bit will indicate if the filter is saturated after gain and offset correction is applied to the signal	0x0	R
3	CH5_ERR_OUTPUT_SAT		CH5 - ADC conversion error. ADC conversion error detected cannot be turned off Conversion errors occurs for following 2 cases: 1: Conversion result is clamped at positive full scale 2: Conversion result is clamped at negative full scale	0x0	R
2	CH4_ERR_MOD_SAT		CH4 - MOD saturation error. Modulator output saturation: If the modulator output is 20 consecutive 1's or 0's this bit will be set to indicate a modulator saturation event	0x0	R
1	CH4_ERR_FILTER_SAT		CH4 - Filter output sat. ADC filter output saturation: this bit will indicate if the filter is saturated after gain and offset correction is applied to the signal	0x0	R
0	CH4_ERR_OUTPUT_SAT		CH4 - ADC conversion error. ADC conversion error detected cannot be turned off Conversion errors occurs for following 2 cases: 1: Conversion result is clamped at positive full scale 2: Conversion result is clamped at negative full scale	0x0	R

CHANNEL 6/7 DSP ERRORS REGISTER

Address: 0x57, Reset: 0x00, Name: CH6_7_SAT_ERR

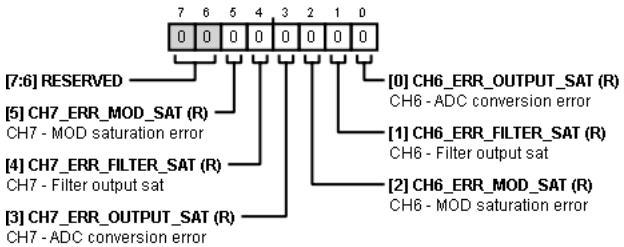


Table 122. Bit descriptions for CH6_7_SAT_ERR

Bits	Bit Name	Settings	Description	Reset	Access
5	CH7_ERR_MOD_SAT		CH7 - MOD saturation error. Modulator output saturation: If the modulator output is 20 consecutive 1's or 0's this bit will be set to indicate a modulator saturation event	0x0	R
4	CH7_ERR_FILTER_SAT		CH7 - Filter output sat. ADC filter output saturation: this bit will indicate if the filter is saturated after gain and offset correction is applied to the signal	0x0	R
3	CH7_ERR_OUTPUT_SAT		CH7 - ADC conversion error. ADC conversion error detected cannot be turned off Conversion errors occurs for following 2 cases: 1: Conversion result is clamped at positive full scale 2: Conversion result is clamped at negative full scale	0x0	R
2	CH6_ERR_MOD_SAT		CH6 - MOD saturation error. Modulator output saturation: If the modulator output is 20 consecutive 1's or 0's this bit will be set to indicate a modulator saturation event	0x0	R
1	CH6_ERR_FILTER_SAT		CH6 - Filter output sat. ADC filter output saturation: this bit will indicate if the filter is saturated after gain and offset correction is applied to the signal	0x0	R
0	CH6_ERR_OUTPUT_SAT		CH6 - ADC conversion error. ADC conversion error detected cannot be turned off Conversion errors occurs for following 2 cases: 1: Conversion result is clamped at positive full scale 2: Conversion result is clamped at negative full scale	0x0	R

CHANNEL 0-7 ERROR REG ENABLE REGISTER

Address: 0x58, Reset: 0xFE, Name: CHX_ERR_REG_EN

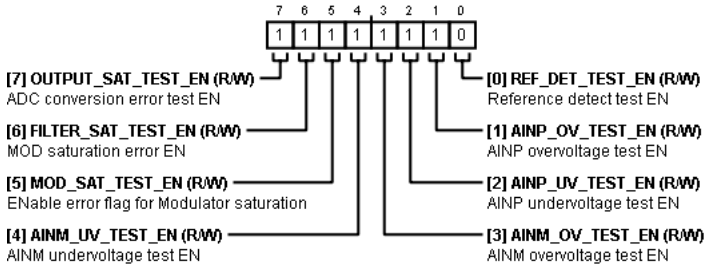


Table 123. Bit descriptions for CHX_ERR_REG_EN

Bits	Bit Name	Settings	Description	Reset	Access
7	OUTPUT_SAT_TEST_EN		ADC conversion error test EN	0x1	R/W
6	FILTER_SAT_TEST_EN		MOD saturation error EN	0x1	R/W
5	MOD_SAT_TEST_EN		ENable error flag for Modulator saturation	0x1	R/W
4	AINM_UV_TEST_EN		AINM undervoltage test EN	0x1	R/W
3	AINM_OV_TEST_EN		AINM overvoltage test EN	0x1	R/W
2	AINP_UV_TEST_EN		AINP undervoltage test EN	0x1	R/W
1	AINP_OV_TEST_EN		AINP overvoltage test EN	0x1	R/W
0	REF_DET_TEST_EN		Reference detect test EN	0x0	R/W

GENERAL ERRORS REGISTER 1

Address: 0x59, Reset: 0x00, Name: GEN_ERR_REG_1

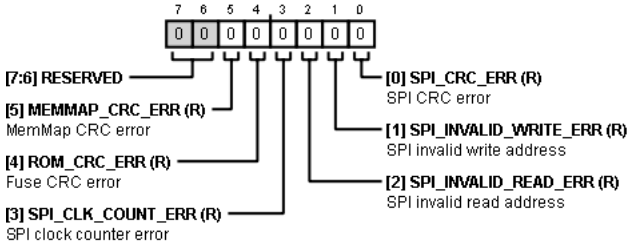


Table 124. Bit descriptions for GEN_ERR_REG_1

Bits	Bit Name	Settings	Description	Reset	Access
5	MEMMAP_CRC_ERR		MemMap CRC error. MemMap CRC error - CRC on MEMMAP is recalculated and compared with a "golden" CRC.	0x0	R
4	ROM_CRC_ERR		Fuse CRC error. Fuse CRC error - Fuse contents copied to shadow registers on powerup. Bias removed from fuse block. Fuse contents and shadow register are verified using a CRC check.	0x0	R
3	SPI_CLK_COUNT_ERR		SPI clock counter error. SPI clock counter error - Count the number of SCLK clock when CSb is low. Must be 16/24/32.	0x0	R
2	SPI_INVALID_READ_ERR		SPI invalid read address. SPI invalid read address - Master attempts to read from an invalid address.	0x0	R
1	SPI_INVALID_WRITE_ERR		SPI invalid write address. SPI invalid write address - Master attempts to write to an invalid address.	0x0	R
0	SPI_CRC_ERR		SPI CRC error. SPI CRC error - Error on 8-bit CRC on SPI reads and writes.	0x0	R

GENERAL ERRORS REGISTER 1 ENABLE

Address: 0x5A, Reset: 0x3E, Name: GEN_ERR_REG_1_EN

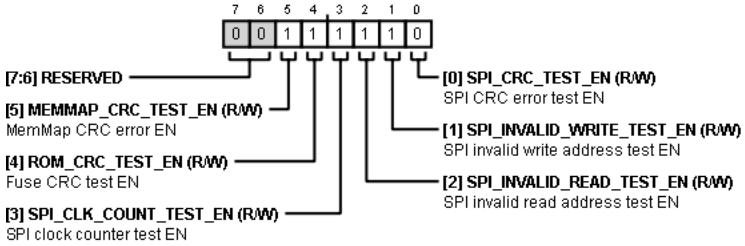


Table 125. Bit descriptions for GEN_ERR_REG_1_EN

Bits	Bit Name	Settings	Description	Reset	Access
5	MEMMAP_CRC_TEST_EN		MemMap CRC error EN	0x1	R/W
4	ROM_CRC_TEST_EN		Fuse CRC test EN	0x1	R/W
3	SPI_CLK_COUNT_TEST_EN		SPI clock counter test EN	0x1	R/W
2	SPI_INVALID_READ_TEST_EN		SPI invalid read address test EN	0x1	R/W
1	SPI_INVALID_WRITE_TEST_EN		SPI invalid write address test EN	0x1	R/W
0	SPI_CRC_TEST_EN		SPI CRC error test EN	0x0	R/W

GENERAL ERRORS REGISTER 2

Address: 0x5B, Reset: 0x00, Name: GEN_ERR_REG_2

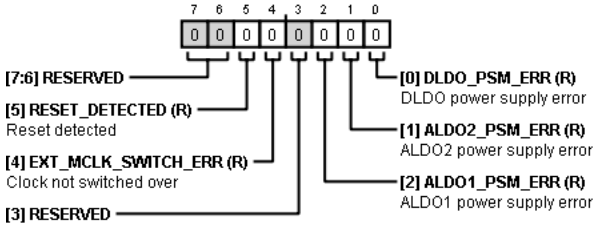


Table 126. Bit descriptions for GEN_ERR_REG_2

Bits	Bit Name	Settings	Description	Reset	Access
5	RESET_DETECTED		Reset detected. Reset detected	0x0	R
4	EXT_MCLK_SWITCH_ERR		Clock not switched over. Clock not switched over	0x0	R
2	ALDO1_PSM_ERR		ALDO1 power supply error. ALDO1 power supply error	0x0	R
1	ALDO2_PSM_ERR		ALDO2 power supply error. ALDO2 power supply error	0x0	R
0	DLDO_PSM_ERR		DLDO power supply error. DLDO power supply error	0x0	R

GENERAL ERRORS REGISTER 2 ENABLE

Address: 0x5C, Reset: 0x3C, Name: GEN_ERR_REG_2_EN

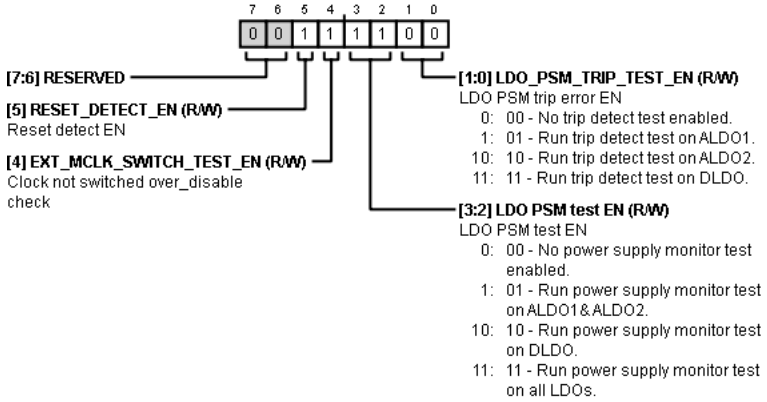


Table 127. Bit descriptions for GEN_ERR_REG_2_EN

Bits	Bit Name	Settings	Description	Reset	Access
5	RESET_DETECT_EN		Reset detect EN	0x1	R/W
4	EXT_MCLK_SWITCH_TEST_EN		Clock not switched over_disable check	0x1	R/W
[3:2]	LDO PSM test EN		LDO PSM test EN	0x3	R/W
		0	00 - No power supply monitor test enabled.		
		1	01 - Run power supply monitor test on ALDO1& ALDO2.		
		10	10 - Run power supply monitor test on DLDO.		
		11	11 - Run power supply monitor test on all LDOs.		

Bits	Bit Name	Settings	Description	Reset	Access
[1:0]	LDO_PSM_TRIP_TEST_EN		LDO PSM trip error EN	0x0	R/W
		0	00 - No trip detect test enabled.		
		1	01 - Run trip detect test on ALDO1.		
		10	10 - Run trip detect test on ALDO2.		
		11	11 - Run trip detect test on DLDO.		

ERROR STATUS REGISTER 1

Address: 0x5D, Reset: 0x00, Name: STATUS_REG_1

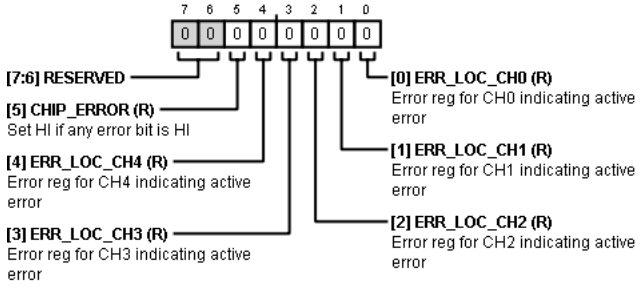


Table 128. Bit descriptions for STATUS_REG_1

Bits	Bit Name	Settings	Description	Reset	Access
5	CHIP_ERROR		Set HI if any error bit is HI. Set HI if any error bit is HI	0x0	R
4	ERR_LOC_CH4		Error reg for CH4 indicating active error. Error reg for CH4 indicating active error	0x0	R
3	ERR_LOC_CH3		Error reg for CH3 indicating active error. Error reg for CH3 indicating active error	0x0	R
2	ERR_LOC_CH2		Error reg for CH2 indicating active error. Error reg for CH2 indicating active error	0x0	R
1	ERR_LOC_CH1		Error reg for CH1 indicating active error. Error reg for CH1 indicating active error	0x0	R
0	ERR_LOC_CH0		Error reg for CH0 indicating active error. Error reg for CH0 indicating active error	0x0	R

ERROR STATUS REGISTER 2

Address: 0x5E, Reset: 0x00, Name: STATUS_REG_2

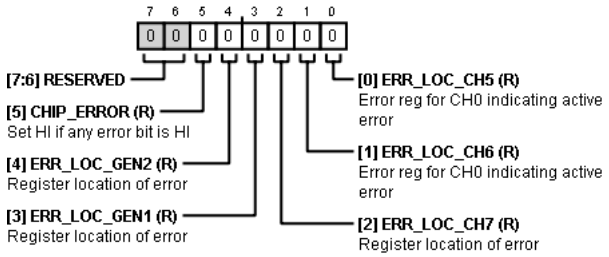


Table 129. Bit descriptions for STATUS_REG_2

Bits	Bit Name	Settings	Description	Reset	Access
5	CHIP_ERROR		Set HI if any error bit is HI. Set HI if any error bit is HI	0x0	R
4	ERR_LOC_GEN2		Register location of error. Register location of general error	0x0	R
3	ERR_LOC_GEN1		Register location of error. Register location of general error	0x0	R
2	ERR_LOC_CH7		Register location of error. Register location of error	0x0	R
1	ERR_LOC_CH6		Error reg for CH0 indicating active error. Register location of error	0x0	R
0	ERR_LOC_CH5		Error reg for CH0 indicating active error. Register location of error	0x0	R

ERROR STATUS REGISTER 3

Address: 0x5F, Reset: 0x00, Name: STATUS_REG_3

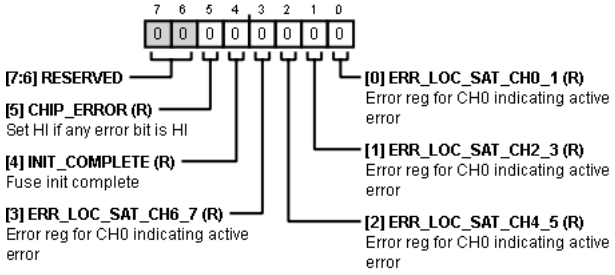


Table 130. Bit descriptions for STATUS_REG_3

Bits	Bit Name	Settings	Description	Reset	Access
5	CHIP_ERROR		Set HI if any error bit is HI. Indicates that there is an error in this register	0x0	R
4	INIT_COMPLETE		Fuse init complete. The INIT complete bit is set after the fuses have been copied over after power up of the device.	0x0	R
3	ERR_LOC_SAT_CH6_7		Error reg for CH0 indicating active error. This bit is set if a saturation event has occurred in the either channel	0x0	R
2	ERR_LOC_SAT_CH4_5		Error reg for CH0 indicating active error. This bit is set if a saturation event has occurred in the either channel	0x0	R
1	ERR_LOC_SAT_CH2_3		Error reg for CH0 indicating active error. This bit is set if a saturation event has occurred in the either channel	0x0	R
0	ERR_LOC_SAT_CH0_1		Error reg for CH0 indicating active error. This bit is set if a saturation event has occurred in the either channel	0x0	R

DECIMATION RATE (N) MSB REGISTER

Address: 0x60, Reset: 0x00, Name: SRC_N_MSB

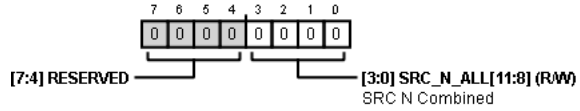


Table 131. Bit descriptions for SRC_N_MSB

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	SRC_N_ALL[11:8]		SRC N Combined	0x0	R/W

DECIMATION RATE (N) LSB REGISTER

Address: 0x61, Reset: 0x80, Name: SRC_N_LSB

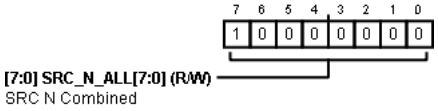


Table 132. Bit descriptions for SRC_N_LSB

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SRC_N_ALL[7:0]		SRC N Combined	0x0	R/W

DECIMATION RATE (IF) MSB REGISTER

Address: 0x62, Reset: 0x00, Name: SRC_IF_MSB

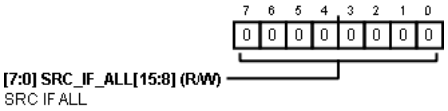


Table 133. Bit descriptions for SRC_IF_MSB

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SRC_IF_ALL[15:8]		SRC IF ALL	0x0	R/W

DECIMATION RATE (IF) LSB REGISTER

Address: 0x63, Reset: 0x00, Name: SRC_IF_LSB

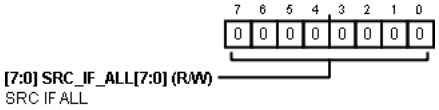


Table 134. Bit descriptions for SRC_IF_LSB

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SRC_IF_ALL[7:0]		SRC IF ALL	0x0	R/W

SRC LOAD SOURCE AND LOAD UPDATE REGISTER

Address: 0x64, Reset: 0x00, Name: SRC_UPDATE

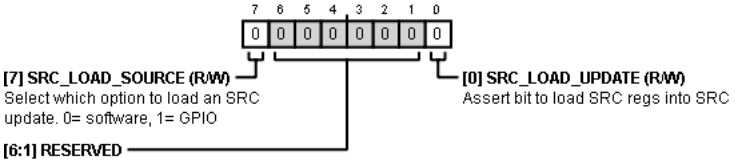


Table 135. Bit descriptions for SRC_UPDATE

Bits	Bit Name	Settings	Description	Reset	Access
7	SRC_LOAD_SOURCE		Select which option to load an SRC update. 0= software, 1= GPIO	0x0	R/W
0	SRC_LOAD_UPDATE		Assert bit to load SRC regs into SRC	0x0	R/W

OUTLINE DIMENSIONS

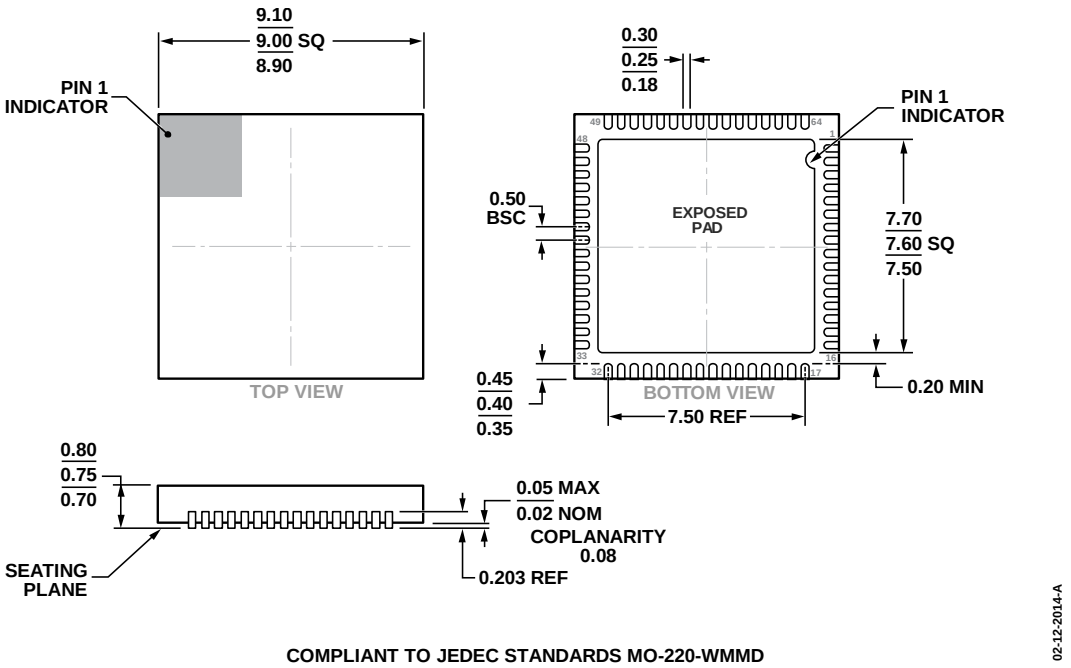


Figure 37.Package Drawing

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7779	−40°C to +105°C	64 pin LFCSP	64-LFCSP-15

PR13295-0-10/15(PrD)