High Accuracy, Hall-Effect-Based, 200 kHz Bandwidth, Galvanically Isolated Current Sensor IC with 100 µΩ Current Conductor

FEATURES AND BENEFITS

- AEC-Q100 Grade 1 qualified
- Typical of 2.5 µs output response time
- 3.3 V supply operation
- Ultra-low power loss: 100 µΩ internal conductor resistance
- Reinforced galvanic isolation allows use in economical, high-side current sensing in high-voltage systems
- 4800 Vrms dielectric strength certified under UL60950-1
- Industry-leading noise performance with greatly improved bandwidth through proprietary amplifier and filter design techniques
- Integrated shield greatly reduces capacitive coupling from current conductor to die due to high dV/dt signals, and prevents offset drift in high-side, high-voltage applications
- Greatly improved total output error through digitally programmed and compensated gain and offset over the full operating temperature range
- Small package size, with easy mounting capability
- Monolithic Hall IC for high reliability
- Output voltage proportional to AC or DC currents
- Factory-trimmed for accuracy
- Extremely stable output offset voltage

Package: 5-pin package (suffix CB)

Not to scale

DESCRIPTION

The Allegro™ ACS773 family of current sensor ICs provide economical and precise solutions for AC or DC current sensing, ideal for motor control, load detection and management, power supply and DC-to-DC converter control, and inverter control. The 2.5 µs response time enables overcurrent fault detection in safety-critical applications.

The device consists of a precision, low-offset linear Hall circuit with a copper conduction path located near the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional output voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy at the factory. Proprietary digital temperature compensation technology greatly improves the IC accuracy and temperature stability.

High-level immunity to current conductor dV/dt and stray electric fields is offered by Allegro proprietary integrated shield technology for low output voltage ripple and low offset drift in high-side, high-voltage applications.

The output of the device increases when an increasing current flows through the primary copper conduction path (from terminal 4 to terminal 5), which is the path used for current sampling. The internal resistance of this conductive path is 100 µΩ typical, providing low power loss.

The thickness of the copper conductor allows survival of the device at high overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads (pins 1 through 3). This allows the ACS773 family of sensor

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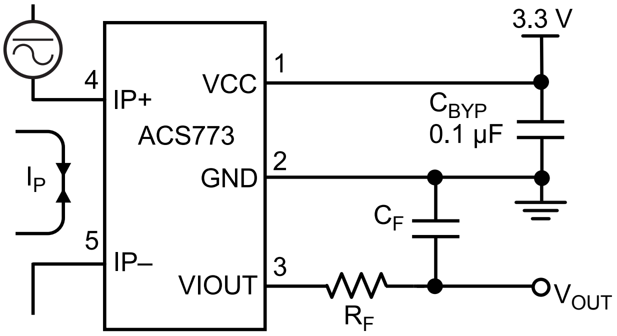
Application 1: the ACS773 outputs an analog signal, V_{OUT}, that varies linearly with the bidirectional AC or DC primary sensed current, I_P, within the range specified. R_F and C_F are for optimal noise management, with values that depend on the application.



Typical Application

DESCRIPTION (continued)

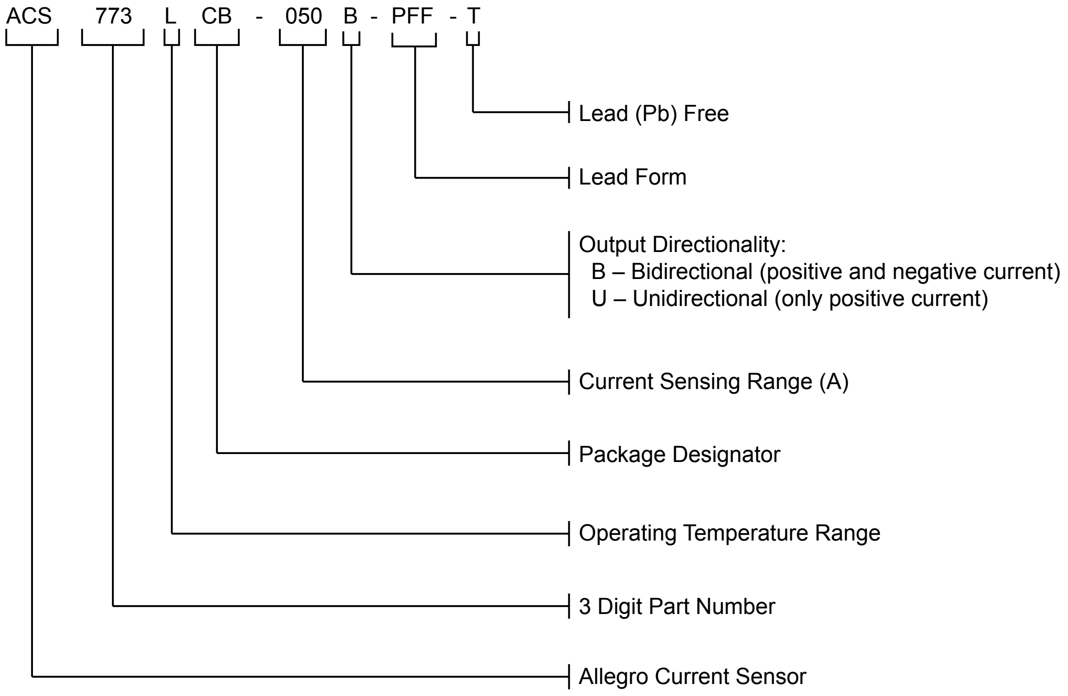
ICs to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The device is fully calibrated prior to shipment from the factory. The ACS773 family is lead (Pb) free. All leads are plated with 100% matte tin, and there is no Pb inside the package. The heavy gauge leadframe is made of oxygen-free copper.

SELECTION GUIDE

Part Number [1]	Package		Primary Sampled Current , I_P (A)	Sensitivity Sens (Typ.) (mV/A) [2]	T_{OP} (°C)	Packing [3]
	Terminals	Signal Pins				
ACS773LCB-050B-PFF-T	Formed	Formed	±50	26.4	–40 to 150	34 pieces per tube
ACS773LCB-100B-PFF-T	Formed	Formed	±100	13.2		
ACS773ECB-200B-PFF-T	Formed	Formed	±200	6.6	–40 to 85	

[1] Additional leadform options available for qualified volumes.
[2] Measured at V_{CC} = 3.3 V.
[3] Contact Allegro for additional packing options.



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}		6.5	V
Reverse Supply Voltage	V_{RCC}		–0.5	V
Output Voltage	V_{IOUT}		6.5	V
Reverse Output Voltage	V_{RIOUT}		–0.5	V
Output Source Current	$I_{OUT(Source)}$	VIOUT to GND	3	mA
Output Sink Current	$I_{OUT(Sink)}$	Minimum pull-up resistor of 500 Ω from VCC to VIOUT	10	mA
Nominal Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range K	–40 to 125	°C
		Range L	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Dielectric Strength Test Voltage [1]	V_{ISO}	Agency type-tested for 60 seconds per UL standard 60950-1, 2nd Edition. Tested at 3000 V_{RMS} for 1 second in production.	4800	V_{RMS}
Working Voltage for Basic Isolation	V_{WVBI}	For basic (single) isolation per UL standard 60950-1, 2nd Edition	990	V_{PK} or V_{DC}
			700	V_{RMS}
Working Voltage for Reinforced Isolation	V_{WFRI}	For reinforced (double) isolation per UL standard 60950-1, 2nd Edition	636	V_{PK} or V_{DC}
			450	V_{RMS}

[1] Allegro does not conduct 60-second testing. It is done only during the UL certification process.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

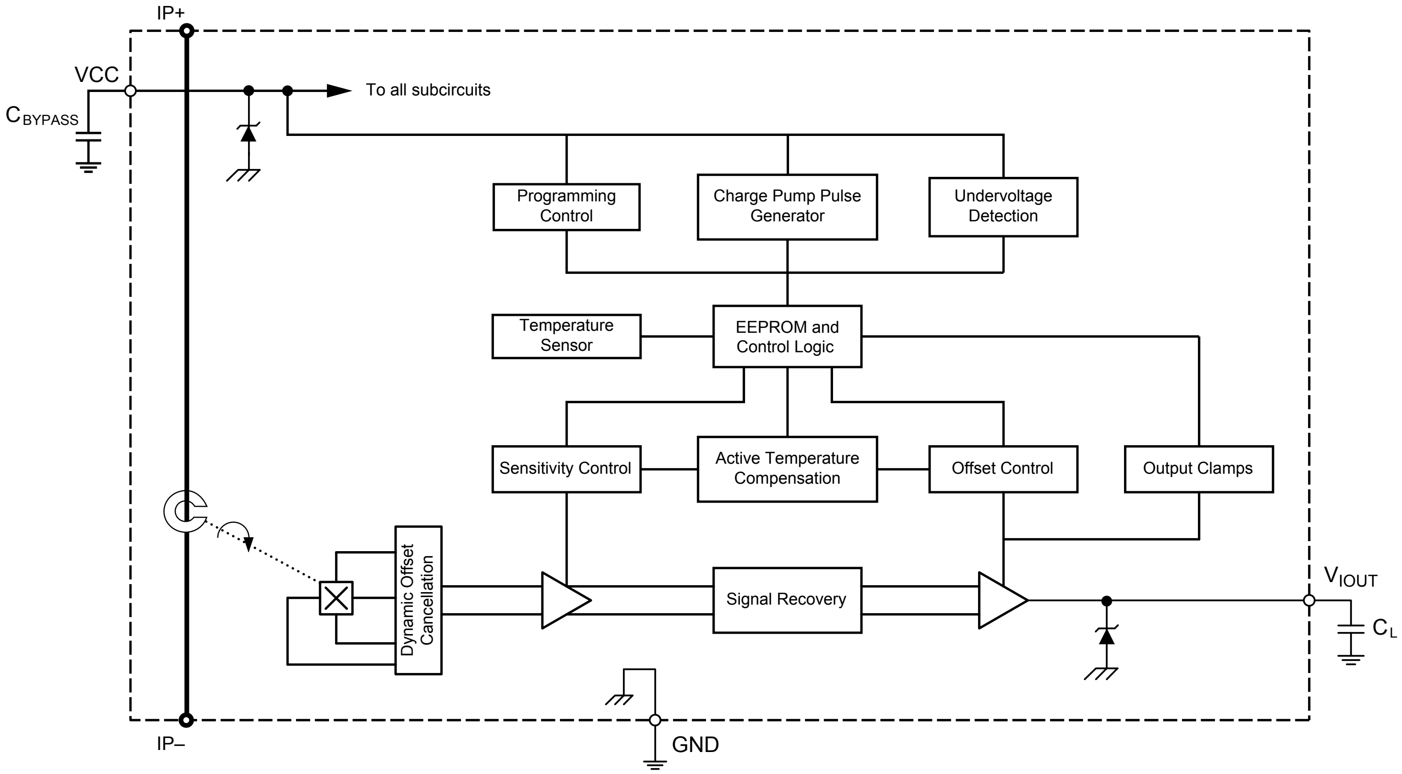
Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Mounted on the Allegro evaluation board with 2800 mm^2 (1400 mm^2 on component side and 1400 mm^2 on opposite side) of 4 oz. copper connected to the primary leadframe and with thermal vias connecting the copper layers. Performance is based on current flowing through the primary leadframe and includes the power consumed by the PCB.	7	°C/W

[2] Additional thermal information available on the Allegro website

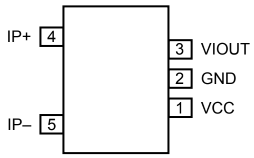
TYPICAL OVERCURRENT CAPABILITIES [3][4]

Characteristic	Symbol	Notes	Rating	Unit
Overcurrent	I_{POC}	T_A = 25°C, current is on for 1 second and off for 99 seconds, 100 pulses applied	1200	A
		T_A = 85°C, current is on for 1 second and off for 99 seconds, 100 pulses applied	900	A
		T_A = 150°C, current is on for 1 second and off for 99 seconds, 100 pulses applied	600	A

[3] Test was done with Allegro evaluation board. The maximum allowed current is limited by T_J(max) only.
[4] For more overcurrent profiles, please see FAQ on the Allegro website, www.allegromicro.com.



Functional Block Diagram



Pinout Diagram

Terminal List Table

Number	Name	Description
1	VCC	Device power supply terminal
2	GND	Signal ground terminal
3	VIOUT	Analog output signal
4	IP+	Terminal for current being sampled
5	IP–	Terminal for current being sampled

COMMON OPERATING CHARACTERISTICS: Valid at T_{OP} = –40°C to 150°C, C_{BYP} = 0.1 µF, and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		3	3.3	3.6	V
Supply Current	I_{CC}	V_{CC} ≤ 5 V, no load on output	–	10	15	mA
Power-On Delay	t_{POD}	T_A = 25°C	–	64	–	µs
Power-On Reset Voltage	V_{PORH}	V_{CC} rising at 1 V/ms	–	2.9	–	V
	V_{PORL}	V_{CC} falling at 1 V/ms	–	2.5	–	V
POR Hysteresis	$V_{HYS(POR)}$		250	–	–	mV
Internal Bandwidth	BW_i	Small signal –3 dB, C_L = 4.7 nF	–	200	–	kHz
Rise Time	t_r	I_P step = 50% of I_P+, 10% to 90% rise time, T_A = 25°C, C_{OUT} = 470 pF	–	2.4	–	µs
Propagation Delay Time	t_{PROP}	T_A = 25°C, C_L = 470 pF, IP step = 50% of IP+	–	1.2	–	µs
Response Time	$t_{RESPONSE}$	T_A = 25°C, C_L = 470 pF, IP step = 50% of IP+, 90% input to 90% output	–	2.5	–	µs
DC Output Impedance	R_{OUT}	T_A = 25°C	–	3.3	–	Ω
Output Load Resistance	$R_{LOAD(MIN)}$	VIOUT to GND, VIOUT to VCC	4.7	–	–	kΩ
Output Load Capacitance	$C_{LOAD(MAX)}$	VIOUT to GND	–	1	10	nF
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	100	–	µΩ
Output Saturation Voltage	$V_{SAT(HIGH)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	V_{CC} – 0.2	–	–	V
	$V_{SAT(LOW)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	–	–	200	mV
ERROR COMPONENTS						
QVO Ratiometry Error [1]	Rat_{ERRQVO}	V_{CC} = 3.15 to 3.45 V	–	±0.15	–	%
Sens Ratiometry Error [1]	$Rat_{ERRSens}$	V_{CC} = 3.15 to 3.45 V	–	±0.3	–	%
Noise	I_N	Input referenced noise density; T_A = 25°C, C_L = 1 nF	–	0.2	–	$\text{mA}/\sqrt{(\text{Hz})}$
		Input referenced noise at 200 kHz; T_A = 25°C, C_L = 1 nF	–	120	–	mA_{RMS}
Nonlinearity [1]	E_{LIN}	Up to full scale of I_P	–0.9	±0.5	0.9	%
Symmetry [1]	E_{SYM}	Over half-scale I_P	–0.8	±0.4	0.8	%

[1] See Characteristic Definitions section of this datasheet.

***X*050B PERFORMANCE CHARACTERISTICS: T_A = –40°C to 150°C, V_{CC} = 3.3 V, unless otherwise specified**

Characteristic	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
NOMINAL PERFORMANCE						
Current Sensing Range [1]	I_{PR}		–50	–	50	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	26.4 × V_{CC} / 3.3	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	Bidirection; I_P = 0 A	–	$V_{CC}/2$	–	V
ACCURACY PERFORMANCE						
Noise	V_N	T_A = 25°C, C_L = 1 nF	–	19.2	–	mV_{p-p}
		T_A = 25°C, C_L = 1 nF	–	3.2	–	mV_{RMS}
Sensitivity Error	E_{Sens}	Full scale of I_P, T_A = 25°C	–1	±0.5	1	%
		Full scale of I_P, T_{OP} = 25°C to 150°C	–1.25	±1	1.25	%
		Full scale of I_P, T_{OP} = –40°C to 25°C	–3.5	±1.5	3.5	%
Electrical Offset Error	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–8	±4	8	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–8	±4	8	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of $I_{PR(max)}$	–	210	250	mA
Total Output Error	$E_{TOT(HT)}$	Full scale of I_P, T_{OP} = 25°C to 150°C	–1.5	±1	1.5	%
	$E_{TOT(LT)}$	Full scale of I_P, T_{OP} = –40°C to 25°C	–3.5	±1.5	3.5	%
LIFETIME ACCURACY CHARACTERISTICS [3]						
Sensitivity Error Including Lifetime	$E_{Sens(LIFE)(HT)}$	T_{OP} = 25°C to 150°C	–2.1	±1.6	2.1	%
	$E_{Sens(LIFE)(LT)}$	T_{OP} = –40°C to 25°C	–3.5	±2.5	3.5	%
Total Output Error Including Lifetime	$E_{TOT(LIFE)(HT)}$	T_{OP} = 25°C to 150°C	–2.1	±1.7	2.1	%
	$E_{TOT(LIFE)(LT)}$	T_{OP} = –40°C to 25°C	–3.5	±2.6	3.5	%
Electric Offset Error Including Lifetime	$E_{OFF(LIFE)(HT)}$	T_{OP} = 25°C to 150°C	–10	±7	10	mV
	$E_{OFF(LIFE)(LT)}$	T_{OP} = –40°C to 25°C	–20	±8.9	20	mV

[1] Device may be operated at higher primary current levels, I_P, ambient, T_A, and internal leadframe temperatures, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2] Typical values are ±3 sigma values.

[3] Min/max limits come from AEC-Q100 Grade 1 testing.

X100B PERFORMANCE CHARACTERISTICS: T_A = –40°C to 150°C, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
NOMINAL PERFORMANCE						
Current Sensing Range [1]	I_{PR}		–100	–	100	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	13.2 × V_{CC} / 3.3	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	Bidirection; I_P = 0 A	–	V_{CC}/2	–	V
ACCURACY PERFORMANCE						
Noise	V_N	T_A = 25°C, C_L = 1 nF	–	9.6	–	mV_{p-p}
		T_A = 25°C, C_L = 1 nF	–	1.6	–	mV_{RMS}
Sensitivity Error	E_{Sens}	Full scale of I_P, T_A = 25°C	–1	±0.5	1	%
		Full scale of I_P, T_{OP} = 25°C to 150°C	–1.25	±1	1.25	%
		Full scale of I_P, T_{OP} = –40°C to 25°C	–3.5	±1.5	3.5	%
Electrical Offset Error	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–8	±4	8	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–8	±4	8	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of $I_{PR(max)}$	–	280	400	mA
Total Output Error	$E_{TOT(HT)}$	Full scale of I_P, T_{OP} = 25°C to 150°C	–1.5	±1	1.5	%
	$E_{TOT(LT)}$	Full scale of I_P, T_{OP} = –40°C to 25°C	–3.5	±1.5	3.5	%
LIFETIME ACCURACY CHARACTERISTICS [3]						
Sensitivity Error Including Lifetime	$E_{Sens(LIFE)(HT)}$	T_{OP} = 25°C to 150°C	–2.1	±1.6	2.1	%
	$E_{Sens(LIFE)(LT)}$	T_{OP} = –40°C to 25°C	–3.5	±2.5	3.5	%
Total Output Error Including Lifetime	$E_{TOT(LIFE)(HT)}$	T_{OP} = 25°C to 150°C	–2.1	±1.7	2.1	%
	$E_{TOT(LIFE)(LT)}$	T_{OP} = –40°C to 25°C	–3.5	±2.6	3.5	%
Electric Offset Error Including Lifetime	$E_{OFF(LIFE)(HT)}$	T_{OP} = 25°C to 150°C	–10	±7	10	mV
	$E_{OFF(LIFE)(LT)}$	T_{OP} = –40°C to 25°C	–20	±8.9	20	mV

[1] Device may be operated at higher primary current levels, I_P, ambient, T_A, and internal leadframe temperatures, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2] Typical values are ±3 sigma values.

[3] Min/max limits come from AEC-Q100 Grade 1 testing.

_X_200B PERFORMANCE CHARACTERISTICS: T_A = –40°C to 85°C, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
NOMINAL PERFORMANCE						
Current Sensing Range [1]	I_{PR}		–200	–	200	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	6.6 × V_{CC} / 3.3	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	Bidirection; I_P = 0 A	–	$V_{CC}/2$	–	V
ACCURACY PERFORMANCE						
Noise	V_N	T_A = 25°C, C_L = 1 nF	–	4.8	–	mV_{p-p}
		T_A = 25°C, C_L = 1 nF	–	0.8	–	mV_{RMS}
Sensitivity Error	E_{Sens}	Half scale of I_P, T_A = 25°C	–1	±0.5	1	%
		Half scale of I_P, T_{OP} = 25°C to 85°C	–1.25	±1	1.25	%
		Half scale of I_P, T_{OP} = –40°C to 25°C	–3.5	±1.5	3.5	%
Electrical Offset Error	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–8	±4	8	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 85°C	–8	±4	8	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of $I_{PR(max)}$	–	380	450	mA
Total Output Error	$E_{TOT(HT)}$	Half scale of I_P, T_{OP} = 25°C to 85°C	–1.5	±1	1.5	%
	$E_{TOT(LT)}$	Half scale of I_P, T_{OP} = –40°C to 25°C	–3.5	±1.5	3.5	%
LIFETIME ACCURACY CHARACTERISTICS [3]						
Sensitivity Error Including Lifetime	$E_{Sens(LIFE)(HT)}$	T_{OP} = 25°C to 85°C	–2.1	±1.6	2.1	%
	$E_{Sens(LIFE)(LT)}$	T_{OP} = –40°C to 25°C	–3.5	±2.5	3.5	%
Total Output Error Including Lifetime	$E_{TOT(LIFE)(HT)}$	T_{OP} = 25°C to 85°C	–2.1	±1.7	2.1	%
	$E_{TOT(LIFE)(LT)}$	T_{OP} = –40°C to 25°C	–3.5	±2.6	3.5	%
Electric Offset Error Including Lifetime	$E_{OFF(LIFE)(HT)}$	T_{OP} = 25°C to 85°C	–10	±7	10	mV
	$E_{OFF(LIFE)(LT)}$	T_{OP} = –40°C to 25°C	–20	±8.9	20	mV

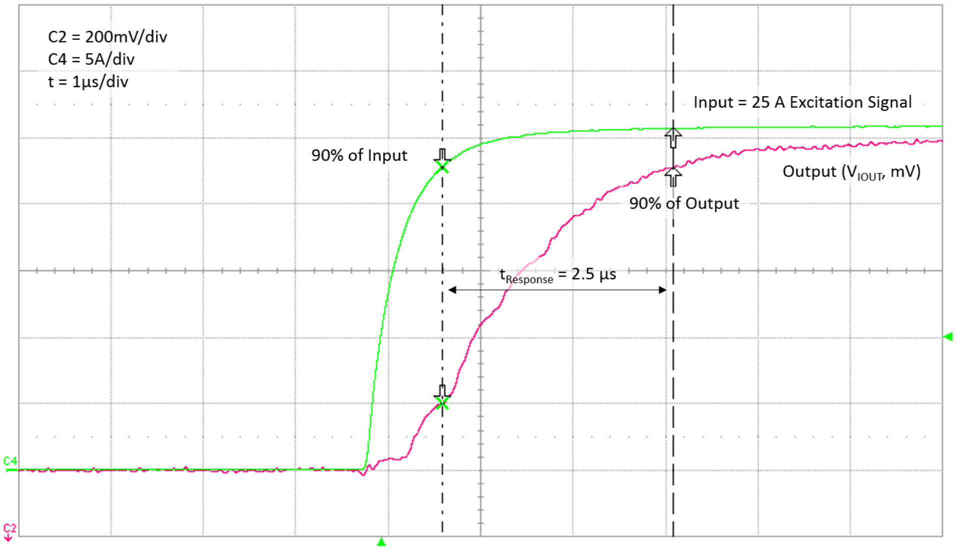
[1] Device may be operated at higher primary current levels, I_P, ambient, T_A, and internal leadframe temperatures, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2] Typical values are ±3 sigma values.

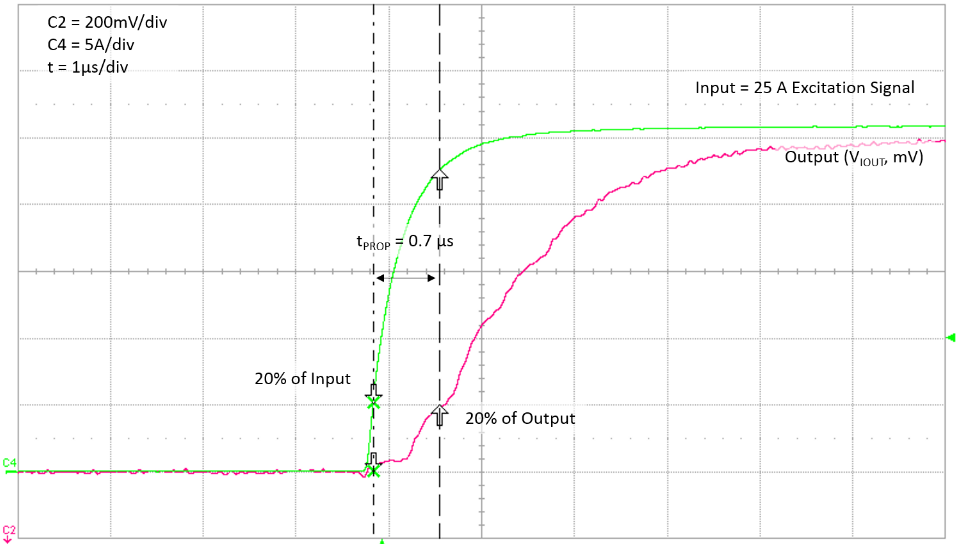
[3] Min/max limits come from AEC-Q100 Grade 1 testing.

CHARACTERISTIC PERFORMANCE DATA

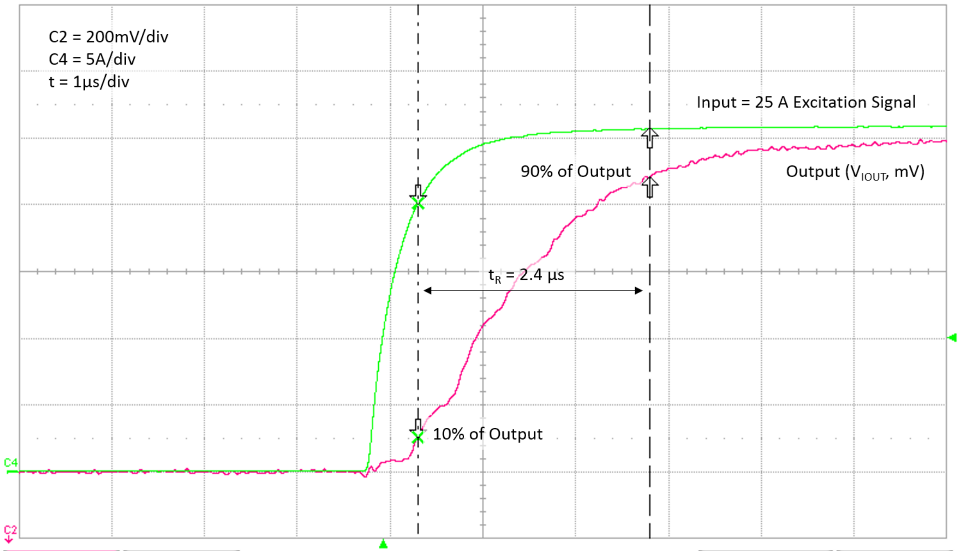
Response Time ($t_{RESPONSE}$)
25 A excitation signal with 10%-90% rise time = 1 µs
Sensitivity = 40 mV/A, C_{BYPASS} = 0.1 µF, C_L = 1 nF



Propagation Delay (t_{PROP})
25 A excitation signal with 10%-90% rise time = 1 µs
Sensitivity = 40 mV/A, C_{BYPASS} = 0.1 µF, C_L = 1 nF



Rise Time (t_R)
25 A excitation signal with 10%-90% rise time = 1 µs
Sensitivity = 40 mV/A, C_{BYPASS} = 0.1 µF, C_L = 1 nF



CHARACTERISTIC DEFINITIONS

Definitions of Accuracy Characteristics

SENSITIVITY (Sens)

The change in sensor IC output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A; 1 G = 0.1 mT) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

SENSITIVITY ERROR (E_{Sens})

The sensitivity error is the percent difference between the measured sensitivity and the ideal sensitivity. For example, in the case of V_{CC} = 3.3 V:

$$E_{\mathrm{Sens}} = \frac{Sens_{\mathrm{Meas(3.3V)}} - Sens_{\mathrm{Ideal(3.3V)}}}{Sens_{\mathrm{IDEAL(3.3V)}}} \times 100\ (\%)$$

NOISE (V_N)

The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

NONLINEARITY (E_{LIN})

The ACS773 is designed to provide a linear output in response to a ramping current. Consider two current levels: I1 and I2. Ideally, the sensitivity of a device is the same for both currents, for a given supply voltage and temperature. Nonlinearity is present when there is a difference between the sensitivities measured at I1 and I2. Nonlinearity is calculated separately for the positive (E_{LINpos}) and negative (E_{LINneg}) applied currents as follows:

$$E_{LINpos} = 100\ (\%) \times \{1 - (Sens_{IPOS2} / Sens_{IPOS1})\}$$

$$E_{LINneg} = 100\ (\%) \times \{1 - (Sens_{INEG2} / Sens_{INEG1})\}$$

where:

$$Sens_{Ix} = (V_{IOUT(Ix)} - V_{IOUT(Q)}) / Ix$$

and I_{POSx} and I_{NEGx} are positive and negative currents.

Then:

$$E_{LIN} = \max(E_{LINpos}, E_{LINneg})$$

SYMMETRY (E_{SYM})

The degree to which the absolute voltage output from the IC varies in proportion to either a positive or negative half-scale primary current. The following equation is used to derive symmetry:

$$100 \times \left(\frac{V_{IOUT\_+half\text{-}scale\ amperes} - V_{IOUT(Q)}}{V_{IOUT(Q)} - V_{IOUT\_-half\text{-}scale\ amperes}} \right)$$

RATIOMETRY ERROR

The device features a ratiometric output. This means that the quiescent voltage output, V_{IOUTQ}, and the magnetic sensitivity, Sens, are proportional to the supply voltage, V_{CC}.The ratiometric change (%) in the quiescent voltage output is defined as:

$$\mathrm{Rat}_{\mathrm{ErrQVO}} = \left[1 - \frac{(V_{IOUTQ(VCC)} / V_{IOUTQ(3.3V)})}{V_{CC} / 3.3\ V} \right] \times 100\%$$

and the ratiometric change (%) in sensitivity is defined as:

$$\mathrm{Rat}_{\mathrm{ErrSens}} = \left[1 - \frac{(Sens_{(VCC)} / Sense_{(3.3V)})}{V_{CC} / 3.3\ V} \right] \times 100\%$$

ZERO CURRENT OUTPUT VOLTAGE ($V_{IOUT(Q)}$)

The output of the sensor when the primary current is zero. It nominally remains at 0.5 × V_{CC} for a bidirectional device and 0.1 × V_{CC} for a unidirectional device. For example, in the case of a bidirectional output device, V_{CC} = 3.3 V translates into $V_{IOUT(Q)}$ = 1.65 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

ELECTRICAL OFFSET VOLTAGE (V_{OE})

The deviation of the device output from its ideal quiescent value of 0.5 × V_{CC} (bidirectional) or 0.1 × V_{CC} (unidirectional) due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

MAGNETIC OFFSET ERROR (I_{ERROM})

The magnetic offset is due to the residual magnetism (remnant field) of the core material. The magnetic offset error is highest when the magnetic circuit has been saturated, usually when the device has been subjected to a full-scale or high-current overload condition. The magnetic offset is largely dependent on the material used as a flux concentrator. The larger magnetic offsets are observed at the lower operating temperatures.

TOTAL OUTPUT ERROR (E_{TOT})

The difference between the current measurement from the sensor IC and the actual current (IP), relative to the actual current. This is equivalent to the difference between the ideal output voltage and the actual output voltage, divided by the ideal sensitivity, relative to the current flowing through the primary conduction path:

$$E_{TOT}(I_P) = \frac{V_{IOUT(IP)} - V_{IOUT(ideal)(IP)}}{Sens_{ideal} \times I_P} \times 100(\%)$$

where

$$V_{IOUT(ideal)(IP)} = V_{IOUT(Q)} + (Sens_{IDEAL} \times I_P)$$

The Total Output Error incorporates all sources of error and is a function of IP.

At relatively high currents, E_{TOT} will be mostly due to sensitivity error, and at relatively low currents, E_{TOT} will be mostly due to Offset Voltage (V_{OE}). In fact, as I_P approaches zero, E_{TOT} approaches infinity due to the offset voltage. This is illustrated in Figure 1 and Figure 2. Figure 1 shows a distribution of output voltages versus I_P at 25°C and across temperature. Figure 2 shows the corresponding E_{TOT} versus I_P.

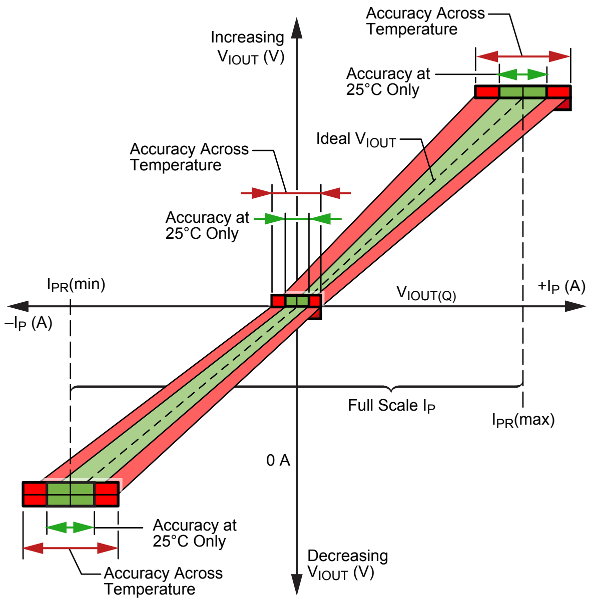


Figure 1: Output Voltage versus Sensed Current

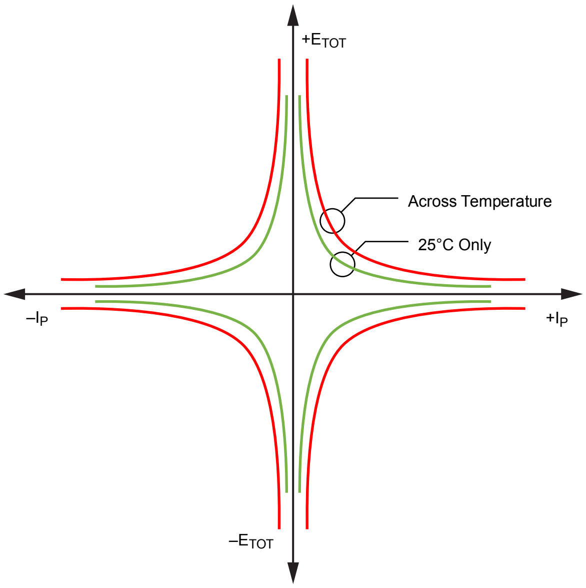


Figure 2: Total Output Error versus Sensed Current

Definitions of Dynamic Response Characteristics

POWER-ON DELAY (t_{POD})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Delay, t_{POD}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.

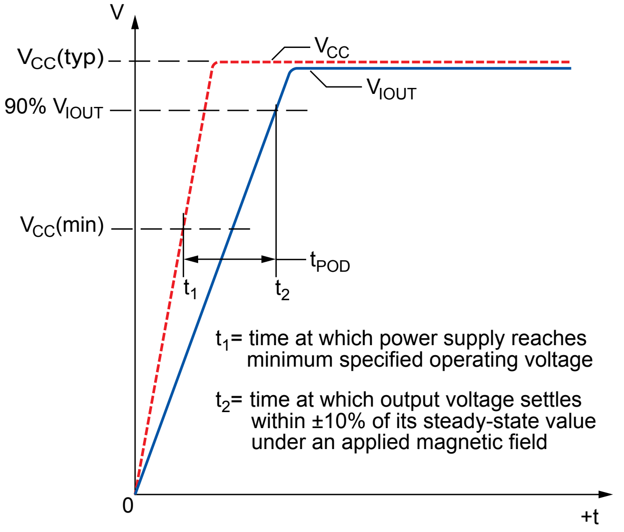


Figure 3: Power-On Delay (t_{POD})

RISE TIME (t_r)

The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

PROPAGATION DELAY (t_{PROP})

The time interval between a) when the sensed current reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value.

RESPONSE TIME ($t_{RESPONSE}$)

The time interval between a) when the applied current reaches 90% of its final value, and b) when the sensor reaches 90% of its output corresponding to the applied current.

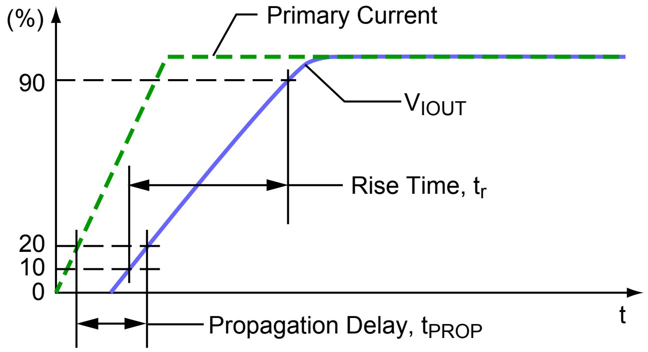


Figure 4: Rise Time (t_r) and Propagation Delay (t_{PROP})

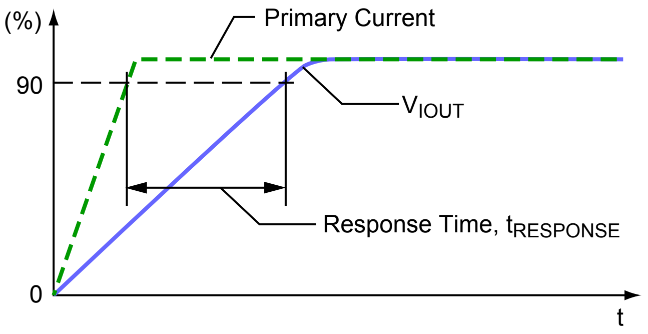


Figure 5: Response Time ($t_{RESPONSE}$)

FUNCTIONAL DESCRIPTION

Power-On Reset (POR)

The descriptions in this section assume: temperature = 25°C, no output load (RL, CL), and I_P = 0 A.

Power-Up

At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH} (location [1] in Figure 6 and [1′] in Figure 7), the POR Release counter starts counting for t_{PORRC} [2, 2′]. At this point, the EEPROM content will be loaded in volatile memory after t_{EELOAD} [3, 3′] and the output will go to $V_{CC}/2$ after t_{PORD} [4, 4′]. The temperature compensation engine will then adjust the device Sensitivity and QVO after time t_{TC} [5, 5′]. The ASIL sequence will then automatically start. ASIL functionality will be described in details in the ASIL Operation at Power-Up section.

V_{CC} drops below V_{CC}(min) = 3 V

If V_{CC} drops below V_{PORH} [6′] but remains higher than V_{PORL} [7′], the output will continue to be $V_{CC}/2$.

Power-Down

As V_{CC} ramps down below V_{PORL} [6, 8’], the output will enter a high-impedance state.

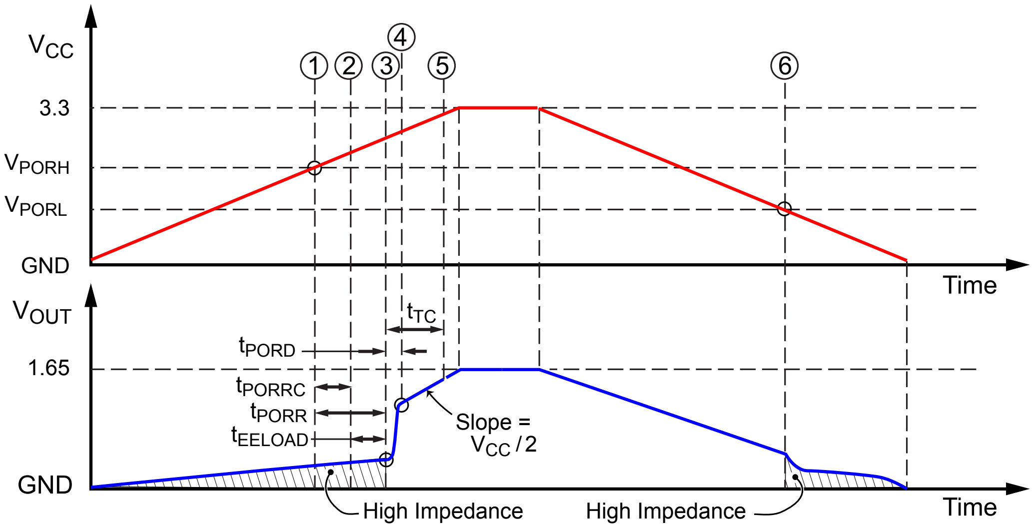


Figure 6: POR: Slow Rise Time Case

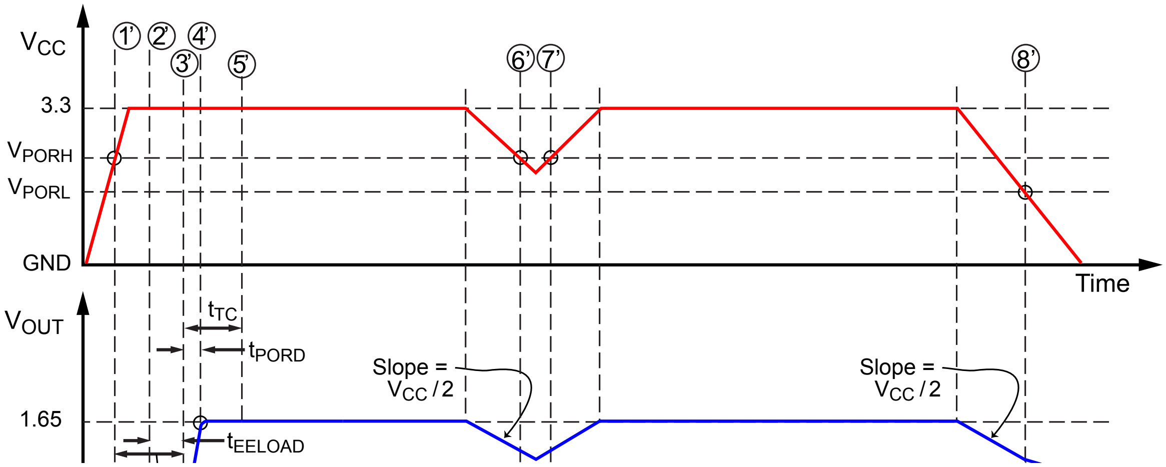


Figure 7: POR: Fast Rise Time Case

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed.

In addition to the removal of the thermal and stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high-frequency sampling clock. For demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

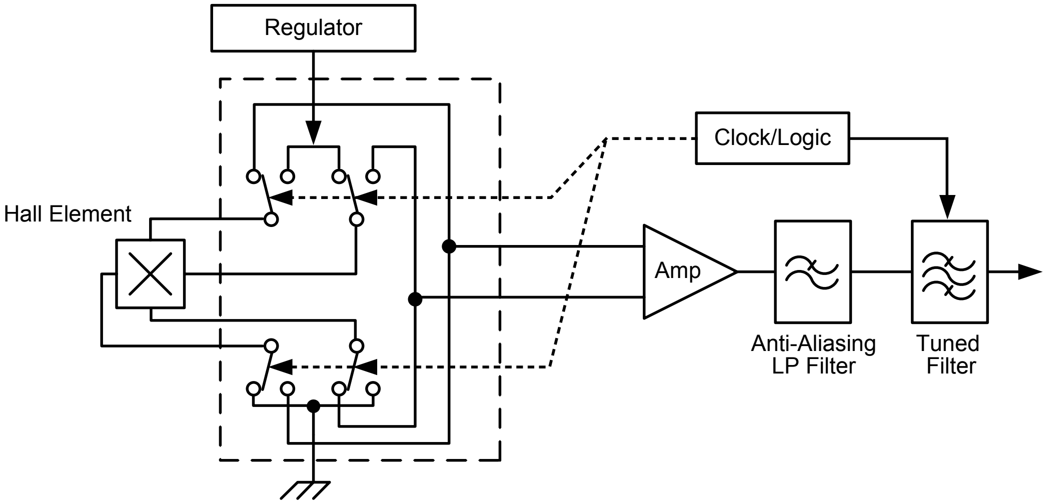
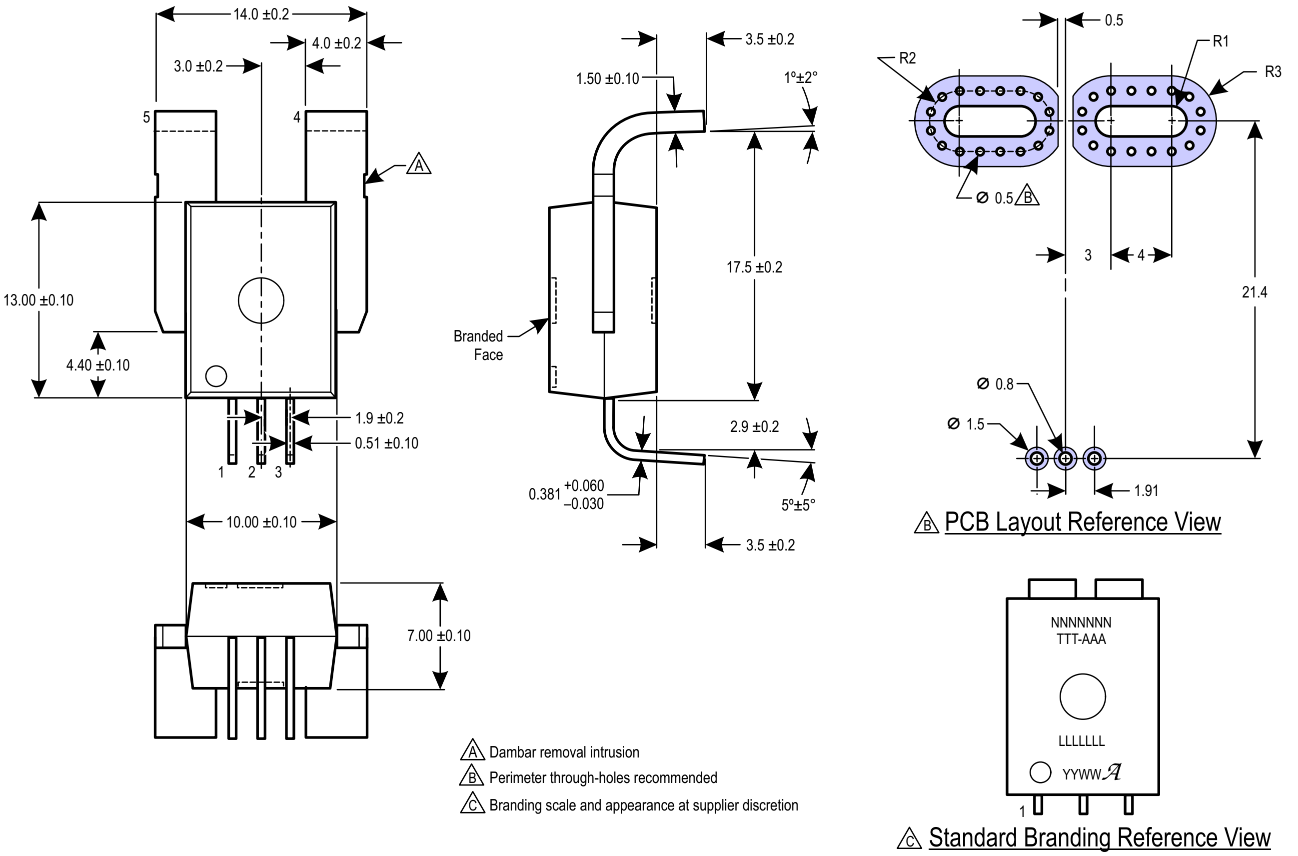


Figure 8: Concept of Chopper Stabilization Technique

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-9111 & DWG-9110)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



N = Device part number
T = Temperature code
A = Amperage range
L = Lot number
Y = Last two digits of year of manufacture
W = Week of manufacture
𝒜 = Supplier emblem

Creepage distance, current terminals to signal pins: 7.25 mm
Clearance distance, current terminals to signal pins: 7.25 mm
Package mass: 4.63 g typical

Figure 9: Package CB, 5-Pin, Leadform PFF

Revision History

Number	Date	Description
–	December 12, 2017	Initial release