

ACPL-M43U-000E

Wide Operating Temperature 1MBd Digital Optocoupler with R²Coupler™ Isolation



Data Sheet



Description

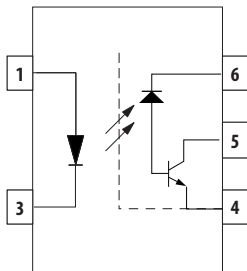
The ACPL-M43U is a single channel, high temperature, high CMR, high speed digital optocoupler in a five lead miniature footprint specifically used for industrial applications. The SO-5 JEDEC registered (MO-155) package outline does not require “through holes” in a PCB. This package occupies approximately one-fourth the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

This digital optocoupler uses an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The ACPL-M43U has an increased common mode transient immunity of 30kV/μs minimum at V_{CM} = 1500V over extended temperature range.

Avago R²Coupler isolation products provide the reinforced insulation and reliability needed for critical in auto-motive and high temperature industrial applications.

Functional Diagram



Truth Table

LED	V _o
ON	LOW
OFF	HIGH

The connection of a 0.1 μF bypass capacitor between pins 4 and 6 is recommended.

Features

- High Temperature and Reliability IPM Driver for Industrial Applications.
- 30 kV/μs High Common-Mode Rejection at V_{CM} = 1500 V (typ)
- Compact, Auto-Insertable SO5 Packages
- Wide Temperature Range: -40°C ~ 125°C
- High Speed: 1MBd (Typ)
- Low LED Drive Current: 10mA (typ)
- Low Propagation Delay: 300ns (typ)
- Worldwide Safety Approval:
 - UL1577 recognized, 3750Vrms/1min
 - CSA Approved
 - IEC/EN/DIN EN 60747-5-2 Approved

Applications

- Industrial Intelligent Power Module isolation for motor controls
- Isolated IGBT/MOSFET gate drive
- AC and brushless dc motor drives
- Industrial inverters for power supplies

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

Part Number	Options		Surface Mount	Tape & Reel	Quantity
	RoHS Compliant	Package			
ACPL-M43U	-000E	SO-5	X		100 per tube
ACPL-M43U	-500E		X	X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

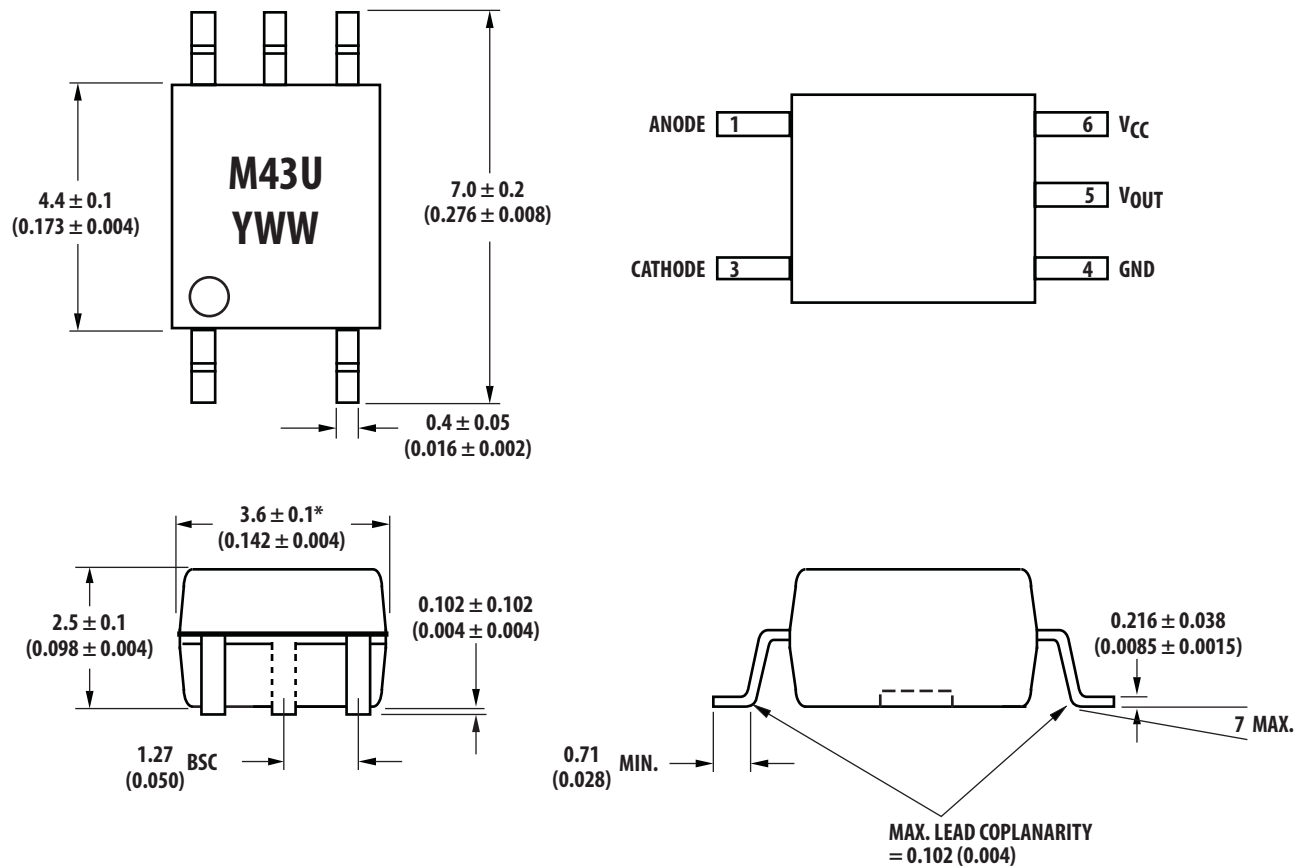
Example 1:

ACPL-M43U-500E to order product of Mini-flat Surface Mount 5-pin package in Tape and Reel packaging with RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

ACPL-M43U Small Outline SO-5 Package (JEDEC MO-155)

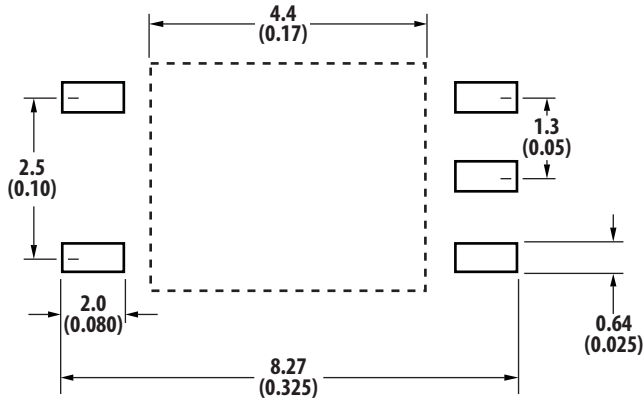


DIMENSIONS IN MILLIMETERS (INCHES)

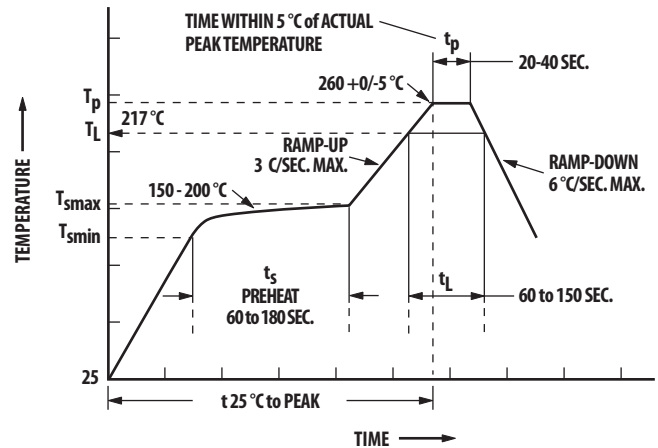
* MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 mm (0.006)

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Land Pattern Recommendation



Recommended Pb-Free IR Profile



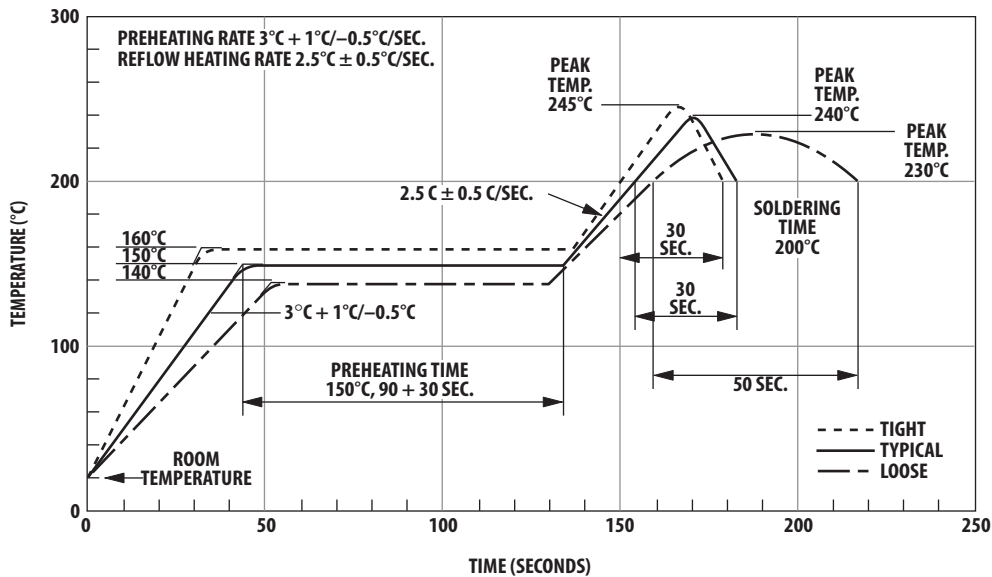
NOTES:

The time from 25 °C to peak temperature = 8 minutes max.

$T_{smax} = 200^\circ\text{C}$, $T_{smin} = 150^\circ\text{C}$

Non-halide flux should be used

Solder Reflow Temperature Profile



Note: Non-halide flux should be used

Regulatory Information

The ACPL-M43U is approved by the following organizations:

UL

Approved under UL 1577, component recognition program up to $V_{ISO} = 3750$ VRMS expected prior to product release.

CSA

Approved under CSA Component Acceptance Notice #5.

IEC/EN/DIN EN 60747-5-2 Approved under:

- IEC 60747-5-2:1997 + A1
- EN 60747-5-2:2001 + A1
- DIN EN 60747-5-2 (VDE 0884 Teil 2)

IEC/EN/DIN EN 60747-5-2 Insulation Characteristics*

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 150 Vrms for rated mains voltage ≤ 300 Vrms for rated mains voltage ≤ 600 Vrms		I – IV I – III I – II	
Climatic Classification		55/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{peak}
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ sec, Partial discharge < 5 pC	V_{PR}	1063	V_{peak}
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.5 = V_{PR}$, Type and Sample Test, $t_m = 60$ sec, Partial discharge < 5 pC	V_{PR}	851	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 10$ sec)	V_{IOTM}	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	$^{\circ}C$
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at $T_S, V_{IO} = 500$ V	R_S	$> 10^9$	Ω

*Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-M43U-000E	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	≥ 5	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	≥ 5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	150	°C	
Operating Temperature	T_A	-40	125	°C	
Lead Soldering Cycle	Temperature		260	°C	
	Time		10	s	
Average Forward Input Current	$I_{F(avg)}$		20	mA	1
Peak Forward Input Current (50% duty cycle, 1ms pulse width)	$I_{F(peak)}$		40	mA	2
Peak Transient Input Current ($\leq 1\mu s$ pulse width, 300ps)	$I_{F(trans)}$		100	mA	
Reversed Input Voltage	V_R		5	V	Pin 3 - 1
Input Power Dissipation	P_{IN}		30	mW	3
Output Power Dissipation	P_O		100	mW	4
Average Output Current	I_O		8	mA	
Peak Output Current	$I_{O(pk)}$		16	mA	
Supply Voltage (Pins 6-4)	V_{CC}	-0.5	30	V	
Output Voltage (Pins 5-4)	V_O	-0.5	20	V	
Solder Reflow Temperature Profile					See Reflow Temperature Profile

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V_{CC}	4.5	15.0	V	
Operating Temperature	T_A	-40	125	°C	

Electrical Specifications (DC)

Over recommended operating $T_A = -40^{\circ}\text{C}$ to 125°C , unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Current Transfer Ratio	CTR	32	45	80	%	$T_A = 25^{\circ}\text{C}$ $V_O = 0.4\text{V}$	1,2,4	5
		20	45		%	$V_O = 0.5\text{V}$		
Logic Low Output Voltage	V_{OL}		0.1	0.4	V	$T_A = 25^{\circ}\text{C}$ $I_O = 3\text{mA}$		
				0.5	V	$I_O = 2.4\text{mA}$		
Logic High Output Current	I_{OH}		0.003	0.5	μA	$T_A = 25^{\circ}\text{C}$ $V_O = V_{CC} = 5.5\text{V}$	7	
			0.01	1	μA	$T_A = 25^{\circ}\text{C}$ $V_O = V_{CC} = 15\text{V}$		
				50	μA			
Logic Low Supply Current	I_{CCL}		50	200	μA	$I_F = 10\text{mA}$, $V_O = \text{open}$, $V_{CC} = 15\text{V}$		11
Logic High Supply Current	I_{CCH}		0.02	1	μA	$T_A = 25^{\circ}\text{C}$ $I_F = 0\text{mA}$, $V_O = \text{open}$, $V_{CC} = 15\text{V}$		11
				2.5	μA			
Input Forward Voltage	V_F	1.45	1.5	1.85	V	$T_A = 25^{\circ}\text{C}$ $I_F = 10\text{mA}$	3	
		1.35	1.5	1.95	V	$I_F = 10\text{mA}$		
Input Reversed Breakdown Voltage	BV_R	5			V	$I_R = 10\mu\text{A}$		
Temperature Coefficient of Forward Voltage	$\Delta V/\Delta T_A$		-1.5		$\text{mV}/^{\circ}\text{C}$	$I_F = 10\text{mA}$		
Input Capacitance	C_{IN}		90		pF	$F = 1\text{MHz}$, $V_F = 0$		
Input-Output Insulation	V_{ISO}	3750			V_{RMS}	$RH \leq 50\%$, $t = 1\text{min}$, $T_A = 25^{\circ}\text{C}$		6, 7
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	$V_{I-O} = 500\text{VDC}$		6
Capacitance (Input-Output)	C_{I-O}		0.6		pF	$F = 1\text{MHz}$		6

Switching Specifications

Over recommended operating ($T_A = -40^\circ\text{C}$ to 125°C), $I_F = 10\text{mA}$, $V_{CC} = 5.0\text{V}$ unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	0.08	0.20	0.80	μs	$T_A=25^\circ\text{C}$ Pulse: $f = 10\text{kHz}$, Duty cycle = 50%, $I_F = 10\text{mA}$, $V_{CC} = 5.0\text{V}$, $R_L = 1.9\text{k}\Omega$, $C_L = 15\text{pF}$, $V_{THHL} = 1.5\text{V}$	5,6,8	9
		0.06		1.00	μs			
Propagation Delay Time to Logic High at Output	t_{PLH}	0.15	0.30	0.80	μs	$T_A=25^\circ\text{C}$ Pulse: $f = 10\text{kHz}$, Duty cycle = 50%, $I_F = 10\text{mA}$, $V_{CC} = 5.0\text{V}$, $R_L = 1.9\text{k}\Omega$, $C_L = 15\text{pF}$, $V_{THLH} = 2.0\text{V}$	5,6,8	9
		0.03		1.00	μs			
Pulse Width Distortion	PWD	0	0.40	0.45	μs	$T_A=25^\circ\text{C}$ Pulse: $f=10\text{kHz}$, Duty cycle = 50%, $I_F = 10\text{mA}$, $V_{CC} = 5.0\text{V}$, $R_L = 1.9\text{k}\Omega$, $C_L = 15\text{pF}$, $V_{THHL} = 1.5\text{V}$, $V_{THLH} = 2.0\text{V}$		12
		0		0.85	μs			
Propagation Delay Difference Between Any 2 Parts	$t_{PLH-tPHL}$	0	0.40	0.50	μs	$T_A=25^\circ\text{C}$ Pulse: $f = 10\text{kHz}$, Duty cycle = 50%, $I_F = 10\text{mA}$, $V_{CC} = 5.0\text{V}$, $R_L = 1.9\text{k}\Omega$, $C_L = 15\text{pF}$, $V_{THHL} = 1.5\text{V}$, $V_{THLH} = 2.0\text{V}$		13
		0		0.90	μs			
Common Mode Transient Immunity at Logic High Output	$ CM_H $	15	30		$\text{kV}/\mu\text{s}$	$V_{CM} = 1500\text{Vp-p}$, $I_F = 0\text{mA}$, $T_A = 25^\circ\text{C}$, $R = 1.9\text{k}\Omega$	9	8, 9
Common Mode Transient Immunity at Logic Low Output	$ CM_L $	15	30		$\text{kV}/\mu\text{s}$	$V_{CM} = 1500\text{Vp-p}$, $I_F = 10\text{mA}$, $T_A = 25^\circ\text{C}$, $R_L = 1.9\text{k}\Omega$		

Notes:

- Derate linearly above 85°C free-air temperature at a rate of $0.25\text{ mA}/^\circ\text{C}$.
- Derate linearly above 85°C free-air temperature at a rate of $0.30\text{ mA}/^\circ\text{C}$.
- Derate linearly above 85°C free-air temperature at a rate of $0.375\text{ mW}/^\circ\text{C}$.
- Derate linearly above 85°C free-air temperature at a rate of $1.875\text{ mW}/^\circ\text{C}$.
- CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F , times 100.
- Device considered a two terminal device: pin 1 and 3 shorted together and pins 4, 5 and 6 shorted together.
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 4500\text{ V}_{\text{RMS}}$ for 1 second (leakage detection current limit, $I\text{-O} \leq 5\text{ }\mu\text{A}$).
- Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM} , to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0\text{V}$). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8\text{V}$).
- The $1.9\text{ k}\Omega$ load represents 1 TTL unit load of 1.6 mA and the $5.6\text{ k}\Omega$ pull-up resistor.
- The frequency at which the ac output voltage is 3 dB below its mid-frequency value.
- Use of a $0.1\text{ }\mu\text{F}$ bypass capacitor connected between pins 4 and 6 is recommended.
- Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
- The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 4500\text{ V}_{\text{RMS}}$ for 1 second (leakage detection current limit, $I\text{-O} \leq 5\text{ }\mu\text{A}$).
- Pulse: $f = 0\text{ kHz}$, Duty Cycle = 10%.
- Use of a $0.1\text{ }\mu\text{F}$ bypass capacitor connected between pins 4 and 6 can improve performance by filtering power supply line noise.
- The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)
- Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM} , to assure that the output will remain in a Logic High state (i.e., $V_O > 3.0\text{V}$).
- Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM} , to assure that the output will remain in a Logic Low state (i.e., $V_O < 1.0\text{V}$).
- Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.

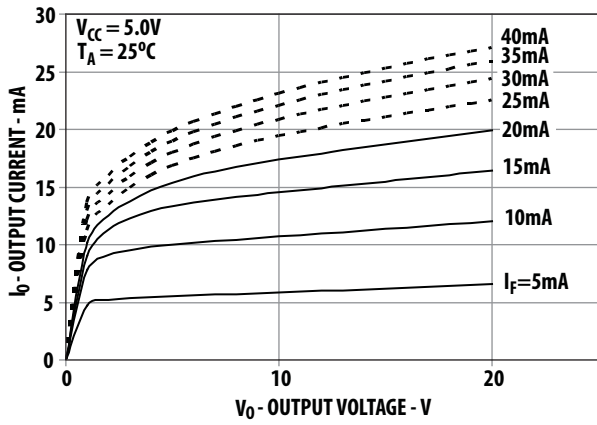


Figure 1. DC and Pulsed Transfer Characteristics.

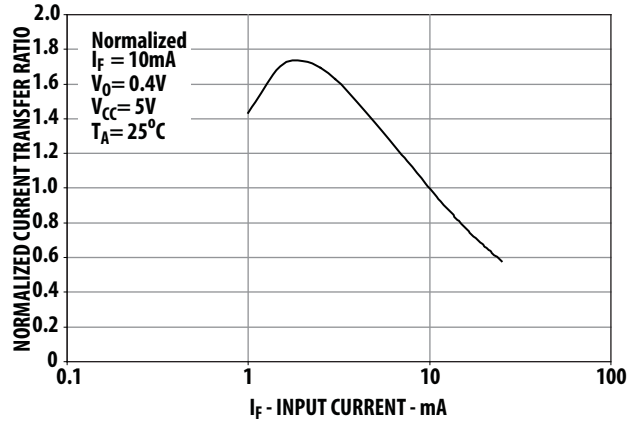


Figure 2. Current Transfer Ratio vs Input Current

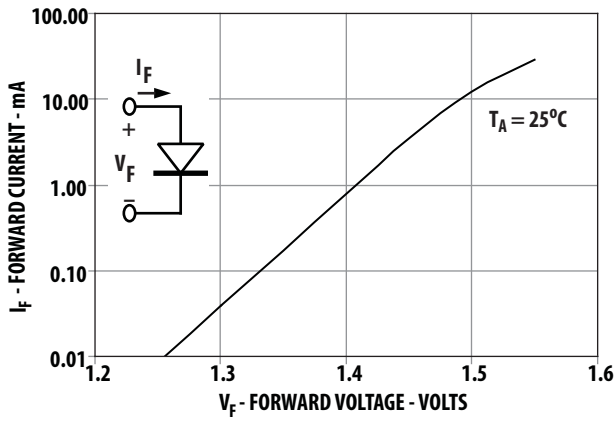


Figure 3. Input Current vs Forward Voltage

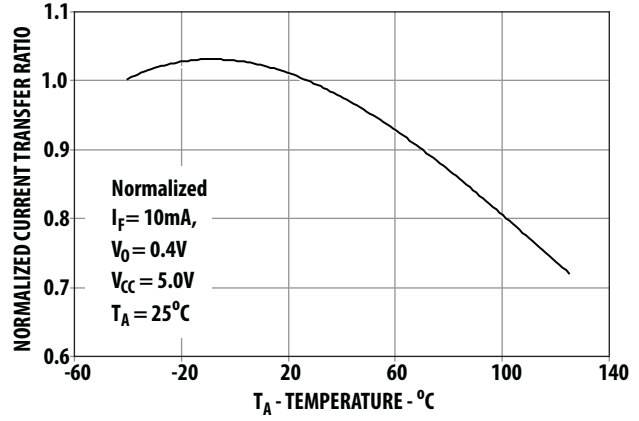


Figure 4. Current Transfer Ratio vs Temperature

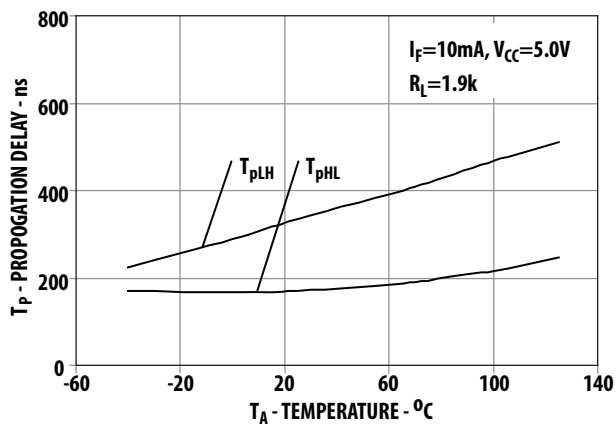


Figure 5. Propagation Delay vs Temperature

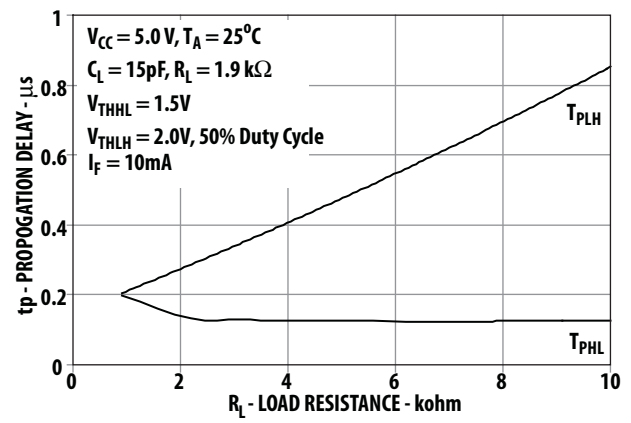


Figure 6. Propagation Delay Time vs Load Resistance

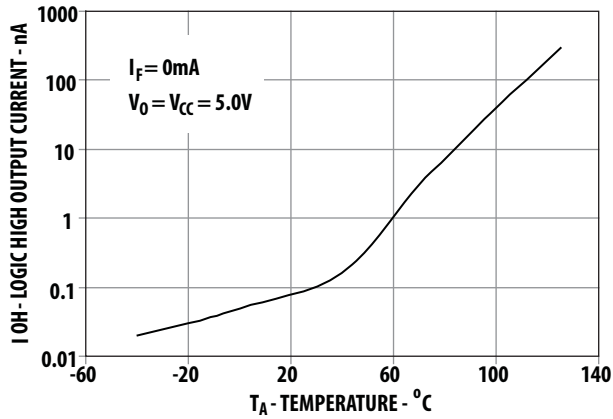


Figure 7. Logic High Output Current vs Temperature.

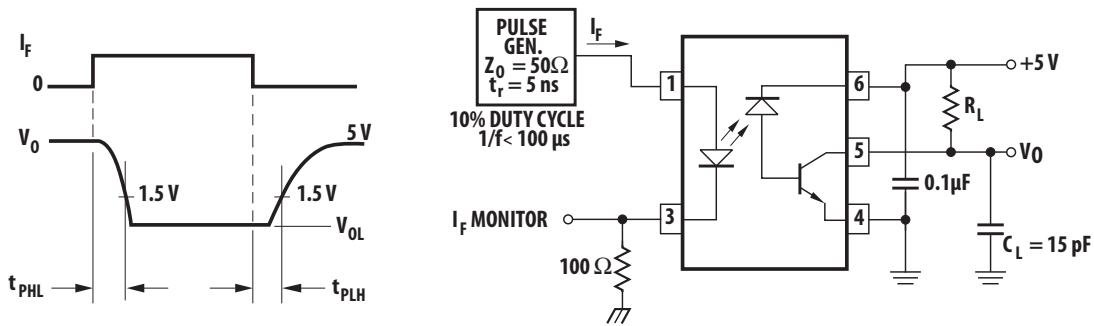


Figure 8. Switching Test Circuit

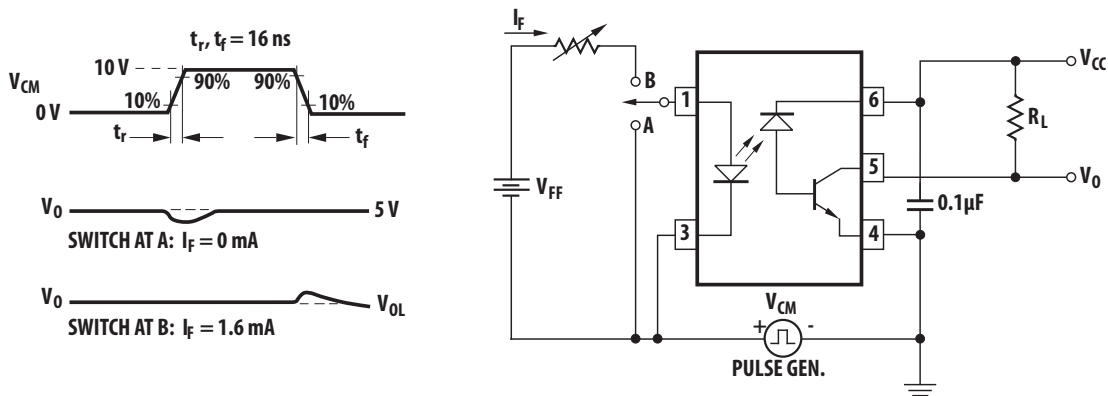


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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